National Semiconductor

January 7, 2008

ADC08200
8-Bit, 20 Msps to 200 Msps, Low Power A/D Converter with Internal Sample-and-Hold

General Description

The ADC08200 is a low-power, 8-bit, monolithic analog-to-digital converter with an on-chip track-and-hold circuit. Optimized for low cost, low power, small size and ease of use, this product operates at conversion rates up to 230 Msps while consuming just 1.05 mW per MHz of clock frequency, or 210 mW at 200 Msps. Raising the PD pin puts the ADC08200 into a Power Down mode where it consumes about 1 mW.

The unique architecture achieves 7.3 Effective Bits with 50 MHz input frequency. The ADC08200 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC08200's reference ladder are available for connections, enabling a wide range of input possibilities. The digital outputs are TTL/CMOS compatible with a separate output power supply pin to support interfacing with 3V or 2.5V logic. The digital inputs (CLK and PD) are TTL/CMOS compatible. The output data format is straight binary.

The ADC08200 is offered in a 24-lead plastic package (TSSOP) and, while specified over the industrial temperature range of −40°C to +85°C, it will function over the to −40°C to +105°C temperature range. An evaluation board is available to assist in the easy evaluation of the ADC08200.

Features

- Single-ended input
- Internal sample-and-hold function
- Low voltage (single +3V) operation
- Small package
- Power-down feature

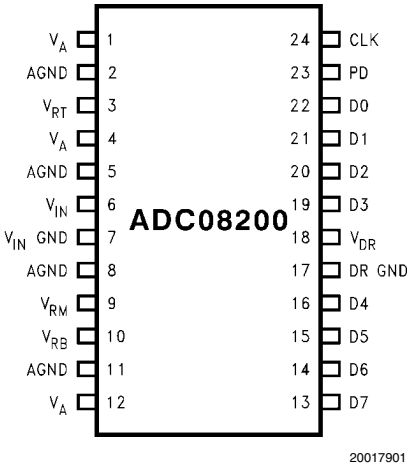
Key Specifications

■ Resolution	8 Bits
■ Maximum sampling frequency	200 Msps (min)
■ DNL	±0.4 LSB (typ)
■ ENOB (f_{IN}= 50 MHz)	7.3 bits (typ)
■ THD (f_{IN}= 50 MHz)	61 dB (typ)
■ Power Consumption	
■ — Operating	1.05 mW/Msps (typ)
— Power Down	1 mW (typ)

Applications

- Flat panel displays
- Projection systems
- Set-top boxes
- Battery-powered instruments
- Communications
- Medical imaging
- Astronomy

Pin Configuration



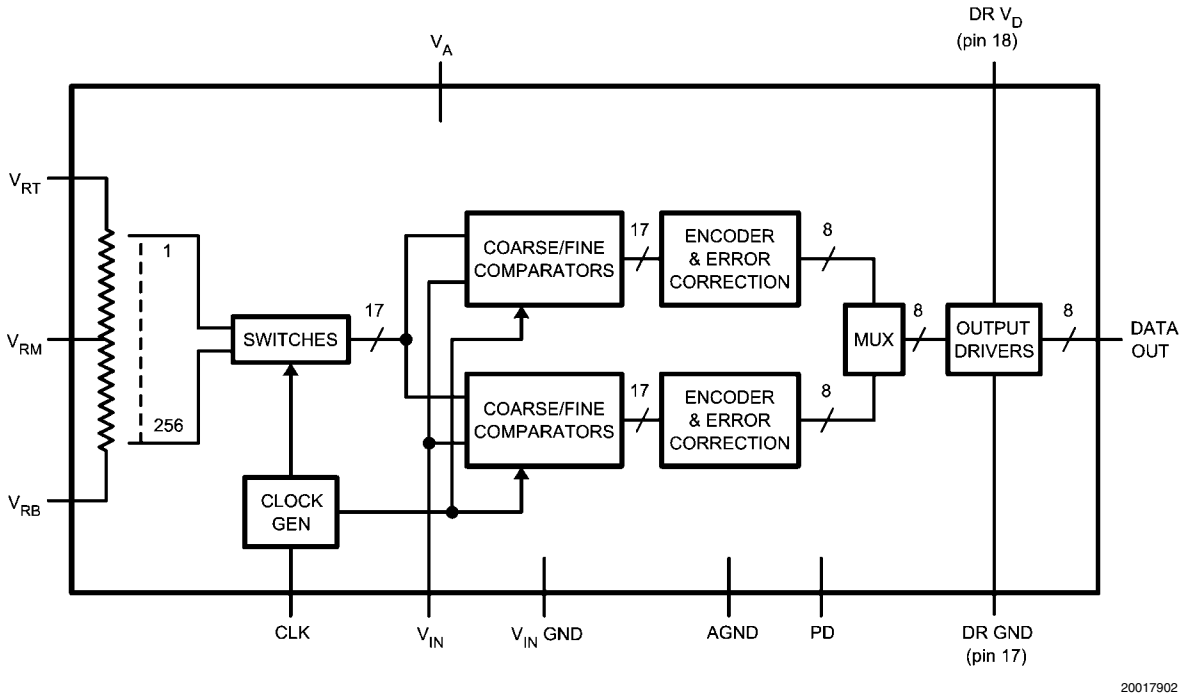
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Ordering Information

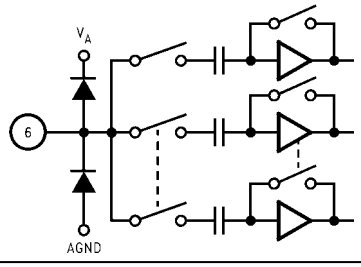
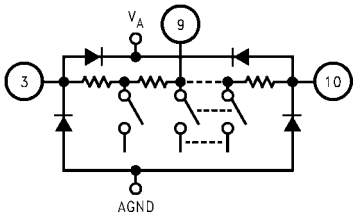
Order Number	Temperature Range	Package
ADC08200CIMT	$-40°C \le T_A \le +105°C$	TSSOP
ADC08200CIMTX	$-40°C \le T_A \le +105°C$	TSSOP (tape and reel)
ADC08200EVAL		Evaluation Board

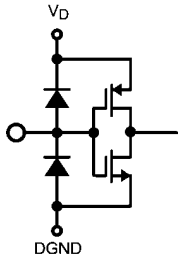
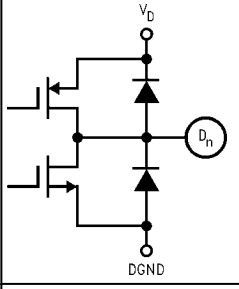
Block Diagram



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Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
6	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT}.
3	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Nominal range is 0.5V to V_A. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
9	V_{RM}		Mid-point of the reference ladder. This pin should be bypassed to a quiet point in the ground plane with a 0.1 µF capacitor.
10	V_{RB}		Analog Input that is the low side (bottom) of the reference ladder of the ADC. Nominal range is 0.0V to (V_{RT} – 0.5V). Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.

Pin No.	Symbol	Equivalent Circuit	Description
23	PD		Power Down input. When this pin is high, the converter is in the Power Down mode and the data output pins hold the last conversion result.
24	CLK		CMOS/TTL compatible digital clock Input. V_{IN} is sampled on the rising edge of CLK input.
13 thru 16 and 19 thru 22	D0–D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input.
7	V_{IN} GND		Reference ground for the single-ended analog input, V_{IN}.
1, 4, 12	V_A		Positive analog supply pin. Connect to a quiet voltage source of +3V. V_A should be bypassed with a 0.1 µF ceramic chip capacitor for each pin, plus one 10 µF capacitor. See Section 3.0 for more information.
18	V_{DR}		Power supply for the output drivers. If connected to V_A, decouple well from V_A.
17	DR GND		The ground return for the output driver supply.
2, 5, 8, 11	AGND		The ground return for the analog supply.

Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A)	3.8V
Driver Supply Voltage (V_{DR})	V_A +0.3V
Voltage on Any Input or Output Pin	−0.3V to V_A
Reference Voltage (V_{RT}, V_{RB})	V_A to AGND
CLK, PD Voltage Range	−0.05V to (V_A + 0.05V)
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Power Dissipation at T_A = 25°C	See (Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2500V
Machine Model	200V
Soldering Temperature, Infrared, 10 seconds (Note 6)	235°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	−40°C ≤ T_A ≤ +105°C
Supply Voltage (V_A)	+2.7V to +3.6V
Driver Supply Voltage (V_{DR})	+2.4V to V_A
Ground Difference |GND - DR GND|	0V to 300 mV
Upper Reference Voltage (V_{RT})	0.5V to (V_A −0.3V)
Lower Reference Voltage (V_{RB})	0V to (V_{RT} −0.5V)
V_{IN} Voltage Range	V_{RB} to V_{RT}

Package Thermal Resistance

Package	θ_{JA}
24-Lead TSSOP	92°C/W

Converter Electrical Characteristics

The following specifications apply for V_A = V_{DR} = +3.0V_{DC}, V_{RT} = +1.9V, V_{RB} = 0.3V, C_L = 5 pF, f_{CLK} = 200 MHz at 50% duty cycle. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}**: all other limits T_J = 25°C (Notes 7, 8)

Symbol	Parameter	Conditions		Typical (Note 9)	Limits (Note 9)	Units (Limits)
DC ACCURACY						
INL	Integral Non-Linearity			+1.0 −0.3	**+1.9** **−1.2**	LSB (max) LSB (min)
DNL	Differential Non-Linearity			±0.4	**±0.95**	LSB (max)
	Missing Codes				**0**	(max)
FSE	Full Scale Error			36	**50**	mV (max)
V_{OFF}	Zero Scale Offset Error			46	**60**	mV (max)
ANALOG INPUT AND REFERENCE CHARACTERISTICS						
V_{IN}	Input Voltage			1.6	**V_{RB}**	V (min)
					V_{RT}	V (max)
C_{IN}	V_{IN} Input Capacitance	V_{IN} = 0.75V +0.5 Vrms	(CLK LOW)	3		pF
			(CLK HIGH)	4		pF
R_{IN}	R_{IN} Input Resistance			>1		MΩ
BW	Full Power Bandwidth			500		MHz
V_{RT}	Top Reference Voltage			1.9	**V_A**	V (max)
					0.5	V (min)
V_{RB}	Bottom Reference Voltage			0.3	**V_{RT} − 0.5**	V (max)
					0	V (min)
V_{RT} - V_{RB}	Reference Voltage Delta			1.6	1.0	V (min)
					2.3	V (max)
R_{REF}	Reference Ladder Resistance	V_{RT} to V_{RB}		160	**120**	Ω (min)
					200	Ω (max)
CLK, PD DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Logical High Input Voltage	V_{DR} = V_A = 3.6V			**2.0**	V (min)
V_{IL}	Logical Low Input Voltage	V_{DR} = V_A = 2.7V			**0.8**	V (max)
I_{IH}	Logical High Input Current	V_{IH} = V_{DR} = V_A = 3.6V		10		nA

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
I_{IL}	Logical Low Input Current	V_{IL} = 0V, V_{DR} = V_A = 2.7V	–50		nA
C_{IN}	Logic Input Capacitance		3		pF
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	High Level Output Voltage	V_A = V_{DR} = 2.7V, I_{OH} = –400 µA	2.6	**2.4**	V (min)
V_{OL}	Low Level Output Voltage	V_A = V_{DR} = 2.7V, I_{OL} = 1.0 mA	0.4	**0.5**	V (max)
DYNAMIC PERFORMANCE					
ENOB	Effective Number of Bits	f_{IN} = 4 MHz, V_{IN} = FS – 0.25 dB	7.5		Bits
		f_{IN} = 20 MHz, V_{IN} = FS – 0.25 dB	7.4		Bits
		f_{IN} = 50 MHz, V_{IN} = FS – 0.25 dB	7.3	**6.9**	Bits (min)
		f_{IN} = 70 MHz, V_{IN} = FS – 0.25 dB	7.2		Bits
		f_{IN} = 100 MHz, V_{IN} = FS – 0.25 dB	7.0		Bits
SINAD	Signal-to-Noise & Distortion	f_{IN} = 4 MHz, V_{IN} = FS – 0.25 dB	47		dB
		f_{IN} = 20 MHz, V_{IN} = FS – 0.25 dB	46		dB
		f_{IN} = 50 MHz, V_{IN} = FS – 0.25 dB	46	**43.3**	dB (min)
		f_{IN} = 70 MHz, V_{IN} = FS – 0.25 dB	45		dB
		f_{IN} = 100 MHz, V_{IN} = FS – 0.25 dB	44		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 4 MHz, V_{IN} = FS – 0.25 dB	47		dB
		f_{IN} = 20 MHz, V_{IN} = FS – 0.25 dB	46		dB
		f_{IN} = 50 MHz, V_{IN} = FS – 0.25 dB	46	**43.4**	dB (min)
		f_{IN} = 70 MHz, V_{IN} = FS – 0.25 dB	45		dB
		f_{IN} = 100 MHz, V_{IN} = FS – 0.25 dB	44		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 4 MHz, V_{IN} = FS – 0.25 dB	60		dBc
		f_{IN} = 20 MHz, V_{IN} = FS – 0.25 dB	58		dBc
		f_{IN} = 50 MHz, V_{IN} = FS – 0.25 dB	60		dBc
		f_{IN} = 70 MHz, V_{IN} = FS – 0.25 dB	57		dBc
		f_{IN} = 100 MHz, V_{IN} = FS – 0.25 dB	54		dBc
THD	Total Harmonic Distortion	f_{IN} = 4 MHz, V_{IN} = FS – 0.25 dB	–60		dBc
		f_{IN} = 20 MHz, V_{IN} = FS – 0.25 dB	–58		dBc
		f_{IN} = 50 MHz, V_{IN} = FS – 0.25 dB	–60		dBc
		f_{IN} = 70 MHz, V_{IN} = FS – 0.25 dB	-56		dBc
		f_{IN} = 100 MHz, V_{IN} = FS – 0.25 dB	–53		dBc
HD2	2nd Harmonic Distortion	f_{IN} = 4 MHz, V_{IN} = FS – 0.25 dB	–66		dBc
		f_{IN} = 20 MHz, V_{IN} = FS – 0.25 dB	-68		dBc
		f_{IN} = 50 MHz, V_{IN} = FS – 0.25 dB	–66		dBc
		f_{IN} = 70 MHz, V_{IN} = FS – 0.25 dB	-60		dBc
		f_{IN} = 100 MHz, V_{IN} = FS – 0.25 dB	–55		dBc
HD3	3rd Harmonic Distortion	f_{IN} = 4 MHz, V_{IN} = FS – 0.25 dB	–72		dBc
		f_{IN} = 20 MHz, V_{IN} = FS – 0.25 dB	–58		dBc
		f_{IN} = 50 MHz, V_{IN} = FS – 0.25 dB	–72		dBc
		f_{IN} = 70 MHz, V_{IN} = FS – 0.25 dB	-58		dBc
		f_{IN} = 100 MHz, V_{IN} = FS – 0.25 dB	–60		dBc
IMD	Intermodulation Distortion	f_1 = 11 MHz, V_{IN} = FS – 6.25 dB f_2 = 12 MHz, V_{IN} = FS – 6.25 dB	-55		dBc
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	DC Input	69.75	**86**	mA (max)
		f_{IN} = 10 MHz, V_{IN} = FS – 3 dB	69.75		mA
I_{DR}	Output Driver Supply Current	DC Input, PD = Low	0.25	**0.6**	mA (max)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
$I_A + I_{DR}$	Total Operating Current	DC Input, PD = Low	70	**86.6**	mA (max)
		CLK Low, PD = Hi	0.3		mA
PC	Power Consumption	DC Input, Excluding Reference	210	**260**	mW (max)
		CLK Low, PD = Hi	1		mW
$PSRR_1$	Power Supply Rejection Ratio	FSE change with 2.7V to 3.3V change in V_A	54		dB
$PSRR_2$	Power Supply Rejection Ratio	SNR reduction with 200 mV at 1MHz on supply	45		dB
AC ELECTRICAL CHARACTERISTICS					
f_{C1}	Maximum Conversion Rate		230	**200**	MHz (min)
f_{C2}	Minimum Conversion Rate		10		MHz
t_{CL}	Minimum Clock Low Time		0.87	**1.0**	ns (min)
t_{CH}	Minimum Clock High Time		0.65	**0.75**	ns (min)
t_{OH}	Output Hold Time, Output Falling (Note 10)	CLK to Data Invalid, V_A = 3.3V to 3.6V, t_A = −40°C to +105°C, C_L = 8 pF	2.4	**3.3**	ns (max)
	Output Hold Time, Output Rising (Note 10)	CLK to Data Invalid, V_A = 3.3V to 3.6V, t_A = −40°C to +105°C, C_L = 8 pF	1.9	**2.5**	ns (max)
t_{OD}	Output Delay, Output Falling (Note 10)	CLK to Data Transition, V_A = 3.3V to 3.6V, V_A = −40°C to +105°C, C_L = 8 pF	3.9	**2.4**	ns (min)
				5.1	ns (max)
	Output Delay, Output Rising (Note 10)	CLK to Data Transition, V_A = 3.3V to 3.6V, t_A = −40°C to +105°C, C_L = 8 pF	3.3	**2.4**	ns (min)
				4.0	ns (max)
t_{SLEW}	Output Slew Rate	Output Falling, V_A = 3.3V, C_L = 8 pF, t_A = −40°C to +105°C	0.73		V/ns
		Output Rising, V_A = 3.3V, C_L = 8 pF, t_A = −40°C to +105°C	0.88		V/ns
	Pipeline Delay (Latency)		6		Clock Cycles
t_{AD}	Sampling (Aperture) Delay	CLK Rise to Acquisition of Data	2.6		ns
t_{AJ}	Aperture Jitter		2		ps rms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DR GND = 0V, unless otherwise specified.

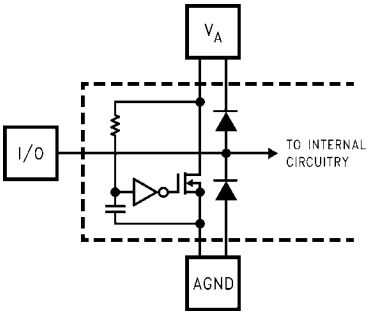
Note 3: When the input voltage at any pin exceeds the power supplies (that is, less than AGND or DR GND, or greater than V_A or V_{DR}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / \theta_{JA}$. The values for maximum power dissipation listed above will be reached only when this device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.

Note 6: See AN-450, “Surface Mounting Methods and Their Effect on Product Reliability”.

Note 7: The analog inputs are protected as shown below. Input voltage magnitudes up to V_A + 300 mV or to 300 mV below GND will not damage this device. However, errors in the A/D conversion can occur if the input goes above V_{DR} or below GND by more than 100 mV. For example, if V_A is $2.7V_{DC}$ the full-scale input voltage must be $\leq 2.8V_{DC}$ to ensure accurate conversions.



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Note 8: To guarantee accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

Note 9: Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: These specifications are guaranteed by design and not tested.

Note 11: Typical output slew rate is based upon the maximum t_{OD} and t_{OH} figures.

Specification Definitions

APERTURE (SAMPLING) DELAY is that time required after the rise of the clock input for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the "hold" mode t_{AD} after the clock goes high.

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

CLOCK DUTY CYCLE is the ratio of the time that the clock wave form is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at 200 Msps with a ramp input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL-SCALE ERROR is a measure of how far the last code transition is from the ideal 1½ LSB below V_{RT} and is defined as:

$$V_{max} + 1.5\ LSB - V_{RT}$$

where V_{max} is the voltage at which the transition to the maximum (full scale) code occurs.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from zero scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used. Measured at 200 Msps with a ramp input.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. it is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

OUTPUT DELAY is the time delay after the rising edge of the input clock before the data update is present at the output pins.

OUTPUT HOLD TIME is the length of time that the output data is valid after the rise of the input clock.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the Output Delay.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC08200, PSRR1 is the ratio of the change in Full-Scale Error that results from a change in the DC power supply voltage, expressed in dB. PSRR2 is a measure of how well an AC signal riding upon the power supply is rejected from the output and is here defined as

$$PSRR2 = 20Log\left(4\sqrt{10^{\frac{-SNR1}{10}} - 10^{\frac{-SNR0}{10}}}\right)$$

where SNR0 is the SNR measured with no noise or signal on the supply line and SNR1 is the SNR measured with a 1 MHz, 200 mV_{P-P} signal riding upon the supply lines.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum

ZERO SCALE OFFSET ERROR is the error in the input voltage required to cause the first code transition. It is defined as

$$V_{OFF} = V_{ZT} - V_{RB}$$

where V_{ZT} is the first code transition input voltage.

Timing Diagram

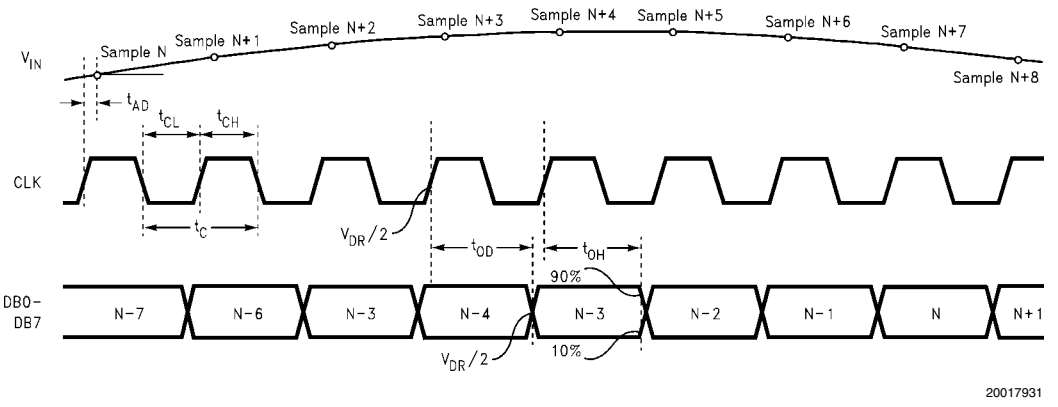
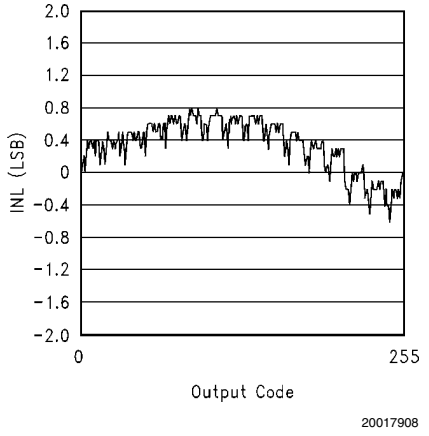


FIGURE 1. ADC08200 Timing Diagram

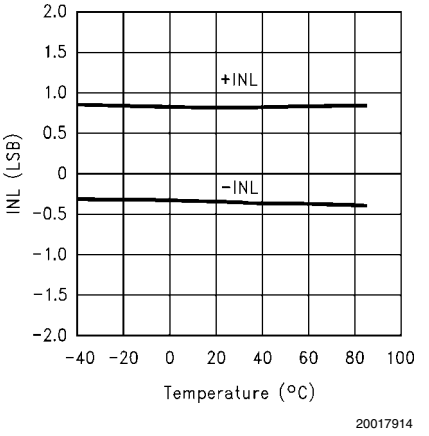
Typical Performance Characteristics

$V_A = V_{DR} = 3V$, $f_{CLK} = 200$ MHz, $f_{IN} = 50$ MHz, unless otherwise stated

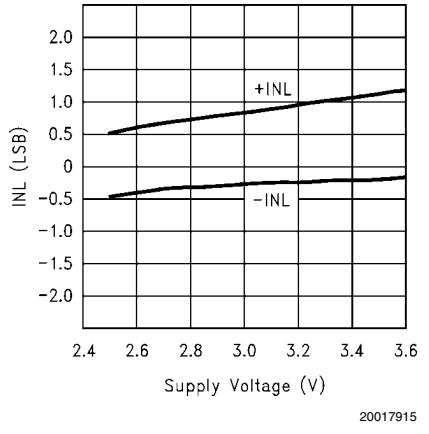
INL



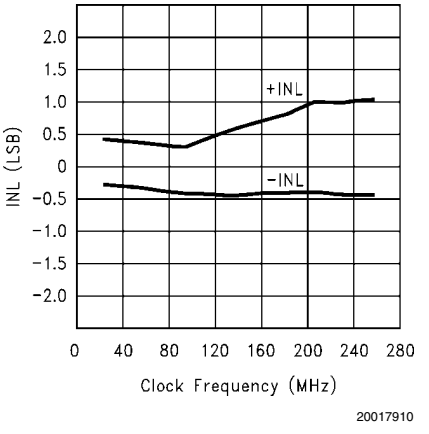
INL vs. Temperature



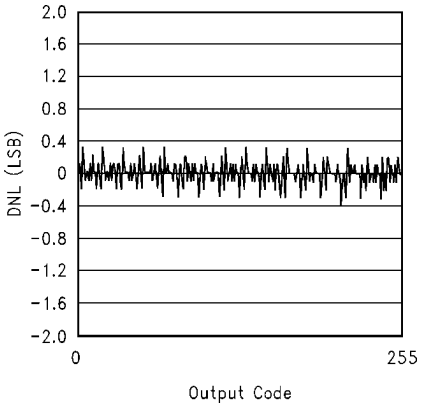
INL vs. Supply Voltage



INL vs. Sample Rate

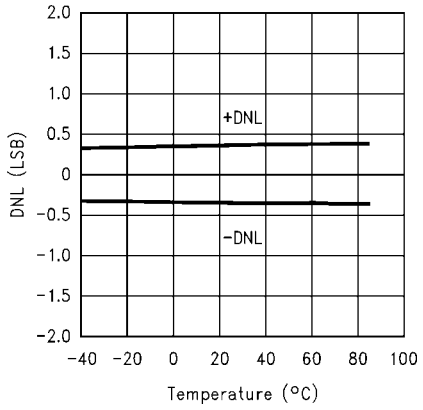


DNL



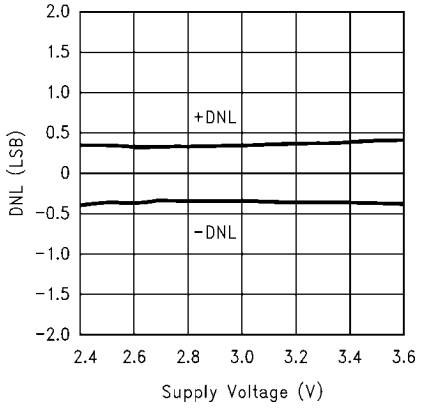
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DNL vs. Temperature



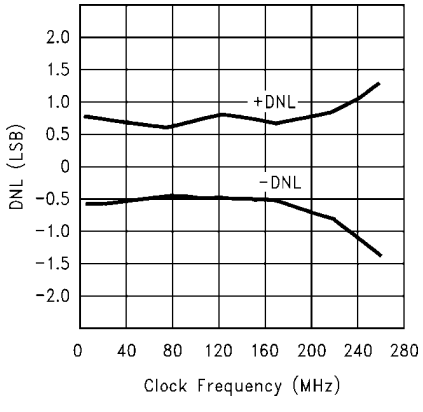
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DNL vs. Supply Voltage



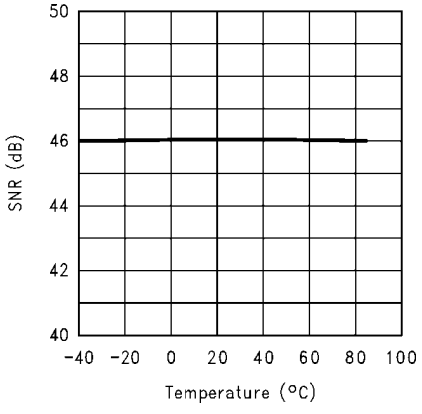
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DNL vs. Sample Rate



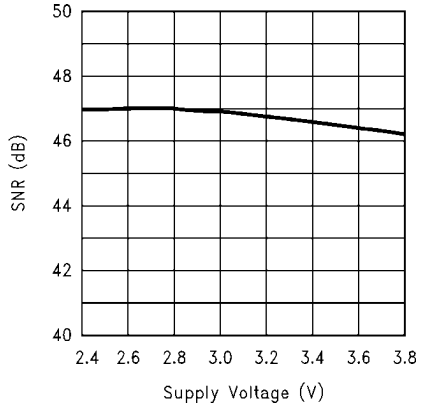
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SNR vs. Temperature



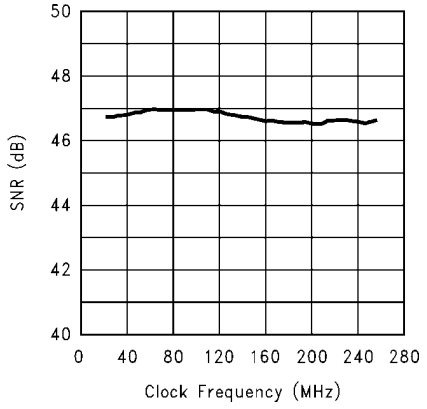
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SNR vs. Supply Voltage



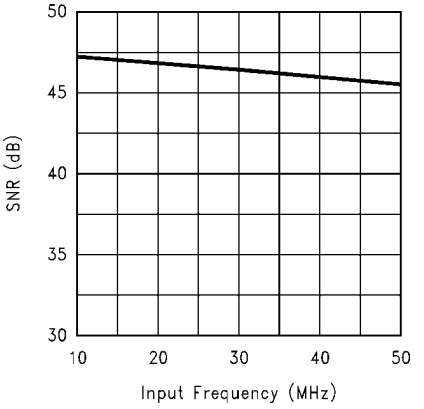
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SNR vs. Sample Rate



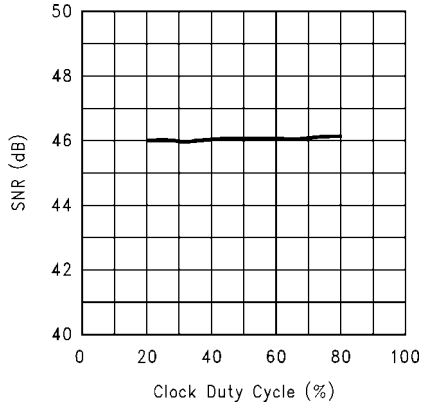
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SNR vs. Input Frequency



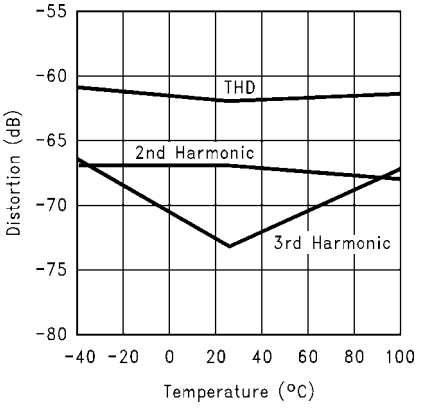
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SNR vs. Clock Duty Cycle



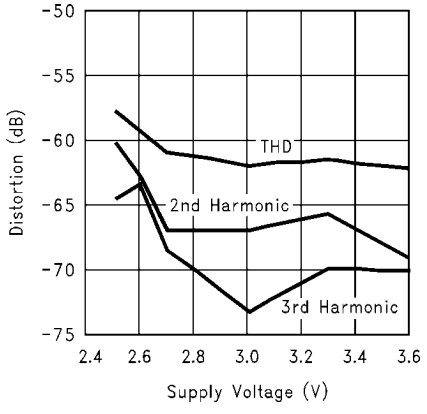
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Distortion vs. Temperature



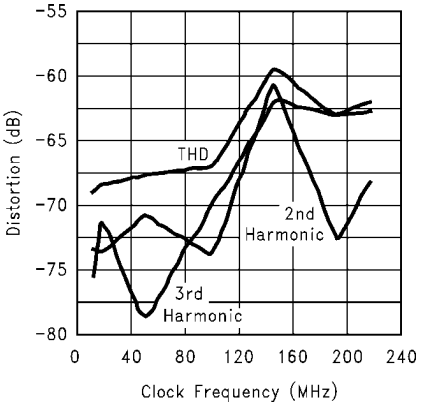
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Distortion vs. Supply Voltage



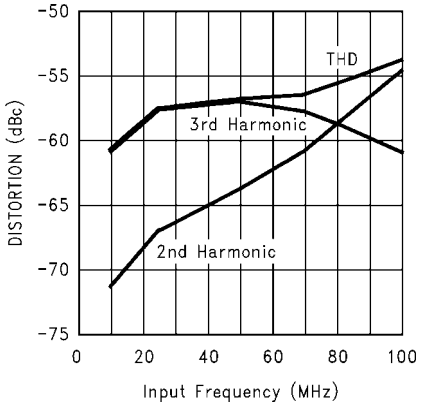
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Distortion vs. Sample Rate



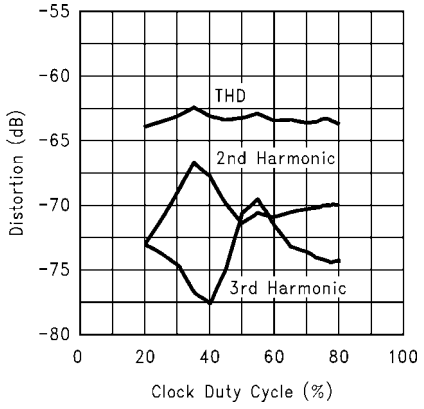
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Distortion vs. Input Frequency



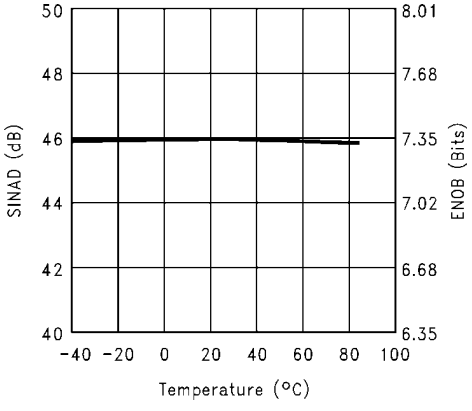
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Distortion vs. Clock Duty Cycle



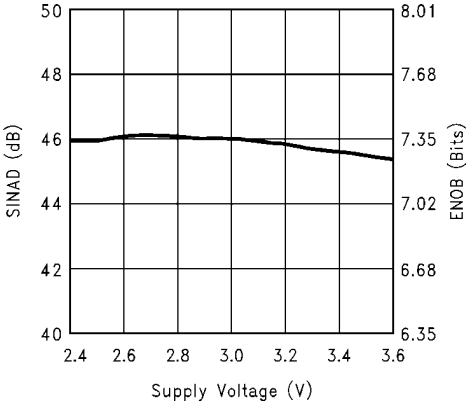
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SINAD/ENOB vs. Temperature



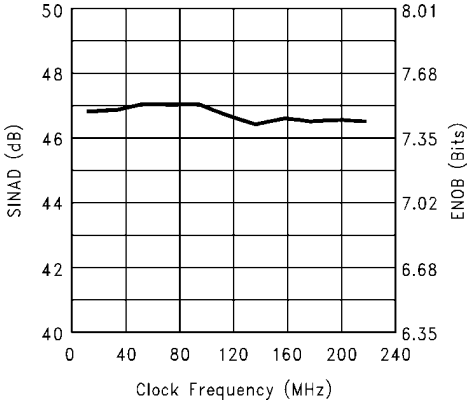
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SINAD/ENOB vs. Supply Voltage



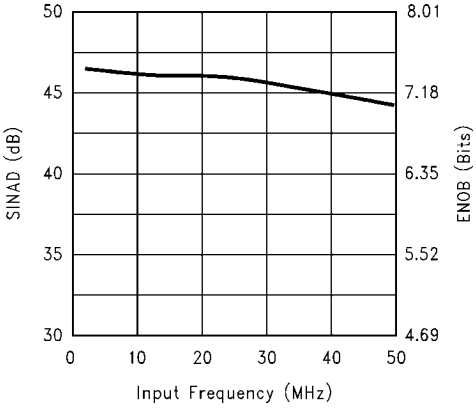
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SINAD/ENOB vs. Sample Rate



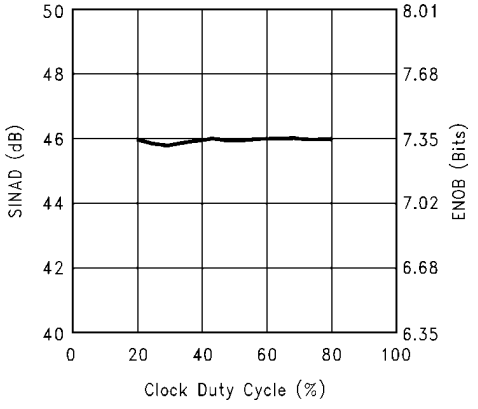
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SINAD/ENOB vs. Input Frequency



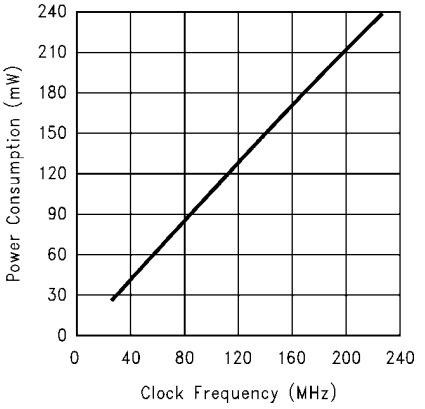
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SINAD/ENOB vs. Clock Duty Cycle



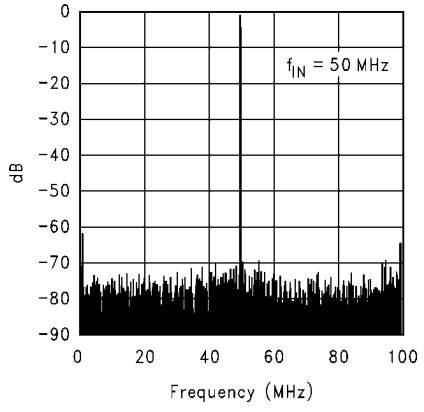
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Power Consumption vs. Sample Rate



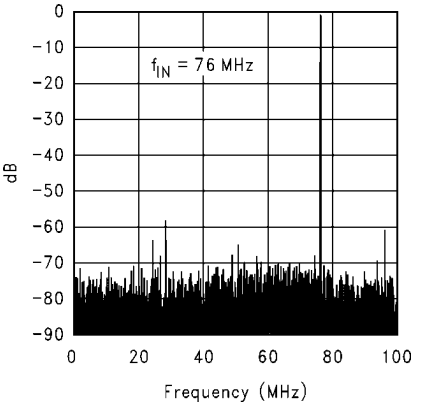
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Spectral Response @ f_{IN} = 50 MHz



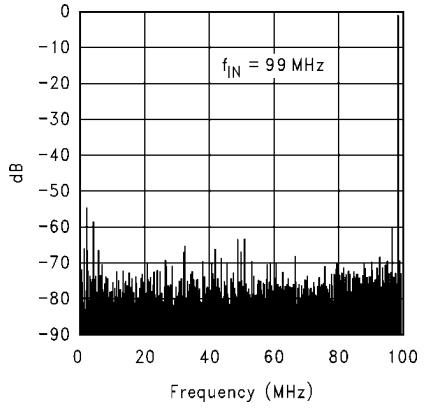
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Spectral Response @ f_{IN} = 76 MHz



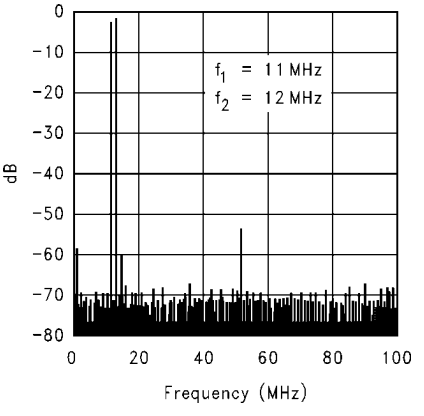
20017947

Spectral Response @ f_{IN} = 99 MHz



20017948

Intermodulation Distortion



20017943

Functional Description

The ADC08200 uses a new, unique architecture that achieves over 7 effective bits at input frequencies up to and beyond 100 MHz.

The analog input signal that is within the voltage range set by V_{RT} and V_{RB} is digitized to eight bits. Input voltages below V_{RB} will cause the output word to consist of all zeroes. Input voltages above V_{RT} will cause the output word to consist of all ones.

Incorporating a switched capacitor bandgap, the ADC08200 exhibits a power consumption that is proportional to frequency, limiting power consumption to what is needed at the clock rate that is used. This and its excellent performance over a wide range of clock frequencies makes it an ideal choice as a single ADC for many 8-bit needs.

Data is acquired at the rising edge of the clock and the digital equivalent of that data is available at the digital outputs 6 clock cycles plus t_{OD} later. The ADC08200 will convert as long as the clock signal is present. The output coding is straight binary.

The device is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode, where the output pins hold the last conversion before the PD pin went high and the device consumes just 1.4 mW . Holding the clock input low will further reduce the power consumption in the power down mode to about 1 mW.

Applications Information

1.0 REFERENCE INPUTS

The reference inputs V_{RT} and V_{RB} are the top and bottom of the reference ladder, respectively. Input signals between these two voltages will be digitized to 8 bits. External voltages applied to the reference input pins should be within the range specified in the Operating Ratings table. Any device used to drive the reference pins should be able to source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin to maintain the desired voltages.

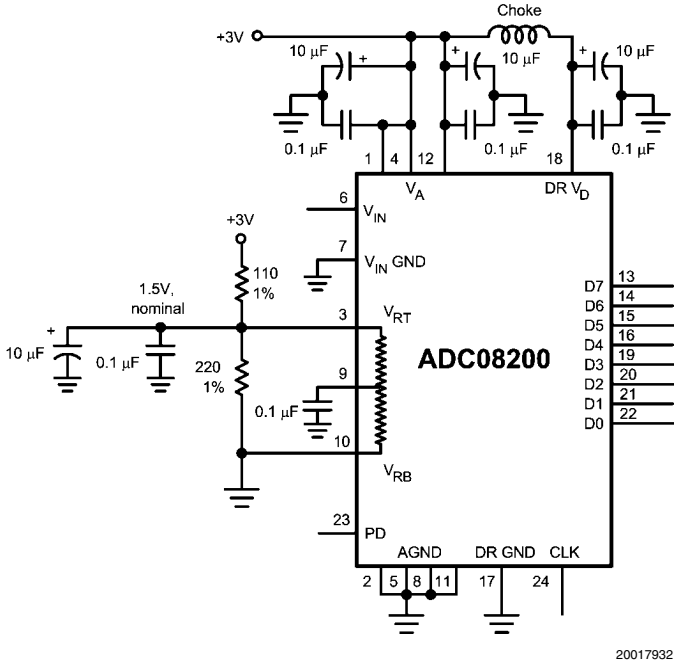


FIGURE 2. Simple, low component count reference biasing. Because of the ladder and external resistor tolerances, the reference voltage of this circuit can vary too much for some applications.

The reference bias circuit of *Figure 2* is very simple and the performance is adequate for many applications. However, circuit tolerances will lead to a wide reference voltage range. Better reference stability can be achieved by driving the reference pins with low impedance sources.

The circuit of *Figure 3* will allow a more accurate setting of the reference voltages. The upper amplifier must be able to source the reference current as determined by the value of the reference resistor and the value of ($V_{RT} - V_{RB}$). The lower amplifier must be able to sink this reference current. Both amplifiers should be stable with a capacitive load. The *LM8272* was chosen because of its rail-to-rail input and output capability, its high current output and its ability to drive large capacitive loads.

The divider resistors at the inputs to the amplifiers could be changed to suit the application reference voltage needs, or the divider can be replaced with potentiometers or DACs for precise settings. The bottom of the ladder (V_{RB}) may be returned to ground if the minimum input signal excursion is 0V.

V_{RT} should always be more positive than V_{RB} by the minimum V_{RT} - V_{RB} difference in the Electrical Characteristics table to minimize noise. While V_{RT} may be as high as the V_A supply voltage and V_{RB} may be as low as ground, the difference between these two voltages ($V_{RT} - V_{RB}$) should not exceed 2.3V to prevent waveform distortion.

The V_{RM} pin is the center of the reference ladder and should be bypassed to a quiet point in the ground plane with a 0.1 µF capacitor. DO NOT leave this pin open and DO NOT load this pin with more than 10µA.

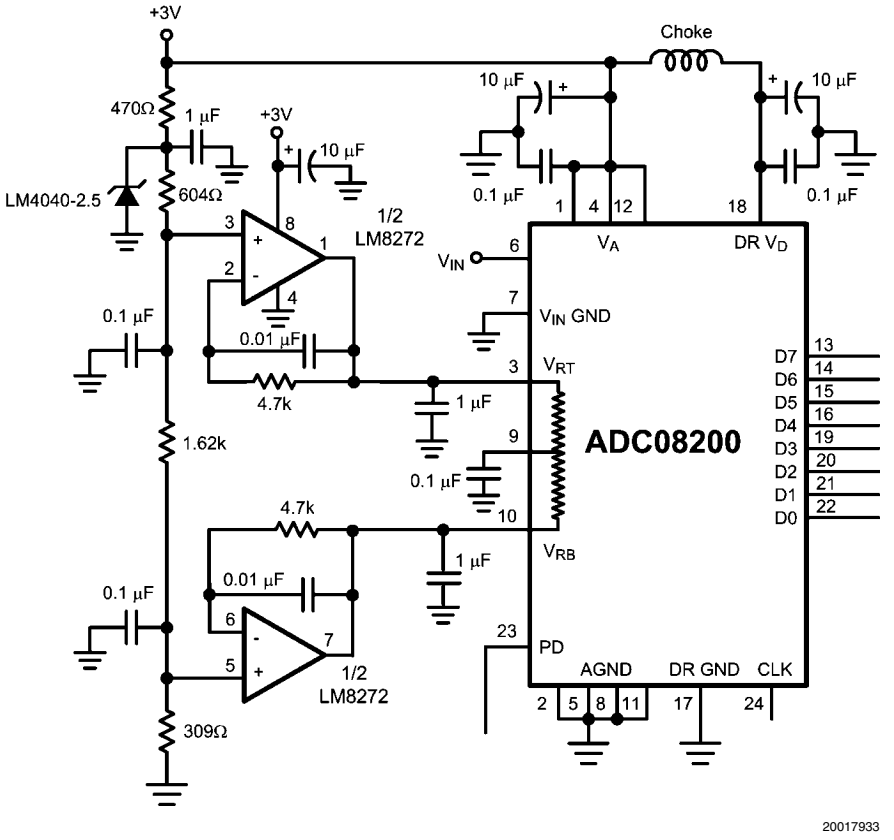


FIGURE 3. Driving the reference to force desired values requires driving with a low impedance source.

2.0 THE ANALOG INPUT

The analog input of the ADC08200 is a switch followed by an integrator. The input capacitance changes with the clock level, appearing as 3 pF when the clock is low, and 4 pF when the clock is high. The sampling nature of the analog input causes current spikes at the input that result in voltage spikes there. Any amplifier used to drive the analog input must be able to settle within the clock high time. The LMH6702 and the LMH6628 have been found to be good amplifiers to drive the ADC08200.

Figure 4 shows an example of an input circuit using the LMH6702. Any input amplifier should incorporate some gain as operational amplifiers exhibit better phase margin and transient response with gains above 2 or 3 than with unity gain. If an overall gain of less than 3 is required, attenuate the input and operate the amplifier at a higher gain, as shown in *Figure 4*.

The RC at the amplifier output filters the clock rate energy that comes out of the analog input due to the input sampling circuit. The optimum time constant for this circuit depends not only upon the amplifier and ADC, but also on the circuit layout and board material. A resistor value should be chosen between 18Ω and 47Ω and the capacitor value chose according to the formula

$$C = \frac{1}{2 \bullet \pi \bullet R \bullet f_{CLK}}$$

The value of "C" in the formula above should include the ADC input capacitance when the clock is high

This will provide optimum SNR performance for Nyquist applications. Best THD performance is realized when the capacitor and resistor values are both zero, but this would compromise SNR and SINAD performance. Generally, the capacitor should not be added for undersampling applications.

The circuit of *Figure 4* has both gain and offset adjustments. If you eliminate these adjustments normal circuit tolerances may result in signal clipping unless care is exercised in the worst case analysis of component tolerances and the input signal excursion is appropriately limited to account for the worst case conditions.

Full scale and offset adjustments may also be made by adjusting V_{RT} and V_{RB}, perhaps with the aid of a pair of DACs.

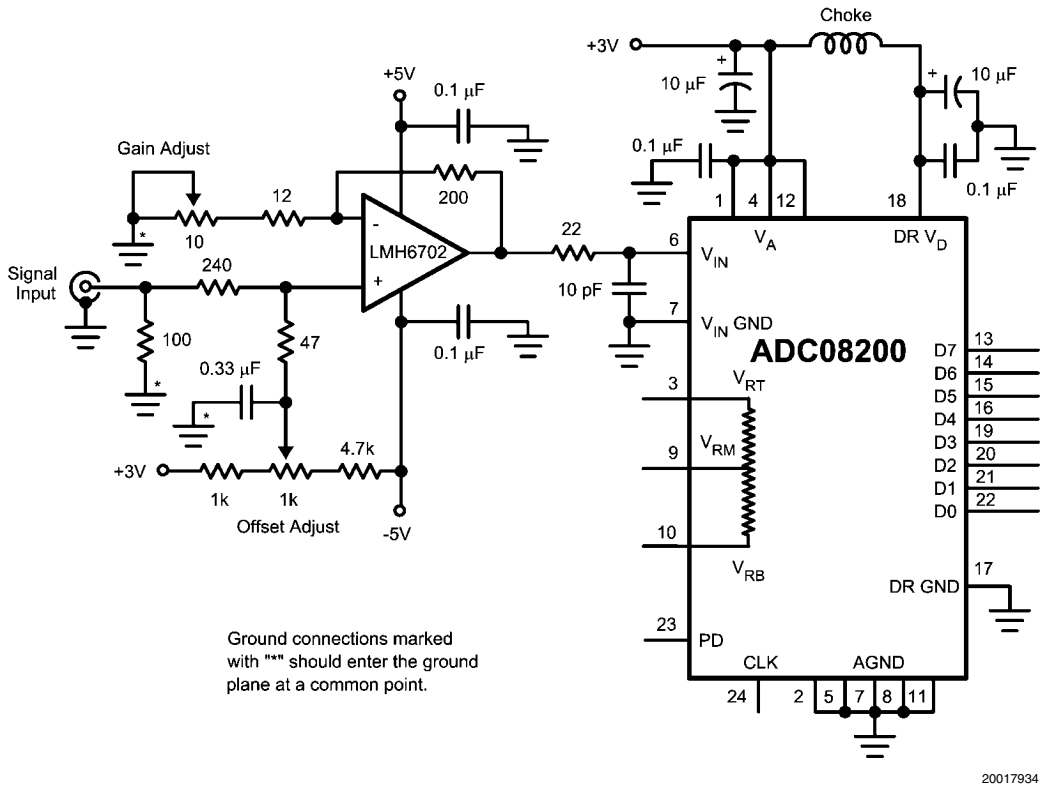


FIGURE 4. The input amplifier should incorporate some gain for best performance (see text).

3.0 POWER SUPPLY CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 10 µF tantalum or aluminum electrolytic capacitor should be placed within an inch (2.5 cm) of the A/D power pins, with a 0.1 µF ceramic chip capacitor placed within one centimeter of the converter's power supply pins. Leadless chip capacitors are preferred because they have low lead inductance.

While a single voltage source is recommended for the V_A and V_{DR} supplies of the ADC08200, these supply pins should be well isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A choke or 27Ω resistor is recommended between these supply lines with adequate bypass capacitors close to the supply pins.

As is the case with all high speed converters, the ADC08200 should be assumed to have little power supply rejection. None of the supplies for the converter should be the supply that is used for other digital circuitry in any system with a lot of digital power being consumed. The ADC supplies should be the same supply used for other analog circuitry.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 300 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC08200 power pins.

4.0 THE DIGITAL INPUT PINS

The ADC08200 has two digital input pins: The PD pin and the Clock pin.

4.1 The PD Pin

The Power Down (PD) pin, when high, puts the ADC08200 into a low power mode where power consumption is reduced to about 1.4 mW with the clock running, or to about 1 mW with the clock held low. Output data is valid and accurate about 1 microsecond after the PD pin is brought low.

The digital output pins retain the last conversion output code when either the clock is stopped or the PD pin is high.

4.2 The ADC08200 Clock

Although the ADC08200 is tested and its performance is guaranteed with a 200 MHz clock, it typically will function well with clock frequencies from 10 MHz to 230 MHz.

The low and high times of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC08200 is designed to maintain performance over a range of duty cycles. While it is specified and performance is guaranteed with a 50% clock duty cycle and 200 Msps, ADC08200 performance is typically maintained with clock high and low times of 0.65 ns and 0.87 ns, respectively, corresponding to a clock duty cycle range of 13% to 82.5% with a 200 MHz clock. Note that minimum low and high times may not be simultaneously asserted.

The **CLOCK** line should be series terminated at the clock source in the characteristic impedance of that line if the clock line is longer than

$$\frac{t_r}{6 \times t_{prop}}$$

where t_r is the clock rise time and t_{prop} is the propagation rate of the signal along the trace. Typical t_{prop} is about 150 ps/inch (59 ps/cm) on FR-4 board material.

If the clock source is used to drive more than just the ADC08200, the **CLOCK** pin should be a.c. terminated with a series RC to ground such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{prop} \times L}{Z_o}$$

where t_{PD} is the signal propagation rate down the clock line, "L" is the line length and Z_O is the characteristic impedance of the clock line. This termination should be located as close as possible to, but within one centimeter of, the ADC08200 clock pin. Further, this termination should be close to but beyond the ADC08200 clock pin as seen from the clock source. Typical t_{prop} is about 150 ps/inch on FR-4 board material. For FR-4 board material, the value of C becomes

$$C \geq \frac{6 \times 10^{-10} \times L}{Z_o}$$

Where L is the length of the clock line in inches.

This termination should be located as close as possible to, but within one centimeter of, the ADC08200 clock pin.

5.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A combined analog and digital ground plane should be used.

Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep all lines separated from each other by at least six times the height above the reference plane, and to keep the analog circuitry well separated from the digital circuitry.

The DR GND connection to the ground plane should not use the same feedthrough used by other ground connections.

High power digital components should not be located on or near a straight line between the ADC or any linear component and the power supply area as the resulting common return current path could cause fluctuation in the analog input “ground” return of the ADC.

Generally, analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. Clock lines should be isolated from ALL other lines, analog AND digital. Even the generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the ground plane.

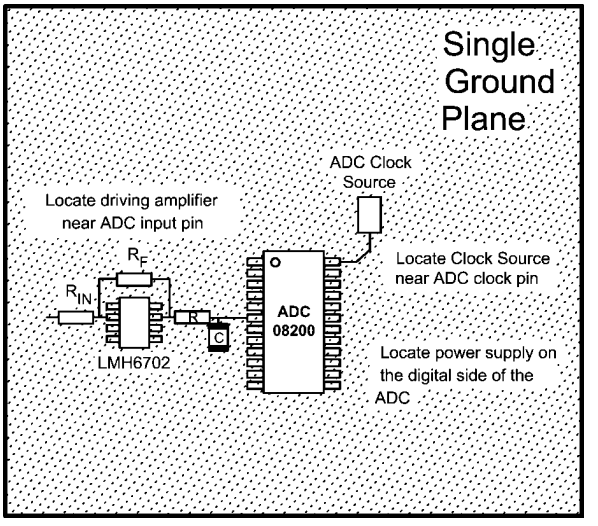


FIGURE 5. Layout Example

Figure 5 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed together away from any digital components.

6.0 DYNAMIC PERFORMANCE

The ADC08200 is a.c. tested and its dynamic performance is guaranteed. To meet the published specifications, the clock source driving the CLK input must exhibit less than 2 ps (rms) of jitter. For best a.c. performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See *Figure 6*.

It is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal. The clock signal can also introduce noise into the analog path.

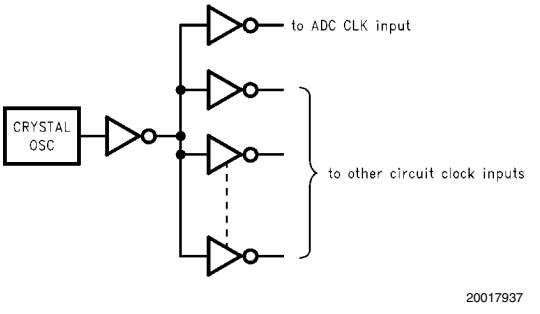


FIGURE 6. Isolating the ADC Clock from Digital Circuitry

7.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 300 mV below the ground pins or 300 mV above the supply pins. Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit undershoot that goes more than a volt below ground. A 51Ω resistor in series with the offending digital input will usually eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC08200. Such practice may lead to conversion inaccuracies and even to device damage.

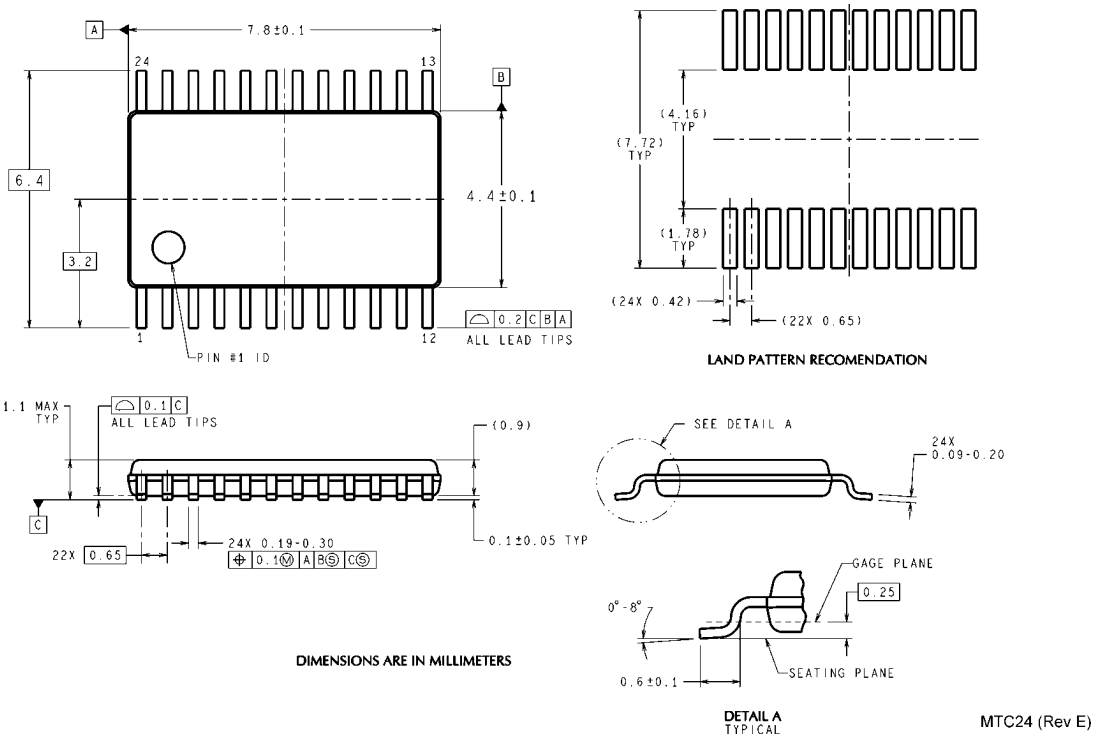
Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current is required from V_{DR} and DR GND. These large charging current spikes can couple into the analog section, degrading dynamic performance. Buffering the digital data outputs (with a 74AF541, for example) may be necessary if the data bus capacitance exceeds 5 pF. Dynamic performance can also be improved by adding 47Ω to 56Ω series resistors at each digital output, reducing the energy coupled back into the converter input pins.

Using an inadequate amplifier to drive the analog input. As explained in Section 2.0, the capacitance seen at the input alternates between 3 pF and 4 pF with the clock. This dynamic capacitance is more difficult to drive than is a fixed capacitance, and should be considered when choosing a driving device.

Driving the V_{RT} pin or the V_{RB} pin with devices that can not source or sink the current required by the ladder. As mentioned in Section 1.0, care should be taken to see that any driving devices can source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin. If these pins are not driven with devices than can handle the required current, these reference pins will not be stable, resulting in a reduction of dynamic performance.

Using a clock source with excessive jitter, using an excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance. The use of simple gates with RC timing is generally inadequate as a clock source.

Physical Dimensions inches (millimeters) unless otherwise noted



MTC24 (Rev E)

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE JEDEC REGISTRATION mo-153, VARIATION AD, DATED 7/93.

24-Lead Package TC
Order Number ADC08200CIMT
NS Package Number MTC24

Notes

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Тел: +7 (812) 336 43 04 (многоканальный)
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