MAXIM

μP Compatible 8 Bit A/D Converter

General Description

The MAX160 and MX7574 are low cost, microprocessor compatible 8 bit analog-to-digital converters which use the successive-approximation technique to achieve conversion times of 4μs (MAX160) and 15μs (MX7574).

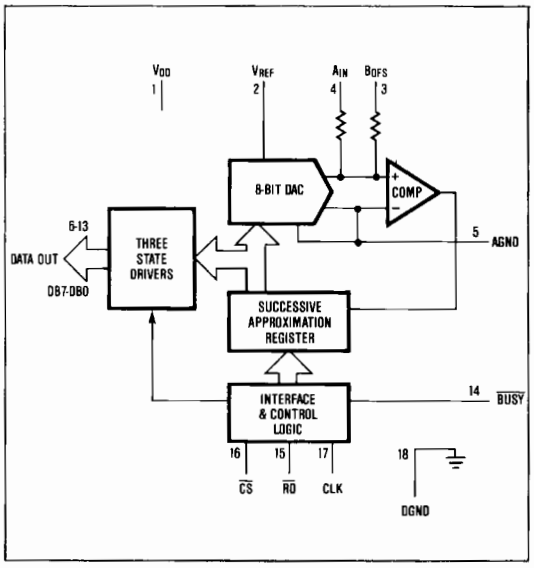
The A/Ds are designed to easily interface with microprocessors by appearing as a memory location or I/O port without the need for external interfacing logic. Data outputs use latched, three-state buffer circuitry to allow direct connection to a microprocessor data bus or system input port. Operation is simplified by an on-chip clock, +5V power supply requirement, and low supply current (5mA max).

The MAX160 provides major performance improvements over the AD7574 in accuracy and speed specifications as well as compatibility with TTL logic levels.

Applications

Digital Signal Processing
High Speed Data Acquisition
Telecommunications
Process Automation
Instrumentation
Avionics

Functional Diagram



Features

- **Improved Second Source (MAX160)**
- **Fast Conversion Time: 4μs (MAX160)**
  15μs (MX7574)
- **No Missing Codes Over Temperature**
- **Single +5V Supply**
- **Ratiometric Operation**
- **No External Clock Necessary**
- **Easy Interface To Microprocessors**

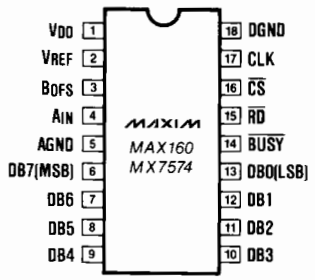
Ordering Information

PART	TEMP. RANGE	PACKAGE†	ERROR
MAX160CPN	0°C to +70°C	Plastic DIP	±½ LSB
MAX160CC/D	0°C to +70°C	Dice*	±½ LSB
MAX160CWN	0°C to +70°C	Small Outline	±½ LSB
MAX160EPN	-40°C to +85°C	Plastic DIP	±½ LSB
MAX160EWN	-40°C to +85°C	Small Outline	±½ LSB
MAX160MJN	-55°C to +125°C	CERDIP**	±½ LSB
MX7574KN	0°C to +70°C	Plastic DIP	±½ LSB
MX7574JN	0°C to +70°C	Plastic DIP	±¾ LSB
MX7574KCWN	0°C to +70°C	Small Outline	±½ LSB
MX7574JCWN	0°C to +70°C	Small Outline	±¾ LSB

† *All devices — 18 lead packages*
* *Consult factory for dice specifications.*
** *Maxim reserves the right to ship Ceramic Packages in lieu of CERDIP packages.*
Ordering Information continued on last page

Pin Configuration

Top View



µP Compatible 8 Bit A/D Converter

ABSOLUTE MAXIMUM RATINGS — MAX160, MX7574

Supply Voltage, V_{DD} to AGND ..... 0V, +7V
V_{DD} to DGND ..... 0V, +7V
AGND to DGND ..... -0.3V, V_{DD}
Digital Inputs/Outputs (Pins 6-17) .... DGND - 0.3V, V_{DD}+ 0.3V
Analog Inputs (Pins 2-4) ..... -20V, +20V
Power Dissipation (Any Package) to +70°C 670mW
Derate Above +70°C by ..... 8.3mW/°C

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Ranges
MAX160CPN, MX7574JN/KN/JCWN/KCWN ... 0°C to +70°C
MX7574AD/BD/AQ/BQ ..... -25°C to +85°C
MAX160EPN ..... -40°C to +85°C
MAX160MDN/MJN ..... -55°C to +125°C
MX7574SD/TD/SQ/TQ ..... -55°C to +125°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS — MAX160, MX7574

(V_{DD} = +5V, V_{REF} = -10V, Unipolar Configuration, Slow Memory Mode using External Clock f_{CLK} = 2.0MHz for MAX160 and 0.5MHz for MX7574 (Fig. 9), T_A = T_{MIN} to T_{MAX}, unless specified otherwise.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ACCURACY (f_{CLK} = 2.0MHz for MAX160 and 0.5MHz for MX7574)						
Resolution			8			bits
Relative Accuracy Error		MAX160, MX7574K/B/T			±½	LSB
		MX7574J/A/S			±¾	
Differential Non-Linearity		MAX160, MX7574K/B/T			±¾	LSB
		MX7574J/A/S			±⅞	
Full Scale Error (Note 1) (Gain Error)		MAX160, MX7574K/B/T; T_A = +25°C			±3	LSB
		MAX160, MX7574K/B/T; T_A = T_{MIN} to T_{MAX}			±4.5	
		MX7574J/A/S; T_A = +25°C			±5	
		MX7574J/A/S; T_A = T_{MIN} to T_{MAX}			±6.5	
Offset Error (Note 2)		**MAX160; T_A = +25°C**			**±20**	mV
		MAX160; T_A = T_{MIN} to T_{MAX}			**±30**	
		MX7574K/B/T; T_A = +25°C			±30	
		MX7574K/B/T; T_A = T_{MIN} to T_{MAX}			±50	
		MX7574J/A/S; T_A = +25°C			±60	
		MX7574J/A/S; T_A = T_{MIN} to T_{MAX}			±80	
Mismatch Between B_{OFS} and A_{IN} Resistances (Note 3)					±1.5	%
ANALOG INPUTS						
V_{REF} Input Resistance			5	10	15	kΩ
A_{IN} Input Resistance			10	20	30	kΩ
B_{OFS} Input Resistance			10	20	30	kΩ
Reference Voltage	V_{REF}	±5% for specified transfer accuracy		-10		V
Reference Voltage Range (Note 4)			-5		-15	V
Nominal Analog Input Range		Unipolar Mode	0		$\|V_{REF}\|$	V
		Bipolar Mode	$-\|V_{REF}\|$		$+\|V_{REF}\|$	
LOGIC INPUTS						
Logic Input High Voltage	V_{INH}	MAX160; $\overline{RD}$, $\overline{CS}$	2.4			V
		MX7574; $\overline{RD}$, $\overline{CS}$	3.0			
		MAX160, MX7574; CLK	3.0			
Logic Input Low Voltage	V_{INL}	MAX160, MX7574; $\overline{RD}$, $\overline{CS}$			0.8	V
		MAX160; CLK			0.8	
		MX7574; CLK			0.4	
Logic Input Current	I_{IN}	$\overline{RD}$, $\overline{CS}$, V_{IN} = 0, V_{DD}; T_A = +25°C			1	µA
		$\overline{RD}$, $\overline{CS}$, V_{IN} = 0, V_{DD}; T_A = T_{MIN} to T_{MAX}			10	
Clock Input High Current		V_{IN} = V_{DD}; T_A = +25°C			2	mA
		V_{IN} = V_{DD}; T_A = T_{MIN} to T_{MAX}			3	
Clock Input Low Current		V_{IN} = 0V; T_A = +25°C			1	µA
		V_{IN} = 0V; T_A = T_{MIN} to T_{MAX}			10	
Input Capacitance (Note 5)	C_{IN}	$\overline{RD}$, $\overline{CS}$		5	7	pF

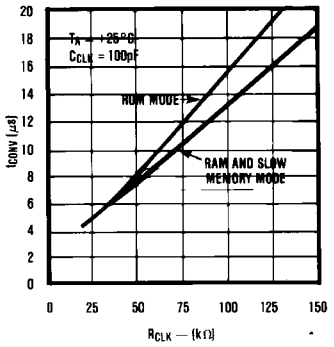
ELECTRICAL CHARACTERISTICS — MAX160, MX7574 (continued)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
LOGIC OUTPUTS							
Logic Output High Voltage	V_{OH}	$\overline{BUSY}$, DB0-DB7 I_{SRC} = 200μA		4.0			V
Logic Output Low Voltage	V_{OL}	$\overline{BUSY}$, DB0-DB7, I_{SINK} = 1.6mA	T_A = +25°C			0.4	V
			T_A = T_{MIN} to T_{MAX} MAX160 MX7574			 0.4 0.8	
Floating State Leakage	I_{LKG}	DB0-DB7, V_{OUT} = 0, V_{DD}	T_A = +25°C T_A = T_{MIN} to T_{MAX}			1 10	μA
Floating State Capacitance (Note 5)		DB0-DB7			5	7	pF
POWER REQUIREMENTS							
Power Supply Requirement	V_{DD}	+5V ±5% for specified performance		4.75		5.25	V
Power Supply Current	I_{DD}	A_{IN} = 0V, ADC in reset condition			1	5	mA
Reference Current	I_{REF}	Conversion complete, before reset				V_{REF}/5	V/kΩ

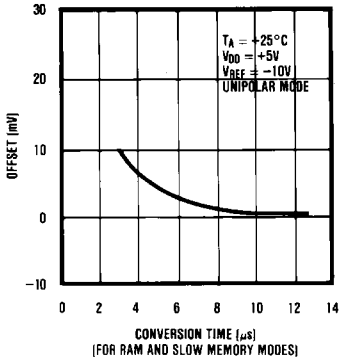
Note 1: Full scale error is measured after correcting for offset error. Max full-scale change from +25°C to T_{MIN} or T_{MAX} is ±1LSB.
Note 2: Maximum offset change from +25°C to T_{MIN} or T_{MAX} is ±10mV. Typical offset temperature coefficient is 50μV/°C.
Note 3: R_{BOFS}/R_{AIN} mismatch causes transfer function rotation about positive full scale. The effect is an offset and gain term when using the circuit of Figure 9b.
Note 4: Typical value, not guaranteed or subject to test.
Note 5: Guaranteed but not tested.

Typical Operating Characteristics

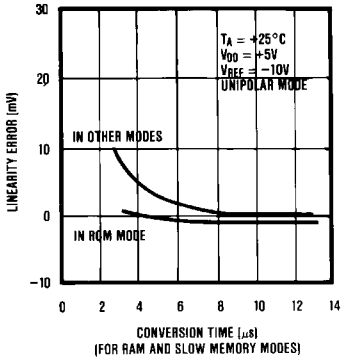
CONVERSION TIME USING INTERNAL CLOCK



OFFSET ERROR vs. CONVERSION TIME



LINEARITY ERROR vs. CONVERSION TIME



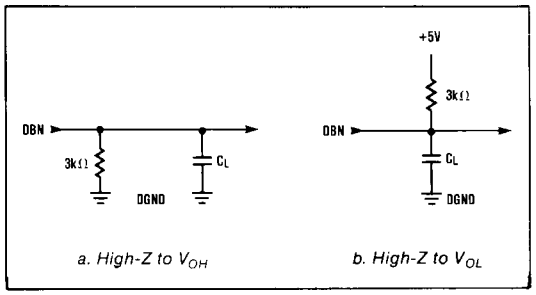


Figure 1. Load Circuits for Data Access Time Test

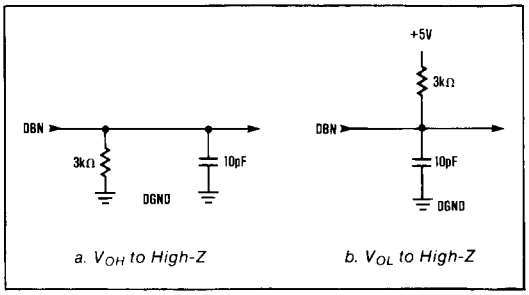


Figure 2. Load Circuits for Data Hold Time Test

TIMING CHARACTERISTICS (Note 1, 2) — MX7574

(V_{DD} = +5V, C_{CLK} = 100pF, R_{CLK} = 180kΩ, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{MIN}		T_A = T_{MAX}		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
STATIC RAM INTERFACE MODE (See Figure 5 and Table 5)										
$\overline{CS}$ Pulse Width Requirement	t_{CS}		100			150		150		ns
$\overline{RD}$ to $\overline{CS}$ Setup Time	t_{WSCS}		0			0		0		ns
$\overline{CS}$ to $\overline{BUSY}$ Propogation Delay (Note 2)	t_{CBPD}	C_L = 20pF C_L = 100pF		50 70	120 150		120 150		180 200	ns
$\overline{BUSY}$ to $\overline{RD}$ Setup Time	t_{BSR}		0			0		0		ns
$\overline{BUSY}$ to $\overline{CS}$ Setup Time	t_{BSCS}		0			0		0		ns
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		40 60	150 300		150 300		220 400	ns
Data Hold Time (Note 4)	t_{RHD}	MX7574S/T MX7574J/K/A/B	50 50	80 80	120 120	30 30	80 120	80 50	180 180	ns ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{RHCS}				250		200		500	ns
Reset Time Requirement			3			3		3		μs
Conversion Time Using Int CLK	t_{CONV}	See Graph		23						μs
Conversion Time Using Ext CLK	t_{CONV}	f_{CLK} = 500kHz	15			15		15		μs
ROM INTERFACE MODE (See Figure 6 and Table 6)										
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		40 60	150 300		150 300		220 400	ns
Data Hold Time (Note 4)	t_{RHD}	MX7574S/T MX7574J/K/A/B	50 50	80 80	120 120	30 30	80 120	80 50	180 180	ns ns
$\overline{RD}$ HIGH to $\overline{BUSY}$ Delay (Note 2)	t_{WBPD}	C_L = 20pF		700	1500		1000		2000	ns
$\overline{BUSY}$ to $\overline{RD}$ LOW Setup Time	t_{BSR}	(Note 5)								
Conversion Time Using Int CLK	t_{CONV}	See Graph		25						μs
SLOW MEMORY INTERFACE MODE (See Figure 7 and Table 7)										
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		40 60	150 300		150 300		220 400	ns
Data Hold Time (Note 4)	t_{RHD}	MX7574S/T MX7574J/K/A/B	50 50	80 80	120 120	30 30	80 120	80 50	180 180	ns ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay (Note 2)	t_{CBPD}	C_L = 20pF C_L = 100pF		40 60	120 150		120 150		180 200	ns
Reset Time Requirement			3			3		3		μs
Conversion Time Using Int Clk	t_{CONV}	See Graph		23						μs
Conversion Time Using Ext Clk	t_{CONV}	f_{CLK} = 500kHz	15			15		15		μs

Note 1: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
Note 2: Busy output crosses 0.8V or 2.4V.
Note 3: Outputs are loaded with circuits in Figure 1 and defined as the time required for an output to cross 0.8 or 2.4V.
Note 4: Outputs are loaded with circuits in Figure 2 and defined as the time required for an output to change 0.5V.
Note 5: $\overline{RD}$ can go low prior to $\overline{BUSY}$ = HIGH, but must not return HIGH until $\overline{BUSY}$ = HIGH. See Table 6.

μP Compatible 8 Bit A/D Converter

TIMING CHARACTERISTICS (Note 1, 2) — MAX160

(V_{DD} = +5V, C_{CLK} = 100pF, R_{CLK} = 22kΩ, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{MIN}		T_A = T_{MAX}		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
STATIC RAM INTERFACE MODE (See Figure 5 and Table 5)										
$\overline{CS}$ Pulse Width Requirement	t_{CS}		100			150		150		ns
$\overline{RD}$ to $\overline{CS}$ Setup Time	t_{WSCS}		0			0		0		ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay (Note 2)	t_{CBPD}	C_L = 20pF C_L = 100pF		60 70	100 110		100 110		130 150	ns
$\overline{BUSY}$ to $\overline{RD}$ Setup Time	t_{BSR}		0			0		0		ns
$\overline{BUSY}$ to $\overline{CS}$ Setup Time	t_{BSCS}		0			0		0		ns
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		50 60	90 100		90 100		120 140	ns
Data Hold Time (Note 4)	t_{RHD}			80	120		120		180	ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{RHCS}				250		230		500	ns
Reset Time Requirement	t_{RESET}		1.5			1.5		1.5		μs
Conversion Time Using Int CLK	t_{CONV}	R_{CLK} = 22kΩ	4	5	6	4	6	4	6	μs
Internal Clock Temperature Drift				250						ppm/°C
Conversion Time Using Ext CLK	t_{CONV}	f_{CLK} = 2.0MHz	4			4		4		μs
ROM INTERFACE MODE (See Figure 6 and Table 6)										
$\overline{RD}$ HIGH to $\overline{BUSY}$ Delay (Note 2)	t_{WBPD}	C_L = 20pF		800	1200		1200		1200	ns
$\overline{BUSY}$ to $\overline{RD}$ LOW Setup Time	t_{BSR}	(Note 5)								
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		50 60	90 100		90 100		120 140	ns
Data Hold Time (Note 4)	t_{RHD}			80	120		120		180	ns
Conversion Time Using Int CLK	t_{CONV}	R_{CLK} = 22kΩ	4	5	6	4	6	4	6	μs
SLOW MEMORY INTERFACE MODE (See Figure 7 and Table 7)										
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		0 0	90 100		90 100		120 140	ns
Data Hold Time (Note 4)	t_{RHD}			80	120		120		180	ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay (Note 2)	t_{CBPD}	C_L = 20pF C_L = 100pF		60 70	100 110		100 110		130 150	ns
Reset Time Requirement			1.5			1.5		1.5		μs
Conversion Time Using Int CLK	t_{CONV}	R_{CLK} = 22kΩ	4	5	6	4	6	4	6	μs
Conversion Time Using Ext CLK	t_{CONV}	f_{CLK} = 2.0MHz	4			4		4		μs

Note 1: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
Note 2: Busy output crosses 0.8V or 2.4V.
Note 3: Outputs are loaded with circuits in Figure 1 and defined as the time required for an output to cross 0.8 or 2.4V.
Note 4: Outputs are loaded with circuits in Figure 2 and defined as the time required for an output to change 0.5V.
Note 5: $\overline{RD}$ can go low prior to $\overline{BUSY}$ = HIGH, but must not return HIGH until $\overline{BUSY}$ = HIGH. See Table 6.

µP Compatible 8 Bit A/D Converter

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power supply voltage, +5V.
2	V_{REF}	Reference Input, nominal -10V.
3	B_{OFS}	Bipolar Offset Input, +10V for bipolar mode, connect to A_{IN} for unipolar mode.
4	A_{IN}	Analog input, 0 to +10V for unipolar mode, -10V to +10V for bipolar mode.
5	AGND	Analog Ground.
6	DB7	Three-state data output, bit 7 (MSB).
7	DB6	Three-state data output, bit 6.
8	DB5	Three-state data output, bit 5.
9	DB4	Three-state data output, bit 4.
10	DB3	Three-state data output, bit 3.

PIN	NAME	FUNCTION
11	DB2	Three-state data output, bit 2.
12	DB1	Three-state data output, bit 1.
13	DB0	Three-state data output, bit 0 (LSB).
14	$\overline{BUSY}$	BUSY output, $\overline{BUSY}$ goes low at the start of a conversion and returns high when the conversion is complete.
15	$\overline{RD}$	READ input, $\overline{RD}$ must be low to access data. See Digital Interface section.
16	$\overline{CS}$	CHIP-SELECT input. Used for conversion control or device addressing. See Digital Interface section.
17	CLK	External clock input/Internal clock frequency set input.
18	DGND	Digital Ground.

Detailed Description

Converter Operation

The MAX160/MX7574 uses the successive approximation technique to convert an unknown analog input to an 8 bit digital output code. The control logic provides easy interface to most microprocessors. Most applications require only passive clock components, a -10V reference, and a +5V power supply.

Figure 3 shows the MAX160/MX7574 functional diagram. When a start command is received from CS or RD (see Digital Interface Section), BUSY goes low indicating that the conversion is in progress. Successive bits, starting with the most significant bit (MSB), are applied to the input of a DAC. The comparator determines whether the addition of the bit causes the DAC output to be larger or smaller than the analog input, A_{IN}. If the DAC output is greater than A_{IN}, the trial bit is turned OFF, otherwise it is kept ON. Each successively smaller bit is tried and compared to A_{IN} in this manner until the least significant bit (LSB) decision has been made.

When all bits have been tried, $\overline{BUSY}$ goes high, indicating that the conversion is complete and the successive approximation register contains a valid representation of the analog input. The data can then be read using the RD input (see Digital Interface Section).

DAC Circuit Details

A thin film R-2R resistor network provides binarily weighted currents for each bit in the internal multiplying DAC (see Figure 4). N-channel MOS switches are used to steer current to either the summing junction or AGND depending on the DAC digital code. The A_{IN} and B_{OFS} input resistors also use series MOS switches (always ON) that match the DAC switches to maintain gain temperature tracking.

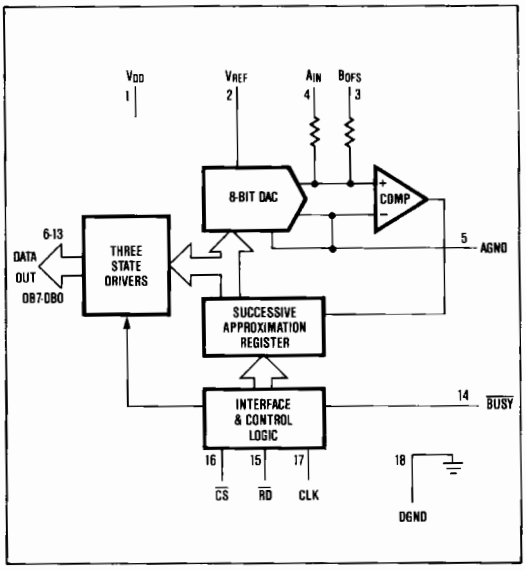


Figure 3. MAX160/MX7574 Functional Diagram

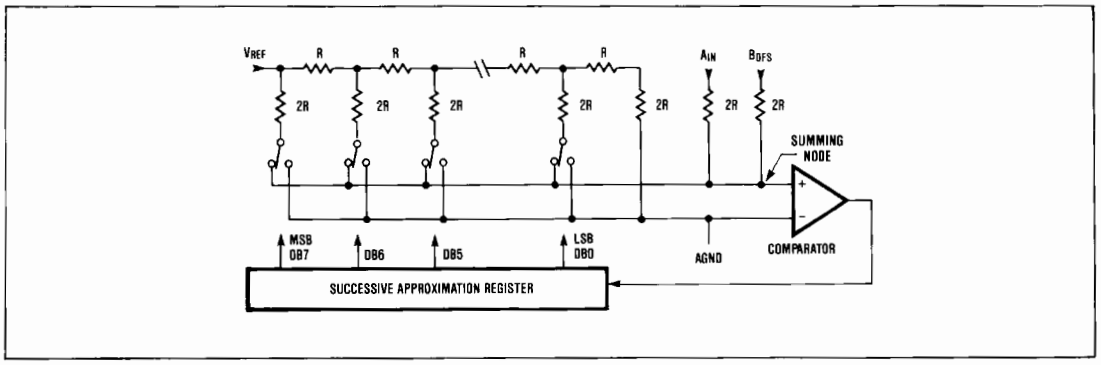


Figure 4. D/A Converter Used in the MAX160/MX7574

Table 5. Truth Table, Static Ram Mode

INPUTS		OUTPUTS		MAX160/MX7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	DB7-DB0	
L	H	H	HI-Z	Write Cycle (Start Convert)
L	⌐	H	HI-Z to DATA	Read Cycle (Data Read)
L	⌐	H	DATA to HI-Z	Reset Converter
H	X (Note 1)	X	HI-Z	Not Selected
L	H	L	HI-Z	No Effect (Converter Busy)
L	⌐	L	HI-Z	No Effect (Converter Busy)
L	⌐	L	HI-Z	Not Allowed, Conversion Error

Note 1: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the state of $\overline{CS}$ or $\overline{BUSY}$.

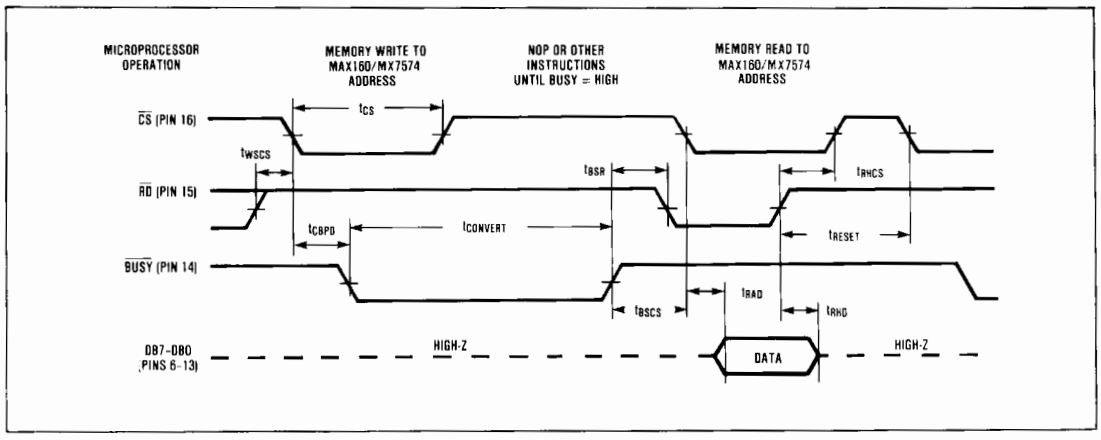


Figure 5. Static RAM Mode Timing Diagram

µP Compatible 8 Bit A/D Converter

Table 6. Truth Table, Rom Mode

INPUTS		OUTPUTS		MAX160/MX7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	DB7-DB0	
L	⌐	H	HI-Z to DATA	Data Read
L	⌐	⌐	DATA to HI-Z	Reset and Start New Conversion
L	⌐	L	HI-Z	No Effect (Converter Busy)
L	⌐	L	HI-Z	Not Allowed, Conversion Error

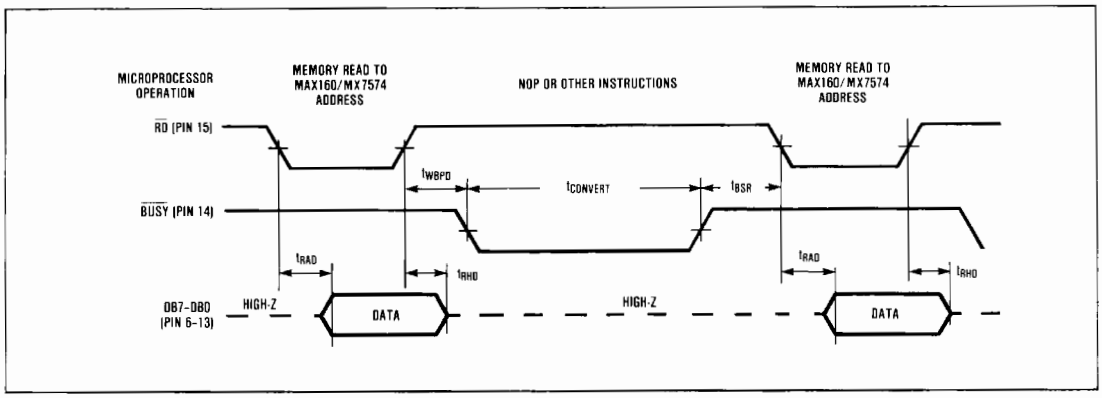


Figure 6. ROM Mode Timing Diagram ($\overline{CS}$ Held Low)

Table 7. Truth Table, Slow Memory Mode

INPUTS	OUTPUTS		MAX160/MX7574 OPERATION
$\overline{CS}$ & $\overline{RD}$	$\overline{BUSY}$	DB7-DB0	
H	H	HI-Z	Not Selected
⌐	H → L	HI-Z	Start Conversion
L	L	HI-Z	Conversion in Progress. µP in WAIT State
L	⌐	HI-Z to DATA	Conversion Complete. µP READS Data
⌐	H	DATA to HI-Z	Converter Reset and Deselected
H	H	HI-Z	Not Selected

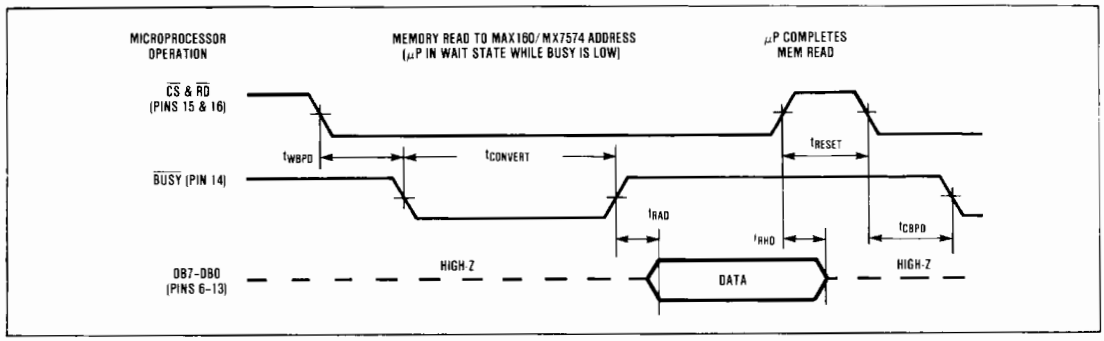


Figure 7. Slow Memory Mode Timing Diagram ($\overline{CS}$ and $\overline{RD}$ Tied Together)

Digital Interface

The MAX160/MX7574 has three interface modes which are determined by the timing of the CS and RD inputs.

Static RAM Interface Mode

Table 5 and Figure 5 show the truth table and timing requirements for interfacing the MAX160/MX7574 as a static RAM.

A conversion is started by executing a memory WRITE instruction to the MAX160/MX7574 address. Once a conversion is in progress, subsequent WRITE operations have no effect. Data is read by executing a memory READ operation to the A/D's address.

$\overline{BUSY}$ must be high before a READ is attempted. In other words, the elapsed time between WRITE and READ must be greater than the conversion time. Once $\overline{BUSY}$ is HIGH (end of conversion) the data READ can be performed. The data readout is destructive, since the MAX160/MX7574 is internally reset when $\overline{RD}$ goes high. Note that $\overline{CS}$ remaining LOW longer than the hold time (t_{RHCS}) will initiate a new conversion.

ROM Interface Mode

Table 6 and Figure 6 show the truth table and timing requirements for interfacing the MAX160/MX7574 as Read Only Memory.

In this mode the $\overline{CS}$ input is not used and is held low. The $\overline{RD}$ input is derived from the decoded device address. A data READ is initiated by executing a memory READ instruction to the MAX160/MX7574 address location. A conversion automatically starts when $\overline{RD}$ returns HIGH. Similar to the RAM mode, attempting a READ before $\overline{BUSY}$ goes HIGH will result in incorrect data being read.

The advantage of the ROM mode is its simplicity. The major disadvantage is that the data obtained is poorly defined in time since the conversion is performed at the end of a previous READ operation. This problem can be overcome by performing two READ operations back to back and only using the data from the second read.

Slow-Memory Interface Mode

Table 7 and Figure 7 show the truth table and timing requirements for interfacing the MAX160/MX7574 as slow memory. This mode is intended for processors that can be forced into a WAIT state for periods as long as the MAX160/MX7574 conversion time.

In this mode $\overline{CS}$ and $\overline{RD}$ are tied together. The decoded device address is used to drive $\overline{CS}/\overline{RD}$. The $\overline{BUSY}$ output is connected to the processor's READY input. A conversion is initiated by executing a memory READ to the MAX160/MX7574 address. $\overline{BUSY}$ then goes LOW and forces the processor into a WAIT state. At the end of the conversion, $\overline{BUSY}$ returns high and the data is available at the data outputs.

The major advantage of the slow memory mode is that it allows the processor to start and end a conversion and read the result with a single READ instruction.

Do not attempt a memory WRITE in this mode, since a three-state bus conflict will arise.

Interface Application Hints

Timing and Control

Failure to observe the timing restrictions of Figures 5-7 may cause the MAX160/MX7574 to change interface modes. For example, in the RAM mode, if $\overline{CS}$ is held low for too long, the converter moves into the ROM mode since a new conversion starts.

Logic Deglitching in μP Applications

Unspecified states in the address bus can cause glitches at the MAX160/MX7574 $\overline{CS}$ or $\overline{RD}$ inputs. Such glitches can cause undesired conversion starts, resets or data reads. The best method for avoiding these problems is to gate the address decode with $\overline{WR}$ or $\overline{RD}$ when in the RAM or ROM modes. In the slow memory mode use latched address inputs.

Initialization After Power-Up

To initialize the MAX160/MX7574 at power-up, perform a memory READ to its address location and ignore the data.

Clock

Internal Oscillator

The MAX160/MX7574 has in internal asynchronous clock oscillator which starts when a convert command is received and stops at the end of a conversion.

The oscillator requires an external resistor and capacitor connected as shown in Figure 8. The internal oscillator has good initial accuracy and stability over temperature and supply voltage. See Typical Operating Characteristics for typical conversion times versus R_{CLK} with C_{CLK} set at 100pF.

To prevent false triggering of the internal clock, R_{CLK} and C_{CLK} must be placed close to the CLK pin and coupling from the $\overline{CS}$ and $\overline{RD}$ inputs must be minimized.

µP Compatible 8 Bit A/D Converter

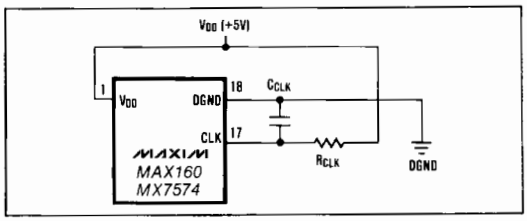


Figure 8. Connecting R_{CLK} and CLK to CLK Oscillator

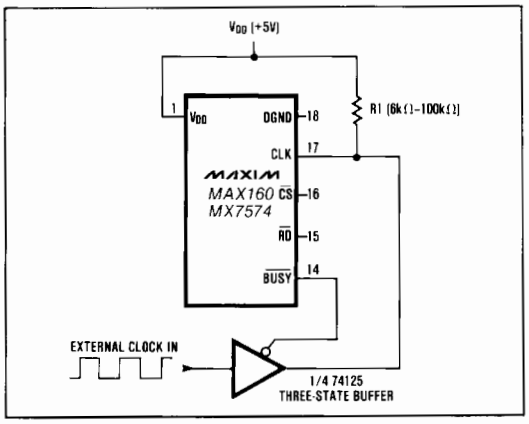


Figure 9. External Clock Operation (Static RAM and Slow Memory Mode)

Operation With External Clock

For applications where synchronous operation is required or the conversion time must be accurately controlled, an external clock can be used.

Figure 9 shows how an external clock is connected. The BUSY output is connected to the three-state enable input of a 74125 buffer. A 500kHz clock provides a conversion time of 15µs.

The external clock should be used only in the static-RAM or slow-memory modes and *not* in the ROM mode. Timing constraints for the external clock operation are as follows:

STATIC RAM MODE

1. When initiating a conversion, $\overline{CS}$ should go low on a positive clock edge to provide optimum settling time for the MSB.

2. A data READ can be performed at any time after BUSY = HIGH.

SLOW MEMORY MODE

1. When starting a conversion, $\overline{CS}$ and $\overline{RD}$ should go low on a positive clock edge to provide optimum settling time for the MSB.

Analog Considerations

Application Hints

Input Loading at V_{REF}, A_{IN}, and B_{OFS}

To prevent input loading effects due to the finite input resistance of these pins, low impedance driving sources must be used (i.e. op-amp buffers, or low output impedance references).

Ratiometric Operation

Ratiometric operation is inherent for the multiplying DAC scheme used on the MAX160/MX7574. However, the user must recognize that comparator limitations such as offset voltage, input noise and gain degrade the transfer function at reference voltages less than -10V.

Offset Correction

Offset error in the transfer function can be trimmed by offsetting the buffer that drives the A_{IN} input. This can be achieved either by summing a cancellation current into the amplifier's summing junction, or by tapping a voltage divider which sits between V_{DD} and V_{REF} and applying the tap voltage to the amplifier's non-inverting input. An example of the latter method can be seen in Figure 12.

Analog and Digital Ground

It is recommended that the AGND and DGND pins be connected locally to prevent noise injection into the A/D converter. In systems where the AGND-DGND connection is not local, clamp diodes should be connected between AGND and DGND to keep the two ground busses within one diode drop of each other.

Unipolar Binary Operation

Figures 10 shows the analog circuit connections and nominal transfer characteristic for unipolar operation. Calibration is as follows:

Offset

If offset trimming is required, it must be done in the signal conditioning circuitry used to drive the A_{IN} input in Figure 10. See also the offset trim example shown in Figure 12.

1. Apply -39.1mV (1 LSB) to the input of the buffer amplifier used to drive R1 (i.e. +39.1 mV at R1).

2. Adjust the offset potentiometer until DB7-DB1 are LOW and DB0 flickers.

Gain (Full Scale)

Offset adjustment must be performed prior to gain adjustment. To trim gain:

1. Apply -9.961V to the input of the buffer that drives R1 (i.e. +9.961V at R1).

2. Adjust trimpot R2 until DB7-DB1 are HIGH and DB0 flickers.

Bipolar (Offset Binary) Operation

Figure 11 illustrates the analog circuitry and transfer function for bipolar operation. The output coding is offset binary. Offset correction can be performed at the buffer amplifier used to drive the signal input terminals of the MAX160/MX7574. See Figure 12 for an example of how offset trimming can be performed. Calibration is as follows:

1. Adjust R6 and R7 for minimum resistance across the potentiometers.

2. Apply +10.000V to the buffer amplifier used to drive the signal input (i.e. -10.000V at R6). Then trim R6 or R7 (whichever is required) until DB7-DB1 are LOW and DB0 flickers.

3. Apply 0V to the buffer amplifier used to drive the signal input terminals. Then trim the offset circuit of the buffer amplifier until the ADC output flickers between 01111111 and 10000000.

4. Apply +10.000V to the input of the buffer amplifier (i.e. -10.000V as applied to R6). Then trim R2 until DB7-DB1 are LOW and DB0 flickers.

5. Apply -9.922V to the input of the buffer amplifier (i.e. +9.922V at the input side of R6). If the ADC output code is not 11111110 ± 1 bit, repeat the calibration procedure.

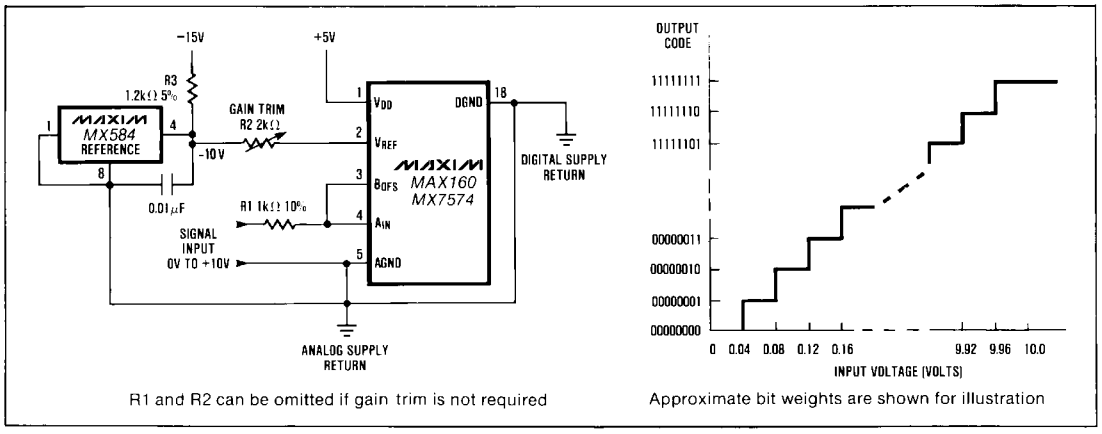


Figure 10. Unipolar (0V to +10V) Operation and Nominal Transfer Characteristic (Output Code is Straight Binary)

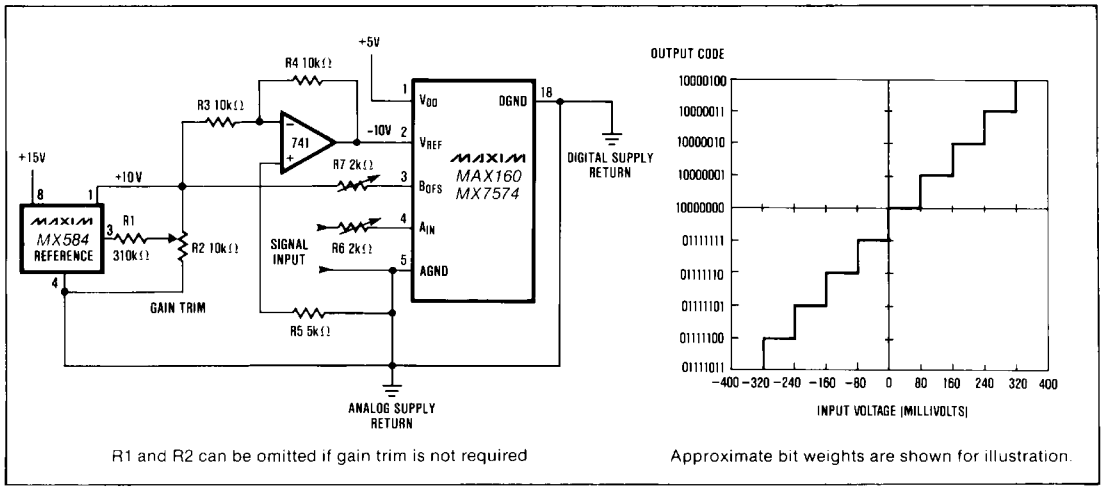


Figure 11. Bipolar (-10V to +10V) Operation and Nominal Transfer Characteristic Around Major Carry (Output Code is Offset Binary)

µP Compatible 8 Bit A/D Converter

Bipolar (Complementary Offset Binary) Operation

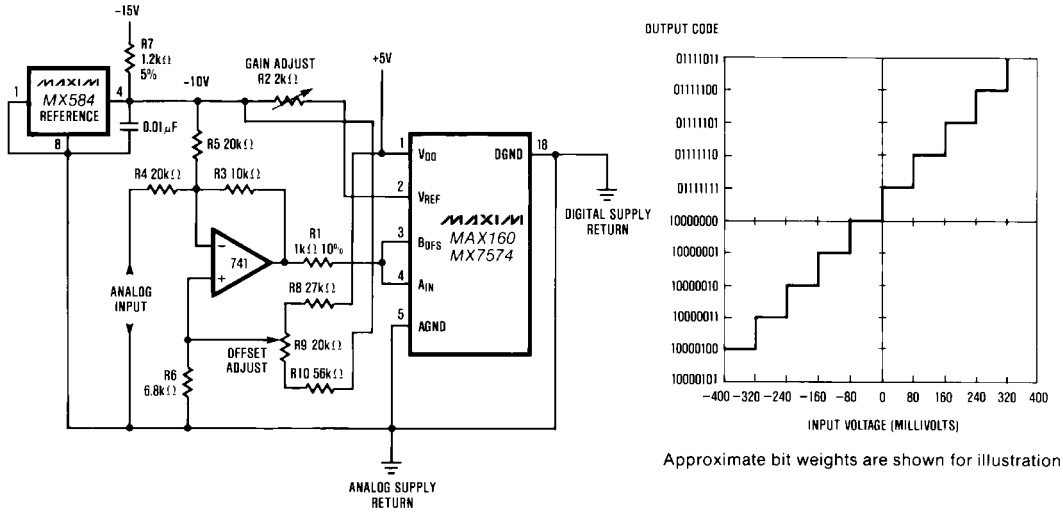
Figure 12 shows the analog connections for offset binary operation. The typical transfer characteristic is also shown. In this bipolar mode, the input signal (-10 to +10V) is conditioned and the A/D basically operates in unipolar mode (0 to +10V). Calibration is as follows (offset adjusted before gain):

Offset

1. Apply 0V to the analog input shown in Figure 12.
2. Adjust R9 until the converter output flickers between codes 01111111 and 10000000.

Gain (Full Scale)

1. Apply -9.922V across the analog input terminals shown in Figure 12.
2. Adjust R2 until DB7-DB1 are HIGH and DB0 flickers between HIGH and LOW.



Approximate bit weights are shown for illustration.

Note 1: R1 and R2 can be omitted if gain trim is not required.
Note 2: R8, R9 and R10 can be omitted if offset trim is not required.
Note 3: R6||R8||R10 = 5kΩ. If R8, R9 and R10 are not used, make R_6 = 5kΩ.

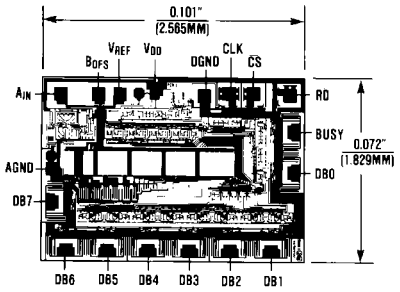
Figure 12. Bipolar (-10V to +10V) Operation and Nominal Transfer Characteristic Around Major Carry (Output Code is Complimentary Offset Binary)

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE†	ERROR
MX7574AQ	-25°C to +85°C	CERDIP**	±¾ LSB
MX7574BQ	-25°C to +85°C	CERDIP**	±½ LSB
MX7574SQ	-55°C to +125°C	CERDIP**	±¾ LSB
MX7574TQ	-55°C to +125°C	CERDIP**	±½ LSB
MX7574AD	-25°C to +85°C	Ceramic	±¾ LSB
MX7574BD	-25°C to +85°C	Ceramic	±½ LSB
MX7574SD	-55°C to +125°C	Ceramic	±¾ LSB
MX7574TD	-55°C to +125°C	Ceramic	±½ LSB

† *All devices — 18 lead packages*
** Maxim reserves the right to ship Ceramic Packages in lieu of *CERDIP packages.*

Chip Topography



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