Miniature Dual-Axis OIS Optimized MEMS Gyroscope

Description

The IDG-2030U (roll & pitch) dual-axis MEMS angular rate sensor is designed for optical image stabilization (OIS) applications in camera modules found in smart phones and other mobile devices.

The OIS gyro includes a narrow programmable full-scale range of ±46.5, ±93, ±187, and ±374 degrees/sec, fast sampling of the gyro output at up to 32KHz, low phase delay including a fast 20MHz read-out through SPI interface, very low rate noise at 5mdps/√Hz and extremely low power consumption at 2.7 mA. Factory-calibrated initial sensitivity reduces production-line calibration requirements.

The space saving 2.3 x 2.3 x 0.65mm LGA surface mount package is reflow solder compatible and RoHS compliant.

The IDG-2030U is pin and function compatible to IDG-2030.

Target Applications

- Smart Phone Camera OIS Modules
- OIS for Digital Still Camera and Video Cameras
- Electronic Image Stabilization (Video Jitter)
- Virtual Reality Mobile Devices

Key Features

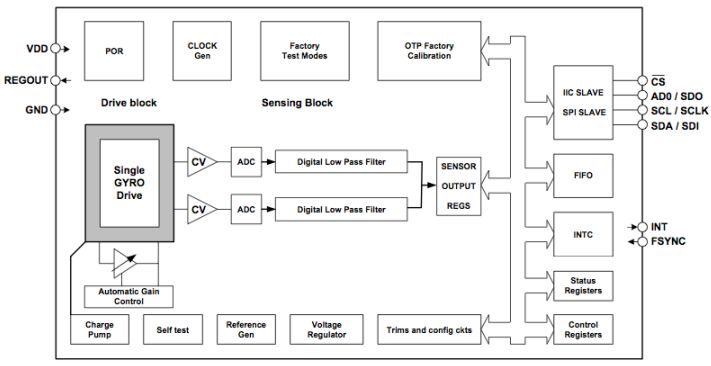
- Resistant to 36 kHz to 40 kHz ultrasonic wash frequencies
- Small 2.3 x 2.3 mm^2 & Low Profile 0.65 mm LGA Package
- Low 5mdps/√Hz Noise
- Minimum Phase Delay of 0.9° at 20Hz
- Narrow FSR Range from ±46.5 dps to ±374 dps
- High Resolution at up to 700 LSB/(º/s)
- Embedded 512-byte FIFO Enables Burst Read
- SPI and I^{2}C High-Speed Interfaces
- FSYNC Pin Supports Image Synchronization
- 400kHz Fast Mode I^{2}C Serial Interface
- 1 MHz R/W SPI Interface, 20MHz Read to Gyro
- Wide 16-Bit Rate Value Data Output
- User-Programmable Integrated Low-Pass Filters
- Wide 1.71V to 3.6V Supply Voltage Range
- Low 5mW Power Consumption
- 6µA Sleep Mode
- High 10,000*g* Shock Survivability

Ordering Information

Part Number	Axes	Temp Range	Pin / Package
IDG-2030U+	X,Y	-40°C to +85°C	12-Pin LGA

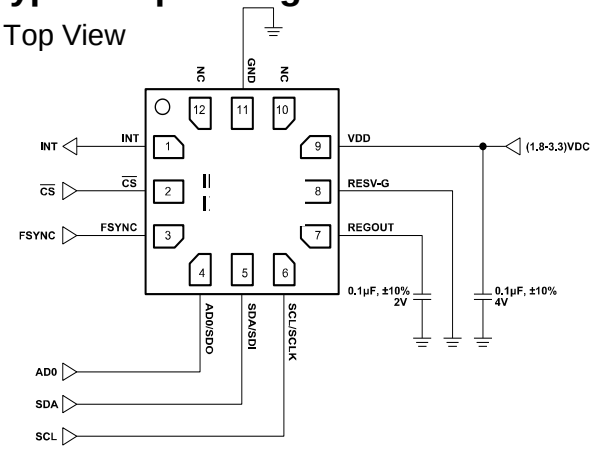
+Denotes RoHS- and green-compliant package.

Block Diagram



Typical Operating Circuit

Top View



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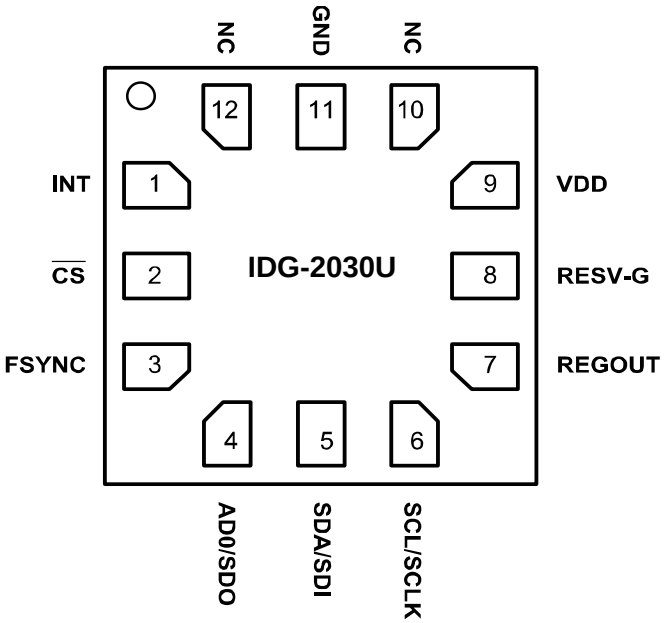
Contents

1 Pin Description

PIN	NAME	DESCRIPTION
1	INT	Interrupt Digital Output (Totem pole or open-drain)
2	$\overline{CS}$	SPI Chip Select (0=SPI mode, 1= I²C mode)
3	FSYNC	Frame Synchronization Digital Input. Connect to GND if not used.
4	AD0 / SDO	I²C Slave Address LSB (AD0); SPI Serial Data Output (SDO)
5	SDA/SDI	I²C Serial Data (SDA); SPI Serial Data Input (SDI)
6	SCL/SCLK	I²C Serial Clock (SCL); SPI Serial Clock (SCLK)
7	REGOUT	Regulator Output. Internal use only, bypass to GND with a 0.1µF cap.
8	RESV-G	Reserved. Connect to GND.
9	VDD	Analog and Digital I/O Power Supply. Bypass to GND with a 0.1µF cap.
10	NC	Not Internally Connected. May be used for PCB trace routing.
11	GND	Power Supply Ground
12	NC	Not Internally Connected. May be used for PCB trace routing.

Pin Configuration



Package: LGA 2.3 x 2.3 x 0.65 mm, Top View

2 Absolute Maximum Ratings

Parameter	Rating
Supply Voltage, VDD	-0.5V to 4.0V
REGOUT	-0.5V to 2V
Input Voltage Level (AD0, FSYNC)	-0.5V to VDD
SCL, SDA, INT (SPI enable)	-0.5V to VDD
SCL, SDA, INT (SPI disable)	-0.5V to VDD
Acceleration (Any Axis, unpowered)	10,000*g* for 0.2ms
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2kV (HBM); 250V (MM)
Latch-up	JEDEC Class II (2),125°C, ±100mA

Stress above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

3 Electrical Characteristics

Typical Operating Circuit, VDD = 2.5V and T_A=25°C unless otherwise noted.

Parameter	Conditions	Min	Typical	Max	Unit	Notes
Sensor Specifications						
GYRO SENSITIVITY Full-Scale Range	FS_SEL=0 (default) FS_SEL=1 FS_SEL=2 FS_SEL=3		±46.5 ±93 ±187 ±374		º/s º/s º/s º/s	1
Sensitivity Scale Factor	FS_SEL=0 FS_SEL=1 FS_SEL=2 FS_SEL=3		700 350 175 87.5		LSB/(º/s) LSB/(º/s) LSB/(º/s) LSB/(º/s)	
Gyro ADC Word Length			16		bits	
Sensitivity Scale Factor Tolerance	25°C		±3		%	1
Sensitivity Scale Factor Variation Over Temperature	-20°C to +75°C		±2		%	2
Nonlinearity	Best fit straight line; 25°C		±0.1		%	2
Cross-Axis Sensitivity			±2		%	1
GYRO ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±15		º/s	1
ZRO Variation Over Temperature	-20°C to +75°C		±8		º/s	2
SELF TEST RESPONSE			60		º/s	4
GYRO NOISE PERFORMANCE	FS_SEL=0					
Total RMS Noise	DLPFCFG=2 (92 Hz) DLPFCFG=1 (184 Hz) DLPFCFG=0 (256 Hz)		0.06 0.085 0.10		º/s-rms º/s-rms º/s-rms	1
Total Peak-to-Peak Noise	DLPFCFG=2 (92 Hz) DLPFCFG=1 (184 Hz) DLPFCFG=0 (256 Hz)		0.30 0.43 0.50		º/s-p-p º/s-p-p º/s-p-p	3
Low-frequency RMS noise Rate Noise Spectral Density	Bandwidth 1Hz to10Hz Bandwidth 0.1 to 1Hz At 10Hz		0.0055 0.0055 0.005		º/s-rms º/s-rms º/s/√Hz	1
GYRO MECHANICAL Mechanical Frequency Sensor Mechanical Bandwidth			27		 kHz kHz	 1 2
Ultrasonic Wash Frequency		36		40	kHz	2,5
VDD POWER SUPPLY Operating Voltage Range	Monotonic ramp. Ramp rate is 10% to 90% of the final value Two Axes Active	1.71		3.6	V	2
Power-Supply Ramp Rate		1		100	ms	2
Normal Operating Current			2.5		mA	1
Sleep Mode Current			6		µA	1
GYRO START-UP TIME ZRO Settling	DLPFCFG=0, to ±1º/s of Final From Sleep Mode to ready From Power On to ready		 35 50		 ms ms	
OPERATING TEMPERATURE RANGE					ºC	2
I²C ADDRESS	AD0 = 0 AD0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, AD0, SCLK, SDI, $\overline{CS}$) VIH, High Level Input Voltage VIL, Low Level Input Voltage CI, Input Capacitance		 0.7*VDD	 < 5	 0.3*VDD	 V V pF	2
DIGITAL OUTPUT (INT, SDO) V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ	0.9*VDD			V	2

Parameter	Conditions	Min	Typical	Max	Unit	Notes
V_{OL1}, LOW-Level Output Voltage $V_{OL.INT1}$, INT Low-Level Output Voltage Output Leakage Current t_{INT}, INT Pulse Width	R_{LOAD}=1MΩ OPEN=1, 0.3mA sink current OPEN=1 LATCH_INT_EN=0		 100 50	0.1*VDD 0.1	V V nA µs	
I^2C I/O (SCL, SDA)						2
V_{IL}, LOW Level Input Voltage			-0.5V to 0.3*VDD		V	
V_{IH}, HIGH-Level Input Voltage			0.7*VDD to VDD + 0.5V		V	
V_{hys}, Hysteresis			0.1*VDD		V	
V_{OL1}, LOW-Level Output Voltage	3mA sink current		0 to 0.4		V	
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V V_{OL} = 0.6V		3 6		mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf		20+0.1C_b to 250		ns	
C_I, Capacitance for Each I/O pin			< 10		pF	
INTERNAL CLOCK SOURCE						2
Sample Rate	Fchoice=0,1,2 SMPLRT_DIV=0		32		kHz	
	Fchoice=3; DLPFCFG=0 or 7 SMPLRT_DIV=0		8		kHz	
	Fchoice=3; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0		1		kHz	
Clock Frequency Initial Tolerance	CLK_SEL=0, 6; 25°C	-5		+5	%	
	CLK_SEL=1,2,3,4,5; 25°C	-1		+1	%	
Frequency Variation over Temperature	CLK_SEL=0,6		-10 to +10		%	
	CLK_SEL=1,2,3,4,5		±1		%	
PLL Settling Time	CLK_SEL=1,2,3,4,5		4		ms	

Note 1: Tested in production

Note 2: Derived from validation of characterization of parts, not guaranteed in production

Note 3: Peak-Peak noise data is based on measurement of RMS noise in production and at 99% normal distribution

Note 4: Assumes environmental noise less than 2dps

Note 5: Please refer to Ultrasonic Wash Application Note.

4 Timing Characteristics

4.1 I²C Timing Diagrams

Parameter	Conditions	Min	Typical	Max	Unit	Notes
I²C Timing Characteristics (I²C FAST-MODE)						1
f_{SCL}, SCL Clock Frequency		0		400	kHz	
$t_{HD.STA}$, START Condition Hold Time, repeated		0.6			µs	
t_{LOW}, SCL Low Period		1.3			µs	
t_{HIGH}, SCL High Period		0.6			µs	
$t_{SU.STA}$, START Condition Setup Time, repeated		0.6			µs	
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	
C_b, Capacitive Load for each Bus Line			< 400		pF	
$t_{VD.DAT}$, Data Valid Time				0.9	µs	
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	

Note 1: Derived from validation or characterization of parts, not guaranteed in production.

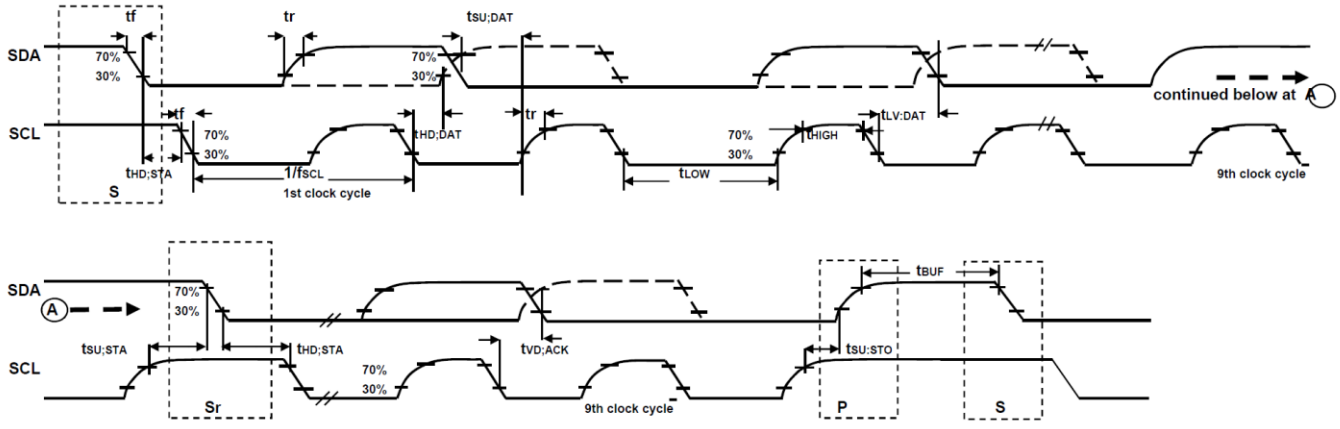


Figure 1: I²C Timing Diagram

4.2 SPI Timing Diagrams

Parameter	Conditions	Min	Typical	Max	Unit	Notes
SPI TIMING (f_{SCLK} = 1 MHz) R/W						1
f_{SCLK}, SCLK Clock Frequency				1	MHz	
t_{LOW}, SCLK Low Period		400			ns	
t_{HIGH}, SCLK High Period		400			ns	
$t_{SU.CS}$, CS Setup Time		8			ns	
$t_{HD.CS}$, CS Hold Time		500			ns	
$t_{SU.SDI}$, SDI Setup Time		11			ns	
$t_{HD.SDI}$, SDI Hold Time		7			ns	
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF			100	ns	
$t_{HD.SDO}$, SDO Hold Time		4				
tDIS.SDO, SDO Output Disable Time				50	ns	
tBUF, CS high time between transactions				600	ns	
SPI TIMING (f_{SCLK} = 20 MHz) Read						1, 2
f_{SCLK}, SCLK Clock Frequency				20	MHz	
t_{LOW}, SCLK Low Period		-	25	-	ns	
t_{HIGH}, SCLK High Period		-	25	-	ns	
$t_{SU.CS}$, CS Setup Time		25			ns	
$t_{HD.CS}$, CS Hold Time		25			ns	
$t_{SU.SDI}$, SDI Setup Time		5			ns	
$t_{HD.SDI}$, SDI Hold Time		6			ns	
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF			30	ns	
$t_{HD.SDO}$, SDO Hold Time		4				
$t_{DIS.SDO}$, SDO Output Disable Time				25	ns	
t_{BUF}, CS high time between transactions				600	ns	

Note 1: Derived from validation of characterization of parts, not guaranteed in production

Note 2: Read of Sensor registers only

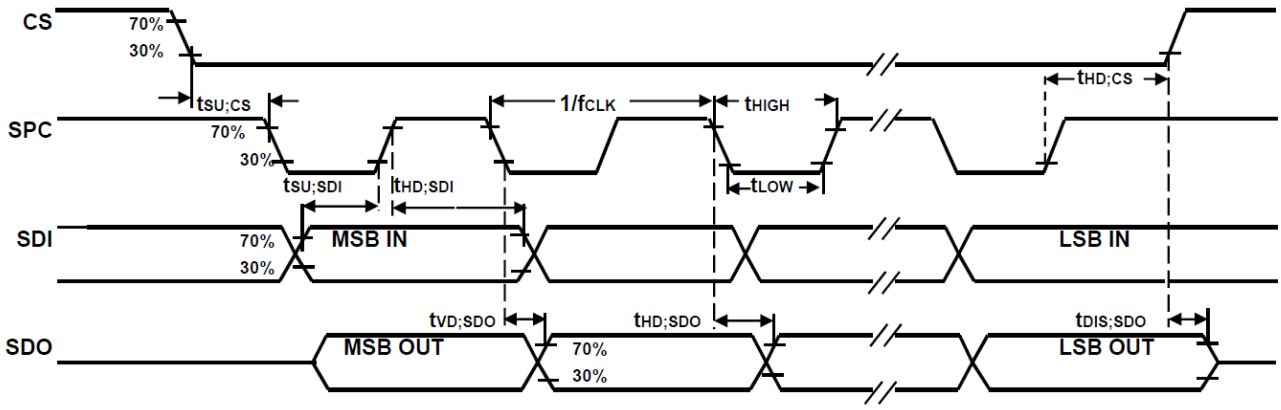


Figure 2: SPI Timing Diagram

5 Functional Description

The IDG-2030U is single-chip, digital output, 2 Axis MEMS gyroscope IC optimized for Optical Image Stabilization applications in mobile devices such as Smartphones, Tablets and Digital Still Cameras. It is designed to be resistant to ultrasonic wash frequencies ranging from 36 kHz to 40 KHz. It also features a 512-byte FIFO for applications such as Electronic Image Stabilization where the gyro output is sampled at a fast rate, e.g.1 kHz, but is only needed at the video frame rate (ex: 30 fps). The FIFO can store the samples within a frame, lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. The FSYNC (Frame Sync) input can alternatively be used by the host to generate an interrupt to allow precise timing to be achieved with Video Frame Sync at the host level for read out of the frame data.
The IDG-2030U consists of a single structure vibratory MEMS rate gyroscope, which detects rotation about the X&Y. When the gyro is rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pick off CV. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate.

This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The FSR range is optimized for image stabilization applications where the narrower range improves hand jitter detection accuracy via the 16 bit ADCs. User-selectable low-pass filters enable a wide range of cut-off frequencies. The ADC sample rate can be programmed to 32 kHz, 8 kHz, 1 kHz, 500 Hz, 333.3 Hz, 250 Hz, 200 Hz, 166.7 Hz, 142.9 Hz, or 125 Hz.

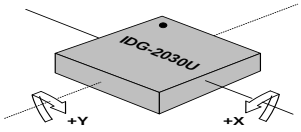


Figure 3: Orientation of Axes of Sensitivity and Polarity of Rotation

Figure 3 shows sensitivity axis orientation and rotation polarity. Note the pin 1 identifier for IDG-2030U.

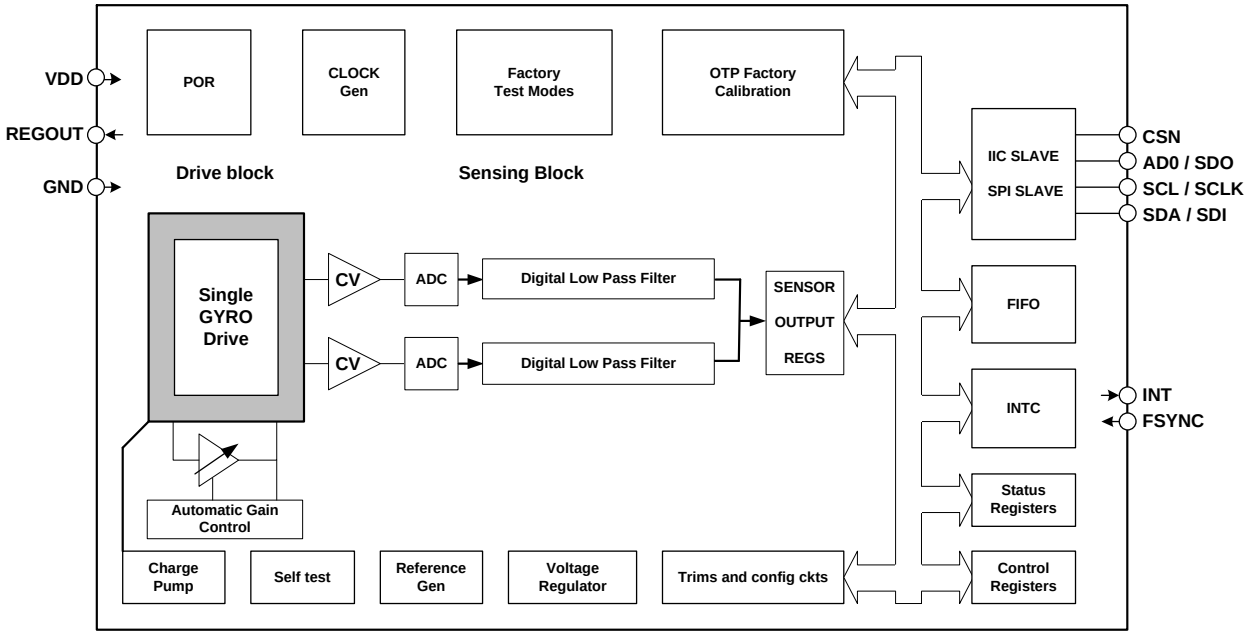


Figure 4: Block Diagram

Figure 4 identifies the key blocks. Two-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning is available in two axis XY configuration. After the signal is digitized, data is processed through a digital low pass filter, sensor data registers and stored at a FIFO. The devices communicate via a register selectable I^2C or SPI serial communications interface. Other blocks include on-board clocking, interrupts and bias circuits.

The IDG-2030U has both I^2C and SPI serial interfaces. The device always acts as a slave when communicating to the system processor. The LSB of the of the I^2C slave address is set by the AD0 pin.

The sensor data registers contain the latest gyro data. They are read-only registers, and are accessed via the Serial Interface. Data from these registers may be read anytime, however, the interrupt function may be used to determine when new data is available.

The IDG-2030U contains a 512-byte FIFO register that is accessible via both the I^2C and SPI Serial Interfaces. The FIFO configuration register determines what data goes into it, with possible choices being gyro data and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources), (2) new data is available to be read (from the FIFO and Data registers), and (3) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

The bias and LDO section generates the internal supply and the reference voltages and currents required by the IDG-2030U with its input as unregulated VDD of 1.71V to 3.6V. The LDO output is bypassed by a 0.1µF capacitor at REGOUT.

6 I2C Serial Interface

6.1 I2C Interface Overview

The Inter Integrated Circuit (I^2C) interface is a two-wire serial interface comprised of Serial Data (SDA, pin 5) and Serial Clock (SCL, pin 6). In general, the lines are open-drain and bi-directional. In a generalized I^2C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master. For the IDG-2030U, pin 4 (AD0) defines the LSB of the I^2C Slave Address.

The IDG-2030U always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the device is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin AD0. This allows up to two IDG-2030U devices to be connected to the same I^2C bus. When used in this configuration, the address of the one of the devices should be b1101000 (pin AD0 is logic low) and the address of the other should be b1101001 (pin AD0 is logic high).

6.2 I2C Communications Protocol

START (S) and STOP (P) Conditions

Communication on the I^2C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see *Figure 5* below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH.

Additionally, the bus remains busy if a repeated START (S) is generated instead of a STOP condition.

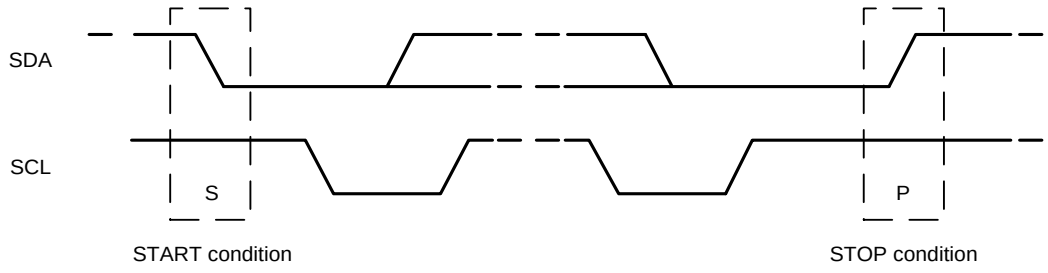


Figure 5: I^2C Start and Stop Conditions

Data Format / Acknowledge

I^2C data bytes are defined to be 8 bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and is unable to transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to *Figure 6*).

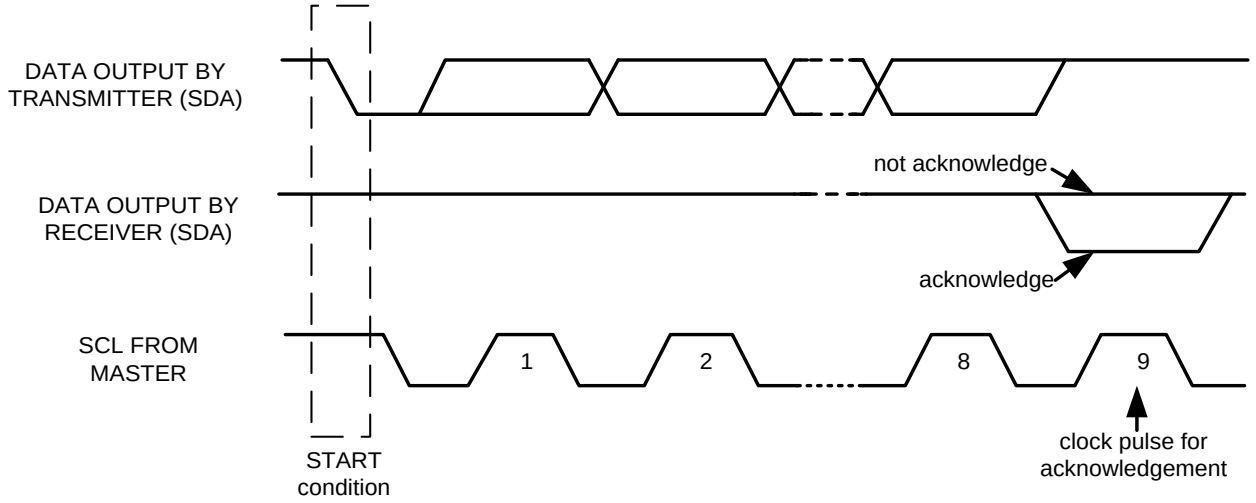


Figure 6: I²C Bus Acknowledge

Table 1 summarizes available I²C signals and commands.

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	The internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 1: I²C Signals and Commands

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (S), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

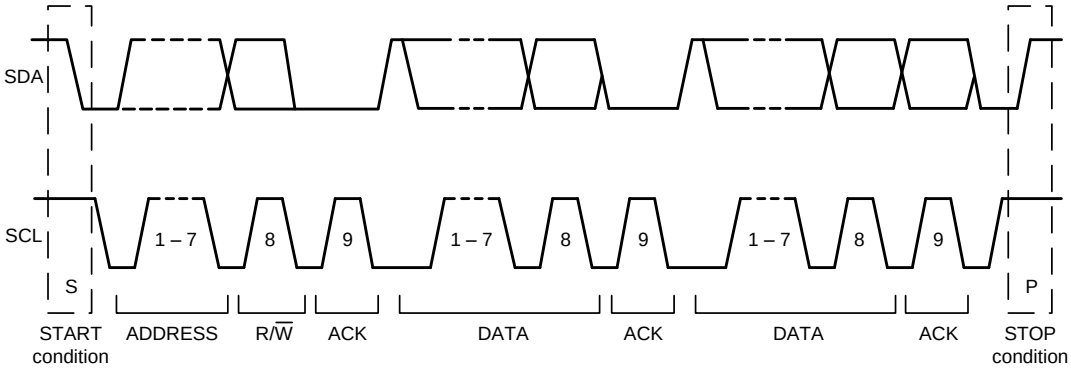


Figure 7: Complete I²C Data Transfer

To write the internal IDG-2030U registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the device acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the device acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the

last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the device automatically increments the register address and loads the data to the appropriate register. Single and two-byte write sequences are shown below.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal device registers, the master sends a start condition, followed by the I^2C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the device, the master transmits a start signal followed by the slave address and read bit. As a result, the device sends an ACK signal and the data. The communication ends with a Not Acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9^{th} clock cycle. The following shows single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

7 SPI Interface

7.1 SPI Interface Overview

The Serial Peripheral Interface Bus (SPI) is a 4-wire synchronous serial interface that uses two control and two data lines. The IDG-2030U always operates as a Slave device during standard Master-Slave SPI operation. With respect to the Master, the Serial Clock output (SCLK, pin 6), the Data Output (SDO, pin 4) and the Data Input (SDI, pin 5) are shared among the Slave devices. The Master generates an independent Chip Select ($\overline{CS}$, pin 2) for each Slave device; $\overline{CS}$ goes low at the start of transmission and goes back high at the end. The Serial Data Output (SDO) line remains in a high-impedance (high-z) state when the device is not selected, so it does not interfere with any active devices.

7.2 SPI Operation

1. Data is delivered MSB first and LSB last
2. Data is latched on rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. SCLK frequency is 1MHz max for SPI in full read/write capability mode.
   At 20MHz, its operation is limited to reading sensor registers only.
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation.

   The following 7 bits contain the Register Address. For multiple-byte Read/Writes, data is two or more bytes;

SPI Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. SPI supports Single or Burst Read/Writes.

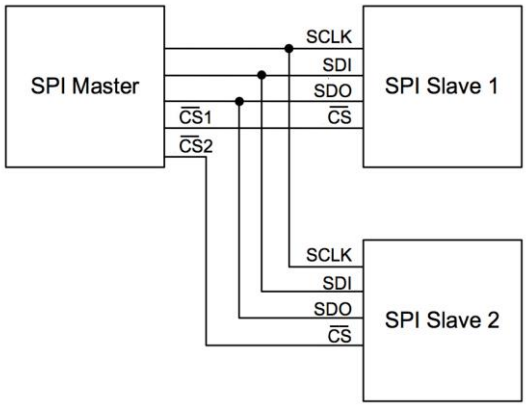


Figure 8: Typical SPI Master / Slave Configuration

As shown in *Figure 8*, each SPI slave requires its own Chip Select ($\overline{CS}$) line. SDO, SDI and SCLK lines are shared. Only one $\overline{CS}$ line is active (low) at a time ensuring that only one slave is selected at a time. The $\overline{CS}$ lines of other slaves are held high which causes their respective SDO pins to be high-Z.

8 Register Maps and Description

8.1 Naming Conventions

Register Names are in CAPITAL LETTERS, while Register Values are in italicized *CAPITAL LETTERS*. For example, the GYRO_XOUT_H register (Register 67) contains the 8 most significant bits, *GYRO_XOUT*[15:8], of the 16-bit X-Axis gyroscope measurement, *GYRO_XOUT*.

The reset value is 0x00 for all registers except register 117, WHO_AM_I , which resets to 0x85.

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
13	19	XG_OFFS_USRH	R/W	X_OFFS_USR[15:8]							
14	20	XG_OFFS_USRL	R/W	X_OFFS_USR[7:0]							
15	21	YG_OFFS_USRH	R/W	Y_OFFS_USR[15:8]							
16	22	YG_OFFS_USRL	R/W	Y_OFFS_USR[7:0]							
19	25	SMPLRT_DIV	R/W	SMPLRT_DIV[7:0]							
1A	26	CONFIG	R/W	-	FIFO _MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		
1B	27	GYRO_CONFIG	R/W	XG_ST	YG_ST	-	FS_SEL [1:0]		-	FCHOICE_B[1:0]	
23	35	FIFO_EN	R/W	-	XG _FIFO_EN	YG _FIFO_EN	-	-	-	-	-
37	55	INT_PIN_CFG	R/W	INT_LEVEL	INT_OPEN	LATCH _INT_EN	INT_RD _CLEAR	FSYNC_ INT_LEVEL	FSYNC _INT _MODE_EN	-	-
38	56	INT_ENABLE	R/W	-	-	-	FIFO _OFLOW _EN	FSYNC_INT _EN	-	-	DATA _RDY_EN
3A	58	INT_STATUS	R	-	-	-	FIFO _OFLOW _INT	FSYNC_INT	-	-	DATA _RDY_INT
43	67	GYRO_XOUT_H	R	GYRO_XOUT[15:8]							
44	68	GYRO_XOUT_L	R	GYRO_XOUT[7:0]							
45	69	GYRO_YOUT_H	R	GYRO_YOUT[15:8]							
46	70	GYRO_YOUT_L	R	GYRO_YOUT[7:0]							
6A	106	USER_CTRL	R/W	-	FIFO_EN	-	I2C_IF _DIS	-	FIFO _RESET	-	SIG_COND _RESET
6B	107	PWR_MGMT_1	R/W	DEVICE _RESET	SLEEP	-	-	-	CLKSEL[2:0]		
72	114	FIFO_COUNTH	R/W	-	-	-	-	-	-	FIFO_COUNT[9:8]	
73	115	FIFO_COUNTL	R/W	FIFO_COUNT[7:0]							
74	116	FIFO_R_W	R/W	FIFO_DATA[7:0]							
75	117	WHO_AM_I	R	-	WHO_AM_I[6:1]						-

Table 2: IDG-2030U Register Map

Note: Register names ending in _H and _L contain the high and low bytes of an internal register value.

8.2 Register Descriptions

This section describes the function and contents of each register for IDG-2030U gyroscope.

Note: *The device will come up in full power mode upon power-up. (i.e. not sleep mode). It is possible to configure the device to come up in "sleep" mode upon customer request for mass production.*

8.3 Registers 0x13 to 0x18 – Gyroscope Offset Adjustment Registers

XG_OFFS_USRH, XG_OFFS_USRL, YG_OFFS_USRH, and YG_OFFS_USRL

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
13	19	X_OFFS_USR[15:8]							
14	20	X_OFFS_USR[7:0]							
15	21	Y_OFFS_USR[15:8]							
16	22	Y_OFFS_USR[7:0]							

These registers are used to remove DC bias from the sensor outputs. The values in these registers are subtracted from the gyroscope sensor values before going into the sensor registers (see registers 67 to 72).

Parameters:
XG_OFFS_USR_H/L: 16-bit offset of X gyroscope (2's complement)
YG_OFFS_USR_H/L: 16-bit offset of Y gyroscope (2's complement)

8.4 Register 0x19 – Sample Rate Divider

SMPRT_DIV

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19	25	SMPLRT_DIV[7:0]							

This register specifies the divider from the gyroscope output rate that can be used to generate a reduced Sample Rate. Please note that this register is only effective when *FCHOICE_B*[1:0] = 2'b00 (Register 27) and *DLPF_CFG* = 1, 2, 3, 4, 5, or 6 (Register 26).
When *FCOICE_B*[1:0] = 2'b00 but *DLPF_CFG* = 0 or 7, the Sample Rate is fixed at 8kHz and the divider in this register does not apply. When *FCHOICE_B*[1:0] = 2'b01, 2'b10, or 2'b11, the Sample Rate is fixed at 32kHz and the divider in this register does not apply.
The sensor register output and FIFO output are both based on the Sample Rate. When this register is effective under the *FCOICE_B* and *DLPF_CFG* settings, the reduced Sample Rate is generated by the formula below:

Sample Rate = Gyroscope Output Rate / (1 + *SMPLRT_DIV*)
where Gyroscope Output Rate = 1kHz.

Parameters:
SMPLRT_DIV 8-bit unsigned value. The Sample Rate is determined by dividing the gyroscope output rate by this value.

8.5 Register 0x1A – Configuration

CONFIG

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1A	26	-	FIFO_MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		

This register configures the FIFO's mode of operation, the external Frame Synchronization (FSYNC) pin sampling and the Digital Low Pass Filter (DLPF) setting. Please note that the DLPF can only be used when *FCHOICE_B*[1:0] =2b'00 (Register 27).
When *FIFO_MODE* is set to 1 and the FIFO is full, additional writes will not be written to the FIFO. When this bit is equal to 0 and the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data. In order to enable and disable writing to the FIFO, use the enable bits in Register 35. For further information regarding the FIFO's operation, please refer to Register 116.
An external signal connected to the FSYNC pin can be sampled by configuring *EXT_SYNC_SET*. Signal changes to the FSYNC pin are latched so that short strobes may be captured. The latched FSYNC signal will be sampled at the Sampling Rate, as defined in register 25. After sampling, the latch will reset to the current FSYNC signal state.
The sampled value will be reported in place of the least significant bit in a sensor data register determined by the value of *EXT_SYNC_SET* according to the following table.

Chip	EXT_SYNC_SET	FSYNC Bit Location
IDG-2030U	0	Input disabled

	2	GYRO_XOUT_L[0]
	3	GYRO_YOUT_L[0]

Table 3: EXT_SYNC_SET

The DLPF is configured by *DLPF_CFG,* when *FCHOICE_B*[1:0] = 2b'00. The gyroscope is filtered according to the value of *DLPF_CFG* and *FCHOICE_B* as shown in *Table 4* below.

FCHOICE_B		DLPF_CFG	Gyroscope		
<1>	<0>		Bandwidth (Hz)	Delay (ms)	Fs (kHz)
0	0	0	250	0.97	8
0	0	1	184	2.9	1
0	0	2	92	3.9	1
0	0	3	41	5.9	1
0	0	4	20	9.9	1
0	0	5	10	17.85	1
0	0	6	5	33.48	1
0	0	7	3600	0.17	8
x	1	x	8800	0.064	32
1	0	x	3600	0.11	32

Table 4: F_CHOICE_B Register (Gyroscope Delay)

Note: Bit 7 is reserved.

Parameters:

FIFO_MODE	When set to 1 and the FIFO is full, additional writes will not be written to the FIFO. When equal to 0 and the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data. In order to disable writing to the FIFO, use the enable bits in Register 35.
EXT_SYNC_SET	3-bit unsigned value. Configures the FSYNC pin sampling.
DLPF_CFG	3-bit unsigned value. Configures the DLPF setting.

8.6 Register 0x1B – Gyroscope Configuration

GYRO_CONFIG

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1B	27	XG_ST	YG_ST	-	FS_SEL[1:0]		-	FCHOICE_B[1:0]	

This register is used to trigger gyroscope self-test and configure the gyroscope' full scale range. Gyroscope self-test permits users to test the mechanical and electrical portions of the gyroscope. When self-test is activated by setting XG_ST, YG_ST bits in register 27, the on-board electronics will actuate the appropriate sensor. This actuation will move the sensor's proof masses over a distance equivalent to a pre-defined Coriolis force. This proof mass displacement results in a change in the sensor output, which is reflected in the output signal. The output signal is used to observe the self-test response. The self-test response (STR) is stored in the sensor data output registers 67 – 72. This self-test-response is used to determine whether the part has passed or failed self-test

FS_SEL selects the full scale range of the gyroscope outputs according to the following *Table 5*.

FS_SEL	Full Scale Range
0	± 46.5
1	± 93
2	± 187
3	± 374

Table 5: FS-SEL and Full Scale Range

FCHOICE_B, in conjunction with *DLPF_CFG* (Register 26), is used to choose the gyroscope output setting. For further information regarding the operation of *FCHOICE_B*, please refer to Section 4.2. Note: Bit 2 is reserved.

Parameters:

XG_ST Setting this bit causes the X axis gyroscope to perform self-test.
YG_ST Setting this bit causes the Y axis gyroscope to perform self-test.
FS_SEL 2-bit unsigned value. Selects the full scale range of gyroscope.
FCHOICE_B 2-bit unsigned value used to choose the gyroscope output setting.

8.7 Register 0x23 – FIFO Enable

FIFO_EN

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
23	35	-	XG_ FIFO_EN	YG_ FIFO_EN	-	-	-	-	-

This register determines which sensor measurements are loaded into the FIFO buffer.
Data stored inside the sensor data registers (Registers 65 to 72) will be loaded into the FIFO buffer if a sensor's respective FIFO_EN bit is set to 1 in this register. The behavior of FIFO writes when the FIFO buffer is full can be configured with the *FIFO_MODE* bit (Register 26). In order to read the data in the FIFO buffer, the *FIFO_EN* bit (Register 106) must be enabled.
When a sensor's FIFO_EN bit is enabled in this register, data from the sensor data registers will be loaded into the FIFO buffer. The sensors are sampled at the Sample Rate as defined in Register 25. For further information regarding sensor data registers, please refer to Registers 65 to 72
Bits 7 and 3 through 0 are reserved.

Parameters:

XG_ FIFO_EN When set to 1, this bit enables GYRO_XOUT_H and GYRO_XOUT_L (Registers 67 and 68) to be written into the FIFO buffer.
YG_ FIFO_EN When set to 1, this bit enables GYRO_YOUT_H and GYRO_YOUT_L (Registers 69 and 70) to be written into the FIFO buffer.

8.8 Register 0x37 – INT Pin / Bypass Enable Configuration

INT_PIN_CFG

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
37	55	INT_LEVEL	INT_OPEN	LATCH _INT_EN	INT_RD _CLEAR	FSYNC_ INT_LEVEL	FSYNC _INT_ MODE_EN	-	-

This register configures the behavior of the interrupt signals at the INT pins. This register is also used to enable the FSYNC Pin to be used as an interrupt to the host application processor.
Bits 1 and 0 are reserved.

Parameters:

INT_LEVEL	When this bit is equal to 0, the logic level for the INT pin is active high. When this bit is equal to 1, the logic level for the INT pin is active low.
INT_OPEN	When this bit is equal to 0, the INT pin is configured as push-pull. When this bit is equal to 1, the INT pin is configured as open drain.
LATCH_INT_EN	When this bit is equal to 0, the INT pin emits a 50us long pulse. When this bit is equal to 1, the INT pin is held high until the interrupt is cleared.
INT_RD_CLEAR	When this bit is equal to 0, interrupt status bits are cleared only by reading INT_STATUS (Register 58) When this bit is equal to 1, interrupt status bits are cleared on any read operation.
FSYNC_INT_LEVEL	When this bit is equal to 0, the logic level for the FSYNC pin (when used as an interrupt to the host processor) is active high. When this bit is equal to 1, the logic level for the FSYNC pin (when used as an interrupt to the host processor) is active low.
FSYNC_INT_MODE_EN	When this bit is equal to 1, the FSYNC pin will trigger an interrupt when it transitions to the level specified by *FSYNC_INT_LEVEL*. When a FSYNC interrupt is triggered, the *FSYNC_INT* bit in Register 58 will be set to 1. An interrupt is sent to the host processor if the FSYNC interrupt is enabled by the *FSYNC_INT_EN* bit in Register 56. When this bit is equal to 0, the FSYNC pin is disabled from causing an interrupt.

8.9 Register 0x38 – Interrupt Enable

INT_ENABLE

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38	56	-	-	-	FIFO_OFLOW_EN	FSYNC_INT_EN	-	-	DATA_RDY_EN

This register enables interrupt generation by interrupt sources.
For information regarding the interrupt status for of each interrupt generation source, please refer to Register 58.
Bits 7 through 5, 2, and 1 are reserved.

Parameters:

FIFO_OFLOW_EN	When set to 1, this bit enables a FIFO buffer overflow to generate an interrupt.
FSYNC_INT_EN	When equal to 0, this bit disables the FSYNC pin from causing an interrupt to the host processor. When set to 1, this bit enables the FSYNC pin to be used as an interrupt to the host processor.

DATA_RDY_EN When set to 1, this bit enables the Data Ready interrupt. The Data Ready interrupt is triggered when all the sensor registers have been written with the latest gyro sensor data.

8.10 Register 0x3A – Interrupt Status

INT_STATUS

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3A	58	-	-	-	FIFO _OFLOW _INT	FSYNC _INT	-	-	DATA _RDY_INT

This register shows the interrupt status of each interrupt generation source. Each bit will clear after the register is read.
For information regarding the corresponding interrupt enable bits, please refer to Register 56.
Bits 7 through 5, 2, and 1 are reserved.

Parameters:

FIFO_OFLOW_INT This bit automatically sets to 1 when a FIFO buffer overflow interrupt has been generated.
The bit clears to 0 after the register has been read.

FSYNC_INT This bit automatically sets to 1 when an FSYNC interrupt has been generated.
The bit clears to 0 after the registers has been read.

DATA_RDY_INT This bit automatically sets to 1 when a Data Ready interrupt is generated.
The bit clears to 0 after the register has been read.

8.11 Registers 0x43 to 0x46 – Gyroscope Measurements

GYRO_XOUT_H, GYRO_XOUT_L, GYRO_YOUT_H, and GYRO_YOUT_L

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
43	67	GYRO_XOUT[15:8]							
44	68	GYRO_XOUT[7:0]							
45	69	GYRO_YOUT[15:8]							
46	70	GYRO_YOUT[7:0]							

These registers store the most recent gyroscope measurements. Gyroscope measurements are written to these registers at the Sample Rate as defined in Register 25.
The gyroscope sensor registers continuously update at the user selectable ODR sample rate whenever the serial interface is idle. It is recommended to use burst reads on host interface to guarantee a read of sensor registers will read measurements from the same sampling instant. Note that if burst reads are not used, the user is responsible for ensuring a set of single byte reads correspond to a single sampling instant by checking the Data Ready interrupt. Failing to do so, may result in reading the low and high byte of the same sensor from different samples which could appear as noise peaks to the user for example. The following should be considered for single byte read mode:

1. Data_RDY_INT gets generated any time the sensor registers get updated with the sensor data. The frequency of this interrupt is the same as the ODR which is user selectable. The INT Configurations, INT status register and INT pin can be configured using the user register 37h, 38h and 3Ah.

2. The sensor register outputs are 16 bits (2 bytes). Both bytes should be read at the same time in order to get reliable data using burst mode. If a single byte read is used, the host needs to read the bytes back to back after Data_RDY_INT is set to ensure both bytes are from same sample.
3. The sensor registers should be read at a faster rate than the selected ODR with the read cycle preferably completed for all the sensors to get consistent and reliable output.

Each 16-bit gyroscope measurement has a full scale defined in *FS_SEL* (Register 27). For each full scale setting, the gyroscopes' sensitivity per LSB in *GYRO_xOUT* is shown in *Table 6* below:

FS_SEL	Full Scale Range
0	± 46.5
1	± 93
2	± 187
3	± 374

Table 6: Gyro Full-Scale Sensitivity per LSB

Parameters:

GYRO_XOUT 16-bit 2's complement value.
Stores the most recent X axis gyroscope measurement.

GYRO_YOUT 16-bit 2's complement value.
Stores the most recent Y axis gyroscope measurement.

8.12 Register 0x6A – User Control

USER_CTRL

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6A	106	-	FIFO_EN	-	I2C_IF _DIS	-	FIFO _RESET	-	SIG_COND _RESET

This register allows the user to enable and disable the FIFO buffer and choose the primary I^2C interface. The FIFO buffer, sensor signal paths and sensor registers can also be reset using this register.
The primary SPI interface will be enabled in place of the disabled primary I^2C interface when *I2C_IF_DIS* is set to 1.
When the reset bits (*FIFO_RESET* and *SIG_COND_RESET*) are set to 1, these reset bits will trigger a reset and then clear to 0.
Bits 7, 5, 3, and 1 are reserved.

Parameters:

FIFO_EN When set to 1, this bit enables FIFO operations.
When this bit is cleared to 0, the FIFO buffer is disabled. The FIFO buffer cannot be read from while disabled. However, it can still be written to. In order to disable writing to the FIFO, please use the enable bits in Register 35.
The FIFO buffer's data will not be lost unless the FIFO is reset, or unless power cycled or soft reset.

I2C_IF_DIS When set to 1, this bit disables the primary I^2C interface and enables the SPI interface instead.

FIFO_RESET This bit resets the FIFO buffer *w*hen set to 1 while *FIFO_EN* equals 0. This bit automatically clears to 0 after the reset has been triggered.

SIG_COND_RESET When set to 1, this bit resets the signal paths for all sensors. This operation will also clear the sensor registers. This bit automatically clears to 0 after the reset has been triggered.

8.13 Register 0x6B – Power Management 1

PWR_MGMT_1

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6B	107	DEVICE _RESET	SLEEP	-	-	-	CLKSEL[2:0]		

This register allows the user to configure the power mode and clock source. It also provides a bit for resetting the entire device.
By setting *SLEEP* to 1, the device can be put into low power sleep mode.
An internal 20MHz oscillator or the gyroscope based clock (PLL) can be selected as the device clock source. The PLL is the default clock source upon power up. In order for the gyroscope to perform to spec, the PLL must be selected as the clock source.
When the internal 20MHz oscillator is chosen as the clock source, the device can operate while having the gyroscope disabled. However, this is not a recommended normal operating mode.
The clock source can be selected according to *Table 7*.

CLKSEL	Clock Source
0	Internal 20MHz oscillator
1	PLL
2	PLL
3	PLL
4	PLL
5	PLL
6	Internal 20MHz oscillator
7	Reserved

Table 7: Clock Source Select CLKSEL

Bits 5 and 4 are reserved.

Parameters:

DEVICE_RESET When set to 1, this bit resets all internal registers to their default values. The bit automatically clears to 0 once the reset is done. The default values for each register can be found in Section 3.
SLEEP When set to 1, this bit puts the DEVICE into sleep mode.
CLKSEL 3-bit unsigned value. Specifies the clock source of the device.

8.14 Register 0x72 and 0x73 – FIFO Count Registers

FIFO_COUNT_H and FIFO_COUNT_L

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
72	114	-	-	-	-	-	-	FIFO_COUNT[9:8]	
73	115	FIFO_COUNT[7:0]							

These registers keep track of the number of samples currently in the FIFO buffer in terms of the number of bytes stored.
These registers shadow the FIFO Count value. Both registers are loaded with the current sample count when FIFO_COUNT_H (Register 114) is read.
Note: Reading only FIFO_COUNT_L will not update the registers to the current FIFO COUNT value. FIFO_COUNT_H must be accessed first to update the contents of both these registers. *FIFO_COUNT* should always be read in high-low order in order to guarantee that the most current FIFO Count value is read.
Bits 7 through 2 of Register 114 are reserved.

Parameters:

FIFO_COUNT	16-bit unsigned value. Indicates the number of bytes stored in the FIFO buffer. This number is in turn the number of bytes that can be read from the FIFO buffer and it is directly proportional to the number of samples available given the set of sensor data bound to be stored in the FIFO (register 35).

8.15 Register 0x74 – FIFO Read Write

FIFO_R_W

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
74	116	FIFO_DATA[7:0]							

This register is used to read and write data from the FIFO buffer.
Data is written to the FIFO in order of register number (from lowest to highest). If all the FIFO enable flags (see below) are enabled, the contents of registers 65 through 72 will be written in order at the Sample Rate.
The contents of the sensor data registers (Registers 65 to 72) are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN (Register 35).
If the FIFO buffer has overflowed, the status bit *FIFO_OFLOW_INT* is automatically set to 1. This bit is located in INT_STATUS (Register 58). When the FIFO buffer has overflowed, the treatment of the new data is determined by the *FIFO_MODE* bit in Register 26.
Check *FIFO_COUNT* to ensure that the FIFO buffer is not read when empty.

Parameters:
FIFO_DATA 8-bit data transferred to and from the FIFO buffer.

8.16 Register 0x75 – Who Am I

WHO_AM_I

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
75	117	-	WHO_AM_I[5:0]						-

This register is used to verify the identity of the device. The default value of the register is 0x85. Bits 0 and 7 are reserved. (Hard coded to 1)

Parameters:
WHO_AM_I The Power-On-Reset value of Bit6:Bit1 is 000 010.

9 Applications Information

9.1 Typical Operating Circuits

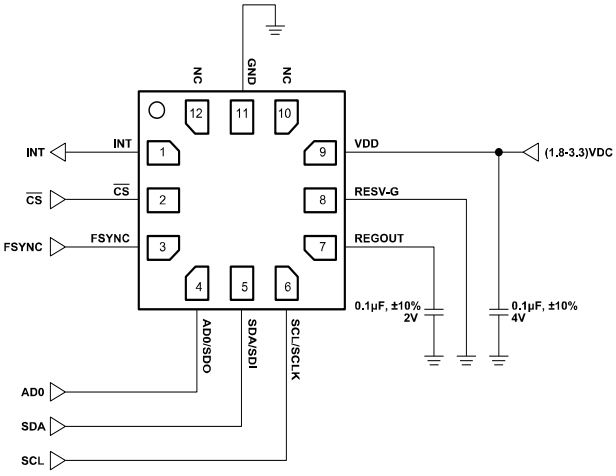


Figure 9: I²C Operation

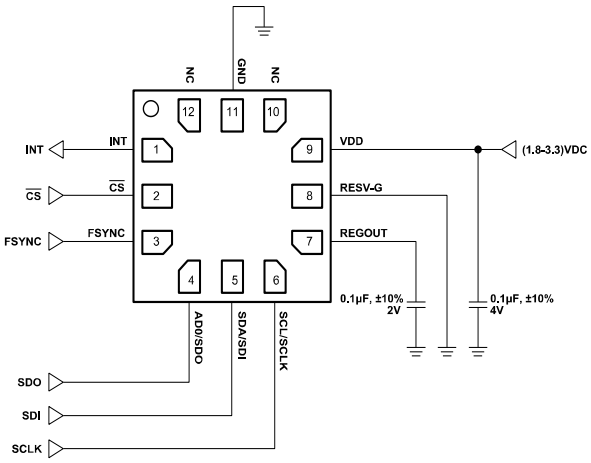


Figure 10: SPI Operation

9.2 System Bus Logic Levels

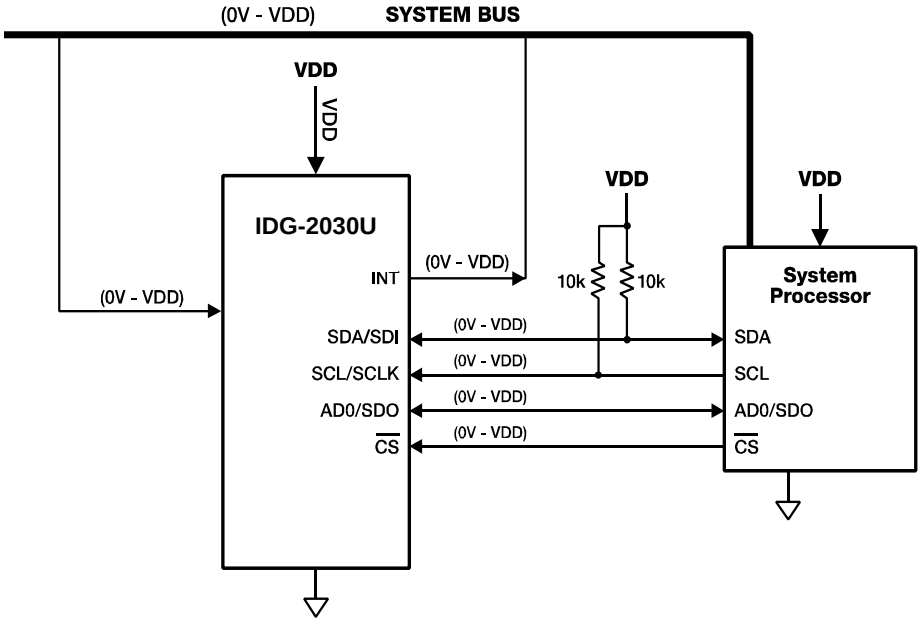


Figure 11: System Bus Logic Levels

As shown in *Figure 11*, the recommended logic levels for signal and data lines are 0V and VDD.

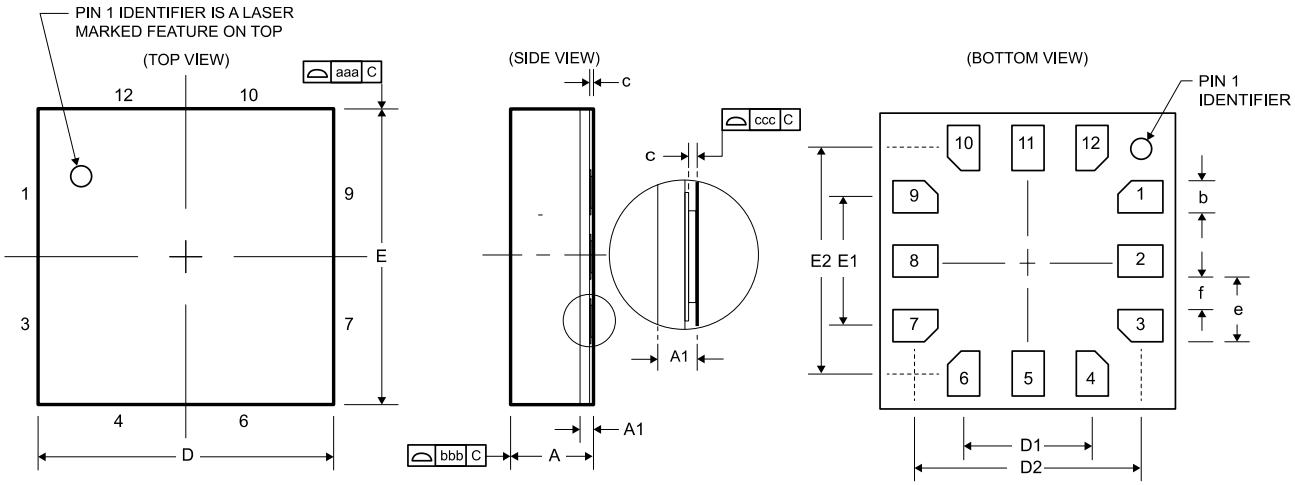
9.3 Adjustable Phase Delay

Parameters	FCHOICE_B		DLPF Configuration	Low pass Cutoff Fc	Frequency	Resulting Phase Delay	Units
Phase Delay	**1**	**0**					
SPI at 20MHz, Typical Operating Circuit, VDD = 2.5V, T_A=25°C.	0	1	X	Bypass	20Hz	0.9	Deg
	1	1	0	250Hz	20Hz 10Hz	7 3.5	Deg Deg
	1	1	1	184Hz	20Hz 10Hz	20 10	Deg Deg
	1	1	2	92Hz	20Hz 10Hz	28 14	Deg Deg

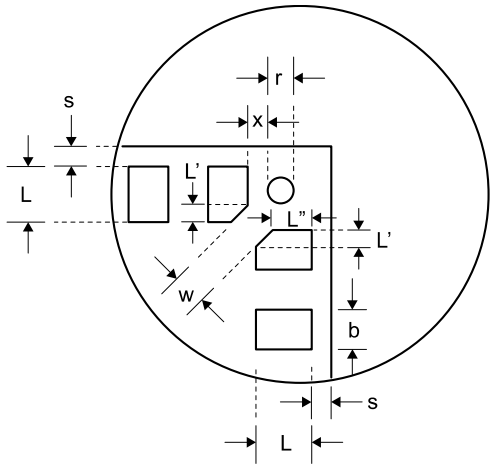
Table 8: Adjustable Phase Delay with FCHOICE_B Register and DLPF Settings

The phase delay is configurable with registers FCHOICE_B and DLPF as shown in *Table 8.*

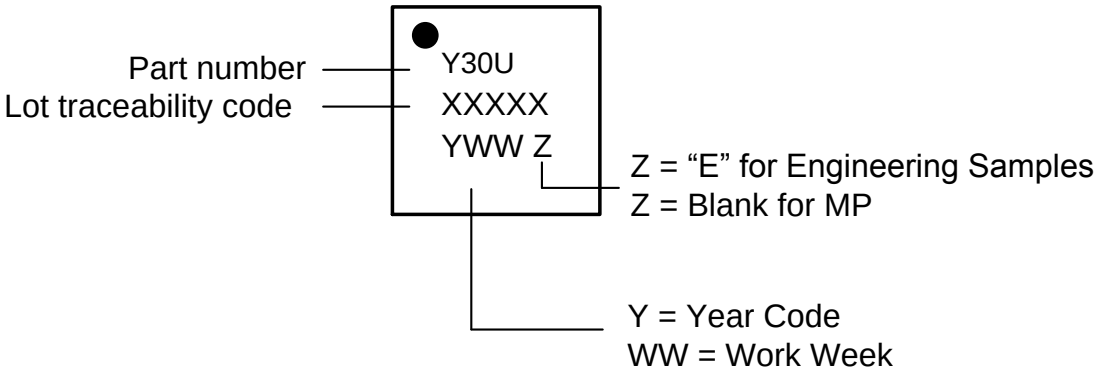
10 Package Information



SYMBOLS	DESCRIPTION	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
A	Package Thickness	0.58	0.645	0.70
A1	Substrate Thickness	---	0.105 REF	---
b	Lead Width	0.2	0.25	0.30
c	Seating Plane	---	0.08	---
D	Package Body Width	2.25	2.30	2.35
D1	Edge Lead Center to Center	---	1.00	---
D2	Center Lead Center to Center	---	1.75	---
E	Package Body Length	2.25	2.30	2.35
E1	Edge Lead Center to Center (axial)	---	1.00	---
E2	Edge Lead Center to Center (centerline)	---	1.75	---
e	Lead Finger (Pad to Pad) Pitch	---	0.50	---
f (e-b)	Lead Finger (Pad to Pad) Space	---	0.25	---
L	Lead Finger (Pad) Length	0.30	0.35	0.40
L'	Corner Lead Finger (Pad) Chamfer Length	---	0.105	---
L"	Corner Lead Finger (Pad) Short Side Length	---	0.245	---
r	Align Feature Dimension	---	0.250	---
x	Space Align Feature to Lead	---	0.20	---
s	Space Lead Finger to Package Edge	---	0.10 REF	---
w	Width Between Corner Leads	0.2	0.25	0.3
aaa	Package Edge Tolerance	---	0.05 REF	---
bbb	Mold Flatness	---	0 REF	---
ccc	Coplanarity	---	0.08 REF	---



TOP VIEW



Part Number Identification:

Product	Top Mark	
	Production Parts	Engineering Samples
IDG-2030U	Y30U	“E” on the last line

11 Revision History

Revision Date	Revision	Description
11/30/2016	1.0	Initial release

Compliance Declaration Disclaimer:
InvenSense believes this compliance information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.

Environmental Compliance
InvenSense products are RoHS and Green compliant.
InvenSense products are in full environmental compliance as evidenced by our Materials Declaration Data Sheets (MDS). The MDS report, along with support documentation consisting of Material Safety Data Sheets (MSDS) and analytical reports for each homogeneous element of the product are available upon request.

DRC Compliance
InvenSense products use materials that comply with DRC (Democratic Republic of the Congo) Conflict-Free Smelter and Mines requirements to meet the SEC implementation of Dodd–Frank Section 1502.

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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