

## 1. General description

Planar passivated Silicon Controlled Rectifier in a SOT78 (TO-220AB) plastic package intended for use in applications requiring very high inrush current capability and high thermal cycling performance.

## 2. Features and benefits

- High thermal cycling performance
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Very high current surge capability

## 3. Applications

- Ignition circuits
- Motor control
- Protection circuits e.g. SMPS inrush current
- Voltage regulation

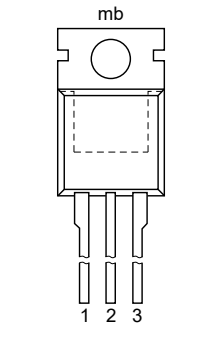

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RRM}$	repetitive peak reverse voltage		-	-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 103\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	13	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	20	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	200	A
		half sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 8.3\text{ ms}$	-	-	220	A
$T_j$	junction temperature		-	-	125	°C
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	3	32	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ °C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit; <a href="#">Fig. 12</a>	200	300	-	V/ $\mu$ s

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p>TO-220AB (SOT78)</p>	
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

## 6. Ordering information

Table 3. Ordering information

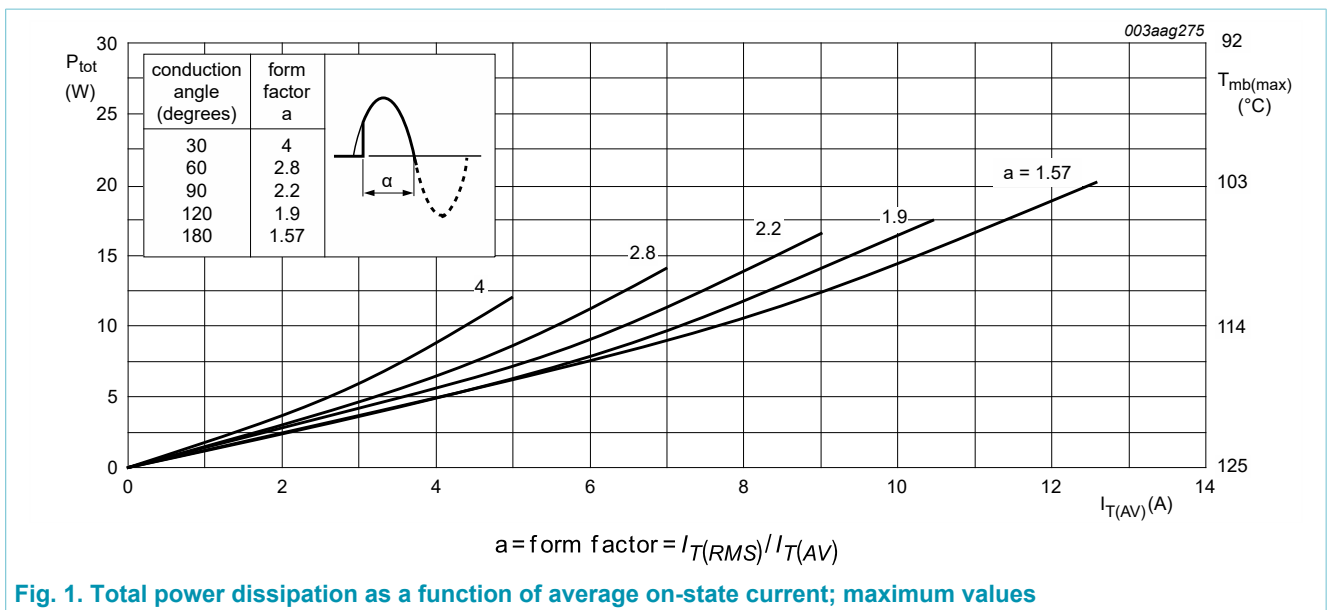
Type number	Package		
	Name	Description	Version
BT152-600R	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	600	V
$V_{RRM}$	repetitive peak reverse voltage		-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 103\text{ }^{\circ}\text{C}$ ; Fig. 1	-	13	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; Fig. 2; Fig. 3	-	20	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 10\text{ ms}$ ; Fig. 4; Fig. 5	-	200	A
		half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 8.3\text{ ms}$	-	220	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN	-	200	$\text{A}^2\text{s}$
$dl_T/dt$	rate of rise of on-state current	$I_G = 100\text{ mA}$	-	200	$\text{A}/\mu\text{s}$
$I_{GM}$	peak gate current		-	5	A
$V_{RGM}$	peak reverse gate voltage		-	5	V
$P_{GM}$	peak gate power		-	20	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
$T_{stg}$	storage temperature		-40	150	$^{\circ}\text{C}$
$T_j$	junction temperature		-	125	$^{\circ}\text{C}$



**Fig. 1. Total power dissipation as a function of average on-state current; maximum values**

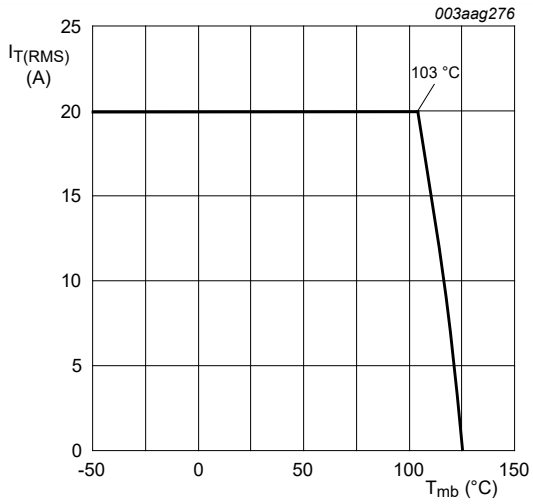


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values

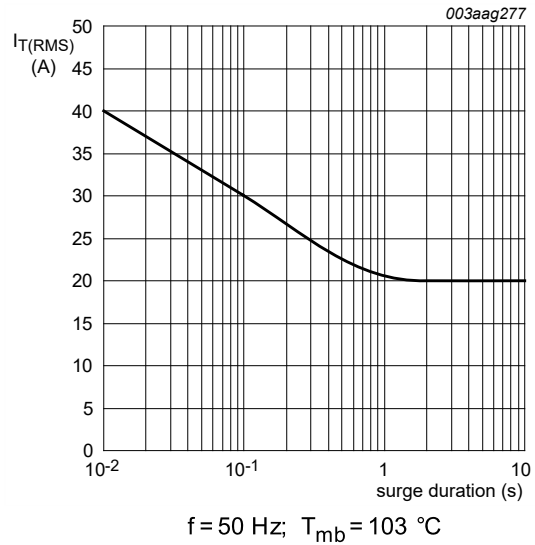


Fig. 3. RMS on-state current as a function of surge duration; maximum values

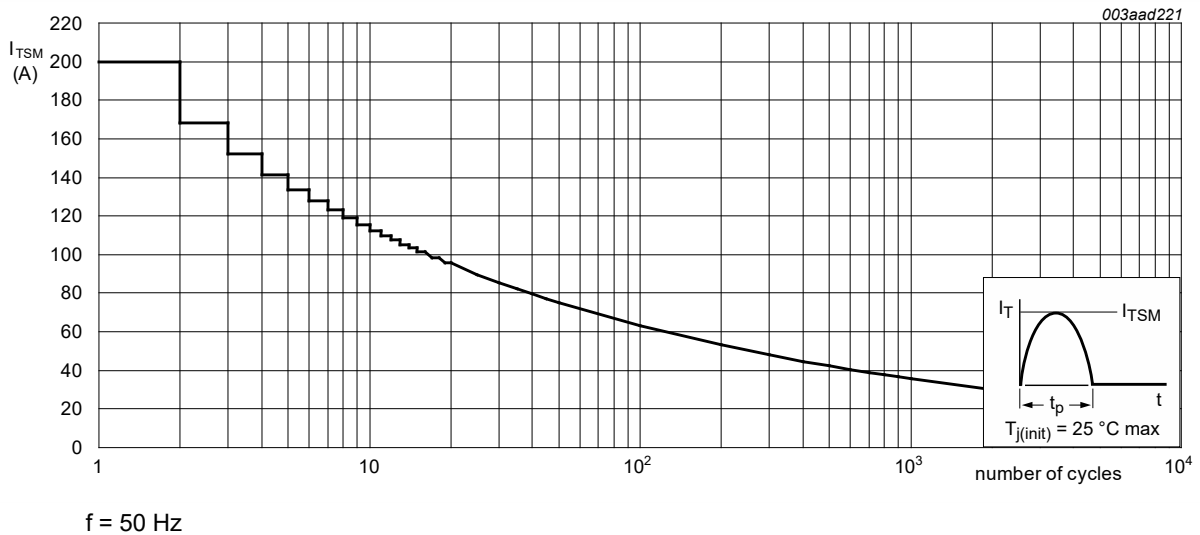
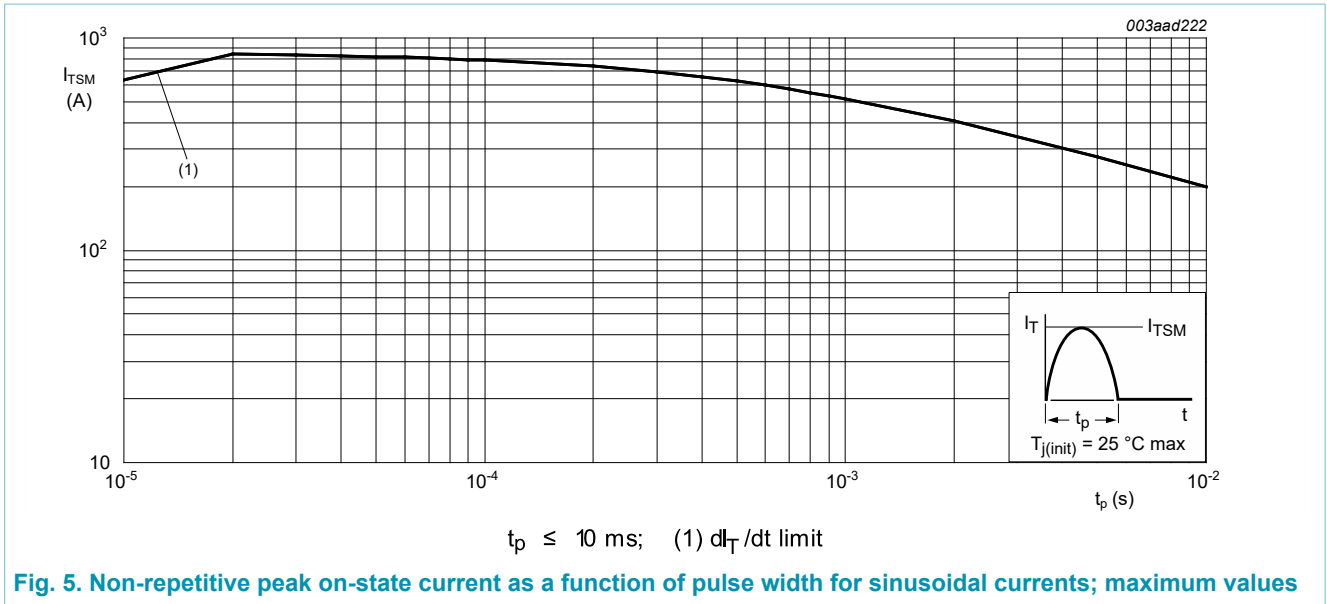


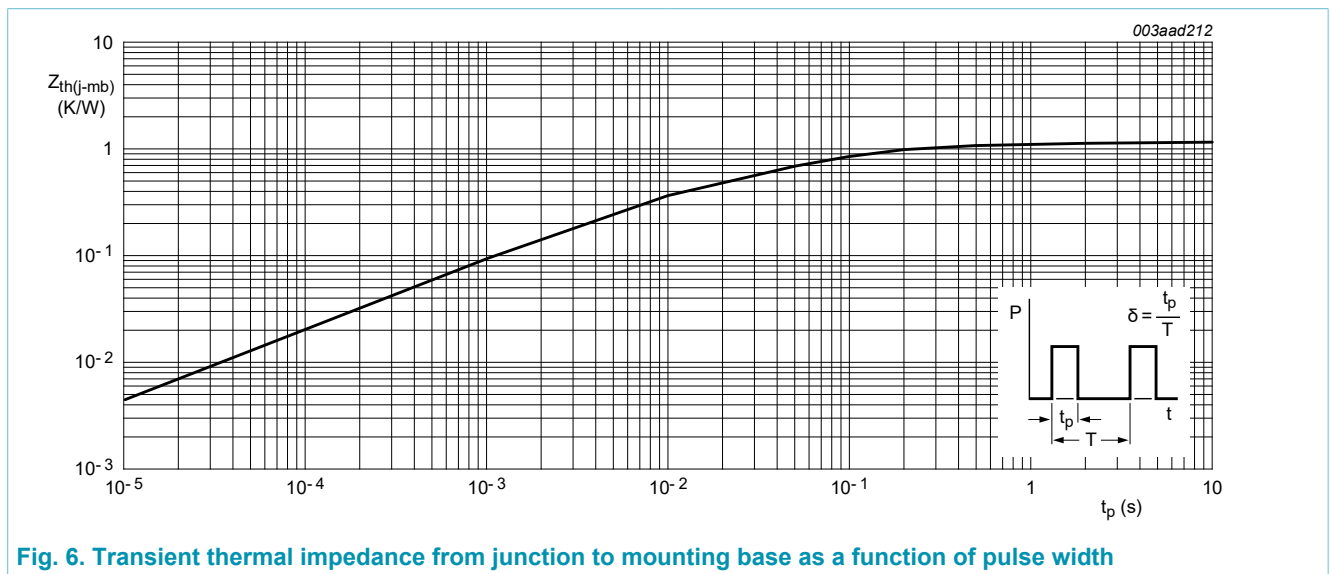
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



## 8. Thermal characteristics

Table 5. Thermal characteristics

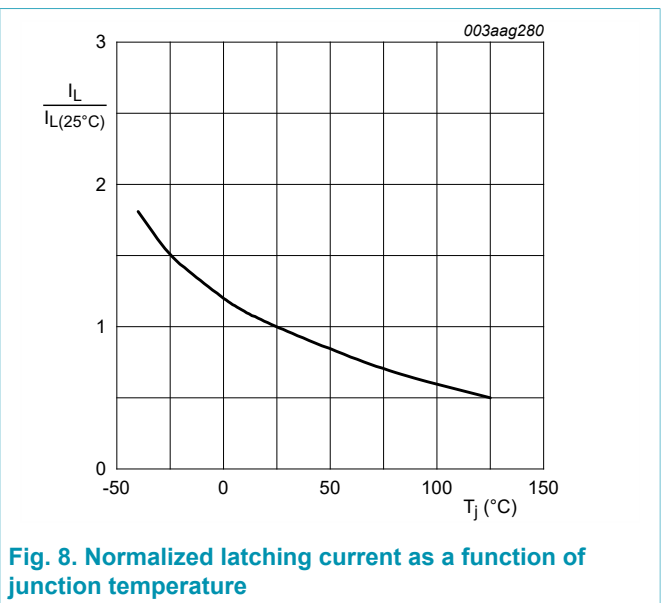
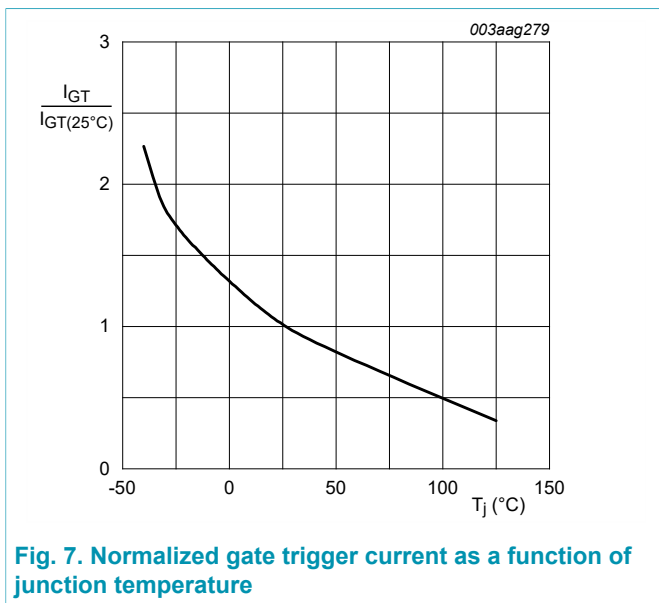
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 6</a>	-	-	1.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	60	-	K/W



## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	3	32	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 8</a>	-	25	80	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>	-	15	60	mA
$V_T$	on-state voltage	$I_T = 40\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	1.4	1.75	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	-	0.6	1	V
		$V_D = 600\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ °C}$	0.25	0.4	-	V
$I_D$	off-state current	$V_D = 600\text{ V}$ ; $T_j = 125\text{ °C}$	-	0.2	1	mA
$I_R$	reverse current	$V_R = 600\text{ V}$ ; $T_j = 125\text{ °C}$	-	0.2	1	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ °C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit; <a href="#">Fig. 12</a>	200	300	-	V/ $\mu$ s
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 40\text{ A}$ ; $V_D = 800\text{ V}$ ; $I_G = 100\text{ mA}$ ; $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	$\mu$ s
$t_q$	commutated turn-off time	$V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ °C}$ ; $I_{TM} = 50\text{ A}$ ; $V_R = 25\text{ V}$ ; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$ ; $dV_D/dt = 50\text{ V}/\mu\text{s}$ ; $R_{GK(ext)} = 100\text{ }\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ )	-	70	-	$\mu$ s



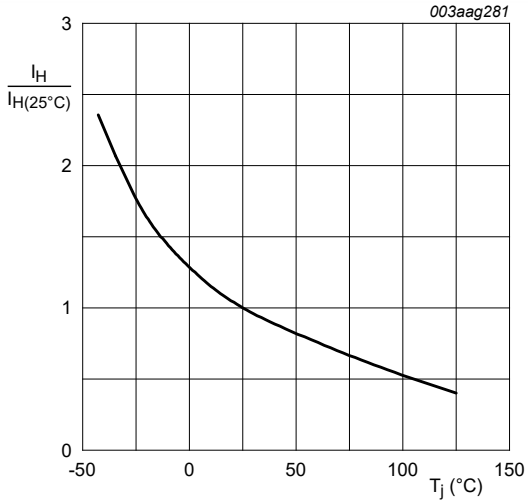
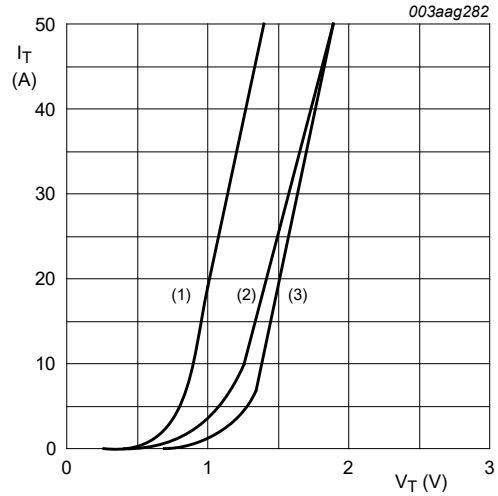


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.06 \text{ V}; R_s = 0.03 \Omega$

- (1)  $T_j = 125^\circ\text{C}$ ; typical values
- (2)  $T_j = 125^\circ\text{C}$ ; maximum values
- (3)  $T_j = 25^\circ\text{C}$ ; maximum values

Fig. 10. On-state current as a function of on-state voltage

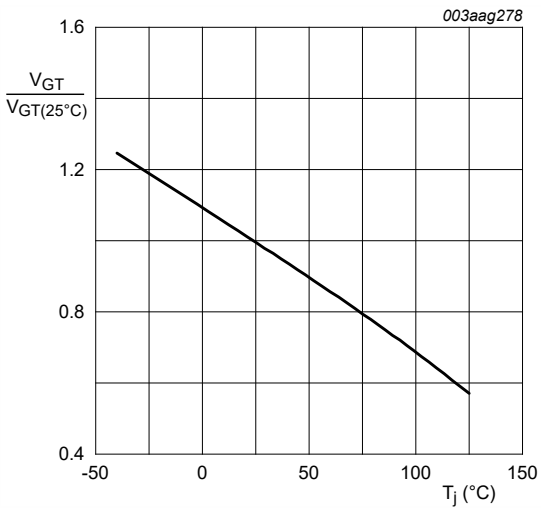
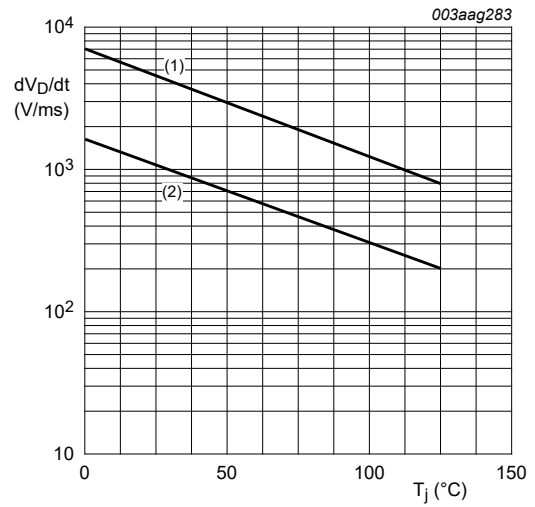


Fig. 11. Normalized gate trigger voltage as a function of junction temperature



- (1)  $R_{GK} = 100 \Omega$
- (2) Gate open circuit

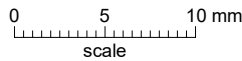
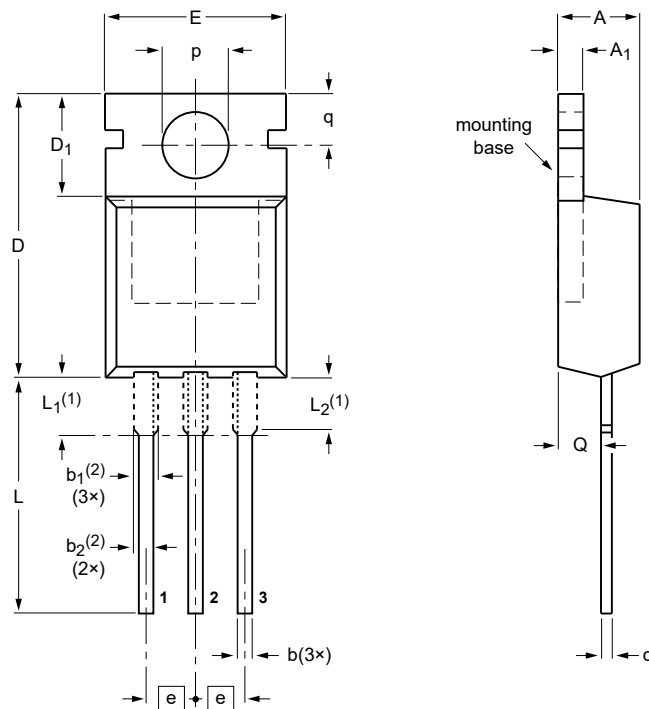
Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values



### 10. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub> (2)	b <sub>2</sub> (2)	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub> (1)	L <sub>2</sub> (1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

**Notes**

- 1. Lead shoulder designs may vary.
- 2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT78		3-lead TO-220AB	SC-46		08-04-23 08-06-13

Fig. 13. Package outline TO-220AB (SOT78)

## 11. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Date of release: 5 September 2018

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