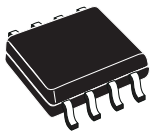
A6727

Single-phase PWM controller for automotive applications

Datasheet - production data



SO-8

Features

- AEC-Q100 compliant
- Flexible power supply from 5 V to 12 V
- Power conversion input as low as 1.5 V
- 1% output voltage accuracy
- High-current integrated drivers
- Adjustable output voltage
- 0.8 V internal reference
- Simple voltage mode control loop
- Sensorless and programmable OCP across
- Low-side $R_{DS(on)}$
- Oscillator internally fixed at 300 kHz
- Internal soft-start
- LS-less to manage pre-bias startup
- Disable function
- OV/UV protection
- FB disconnection protection
- SO-8 package

Applications

- Dedicated to automotive applications

Description

The A6727 is a single-phase step-down controller with integrated high-current drivers that provides complete control logic, protection and reference voltage to realize a general DC-DC converter by using a compact SO-8 package. The device flexibility allows the management of conversions with power input V_{IN} as low as 1.5 V and device supply voltage in the range of 5 V to 12 V.

The A6727 provides simple control loop with voltage mode error-amplifier. The integrated 0.8 V reference allows the regulation of output voltages with ±1% accuracy over line and temperature variations. The oscillator is internally fixed to 300 kHz.

The A6727 provides programmable overcurrent protection as well as over and undervoltage protection. The current information is monitored across the low-side MOSFET $R_{DS(on)}$ saving the use of expensive and space-consuming sense resistors while output voltage is monitored through FB pin.

FB disconnection protection prevents excessive and dangerous output voltages from floating FB pin.

Table 1. Device summary

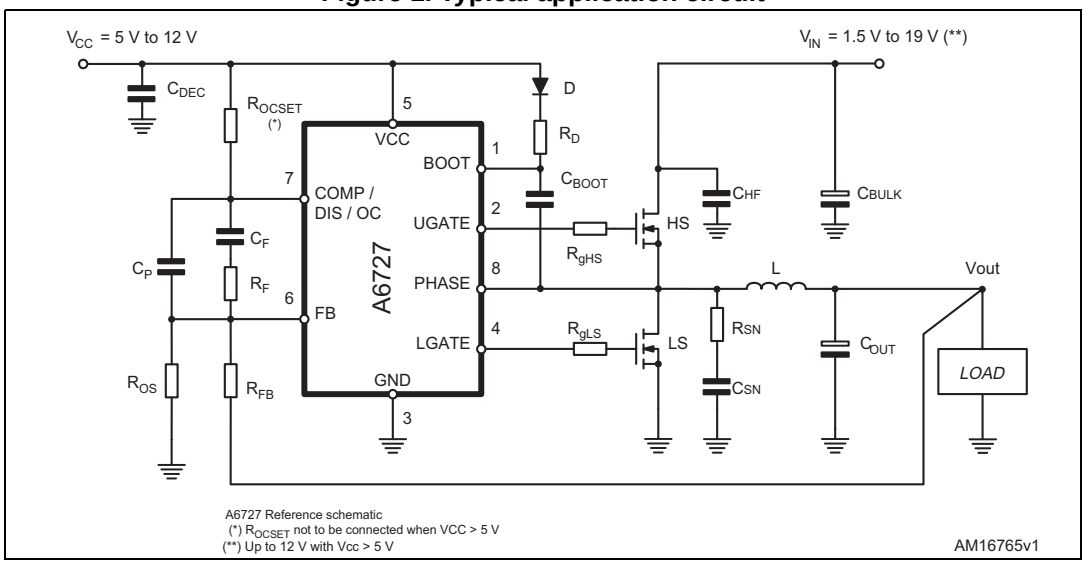
Order code	Package	Packaging
A6727	SO-8	Tube
A6727TR		Tape and reel

Contents

1 Typical application circuit and block diagram

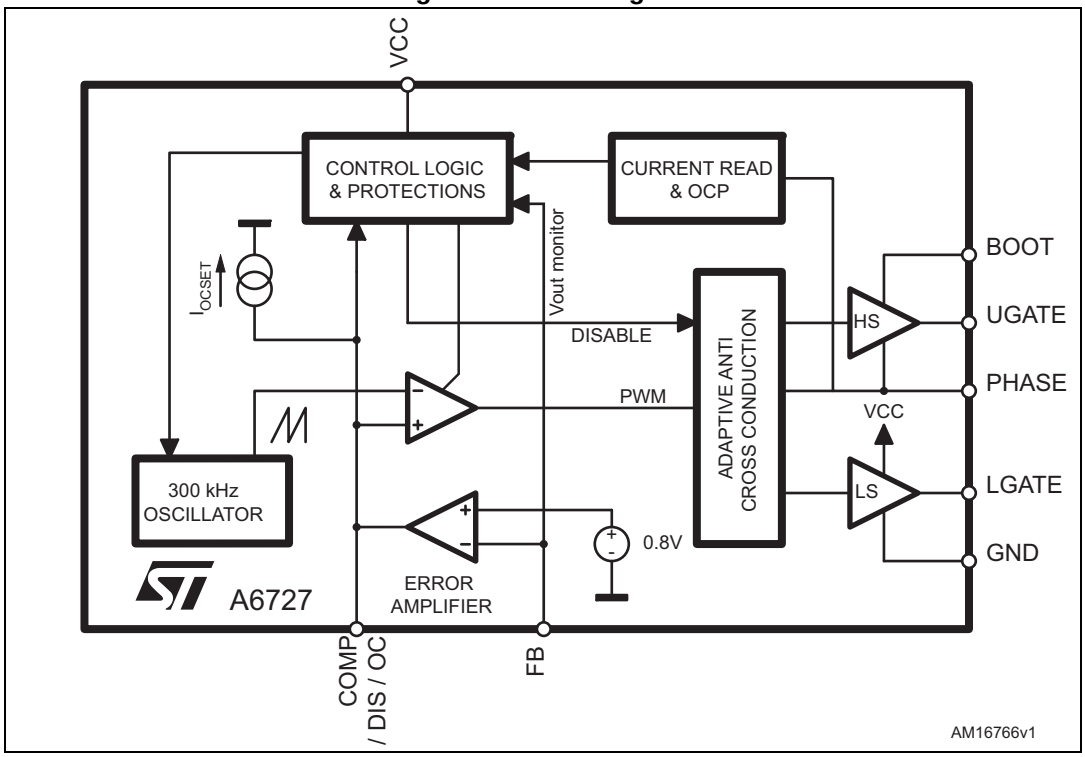
1.1 Application circuit

Figure 1. Typical application circuit



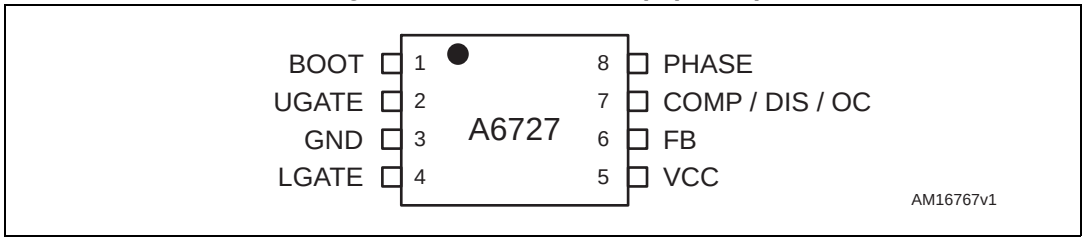
1.2 Block diagram

Figure 2. Block diagram



2 Pin description and connection diagram

Figure 3. Pin connection (top view)



2.1 Pin description

Table 2. Pin description

Pin #	Name	Function
1	BOOT	HS driver supply. Connect through a capacitor (100 µF) to the floating node (LS drain) pin and provide necessary bootstrap diode.
2	UGATE	HS driver output. Connect to HS MOSFET gate.
3	GND	All internal references, logic and drivers are connected to this pin. Connect to the PCB ground plane.
4	LGATE	LS driver output. Connect to LS MOSFET gate.
5	VCC	Device and LS driver power supply. Operative range from 4.1 V to 13.2 V. Filter with at least 1 µF MLCC to GND.
6	FB	Error amplifier inverting input. Connect to the output regulated voltage through a resistor R_{FB}. Additional resistor R_{OS} to GND may be used to regulate voltages higher than the reference.
7	COMP / DIS / OC	*COMP*. Error amplifier output. Connect to FB through an R_F - C_F // C_P to compensate the control loop. *DIS*. The device can be disabled by forcing this pin lower than 0.5 V (typ.). To disable the device, the external pull-down overcomes 10 mA of COMP output current for about 15 ms. Once disabled, COMP output current drops to 20 mA. *OC.* Overcurrent threshold set. Connect to VCC through an R_{OCSET} resistor (only if VCC is supplied by 5 V bus) to program OC threshold. When VCC > 5 V, R_{OCSET} needs to be not-connected.
8	PHASE	HS driver return path, current reading and adaptive deadtime monitor. Connect to the LS drain to sense $R_{DS(on)}$ drop to measure the output current. This pin is also used by the adaptive deadtime control circuitry to monitor when HS MOSFET is off.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction-to-ambient (1)	85	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-40 to 150	°C

1. The component is mounted on a 2S2P board in free air (6.7 cm x 6.7 cm, 35 mm (P) and 17.5 mm (S) copper thickness).

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	to GND	-0.3 to 15	V
V_{BOOT}	to PHASE to GND	15 45	V
V_{UGATE}	to PHASE to PHASE; t < 50 ns to GND	-0.3 to (V_{BOOT} - V_{PHASE}) + 0.3 -1 V_{BOOT} + 0.3	V
V_{PHASE}	to GND	-8 to 30	V
V_{LGATE}	to GND to GND; t < 50 ns	-0.3 to V_{CC} + 0.3 -1	V
	COMP to GND	-0.3 to 7	V
	FB to GND	-0.3 to 3.6	V

3.2 Electrical characteristics

V_{CC} = 12 V; T_A = - 40 °C to 85 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Recommended operating conditions						
V_{CC}	Device supply voltage	See *Figure 1*	4.1		13.2	V
V_{IN}	Conversion input voltage				13.2	V
		V_{CC} < 7.0 V			19.0	V
Supply current and power-on						
I_{CC}	VCC supply current	UGATE and LGATE = open		6		mA
I_{BOOT}	BOOT supply current	UGATE = open; PHASE to GND		0.5		mA
UVLO	VCC turn-on	VCC rising			4.1	V
	Hysteresis			0.2		V
Oscillator						
F_{SW}	Main oscillator accuracy	T_A = 25 °C	270	300	330	kHz
			250	300	350	kHz
DV_{OSC}	PWM ramp amplitude			1.5		V
d_{MAX}	Maximum duty cycle		80			%
Reference						
	Output voltage accuracy	V_{OUT} = 0.8 V, T_A = 25 °C	-1	-	1	%
		V_{OUT} = 0.8 V	-1.5		1.5	%
Error amplifier						
A_0	DC gain(1)			120		dB
GBWP	Gain-bandwidth product(1)			15		MHz
SR	Slew rate(1)			8		V/µs
I_{FB}	Input bias current	Sourced from FB		100		nA
DIS	Disable threshold	COMP falling	0.43	0.5		V
Gate drivers						
I_{UGATE}	HS source current	BOOT - PHASE = 5 V to 12 V		1.5		A
R_{UGATE}	HS sink resistance	BOOT - PHASE = 5 V to 12 V		1.1		Ω
I_{LGATE}	LS source current	VCC = 5 V to 12 V		1.5		A
R_{LGATE}	LS sink resistance	VCC = 5 V to 12 V		0.65		Ω
Overcurrent protection						

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OCSET}	OCSET current source T_A = 25 °C	Sunk from COMP pin, before SS	55	60	65	µA
	OCSET current source		52	60	68	
V_{CC_OC}	OC switch-over threshold	VCC rising		8		V
V_{OC_TH}	Fixed OC threshold	V_{PHASE} to GND, VCC > V_{CC_OC}		-400		mV
Over and undervoltage protections						
OVP	OVP threshold	FB rising		1		V
UVP	UVP threshold	FB falling		0.6		V

1. Guaranteed by design, not to be tested.

4 Device description

The A6727 is a single-phase PWM controller with embedded high-current drivers that provides complete control logic and protection to realize a general DC-DC step-down converter. Designed to drive N-channel MOSFETs in a synchronous buck topology, with its high level of integration, this 8-pin device allows a reduction of cost and size of the power supply solution.

The A6727 is designed to operate from a 5 V to 12 V supply bus. Thanks to the high precision 0.8 V internal reference, the output voltage can be precisely regulated as low as 0.8 V with ±1% accuracy over line and temperature variations (between 0 °C and +70 °C).The switching frequency is internally set to 300 kHz.

This device provides a simple control loop with a voltage-mode error amplifier. The error amplifier features a 15 MHz gain-bandwidth product and 8 V/µs slew rate, allowing high regulator bandwidth for fast transient response.

To avoid load damages, the A6727 provides overcurrent protection as well as overvoltage, undervoltage and feedback disconnection protection. When the device is supplied from 5 V, overcurrent trip threshold is programmable by a simple resistor. Output current is monitored through low-side MOSFET $R_{DS(on)}$, saving the use of expensive and space-consuming sense resistor. Output voltage and feedback disconnection are monitored through FB pin.

The A6727 implements soft-start by increasing the internal reference from 0 V to 0.8 V in 5.1 ms (typ.) in closed loop regulation. Low-side-less feature allows the device to perform the soft-start over pre-biased output avoiding high-current return through the output inductor and dangerous negative spikes at the load side.

5 Driver section

The integrated high-current drivers allow different types of power MOSFET to be used (also multiple MOSFETs to reduce the equivalent $R_{DS(on)}$), maintaining fast switching transition.

The driver for the high-side MOSFET uses BOOT pin as supply and PHASE pin as return. The driver for low-side MOSFET uses the VCC pin as supply and GND pin as return.

The controller embodies an anti-shoot-through and adaptive deadtime control to minimize low-side body diode conduction time, maintaining good efficiency and saving the use of Schottky diode:

- the device senses the PHASE pin to check that high-side MOSFET is off. When the sensed voltage drops below an internal threshold, the low-side MOSFET is suddenly turned on.
- the device senses the LGATE pin to check that low-side MOSFET is off. When the sensed voltage drops below an internal threshold, the high-side MOSFET is suddenly turned on.

If the current flowing in the inductor is negative, the voltage on PHASE pin never drops. To allow the low-side MOSFET to turn on even in this case, a watchdog controller is enabled: if the source of the high-side MOSFET doesn't drop, the low-side MOSFET is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

Power conversion input is flexible: 5 V, 12 V bus or any bus that allows the conversion (see maximum duty cycle limitation and recommended operating conditions, in *Table 5*) to be chosen freely.

5.1 Power dissipation

The A6727 embeds high-current MOSFET drivers for both high-side and low-side MOSFETs. The dissipated power by the device avoids overcoming the maximum junction operative temperature.

Two main terms contribute to the device power dissipation: bias power and driver power.

- Bias power (P_{DC}) depends on the static consumption of the device through the supply pins and it is calculated as follows (assuming to supply HS and LS drivers with the same VCC of the device):

Equation 1

$$P_{DC} = V_{CC} \cdot (I_{CC} + I_{BOOT})$$

- Driver power is the power needed by the driver to continuously switch on and off the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} is dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance. This last term has to be determined to calculate the device power dissipation. The total power dissipated to switch the MOSFETs is:

Equation 2

$$P_{SW} = F_{SW} \cdot [Q_{gHS} \cdot (V_{BOOT} - V_{PHASE}) + Q_{gLS} \cdot V_{CC}]$$

where V_{BOOT} - V_{PHASE} is the voltage across the bootstrap capacitor. The external gate resistor helps the device to dissipate the switching power since the same power P_{SW} is dissipated by the internal driver impedance and the external resistor. This process causes a general cooling of the device.

6 Soft-start and disable

The A6727 implements a soft-start to smoothly charge the output filter avoiding the high in-rush currents to the input power supply. The device progressively increases the internal reference from 0 V to 0.8 V in about 5.1 ms, in closed loop regulation, gradually charging the output capacitors to the final regulation voltage.

In case of an overcurrent triggering during the soft-start, the overcurrent logic overrides the soft-start sequence and shuts down both the high-side and low-side gates for the internal soft-start residual time (up to 2048 clock cycles) plus 2048 clock cycles, then it begins a new soft-start.

The device begins soft-start phase only when VCC power supply is above UVLO threshold and the overcurrent threshold setting phase has been completed.

6.1 Low-side-less startup (LS-less)

In order to manage the startup over pre-biased output, the A6727 performs a special sequence enabling LS driver to switch: during the soft-start phase, LS driver is disabled (LS = OFF) until HS starts switching. In this manner, the dangerous negative spike on the output voltage is avoided.

If the output voltage is pre-biased to a voltage lower than the programmed one, neither HS nor LS turn on until the soft-start ramp exceeds the output pre-bias voltage; then V_{OUT} ramps up from there, without any drop or current return.

If the output voltage is pre-biased to a voltage higher than the programmed one, HS never starts switching. In this case, at the end of soft-start time, LS is enabled and discharges the output to the final regulation value.

This particular feature masks the LS turn-on only from the control loop point of view: protections by-pass LS-less, turning on the LS MOSFET if needed.

Figure 4. LS-less startup

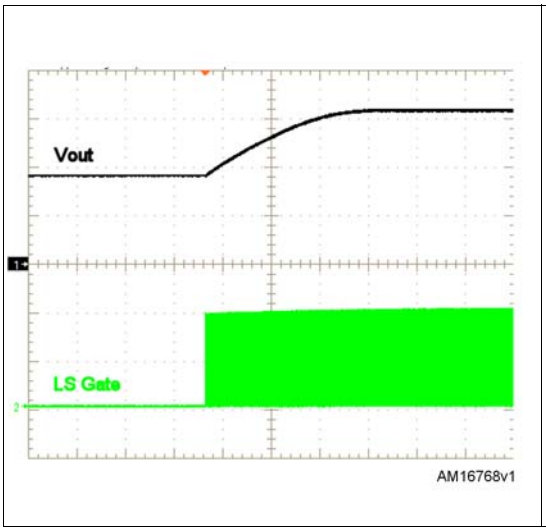
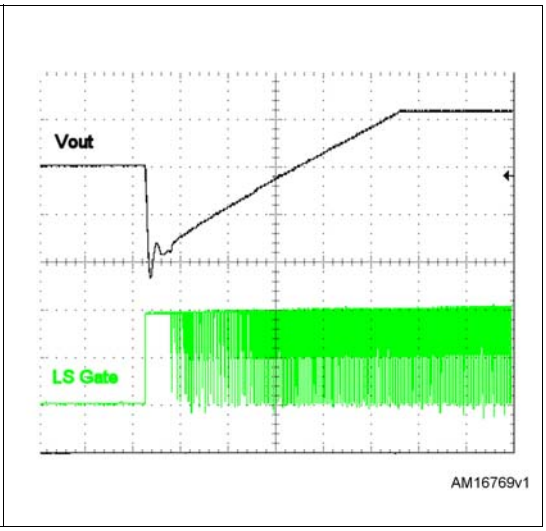


Figure 5. Non-LS-less startup



6.2 Enable / disable

The device can be disabled externally by pushing COMP/DIS pin under 0.5 V (typ.). In disable condition HS and LS MOSFETs are turned off, and a 20 mA current sources from COMP/DIS pin. Setting the pin, this current pulls it over the threshold and the device enables again performing a new SS.

To disable the device, the external pull-down needs to overcome 10 mA of COMP output current for about 15 ms. Once disabled, COMP output current drops below 20 mA.

Figure 6. Startup sequence; V_{CC} = 5 V

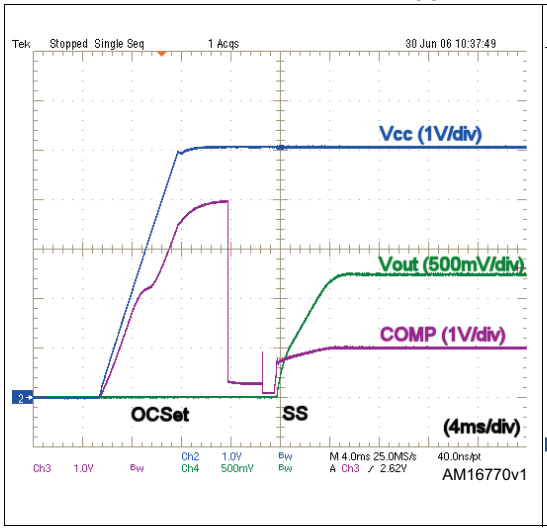
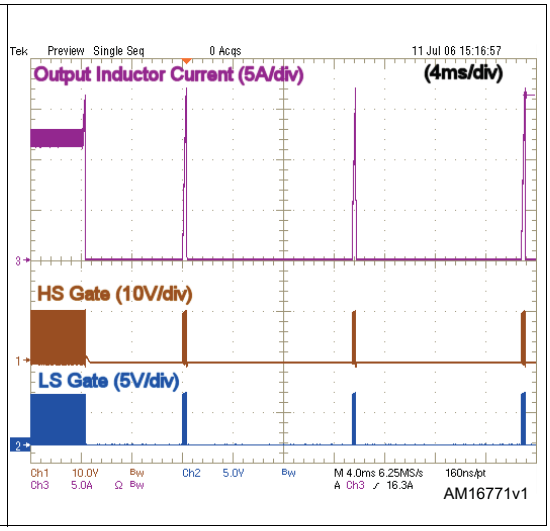


Figure 7. Overcurrent hiccup



7 Overcurrent protection

The overcurrent function protects the converter from a shorted output or overload, by sensing the output current information across the low-side MOSFET drain-source on-resistance, $R_{DS(on)}$. This method reduces costs and enhances converter efficiency by avoiding the use of expensive and space-consuming sense resistors.

The low-side $R_{DS(on)}$ current sense is implemented by comparing the voltage at the PHASE node when LS MOSFET is turned on with the programmed OCP threshold voltage, internally held. If the monitored voltage drop (GND to PHASE) exceeds this threshold, an overcurrent event is detected. If two overcurrent events are detected in two consecutive switching cycles, the protection is triggered and the device turns off both LS and HS MOSFETs for 2048 clock cycles (plus internal SS remaining time, if triggered during an SS phase); then it begins a new soft-start.

If the overcurrent condition is not removed, the continuous fault causes the A6727 to enter hiccup mode with a typical period of 13.6 ms (*Figure 6*), assuring safe load protection and very low power dissipation.

7.1 Overcurrent threshold setting

When supplied with VCC = 5 V, the A6727 allows an overcurrent threshold ranging from 50 mV to 500 mV to be programmed, by adding a resistor (R_{OCSET}) between COMP and VCC.

During a short period of time (5.5 ms - 6.5 ms) following the first enable (given VCC over UVLO threshold), an internal 60 µA current (I_{OCSET}) is sunk, determining a voltage drop across R_{OCSET}. This voltage drop, differently sensed between VCC and COMP, divided by a factor 3, is sampled and internally held by the device as overcurrent threshold until next VCC cycling. Different sensing versus VCC allows the OCSET procedure to be fully independent from VIN rail. The OC setting procedure overall time length ranges from 5.5 ms to 6.5 ms, proportionally to the threshold.

Connecting an R_{OCSET} resistor between COMP and VCC, the programmed threshold is:

Equation 3:

$$I_{OCth} = \frac{1}{3} \cdot \frac{I_{OCSET} \cdot R_{OCSET}}{R_{DS(on)}}$$

R_{OCSET} values range from 2.5 kΩ to 25 kΩ.

R_{OCSET} low values make the system sensitive to start-up in-rush current and noise.This may result in a continuous OCP triggering and hiccup mode.

If R_{OCSET} is not connected (and VCC = 5 V), the device sets the maximum threshold.

If the device is supplied with a VCC higher than 7 V, R_{OCSET} cannot be connected. In this case, as soon as VCC rises over V_{CC_OC} (8 V typ.), the A6727 switches OC threshold to 400 mV (internally fixed value).

See *Figure 6* for OC threshold setting and soft-start oscilloscope sample waveforms.

8 Output voltage monitor and protections

The A6727 monitors the voltage at FB pin and compares it to internal reference voltage in order to provide undervoltage and overvoltage protections.

8.1 Undervoltage protection

If the voltage at FB pin drops below UV threshold (0.6 V typ.), the device turns off both HS and LS MOSFETs, waits for 2048 clock cycles and then performs a new soft-start. If undervoltage condition is not removed, the device enters the hiccup mode with a typical period of 13.6 ms.

UVP is active from the end of soft-start.

8.2 Overvoltage protection

If the voltage at FB pin rises over OV threshold (1 V typ.), overvoltage protection turns off HS MOSFET and turns on LS MOSFET overriding PWM logic as long as overvoltage is detected.

OVP is always active with top priority as soon as the overcurrent threshold setting phase has been completed.

8.3 Feedback disconnection protection

In order to provide load protection even if FB pin is not connected, a 100 nA bias current is always sourced from this pin. If FB pin is not connected, this current permanently pulls up FB over OVP threshold: thus LS is latched on preventing output voltage from rising out of control.

8.4 Undervoltage lock out

In order to avoid anomalous behaviors of the device when the supply voltage is too low to support its internal rails, UVLO is provided: the device starts up when VCC reaches UVLO upper threshold and shut downs when VCC drops below UVLO lower threshold.

9 Application details

9.1 Output voltage selection

The A6727 is capable of precisely regulating an output voltage as low as 0.8 V. In fact, the device has a fixed 0.8 V internal reference that guarantees the output regulated voltage within ±1% tolerance over line and temperature variations between 0 °C and +70 °C (excluding output resistor divider tolerance, when present).

The output voltage higher than 0.8 V can be easily achieved by adding a resistor R_{OS} between FB pin and ground. Referring to *Figure 1*, the steady-state DC output voltage is:

Equation 4

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{FB}}{R_{OS}}\right)$$

where V_{REF} is 0.8 V.

9.2 Compensation network

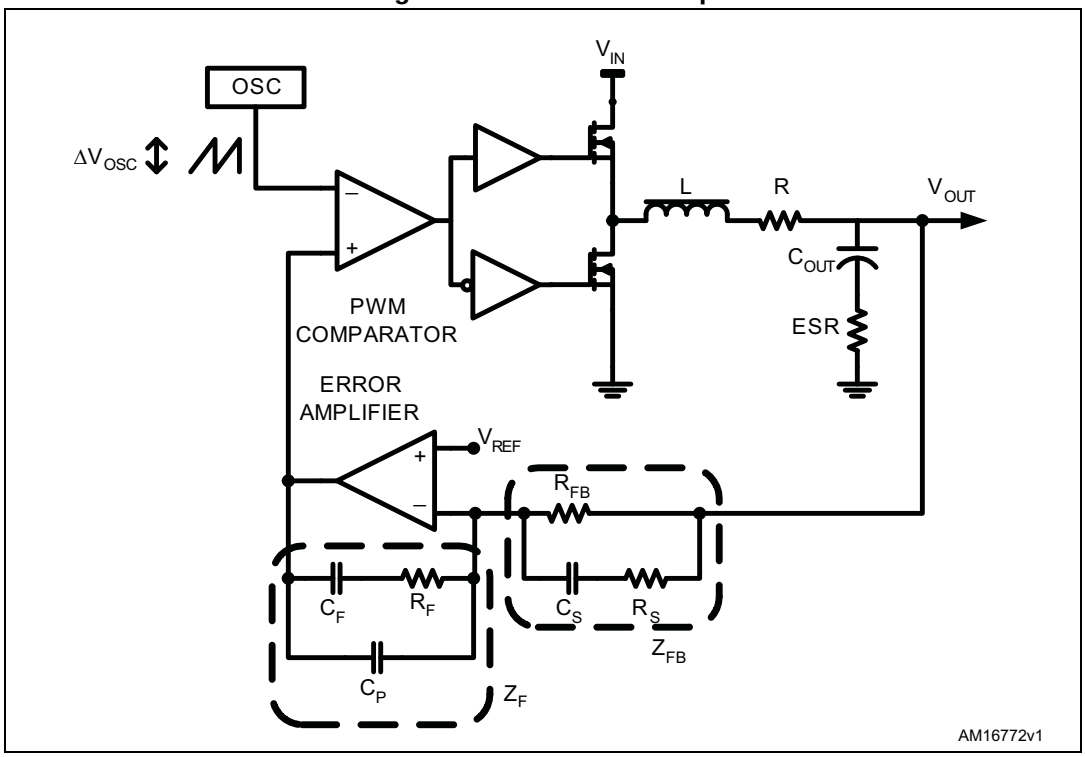
The control loop showed in *Figure 8* is a voltage mode control loop. The error amplifier is a voltage mode type. The output voltage is regulated to the internal reference (when present, the offset resistor, between FB node and GND, can be neglected in control loop calculation).

Error amplifier output is compared with oscillator sawtooth waveform to provide the driver section with the PWM signal. The PWM signal is then transferred to the switching node with V_{IN} amplitude. This waveform is filtered by the output filter.

The converter transfer function is the small signal transfer function between the output of the EA and V_{OUT}. This function has a double pole at frequency F_{LC} depending on the L-C_{OUT} resonance and a zero at F_{ESR} depending on the output capacitor ESR. The DC gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

The compensation network closes the loop joining V_{OUT} and EA output with transfer function ideally equal to $-Z_F/Z_{FB}$.

Figure 8. PWM control loop

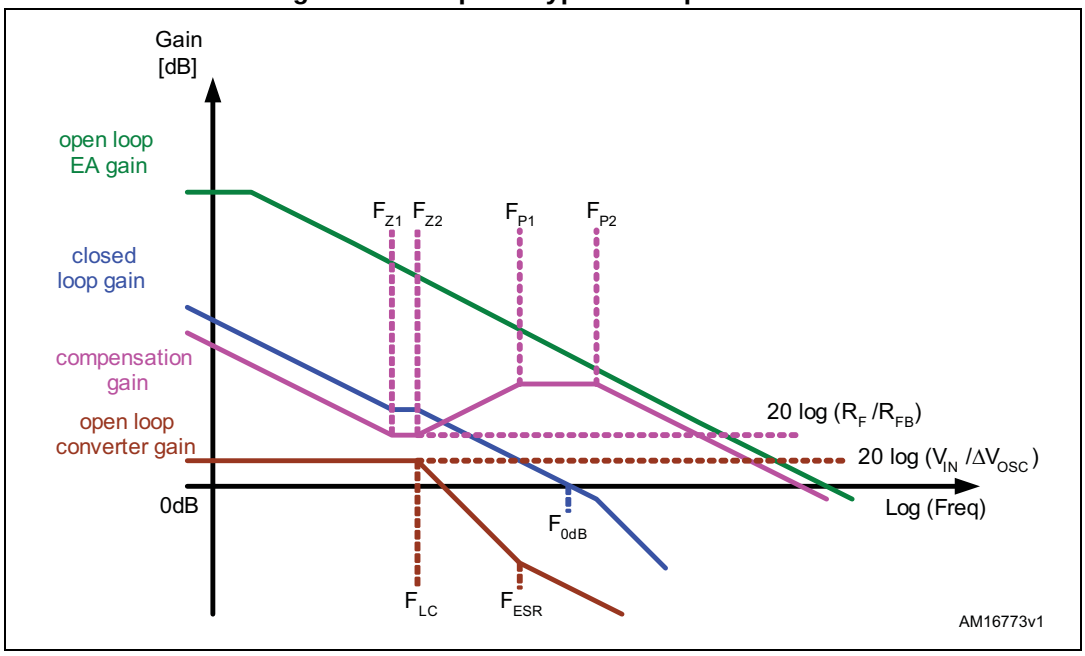


Compensation goal is to close the control loop assuring high DC regulation accuracy, good dynamic performances and stability. To achieve this, the overall loop needs high DC gain, high bandwidth and good phase margin.

The loop bandwidth (F_{0dB}) can be fixed choosing the right R_F/R_{FB} ratio, however, it should not exceed F_{SW} / 2p. To achieve a good phase margin, the control loop gain has to cross 0 dB axis with -20 dB/decade slope.

Figure 9 shows an asymptotic bode plot of a type III compensation.

Figure 9. Example of type III compensation.



- Open loop converter singularities:

Equation 5

a) $$F_{LC} = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}}$$

b) $$F_{ESR} = \frac{1}{2\pi \cdot C_{OUT} \cdot ESR}$$

- Compensation network singularity frequencies are:

Equation 6

a) $$F_{Z1} = \frac{1}{2\pi \cdot R_F \cdot C_F}$$

b) $$F_{Z2} = \frac{1}{2\pi \cdot (R_{FB} + R_S) \cdot C_S}$$

c) $$F_{P1} = \frac{1}{2\pi \cdot R_F \cdot \left(\frac{C_F \cdot C_P}{C_F + C_P}\right)}$$

d) $$F_{P2} = \frac{1}{2\pi \cdot R_S \cdot C_S}$$

To place the poles and zeroes of the compensation network, the following suggestions may be followed:

a) set the gain R_F/R_{FB} in order to get the desired closed loop regulator bandwidth according to the approximated formula (suggested values for R_{FB} range from 2 kΩ to 5 kΩ):

Equation 7

$$\frac{R_F}{R_{FB}} = \frac{F_{0dB}}{F_{LC}} \cdot \frac{\Delta V_{OSC}}{V_{IN}}$$

b) place F_{Z1} below F_{LC} (typically 0.5*F_{LC}):

$$C_F = \frac{1}{\pi \cdot R_F \cdot F_{LC}}$$

c) place F_{P1} at F_{ESR}:

$$C_P = \frac{C_F}{2\pi \cdot R_F \cdot C_F \cdot F_{ESR} - 1}$$

d) place F_{Z2} at F_{LC} and F_{P2} at half of the switching frequency:

$$R_S = \frac{R_{FB}}{\frac{F_{SW}}{2 \cdot F_{LC}} - 1}$$

$$C_S = \frac{1}{\pi \cdot R_S \cdot F_{SW}}$$

e) check that compensation network gain is lower than open loop EA gain;

f) estimate phase margin obtained (it should be greater than 45°) and repeat, modifying parameters, if necessary.

9.3 Layout guidelines

The A6727 provides control functions and high-current integrated drivers to implement high-current step-down DC-DC converters. In this kind of application, a good layout is very important.

When placing components, the power section is the first priority because the length of each connection and loop have to be reduced as minimum as possible. To minimize noise and voltage spikes (EMI and losses), power connections (highlighted in *Figure 10*) must be part of a power plane and realized by wide and thick copper traces: loop must be minimized. The critical components, such as the power MOSFETs, must be very close one to the other. The use of multi-layer printed circuit board is recommended.

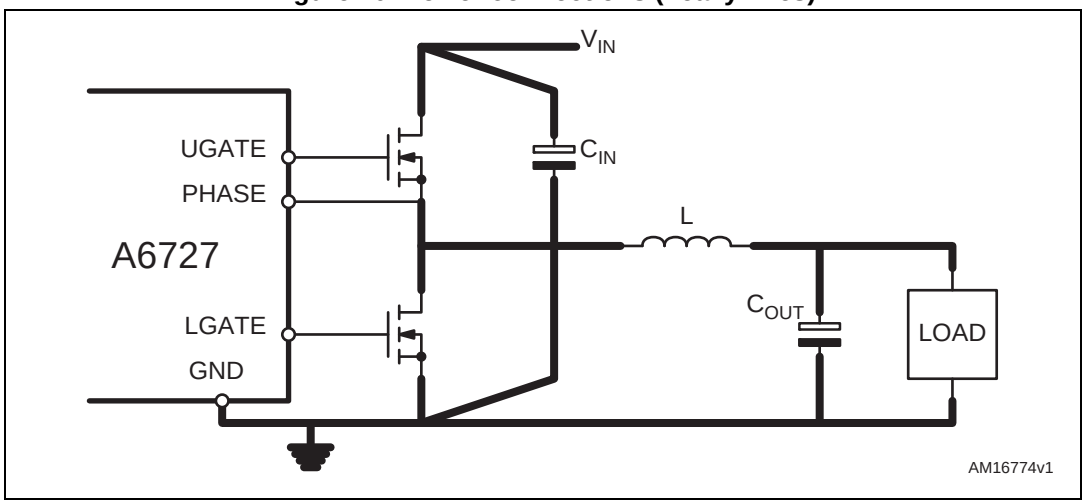
The input capacitance (C_{IN}), or at least a portion of the total capacitance needed, has to be placed close to the power section in order to eliminate the stray inductance generated by the copper traces. Low ESR and ESL capacitors are preferred, MLCC should be connected near the HS drain.

Use a proper number of vias when power traces have to move between different planes on the PCB in order to reduce both parasitic resistance and inductance. Moreover, the same

high-current trace on more than one PCB layer reduces the parasitic resistance associated to that connection.

The output bulk capacitors (C_{OUT}) have to be connected as close as possible to the load, minimizing parasitic inductance and resistance associated to the copper trace.

Figure 10. Power connections (heavy lines)

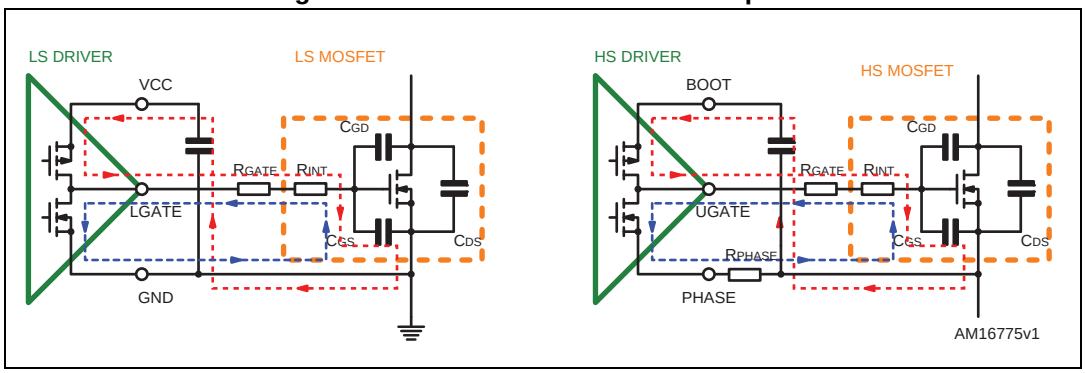


Gate traces and phase trace must be sized according to the driver RMS current delivered to the power MOSFET. The device robustness allows the management of applications with the power section far from the controller without losing performances. Anyway, when possible, the distance between the controller and the power section has to be minimized. See *Figure 11* for driver current paths.

Small signal components and connections to critical nodes of the application, as well as bypass capacitors for the device supply, are also important. Locate bypass capacitor (VCC and bootstrap capacitor) and loop compensation components close to the device. With regard to the overcurrent programmability, place R_{OCSET} close to the device and avoid leakage current paths on COMP/OC pin, since the internal current source is only 60 mA.

Systems, which do not use the Schottky diode in parallel to the low-side MOSFET, might show big negative spikes on the phase pin. This spike must be limited within the absolute maximum ratings (for example, adding a gate resistor in series to HS MOSFET gate, or a phase resistor in series to PHASE pin), as well as the positive spike.The further consequence is that the bootstrap capacitor is overcharged. This extra-charge can cause, in the worst case, a condition of maximum input voltage and during particular transients, BOOT-to-PHASE voltage overcomes the absolute maximum ratings causing device failures. This extra-charge has to be limited by adding a small resistor in series to the bootstrap diode (see R_D in *Figure 1*).

Figure 11. Driver turn-on and turn-off paths



10 Application information

10.1 Output inductor

The inductor value is defined by a compromise among the dynamic response, ripple, efficiency, cost and size. Usually, the inductance is calculated to maintain the inductor ripple current (ΔI_L) between 20% and 30% of the maximum output current. Given the switching frequency (F_{SW}), the input voltage (V_{IN}), the output voltage (V_{OUT}) and the desired ripple current (DI_L), the inductance can be calculated as follows:

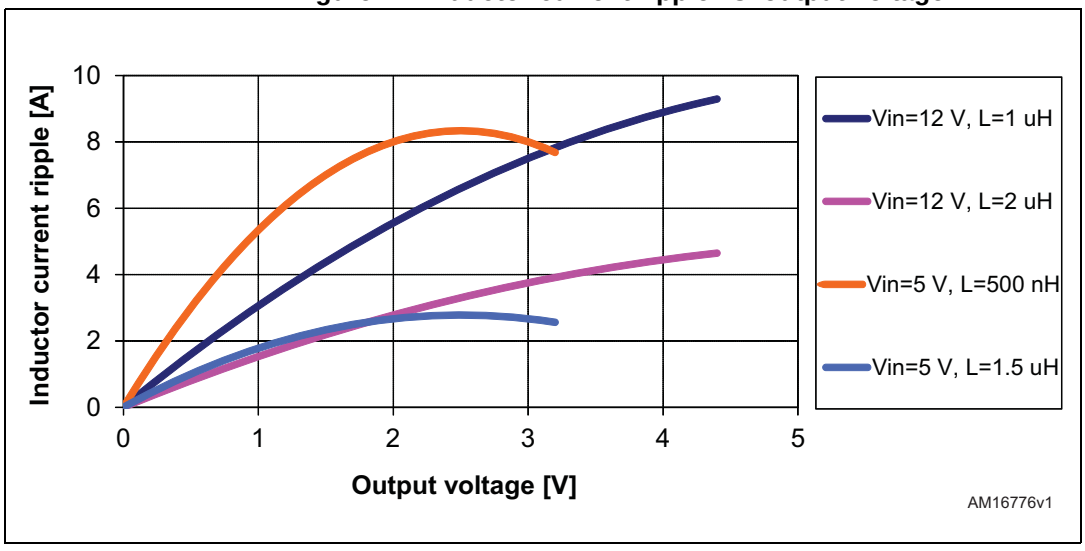
Equation 8

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

Figure 12 shows the ripple current vs. the output voltage for different inductance, with V_{IN} = 5 V and V_{IN} = 12 V.

Increasing the value of the inductance, the inductor ripple current (and output voltage ripple accordingly) reduces but, at the same time, the converter response time to load transients increases. Higher inductance means that the inductor needs more time to change its current from initial to final value. Until the inductor has finished its charging, the additional output current is supplied by the output capacitors. Minimizing the response time, the required output capacitance can be minimized. If the compensation network is designed with high bandwidth, during a load transient the device can saturate duty cycle (0% or 80%). When this condition is reached, the response time is limited only by the time required to charge the inductor.

Figure 12. Inductor current ripple vs. output voltage



10.2 Output capacitors

Output capacitor choice depends on the output voltage ripple and the output voltage deviation during a load transient.

During steady-state conditions, the output voltage ripple is influenced by both ESR and capacitive value of the output capacitors as follows:

Equation 9

$$\Delta V_{OUT\_ESR} = \Delta I_L \cdot ESR$$

Equation 10

$$\Delta V_{OUT\_C} = \Delta I_L \cdot \frac{1}{8 \cdot C_{OUT} \cdot F_{SW}}$$

Where ΔI_L is the inductor current ripple. Since they are not in phase, the total ripple is lower than the sum of their modules. Both ESL and board parasitic inductance can contribute to the output ripple significantly.

During a load variation, the output capacitors supply the load with the current or absorb the current in excess delivered by the inductor until converter reaction is completed. In fact, even if the controller reacts immediately to the load transient saturating the duty cycle to 80% or 0%, the current slew rate is limited by the inductance. The output voltage drop, based on ESR and capacitive charge/discharge and considering an ideal load-step, can be estimated as follows:

Equation 11

$$\Delta V_{OUT\_ESR} = \Delta I_{OUT} \cdot ESR$$

Equation 12

$$\Delta V_{OUT\_C} = \frac{L \cdot \Delta I_{OUT}^{2}}{2 \cdot C_{OUT} \cdot \Delta V_L}$$

Where ΔV_L is the voltage applied to the inductor during the transient ($D_{MAX} \cdot V_{IN} - V_{OUT}$ for the load appliance or V_{OUT} for the load removal).

MLCC capacitors typically have low ESR to minimize the ripple but also have low capacitance which doesn't minimize the voltage deviation during the load transient. On contrary, electrolytic capacitors usually have higher capacitance to minimize capacitive voltage deviation during the load transient, but also higher ESR value resulting in higher ripple voltage and resistive voltage drop. For these reasons, a mix between the electrolytic and MLCC capacitor is suggested so to minimize the ripple and reduce the voltage deviation in dynamic mode.

10.3 Input capacitors

The input capacitor bank is designed mainly to stand input RMS current, which depends on the output current (I_{OUT}) and duty cycle (D) for the regulation as follows:

Equation 13

$$I_{rms} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

The equation reaches its maximum value, $I_{OUT}/2$, when D = 0.5. Losses depend on the input capacitor ESR:

Equation 14

$$P = ESR \cdot I_{rms}^{2}$$

11 Package mechanical data

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Table 6. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 13. SO-8 package dimensions

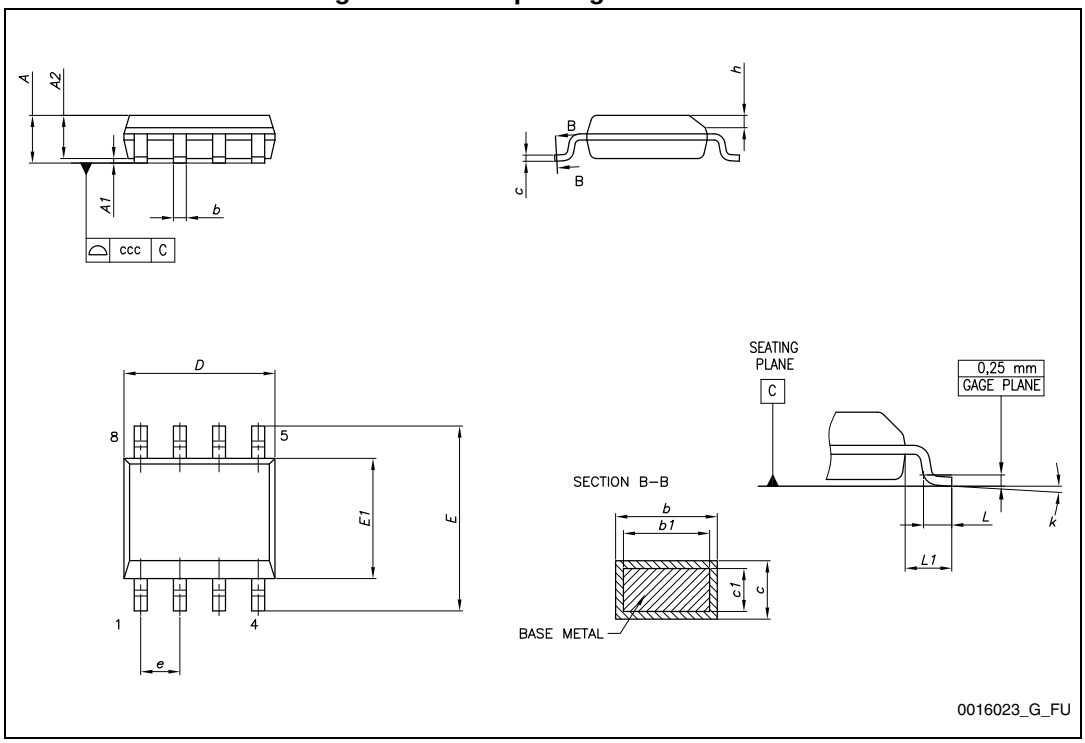


Figure 14. SO-8 footprint

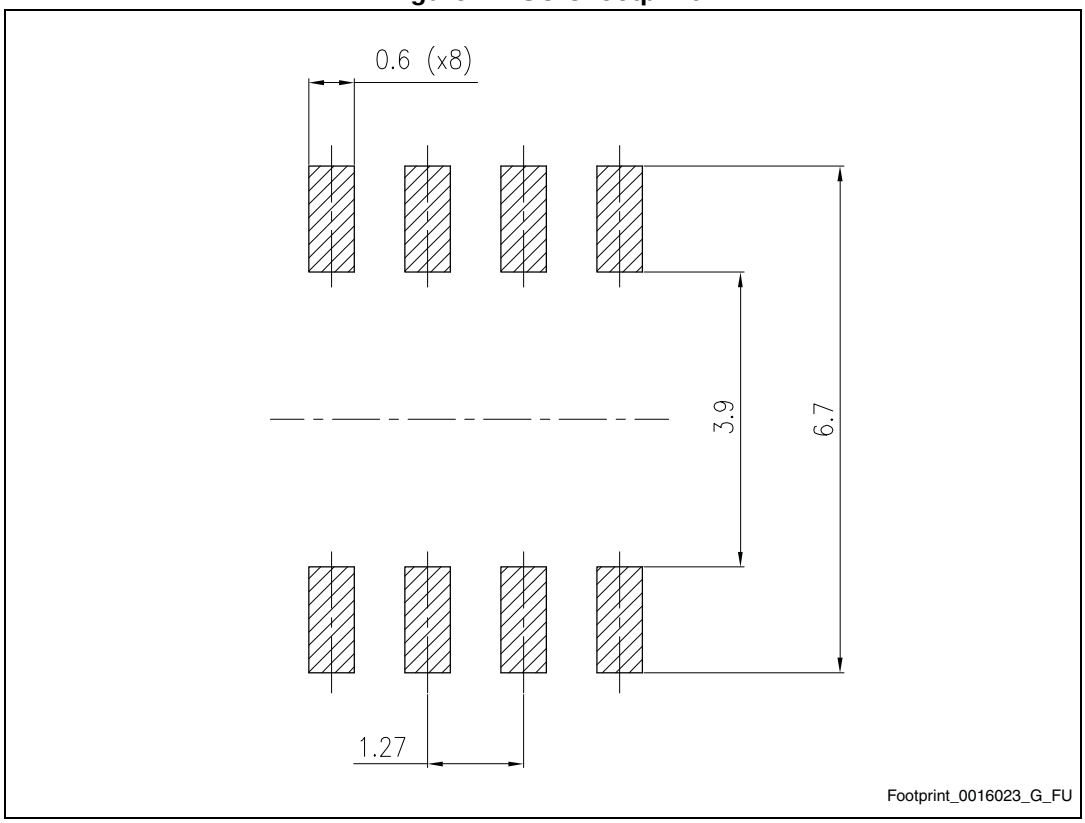
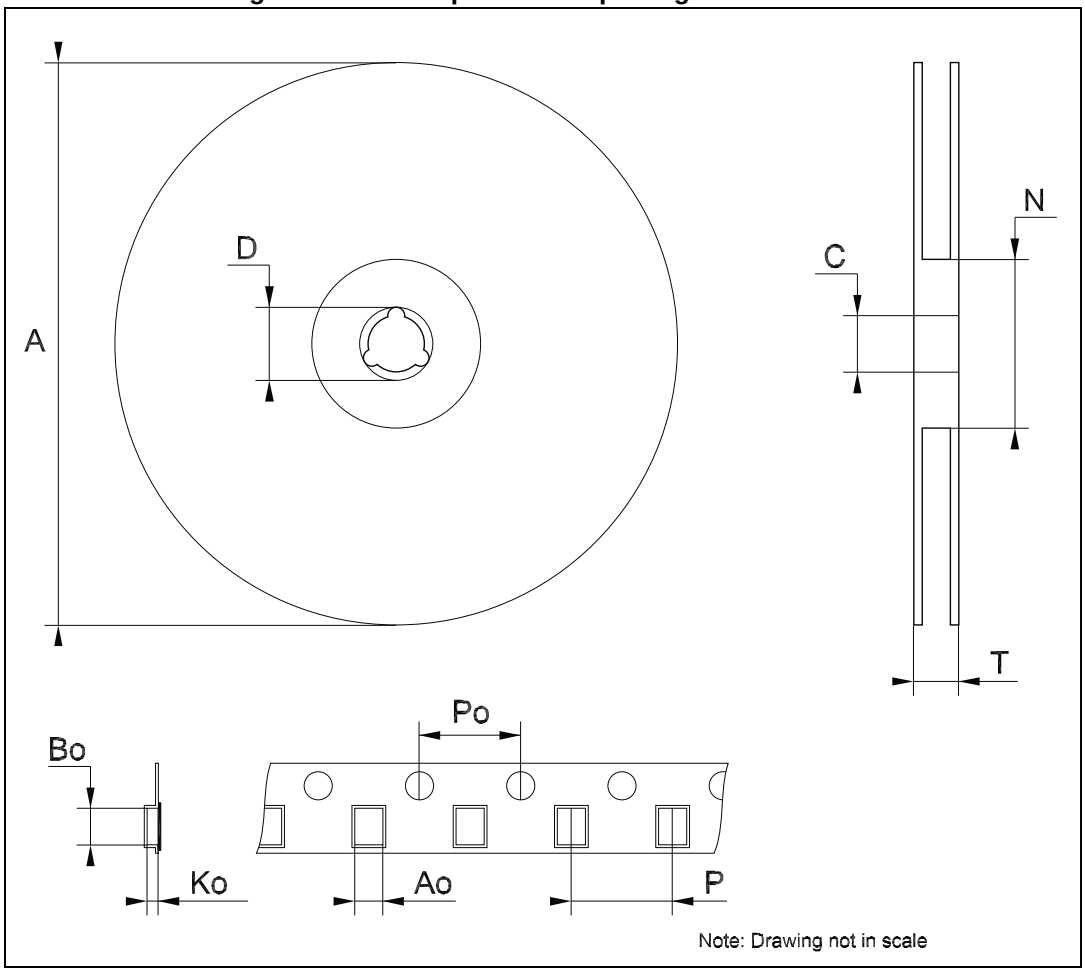


Table 7. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

Figure 15. SO-8 tape and reel package dimensions



12 Revision history

Table 8. Document revision history

Date	Revision	Changes
15-Jul-2013	1	Initial release.

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