

TMS570LS Series 16/32-BIT RISC Flash Microcontroller

Check for Samples: [TMS570LS20206-EP](#), [TMS570LS20216-EP](#)

1 TMS570LS Series 16/32-BIT RISC Flash Microcontroller

1.1 Features

- The TMS570LS20206-EP and TMS570LS20216-EP use the same silicon (die) as the TMS570LS Series IEC 61508 SIL3 certified microcontroller family however it is instead certified to meet GEIA-STD-00021-1 for Aerospace Qualified Electronic Components and tested for operation over the military temperature range.
- High-Performance Microcontroller
 - Dual CPUs running in Lockstep
 - ECC on Flash and SRAM
 - CPU and Memory BIST (Built-In Self Test)
 - Error Signaling Module (ESM) w/ Error Pin
- ARM® Cortex™-R4F 32-Bit RISC CPU
 - Efficient 1.6 DMIPS/MHz with 8-stage pipeline
 - Floating Point Unit with Single/Double Precision
 - Memory Protection Unit (MPU)
 - Open Architecture With Third-Party Support
- Operating Features
 - Up to 160-MHz System Clock
 - Core Supply Voltage (V_{CC}): 1.5 V
 - I/O Supply Voltage (V_{CCIO}): 3.3 V
- Integrated Memory
 - 2M-Byte Flash with ECC
 - 60K-Byte RAM with ECC
- Multiple Communication interfaces including FlexRay, CAN, and LIN
- NHET Timer and 2x 12-bit ADCs
- External Memory Interface (EMIF)
 - 16bit Data, 22bit Address, 4 Chip Selects
- Common TMS570 Platform Architecture
 - Consistent Memory Map across the family
 - Real-Time Interrupt (RTI) OS Timer
 - Vectored Interrupt Module (VIM)
 - Cyclic Redundancy Checker (CRC, 2 Channels)
- Direct Memory Access (DMA) Controller
 - 32 DMA requests and 16 Channels/ Control Packets
 - Parity on Control Packet Memory
 - Dedicated Memory Protection Unit (MPU)
- Frequency-Modulated Zero-Pin Phase-Locked Loop (FMzPLL)-Based Clock Module
 - Oscillator and PLL clock monitor
- Up to 115 Peripheral IO pins
 - 16 Dedicated GIO - 8 w/ External Interrupts
 - Programmable External Clock (ECLK)
- Communication Interfaces
 - Three Multi-buffered Serial Peripheral Interface (MibSPI) each with:
 - Four Chip Selects and one Enable pin
 - 128 buffers with parity
 - One with parallel mode
 - Two UART (SCI) interfaces with Local Interconnect Network Interface (LIN 2.0)
 - Three CAN (DCAN) Controller
 - Two with 64 mailboxes, one with 32
 - Parity on mailbox RAM
 - Dual Channel FlexRay™ Controller
 - 8K-Byte message RAM with parity
 - Transfer Unit with MPU and parity
- High-End Timer (NHET)
 - 32 Programmable I/O Channels
 - 128 Words High-End Timer RAM with parity
 - Transfer Unit with MPU and parity
- Two 12-Bit Multi-Buffered ADCs (MibADC)
 - 24 total ADC Input channels
 - Each has 64 Buffers with parity
- Trace and Calibration Interfaces
 - Embedded Trace Module (ETMR4)
 - Data Modification Module (DMM)
 - RAM Trace Port (RTP)
 - Parameter Overlay Module (POM)
- On-Chip emulation logic including IEEE 1149.1 JTAG, Boundary Scan and ARM Coresight components
- Full Development Kit Available
 - Development Boards
 - Code Composer Studio Integrated Development Environment (IDE)
 - HaLCoGen Code Generation Tool
 - HET Assembler and Simulator
 - nowFlash Flash Programming Tool



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

- **Packages Supported**
 - 337-Pin Ball Grid Array (GWT)
 - 144-Pin Lidded Quad Flat Pack (PGE)
- **Community Resources**
 - [TI E2E Community](#)

1.2 SUPPORTS DEFENSE AND AEROSPACE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Rated From –55°C to 125°C**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

1.3 Description

The TMS570LS series is a high performance microcontroller family. The architecture includes Dual CPUs in lockstep, CPU and Memory Built-In Self Test (BIST) logic, ECC on both the Flash and the data SRAM, parity on peripheral memories, and loop back capability on peripheral IOs.

The TMS570LS family integrates the ARM® Cortex™-R4F Floating Point CPU which offers an efficient 1.6 DMIPS/MHz, and has configurations which can run up to 160 MHz providing more than 250 DMIPS. The TMS570LS series also provides Flash (2MB) and data SRAM (160KB) options with single bit error correction and double bit error detection.

The TMS570LS devices feature peripherals for real-time control-based applications, including up to 32 nHET timer channels and two 12-bit A to D converters supporting up to 24 inputs. There are multiple communication interfaces including a 2-channel FlexRay, 3 CAN controllers supporting 64 mailboxes each, and 2 LIN/UART controllers.

With a wide choice of communication and control peripherals, the TMS570LS series is an ideal solution for high performance real time control applications.

The devices included in the TMS570LS series and described in this document are:

- TMS570LS20206
- TMS570LS20216

The TMS570LS series microcontrollers contain the following:

- Dual TMS570 16/32-Bit RISC (ARM Cortex™-R4F) in Lockstep
- Up to 2M-Byte Program Flash with ECC
- Up to 160K-Byte Static RAM (SRAM) with ECC
- Real-Time Interrupt (RTI) Operating System Timer
- Vectored Interrupt Module (VIM)
- Cyclic Redundancy Checker (CRC) with Parallel Signature Analysis (PSA)
- Direct Memory Access (DMA) Controller
- Frequency-Modulated Phase-Locked Loop (FMzPLL)-Based Clock Module With Prescaler
- Three Multi-buffered Serial Peripheral Interfaces (MibSPI)
- Two UARTs (SCI) with Local Interconnect Network Interfaces (LIN)
- Three CAN Controllers (DCAN)
- High-End Timer (NHET) with dedicated Transfer Unit (HTU)
- Available FlexRay Controller with dedicated PLL and Transfer Unit (FTU)
- External Clock Prescale (ECP) Module
- Two 16-Channel 12-Bit Multi-Buffered ADCs (MibADC) - 8 shared channels between the two ADCs
- Address Bus Parity with Failure Detection
- Error Signaling Module (ESM) with external error pin
- Voltage Monitor (VMON) with out of range reset assertion
- Embedded Trace Module (ETMR4)
- Data Modification Module (DMM)
- RAM Trace Port (RTP)
- Parameter Overlay Module (POM)
- 16 Dedicated General-Purpose I/O (GIO) Pins for GWT; 8 Dedicated GIO Pins for PGE
- 115 Total Peripheral I/Os for GWT; 68 Total Peripheral I/Os for PGE
- 16-Bit External Memory Interface (EMIF)

The devices utilize the big-endian format where the most significant byte of a word is stored at the lowest numbered byte and the least significant byte at the highest numbered byte.

The device memory includes general-purpose SRAM supporting single-cycle read/write accesses in byte, halfword, and word modes. The flash memory on this device is a nonvolatile, electrically erasable and programmable memory implemented with a 64-bit-wide data bus interface. The flash operates on a 3.3V supply input (same level as I/O supply) for all read, program and erase operations. When in pipeline mode, the flash operates with a system clock frequency of up to 160 MHz.

The device has nine communication interfaces: three MibSPIs, two LIN/SCIs, three DCANs and one FlexRay™ controller (optional). The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The LIN supports the Local Interconnect standard 2.0 and can be used as a UART in full-duplex mode using the standard Non-Return-to-Zero (NRZ) format. The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The DCAN is ideal for applications operating in noisy and harsh environments that require reliable serial communication or multiplexed wiring. The FlexRay uses a dual channel serial, fixed time base multimaster communication protocol with communication rates of 10 megabits per second (Mbps) per channel. A FlexRay Transfer Unit (FTU) enables autonomous transfers of FlexRay data to and from main CPU memory. Transfers are protected by a dedicated, built-in Memory Protection Unit (MPU).

The NHET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The NHET can be used for pulse width modulated outputs, capture or compare inputs, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. A High End Timer Transfer Unit (HET-TU) provides features to transfer NHET data to or from main memory. A Memory Protection Unit (MPU) is built into the HET-TU to protect against erroneous transfers.

The device has two 12-bit-resolution MibADCs with 24 total channels and 64 words of parity protected buffer RAM each. The MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. Eight channels are shared between the two ADCs. There are three separate groupings, two of which are triggerable by an external event. Each sequence can be converted once when triggered or configured for continuous conversion mode.

The frequency-modulated phase-locked loop (FMzPLL) clock module contains a phase-locked loop, a clock-monitor circuit, a clock-enable circuit, and a prescaler. The function of the FMzPLL is to multiply the external frequency reference to a higher frequency for internal use. The FMzPLL provides one of the six possible clock source inputs to the global clock module (GCM). The GCM module provides system clock (HCLK), real-time interrupt clock (RTICK1), CPU clock (GCLK), NHET clock (VCLK2), DCAN clock (AVCLK1), and peripheral interface clock (VCLK) to all other peripheral modules.

The device also has an external clock prescaler (ECP) module that when enabled, outputs a continuous external clock on the ECLK pin. The ECLK frequency is a user-programmable ratio of the peripheral interface clock (VCLK) frequency.

The Direct Memory Access Controller (DMA) has 32 DMA requests, 16 Channels/ Control Packets and parity protection on its memory. The DMA provides memory to memory transfer capabilities without CPU interaction. A Memory Protection Unit (MPU) is built into the DMA to protect memory against erroneous transfers.

The Error Signaling Module (ESM) monitors all device errors and determines whether an interrupt or external Error pin is triggered when a fault is detected.

The External Memory Interface (EMIF) provides a memory extension to asynchronous memories or other slave devices.

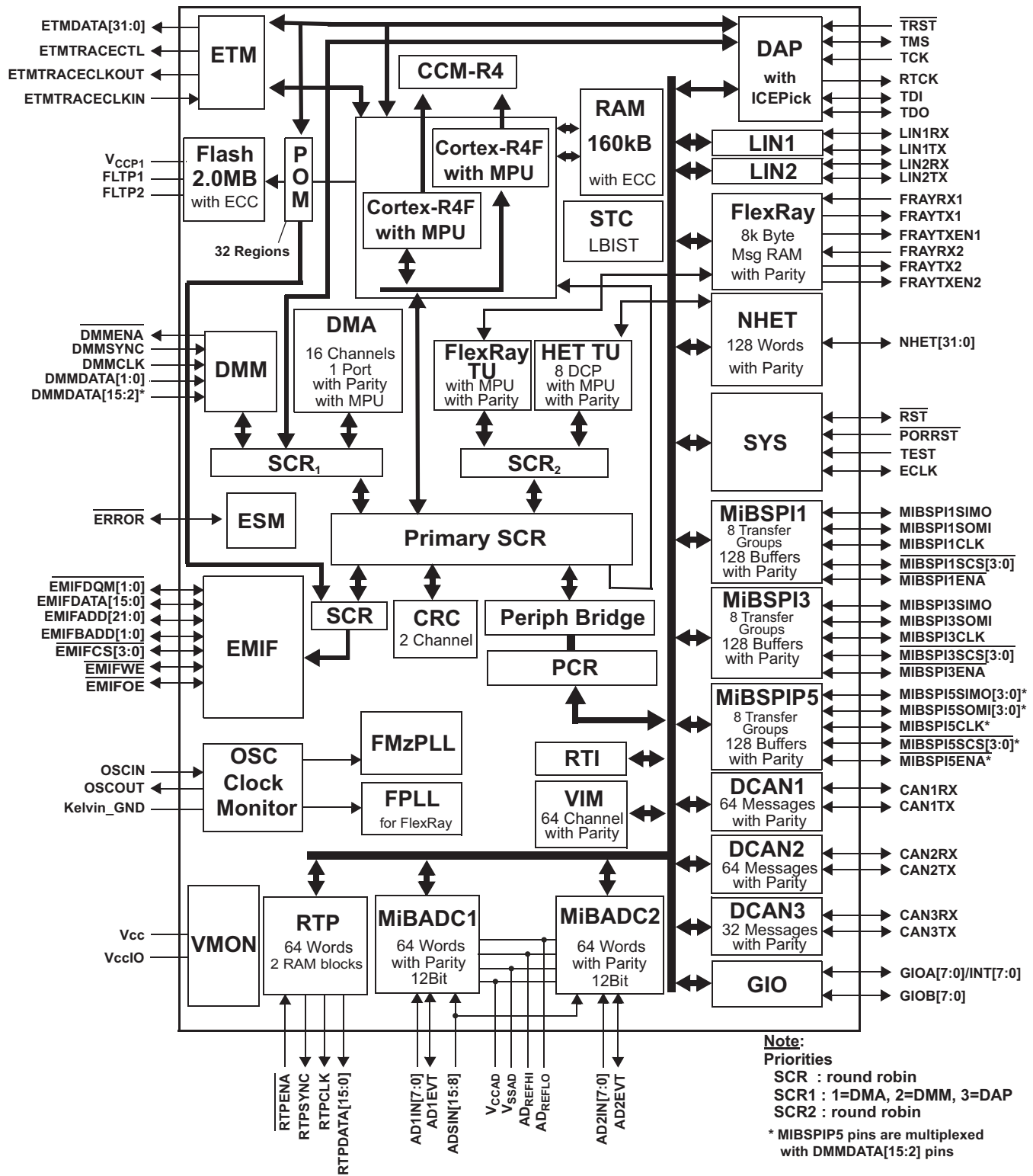
Several interfaces are implemented to enhance the debugging capabilities of application code. In addition to the built in ARM Cortex™-R4F CoreSight™ debug features, an External Trace Macrocell (ETM) provides instruction and data trace of program execution. For instrumentation purposes, a RAM Trace Port Module (RTP) is implemented to support high-speed output of RAM accesses by the CPU or any other master. A Direct Memory Module (DMM) gives the ability to write external data into the device memory. Both the RTP and DMM have no or only minimum impact on the program execution time of the application code. A Parameter Overlay Module (POM) can re-route Flash accesses to the EMIF, thus avoiding the re-programming steps necessary for parameter updates in Flash.

1.4 ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE | ORDERABLE PART NUMBER | TOP-SIDE MARKING | VID NUMBER |
|----------------|-------------|-----------------------|------------------|----------------|
| -55°C to 125°C | NFBGA (GWT) | S5LS20206ASGWTMEP | S20206ASGWTMEP | V62/12622-01YE |
| | | S5LS20216ASGWTMEP | S20216ASGWTMEP | V62/12622-02YE |
| | LQFP (PGE) | S5LS20206ASPGEMEP | S20206ASPGEMEP | V62/12622-01XE |
| | | S5LS20216ASPGEMEP | S20216ASPGEMEP | V62/12622-02XE |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

1.5 Functional Block Diagram



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2 Device Overview

2.1 Terms and Acronyms

Table 2-1. Terms and Acronyms

| Terms and Acronyms | Description | Comments |
|--------------------|--|---|
| ADC | Analog To Digital Converter | |
| AHB | Advanced High-performance Bus | Part of the R4 core |
| CCM-R4 | CPU Compare Module for Cortex™-R4F | |
| CRC | Cyclic Redundancy Check Controller | |
| DAP | Debug Access Port | DAP is an implementation of an ARM Debug Interface. |
| DCAN | Controller Area Network | |
| DMA | Direct Memory Access | |
| DMM | Data Modification Module | |
| ECC | Error Correction Code | |
| EMIF | External Memory Interface | |
| ESM | Error Signaling Module | |
| ETM | Embedded Trace Module | |
| FMzPLL | Frequency-Modulated Zero-Pin Phase-Locked Loop | |
| FPLL | FlexRay Phase-Locked Loop | |
| GIO | General-Purpose Input/Output | |
| HET | High-End Timer | |
| ICEPICK | In Circuit Emulation TAP (Test Access Port) Selection Module | ICEPick can connect or isolate a module level TAP to or from a higher level chip TAP. ICEPick was designed with both emulation and test requirements in mind. |
| JTAG | Joint Test Access Group | IEEE Committee responsible for Test Access Ports |
| LBIST | Logic Built-In Self Test | Test the integrity of R4 CPU |
| LIN | Local Interconnect Network | |
| VIM | Vectored Interrupt Manager | |
| MibSPI | Multi-Buffered Serial Peripheral Interface | |
| MPU | Memory Protection Unit | |
| OSC | Oscillator | |
| PBIST | Programmable Built-In Self Test | Test the integrity of SRAM |
| PCR | Peripheral Central Resource | |
| POM | Parameter Overlay Module | The POM provides a mechanism to redirect accesses to non-volatile memory into a volatile memory external to the device. |
| PSA | Parallel Signature Analysis | |
| RTI | Real-Time Interrupt | |
| RTP | RAM Trace Port | |
| SCR | Switch Central Resource | |
| SCI | Serial Communication Interface | |
| SECCED | Single Error Correction and Double Error Detection | |
| STC | Self Test Controller | |
| SYS | System Module | |
| TU | Transfer Unit | |
| VBUS | Virtual Bus | One of the protocols that comprises CBA (Common Bus Architecture) |
| VBUSP | Virtual Bus-Pipelined | One of the protocols that comprises CBA (Common Bus Architecture) |
| VMON | Voltage Monitor | |

2.2 Device Characteristics

The table below shows the different configurations options offered in the TMS570LS series of devices:

Table 2-2. Characteristics of the TMS570LS Series Devices

| Feature | TMS570LS20216 | | TMS570LS20206 | |
|---------------------|------------------|------------------|------------------|------------------|
| | 337 BGA (GWT) | 144 QFP (PGE) | 337 BGA (GWT) | 144 QFP (PGE) |
| Package Type | 337 BGA (GWT) | 144 QFP (PGE) | 337 BGA (GWT) | 144 QFP (PGE) |
| Speed | 160MHz | 140MHz | 160MHz | 140MHz |
| Flash Size | 2MB | 2MB | 2MB | 2MB |
| RAM Size | 160KB | 160kB | 160KB | 160kB |
| FlexRay | 2ch | 2ch | - | - |
| CAN | 3 | 2 | 3 | 2 |
| MibSPI | 3 | 3 | 3 | 3 |
| UART / LIN | 2 | 2 | 2 | 2 |
| NHET Channels | 32 | 25 | 32 | 25 |
| 12-Bit ADC Channels | 24 | 20 | 24 | 20 |
| EMIF | 16-bit | - | 16-bit | - |
| GIO | 16 | 8 | 16 | 8 |
| ETM | 32-bit | - | 32-bit | - |
| RTP | 16-bit | - | 16-bit | - |
| DMM | 16-bit | - | 16-bit | - |

2.3 Memory

2.3.1 Memory Map

The memory map, including all available Flash and RAM memory configurations for the device family, is shown below.

| | | |
|-------------|--|-------------|
| 0xFFFFFFFF | SYSTEM Modules | 0xFFFFFFFF |
| 0xFFFF80000 | | 0xFFFF80000 |
| 0xFFFF7FFFF | Peripherals | 0xFFFF7FFFF |
| 0xFF000000 | | 0xFF000000 |
| 0xFEFFFFFFF | CRC | 0xFEFFFFFFF |
| 0xFE000000 | | 0xFE000000 |
| | RESERVED | |
| 0x6FFFFFFF | | |
| | EMIF (256MB) | 0x603FFFFFF |
| | | 0x60000000 |
| 0x60000000 | | 0x60000000 |
| 0x204FFFFFF | | 0x204FFFFFF |
| | Flash - ECC (2MB Mirrored Image) | |
| 0x20400000 | | 0x20400000 |
| | RESERVED | |
| 0x201FFFFFF | | 0x201FFFFFF |
| | Flash (2MB) (Mirrored Image) | |
| 0x20000000 | | 0x20000000 |
| | RESERVED | |
| 0x08427FFF | | 0x08427FFF |
| 0x08400000 | RAM - ECC (160kB) | 0x08400000 |
| | RESERVED | |
| 0x08027FFF | | 0x08027FFF |
| | RAM (160kB) | |
| 0x08000000 | | 0x08000000 |
| | RESERVED | |
| 0x004FFFFFF | | 0x004FFFFFF |
| | Flash - ECC (2MB) | |
| 0x00400000 | | 0x00400000 |
| | RESERVED | |
| 0x001FFFFFF | | 0x001FFFFFF |
| | Flash (2MB) | |
| 0x00000000 | | 0x00000000 |

Figure 2-1. Memory Map of TMS570LS20216 and TMS570LS20206

The Parameter Overlay memory space maps to the lower 4MB of the EMIF CS0 memory space. ECC must be disabled by software via the CPU CP15 register if POM is used to overlay the program memory to the EMIF space; otherwise ECC errors will be generated. The contents of memory connected to the EMIF are not guaranteed after a power on reset. The addressable EMIF memory range is limited to the lower 32MB of each EMIF chip select for 16bit memories, and to the lower 16MB of each EMIF chip select for 8bit memories. The default EMIF data width is 16bit. The EMIF pins do not have GIO functionality.

2.3.2 Flash Memory

The F035 (130nm Flash Process) Flash memory is a nonvolatile electrically erasable and programmable memory. The Flash has a state machine for simplifying the program and erase functions.

This device's 2M-Byte flash memory contains four 512K-Byte memory arrays (or banks) consisting of 22 total sectors. 1M-Byte versions of the device contain only the first two 512K-Byte banks (Bank 0 and Bank 1) and have a total of 14 sectors. The bank and sector configurations are shown in Flash Memory Banks and Sectors . When in pipeline mode, the Flash operates with a system clock frequency of up to 160MHz (versus a system clock in non-pipeline mode of up to 36MHz). The flash in pipeline mode is capable of accessing 128 bits at a time and provides two 64-bit pipelined words to the CPU. The minimum size for an erase operation is one sector. A single program operation can program either one 32-bit word or one 16-bit half word at a time.

Table 2-3. Flash Memory Banks and Sectors

| Sector NO. | Segment | Low Address | High address | MEMORY ARRAYS (OR BANKS) |
|--------------------|------------|-------------|--------------|--------------------------|
| Bank 0: 512K Bytes | | | | |
| 0 | 32K Bytes | 0x0000_0000 | 0x0000_7FFF | BANK0 (512K Bytes) |
| 1 | 32K Bytes | 0x0000_8000 | 0x0000_FFFF | |
| 2 | 32K Bytes | 0x0001_0000 | 0x0001_7FFF | |
| 3 | 8K Bytes | 0x0001_8000 | 0x0001_9FFF | |
| 4 | 8K Bytes | 0x0001_A000 | 0x0001_BFFF | |
| 5 | 16K Bytes | 0x0001_C000 | 0x0001_FFFF | |
| 6 | 64K Bytes | 0x0002_0000 | 0x0002_FFFF | |
| 7 | 64K Bytes | 0x0003_0000 | 0x0003_FFFF | |
| 8 | 128K Bytes | 0x0004_0000 | 0x0005_FFFF | |
| 9 | 128K Bytes | 0x0006_0000 | 0x0007_FFFF | |
| Bank 1: 512K Bytes | | | | |
| 0 | 128K Bytes | 0x0008_0000 | 0x0009_FFFF | BANK1 (512K Bytes) |
| 1 | 128K Bytes | 0x000A_0000 | 0x000B_FFFF | |
| 2 | 128K Bytes | 0x000C_0000 | 0x000D_FFFF | |
| 3 | 128K Bytes | 0x000E_0000 | 0x000F_FFFF | |
| Bank 2: 512K Bytes | | | | |
| 0 | 128K Bytes | 0x0010_0000 | 0x0011_FFFF | BANK2 (512K Bytes) |
| 1 | 128K Bytes | 0x0012_0000 | 0x0013_FFFF | |
| 2 | 128K Bytes | 0x0014_0000 | 0x0015_FFFF | |
| 3 | 128K Bytes | 0x0016_0000 | 0x0017_FFFF | |
| Bank 3: 512K Bytes | | | | |
| 0 | 128K Bytes | 0x0018_0000 | 0x0019_FFFF | BANK3 (512k Bytes) |
| 1 | 128K Bytes | 0x001A_0000 | 0x001B_FFFF | |
| 2 | 128K Bytes | 0x001C_0000 | 0x001D_FFFF | |
| 3 | 128K Bytes | 0x001E_0000 | 0x001F_FFFF | |

NOTE

- The external flash pump voltage (VccP) is required for all flash operations (program, erase, and read). After a system reset, pipeline mode is disabled (FRDCNTL[2:0] is a "000"). In other words, the device powers up and comes out of reset in non-pipeline mode.
 - The user must program proper ECC bits throughout the entire flash memory to avoid ECC errors due to Cortex R4 speculative fetches if flash ECC is enabled.
 - The flash on this device does not support EEPROM emulation.
-

2.3.3 System Modules Assignment

This table shows the memory map for the Cyclic Redundancy Check (CRC) module, the Cortex™-R4F CoreSight™ debug module, and the System modules.

Table 2-4. System Modules Assignment

| Frame Name | Address Range | |
|------------------------------|---------------------|----------------------|
| | Frame Start Address | Frame Ending Address |
| CRC | 0xFE00_0000 | 0xFEFF_FFFF |
| CoreSight Debug ROM Register | 0xFFA0_0000 | 0xFFA0_0FFF |
| Cortex-R4F Debug Register | 0xFFA0_1000 | 0xFFA0_1FFF |
| ETM-R4 Register | 0xFFA0_2000 | 0xFFA0_2FFF |
| CoreSight TPIU Register | 0xFFA0_3000 | 0xFFA0_3FFF |
| POM Register | 0xFFA0_4000 | 0xFFA0_4FFF |
| DMA RAM | 0xFFF8_0000 | 0xFFF8_0FFF |
| VIM RAM | 0xFFF8_2000 | 0xFFF8_2FFF |
| RTP RAM | 0xFFF8_3000 | 0xFFF8_3FFF |
| Flash Wrapper Register | 0xFFF8_7000 | 0xFFF8_7FFF |
| PCR Register | 0xFFFF_E000 | 0xFFFF_E0FF |
| FlexRay PLL/STC CLK Register | 0xFFFF_E100 | 0xFFFF_E1FF |
| PBIST Register | 0xFFFF_E400 | 0xFFFF_E5FF |
| STC Register | 0xFFFF_E600 | 0xFFFF_E6FF |
| EMIF Register | 0xFFFF_E800 | 0xFFFF_E8FF |
| DMA Register | 0xFFFF_F000 | 0xFFFF_F3FF |
| ESM Register | 0xFFFF_F500 | 0xFFFF_F5FF |
| CCMR4 Register | 0xFFFF_F600 | 0xFFFF_F6FF |
| DMM Register | 0xFFFF_F700 | 0xFFFF_F7FF |
| RAM ECC even Register | 0xFFFF_F800 | 0xFFFF_F8FF |
| RAM ECC odd Register | 0xFFFF_F900 | 0xFFFF_F9FF |
| RTP Register | 0xFFFF_FA00 | 0xFFFF_FAFF |
| RTI Register | 0xFFFF_FC00 | 0xFFFF_FCFF |
| VIM Parity Register | 0xFFFF_FD00 | 0xFFFF_FDFF |
| VIM Register | 0xFFFF_FE00 | 0xFFFF_FEFF |
| System Register | 0xFFFF_FF00 | 0xFFFF_FFFF |

2.3.4 Peripheral Selects

The peripheral frame contains the memory map for the peripheral registers as well as the peripheral memories. The first table shows the memory map for the peripheral module registers and following table shows the memory map for the peripheral module memories.

Table 2-5. Peripheral Select Assignment

| Peripheral Module | Address Range | | Peripheral Selects |
|-------------------|---------------|----------------|--------------------|
| | Base Address | Ending Address | |
| MIBSPI5 | 0xFFFF7_FC00 | 0xFFFF7_FDFE | PS[0] |
| MIBSPI3 | 0xFFFF7_F800 | 0xFFFF7_F9FF | PS[1] |
| MIBSPI1 | 0xFFFF7_F400 | 0xFFFF7_F5FF | PS[2] |
| LIN2 | 0xFFFF7_E500 | 0xFFFF7_E5FF | PS[6] |
| LIN1 | 0xFFFF7_E400 | 0xFFFF7_E4FF | |
| DCAN3 | 0xFFFF7_E000 | 0xFFFF7_E1FF | PS[7] |
| DCAN2 | 0xFFFF7_DE00 | 0xFFFF7_DFFF | PS[8] |
| DCAN1 | 0xFFFF7_DC00 | 0xFFFF7_DDFF | |
| FlexRay | 0xFFFF7_C800 | 0xFFFF7_CFFF | PS[12]+PS[13] |
| MIBADC2 | 0xFFFF7_C200 | 0xFFFF7_C3FF | PS[15] |
| MIBADC1 | 0xFFFF7_C000 | 0xFFFF7_C1FF | |
| GIO | 0xFFFF7_BC00 | 0xFFFF7_BCFF | PS[16] |
| NHET | 0xFFFF7_B800 | 0xFFFF7_B8FF | PS[17] |
| HET TU | 0xFFFF7_A400 | 0xFFFF7_A4FF | PS[22] |
| FlexRay TU | 0xFFFF7_A000 | 0xFFFF7_A1FF | PS[23] |

Table 2-6. Peripheral Memory Selects

| Peripheral Module Memory | Address Range | | Peripheral Selects |
|--------------------------|---------------|----------------|--------------------|
| | Base Address | Ending Address | |
| MIBSPI5 RAM | 0xFF0A0000 | 0xFF0BFFFF | PCS[5] |
| MIBSPI3 RAM | 0xFF0C0000 | 0xFF0DFFFF | PCS[6] |
| MIBSPI1 RAM | 0xFF0E0000 | 0xFF0FFFFFFF | PCS[7] |
| DCAN3 RAM | 0xFF1A0000 | 0xFF1BFFFF | PCS[13] |
| DCAN2 RAM | 0xFF1C0000 | 0xFF1DFFFF | PCS[14] |
| DCAN1 RAM | 0xFF1E0000 | 0xFF1FFFFFFF | PCS[15] |
| MIBADC2 RAM | 0xFF3A0000 | 0xFF3BFFFF | PCS[29] |
| MIBADC1 RAM | 0xFF3E0000 | 0xFF3FFFFFFF | PCS[31] |
| NHET RAM | 0xFF460000 | 0xFF47FFFF | PCS[35] |
| HET TU RAM | 0xFF4E0000 | 0xFF4FFFFFFF | PCS[39] |
| FlexRay TU RAM | 0xFF500000 | 0xFF51FFFF | PCS[40] |

2.3.5 Memory Auto-Initialization

This device allows some of the on-chip memories to be initialized via the memory hardware initialization control registers in the System module. The purpose of having the hardware initialization is to program the memory arrays with error detection capability to a known state based on their error detection scheme (odd/even parity or ECC). The MINITGCR register enables the memory initialization sequence, and the MSINENA register selects the memories that are to be initialized. Please refer to the Architecture chapter of the Technical Reference Manual (TRM) for more information.

The mapping of the different memories to the specific bits in the MSINENA register is shown in the following table.

Table 2-7. Memory Initialization

| Connecting Module | Address Range | | RAM Select |
|-------------------|--------------------|----------------|------------------|
| | Base Address | Ending Address | |
| RAM | 0x08000000 | 0x0801FFFF | 0 |
| MIBSPI5 RAM | 0xFF0A0000 | 0xFF0BFFFF | 12 |
| MIBSPI3 RAM | 0xFF0C0000 | 0xFF0DFFFF | 11 |
| MIBSPI1 RAM | 0xFF0E0000 | 0xFF0FFFFFFF | 7 |
| DCAN3 RAM | 0xFF1A0000 | 0xFF1BFFFF | 10 |
| DCAN2 RAM | 0xFF1C0000 | 0xFF1DFFFF | 6 |
| DCAN1 RAM | 0xFF1E0000 | 0xFF1FFFFFFF | 5 |
| FlexRay RAM | RAM is not visible | | 9 ⁽¹⁾ |
| MIBADC2 RAM | 0xFF3A0000 | 0xFF3BFFFF | 14 |
| MIBADC1 RAM | 0xFF3E0000 | 0xFF3FFFFFFF | 8 |
| NHET RAM | 0xFF460000 | 0xFF47FFFF | 3 |
| HET TU RAM | 0xFF4E0000 | 0xFF4FFFFFFF | 4 |
| DMA RAM | 0xFFF80000 | 0xFFF80FFF | 1 |
| VIM RAM | 0xFFF82000 | 0xFFF82FFF | 2 |
| FlexRay TU RAM | 0xFF500000 | 0xFF51FFFF | 13 |

(1) reserved only; the FlexRay RAM has its own Initialization mechanism.

The associated ECC RAM will get initialized as well, if the ECC functionality is enabled.

The associated Parity RAM will get initialized as well, if the Parity functionality is enabled.

NOTE

The user must initialize entire SRAM with ECC bits to avoid ECC errors due to Cortex R4 speculative fetches if SRAM ECC is enabled.

2.3.6 PBIST RAM Self Test

The PBIST (Programmable Built-In Self Test) architecture provides a run-time-programmable memory BIST engine for varying levels of test coverage across the device's embedded RAM memory. The PBIST architecture consists of a small CPU with an instruction set targeted specifically towards testing RAM memories. This CPU includes both control and instruction registers necessary to execute the individual memory algorithms. In order to minimize test load overhead, once an algorithm is loaded into the instruction registers, it can be run on multiple memories of different sizes or types. The memory configuration information and test algorithm code is stored in an on-chip ROM. The PBIST RAM groups implemented on this device are shown in the following table. More information about memory self test can be found in the PBIST chapter of the device TRM.

Table 2-8. PBIST RAM Grouping

| RAM Group | Module | Memory Type | RGS /RDS ⁽¹⁾ | Test Pattern (Algorithm) | | | | | | | | |
|-----------|-----------|-------------------------------|-------------------------|-------------------------------------|-------------------------------------|---|---|--|--|---|---|--|
| | | | | Triple slow read [ROM clock cycles] | Triple fast read [ROM clock cycles] | March 13N [HCLK/VCLK ⁽²⁾ cycles] | Down 1A [HCLK/VCLK ⁽²⁾ cycles] | Pre-charge [HCLK/VCLK ⁽²⁾ cycles] | Map column [HCLK/VCLK ⁽²⁾ cycles] | DTXN 2A [HCLK/VCLK ⁽²⁾ cycles] | PMOS open [HCLK/VCLK ⁽²⁾ cycles] | |
| 1 | PBIST ROM | ROM | 0/1 | 12290 | 4098 | | | | | | | |
| 2 | STC ROM | ROM | 13/1 | 24578 | 8194 | | | | | | | |
| 3 | DCAN1 | SP | 1/0..2 | | | 12600 | 2637 | 2064 | 1914 | 5490 | 11544 | |
| 4 | DCAN2 | SP | 2/0..2 | | | 12600 | 2637 | 2064 | 1914 | 5490 | 11544 | |
| 5 | DCAN3 | SP | 3/0..2 | | | 6360 | 1341 | 1104 | 1146 | 2754 | 5016 | |
| 6 | ESRAM | SP, multi-strobe w/page mode | 4/21..22 | | | 266320 | 52254 | 41120 | 33212 | 181260 | 409616 | |
| 7 | MibSPI | SP | 5/0..5 | | | 50160 | 10458 | 7968 | 6900 | 21924 | 52272 | |
| 8 | VIM | SP | 6/0 | | | 4200 | 879 | 688 | 638 | 1830 | 3848 | |
| 9 | MibADC | 2P, sync write async read | 7/0..1 | | | 8400 | 1758 | 1376 | 1276 | 3660 | 7696 | |
| 10 | DMA | 2P, sync write async read | 8/0..5 | | | 18960 | 4410 | 3072 | 2772 | 6084 | Not Available | |
| 11 | NHET | 2P, sync write async read | 9/0..11 | | | 25440 | 5940 | 4224 | 4008 | 8136 | 20064 | |
| 12 | HET TU | 2P, sync write async read | 10/0..5 | | | 6480 | 1530 | 1152 | 1236 | 2052 | 4272 | |
| 13 | RTP | 2P, sync write async read | 11/0..8 | | | 37800 | 8775 | 6048 | 5310 | 12150 | 34632 | |
| 14 | FlexRay | SP | 12/0..7 | | | 175040 | 34872 | 27296 | 22608 | 108912 | 246336 | |
| 15 | ESRAM | SP, multi-strobe w/ page mode | 4/20 | | | 133160 | 26127 | 20560 | 16606 | 90630 | 204808 | |

SP = Single Port RAM; 2P = Two Port RAM

(1) RGS (RAM group select) and RDS (return data select) stand for a unique RAM select id. More information about the RGS and the RDS can be found in the technical reference manual (TRM)

(2) The test clock for ESRAM, DMA and RTP is HCLK; the test clock for other modules is VCLK.

NOTE

- The March13N test algorithm is recommended for application testing.
- The maximum PBIST test execution speed is limited to 100MHz.
- The supply current while performing PBIST self test is different than the device operating mode current. These values can be found in the I_{cc} section of the device electrical specifications.

2.4 Pin Assignments

2.4.1 GWT BGA Package Pinout (337 ball)

| | A | B | C | D | E | F | G | H | J | K | L | |
|----|-----------|---------------------------|---------------|--------------------------|-----------------|--------------|-----------------|-----------------|-----------------|--------------|--------------|----|
| 19 | VSS | VSS | TMS | NHET [10] | MIBSPI5 CS[0] | MIBSPI1 SIMO | MIBSPI1 ENA | MIBSPI5 CLK | MIBSPI5 SIMO[0] | NHET [28] | DMM DATA[0] | 19 |
| 18 | VSS | TCK | TDO | $\overline{\text{TRST}}$ | NHET [08] | MIBSPI1 CLK | MIBSPI1 SOMI | MIBSPI5 ENA | MIBSPI5 SOMI[0] | NHET [0] | DMM DATA[1] | 18 |
| 17 | TDI | $\overline{\text{RST}}$ | EMIF_ADDR[21] | EMIF_WE | MIBSPI5 SOM[1] | DMM CLK | MIBSPI5 SIMO[3] | MIBSPI5 SIMO[2] | NHET [31] | EMIF_CS[1] | EMIF_CS[0] | 17 |
| 16 | RTCK | FRAY TXEN1 | EMIF_ADDR[20] | EMIF_BA[1] | MIBSPI5 SIMO[1] | DMM ENA | MIBSPI5 SOMI[3] | MIBSPI5 SOMI[2] | DMM SYNC | EMIF_DATA[0] | EMIF_DATA[1] | 16 |
| 15 | FRAY RX1 | FRAY TX1 | EMIF_ADDR[19] | EMIF_ADDR[18] | ETM DATA[06] | ETM DATA[05] | ETM DATA[04] | ETM DATA[03] | ETM DATA[02] | ETM DATA[16] | ETM DATA[17] | 15 |
| 14 | NHET [26] | $\overline{\text{ERROR}}$ | EMIF_ADDR[17] | EMIF_ADDR[16] | ETM DATA[07] | VCCIO | VCCIO | VCCIO | VCC | VCC | VCCIO | 14 |
| 13 | NHET [17] | NHET [19] | EMIF_ADDR[15] | EMIF_BA[0] | ETM DATA[12] | VCCIO | | | | | | 13 |
| 12 | ECLK | NHET [04] | EMIF_ADDR[14] | EMIF_OE | ETM DATA[13] | VCCIO | | VSS | VSS | VCC | VSS | 12 |
| 11 | NHET [14] | NHET [30] | EMIF_ADDR[13] | EMIF_DQM[1] | ETM DATA[14] | VCCIO | | VSS | VSS | VSS | VSS | 11 |
| 10 | CAN1 TX | CAN1 RX | EMIF_ADDR[12] | EMIF_DQM[0] | ETM DATA[15] | VCC | | VCC | VSS | VSS | VSS | 10 |
| | A | B | C | D | E | F | G | H | J | K | L | |

Figure 2-2. GWT Package Pinout Top Left Quadrant (337 ball) [Top View]

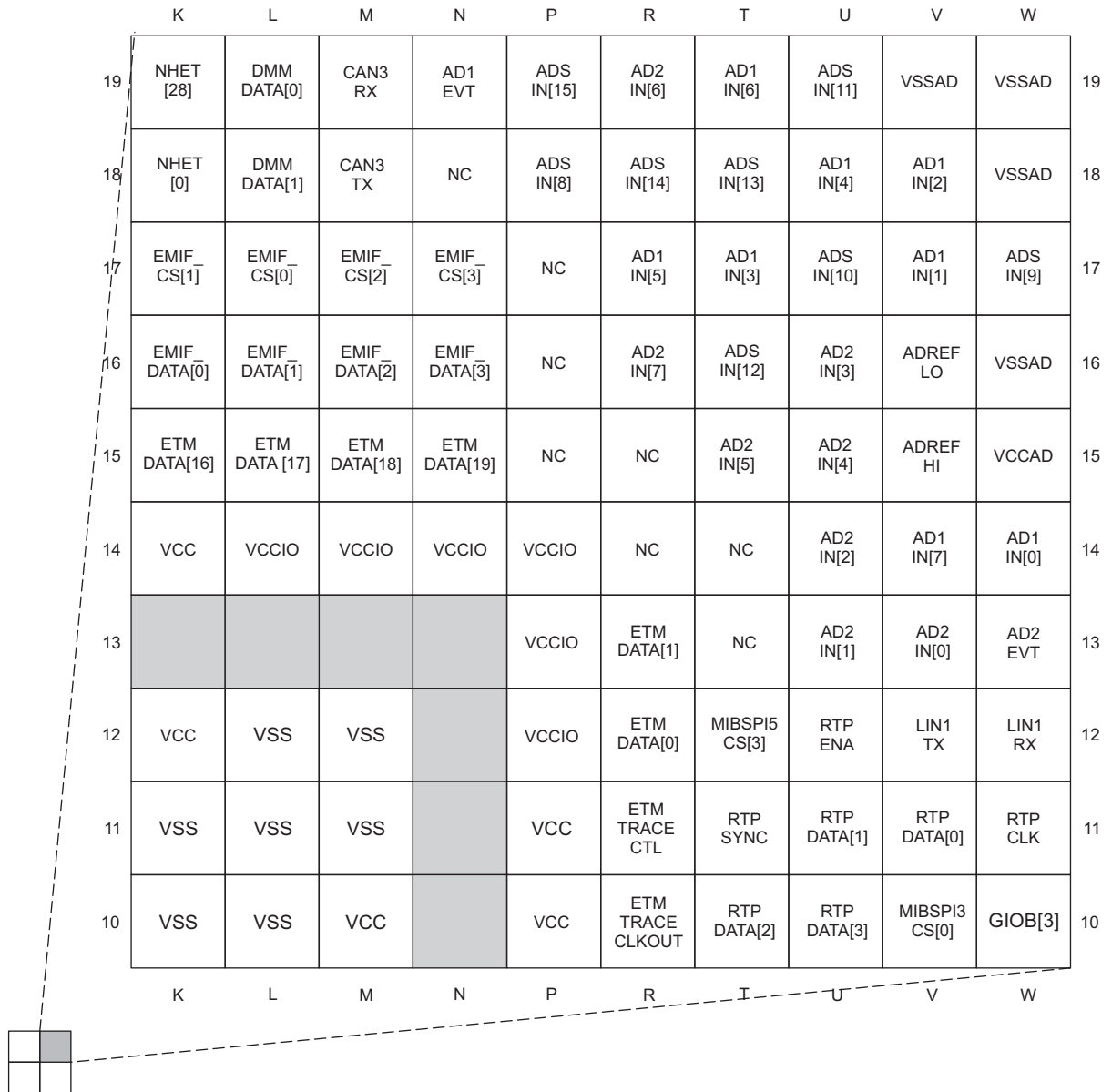


Figure 2-3. GWT Package Pinout Top Right Quadrant (337 ball) [Top View]

| | | | | | | | | | | | | |
|----|-----------|---------------|---------------|--------------|--------------|---------------|---------------|-----------|---------------|--------------|--------------|----|
| | A | B | C | D | E | F | G | H | J | K | L | |
| 10 | CAN1TX | CAN1RX | EMIF_ADDR[12] | EMIF_DQM[0] | ETM_DATA[15] | VCC | | VCC | VSS | VSS | VSS | 10 |
| 9 | NHET [27] | FRAY_TXEN2 | EMIF_ADDR[11] | EMIF_ADDR[5] | ETM_DATA[8] | VCC | | VSS | VSS | VSS | VSS | 9 |
| 8 | FRAY_RX2 | FRAY_TX2 | EMIF_ADDR[10] | EMIF_ADDR[4] | ETM_DATA[9] | VCCP | | VSS | VSS | VCC | VSS | 8 |
| 7 | LIN2_RX | LIN2_TX | EMIF_ADDR[9] | EMIF_ADDR[3] | ETM_DATA[10] | VCCIO | | | | | | 7 |
| 6 | GIOA [4] | MIBSPI5_CS[1] | EMIF_ADDR[8] | EMIF_ADDR[2] | ETM_DATA[11] | VCCIO | VCCIO | VCCIO | VCCIO | VCC | VCC | 6 |
| 5 | GIOA [0] | GIOA [5] | EMIF_ADDR[7] | EMIF_ADDR[1] | ETM_DATA[20] | ETM_DATA[21] | ETM_DATA[22] | FLTP2 | FLTP1 | ETM_DATA[23] | ETM_DATA[24] | 5 |
| 4 | NHET [16] | NHET [12] | EMIF_ADDR[6] | EMIF_ADDR[0] | EMIF_DATA[4] | EMIF_DATA[5] | EMIF_DATA[6] | NHET [21] | NHET [23] | EMIF_DATA[7] | EMIF_DATA[8] | 4 |
| 3 | NHET [29] | NHET [22] | MIBSPI3_CS[3] | NC | NHET [11] | MIBSPI1_CS[1] | MIBSPI1_CS[2] | GIOA [6] | MIBSPI1_CS[3] | NC | NC | 3 |
| 2 | VSS | MIBSPI3_CS[2] | GIOA [1] | NC | NC | GIOB [2] | GIOB [5] | CAN2_TX | GIOB [6] | GIOB [1] | KELVIN_GND | 2 |
| 1 | VSS | VSS | GIOA [2] | NC | GIOA [3] | GIOB [7] | GIOB [4] | CAN2_RX | NHET [18] | OSCIN | OSCOUT | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | |

Figure 2-4. GWT Package Pinout Bottom Left Quadrant (337 ball) [Top View]

| | K | L | M | N | P | R | T | U | V | W | |
|----|--------------|--------------|--------------|---------------|---------------|------------------|---------------|--------------|---------------|----------------------------|----|
| 10 | VSS | VSS | VCC | | VCC | ETM TRACE CLKOUT | RTP DATA[2] | RTP DATA[3] | MIBSPI3 CS[0] | GIOB[3] | 10 |
| 9 | VSS | VSS | VSS | | VCCIO | ETM TRACE CLKIN | RTP DATA[4] | RTP DATA[5] | MIBSPI3 CLK | MIBSPI3 ENA | 9 |
| 8 | VCC | VSS | VSS | | VCCIO | ETM DATA[31] | EMIF_DATA[15] | RTP DATA[6] | MIBSPI3 SOMI | MIBSPI3 SIMO | 8 |
| 7 | | | | | VCCIO | ETM DATA[30] | EMIF_DATA[14] | RTP DATA[7] | NHET [9] | $\overline{\text{PORRST}}$ | 7 |
| 6 | VCC | VCC | VCCIO | VCCIO | VCCIO | ETM DATA[29] | EMIF_DATA[13] | RTP DATA[8] | NHET [5] | MIBSPI5 CS[2] | 6 |
| 5 | ETM DATA[23] | ETM DATA[24] | ETM DATA[25] | ETM DATA[26] | ETM DATA[27] | ETM DATA[28] | EMIF_DATA[12] | RTP DATA[9] | MIBSPI3 CS[1] | NHET [2] | 5 |
| 4 | EMIF_DATA[7] | EMIF_DATA[8] | EMIF_DATA[9] | EMIF_DATA[10] | EMIF_DATA[11] | NC | RTP DATA[11] | RTP DATA[10] | VSS | NC | 4 |
| 3 | NC | NC | NHET [25] | NC | NC | NC | RTP DATA[14] | RTP DATA[13] | RTP DATA[12] | NHET [6] | 3 |
| 2 | GIOB [1] | KELVIN GND | GIOB [0] | NHET [13] | NHET [20] | MIBSPI1 CS[0] | RTP DATA[15] | TEST | NHET [1] | VSS | 2 |
| 1 | OSCIN | OSCOUT | GIOA [7] | NHET [15] | NHET [24] | NC | NHET [7] | NHET [3] | VSS | VSS | 1 |
| | K | L | M | N | P | R | T | U | V | W | |

Figure 2-5. GWT Package Pinout Bottom Right Quadrant (337 ball) [Top View]

2.4.2 PGE QFP Package Pinout (144 pin)

(TOP VIEW)

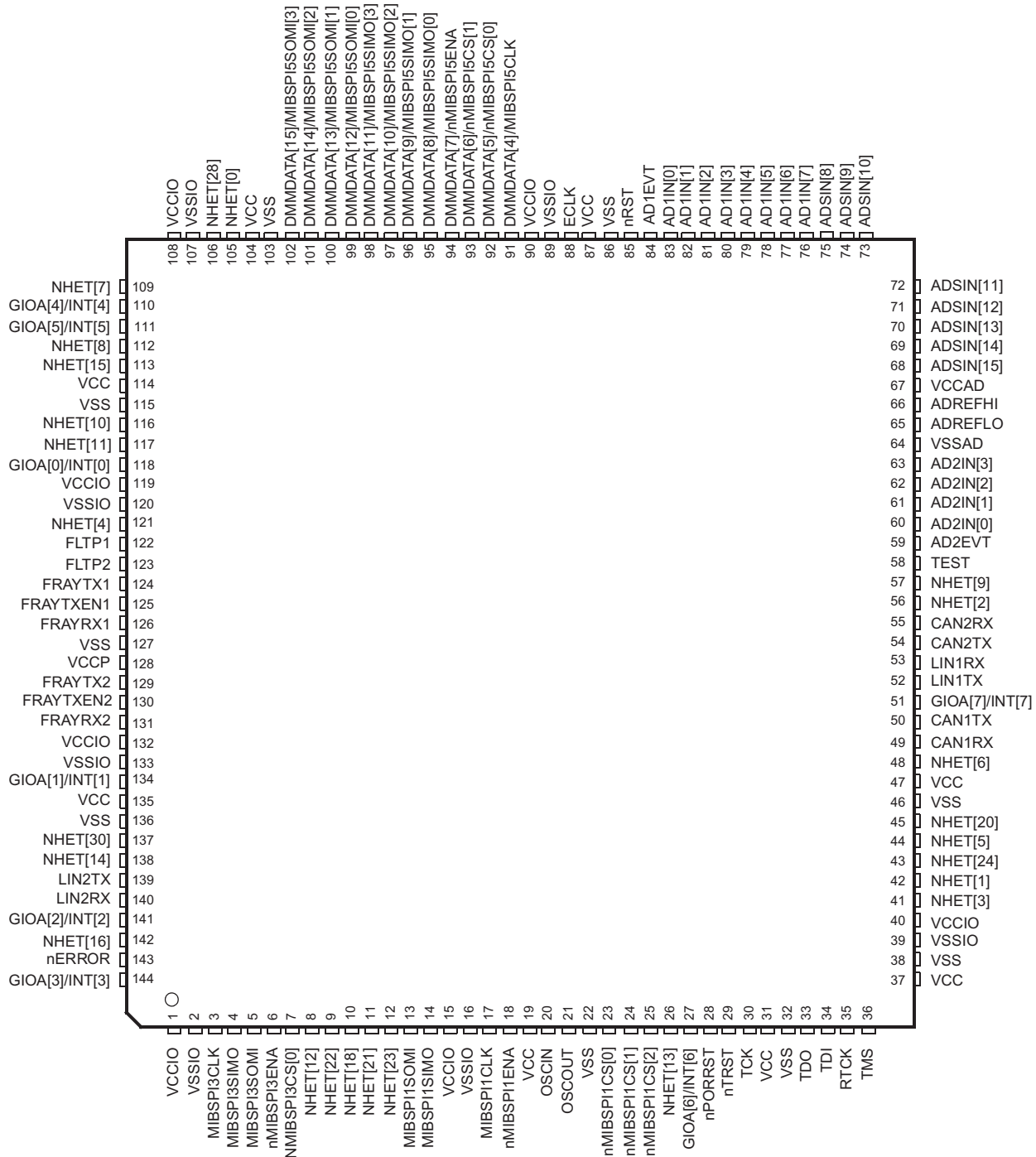


Figure 2-6. PGE Pinout (144 pin) [Top View]

2.5 Terminal Functions

This following table describes the pins on the device.

NOTE

Table Abbreviations: PWR = power, GND = ground, REF = reference voltage, NC = no connect, IPD = Internal Pull Down, IPU = Internal Pull Up, I/O = Input/Output, I = Input, O = Output

Table 2-9. Terminal Functions

| Name | Terminal | | | | Type | Internal pullup/pulldown | Description |
|------------------------------|---------------|-----|---------------|-----|----------|--------------------------|--|
| | TMS570LS20216 | | TMS570LS20206 | | | | |
| | 337 | 144 | 337 | 144 | | | |
| HIGH-END TIMER (NHET) | | | | | | | |
| NHET[0] | K18 | 105 | K18 | 105 | 3.3V I/O | 2mA - z | <p>Timer input capture or output compare. The applicable NHET pins can be programmed as general-purpose input/output (GIO) pins. NHET pins are high-resolution.</p> <p>The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structures. The next higher odd HR pin structure is always implemented, even if the next higher odd HR pad and/or pin itself is not. The HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O.</p> <p>NHET[0] provides SPI clock when used for SPI emulation.</p> <p>Each NHET pin is equipped with an input suppression filter that can be used to eliminate the sampling of pulses that are smaller than a programmable duration GIOA[0]/INT[0] is also connected to the NHET Pin Disable input of the NHET module.</p> <p>NHET pins can be programmed as a GIO pins when not used as NHET functional pins.</p> |
| NHET[1] | V2 | 42 | V2 | 42 | | | |
| NHET[2] | W5 | 56 | W5 | 56 | | | |
| NHET[3] | U1 | 41 | U1 | 41 | | | |
| NHET[4] | B12 | 121 | B12 | 121 | | | |
| NHET[5] | V6 | 44 | V6 | 44 | | | |
| NHET[6] | W3 | 48 | W3 | 48 | | | |
| NHET[7] | T1 | 109 | T1 | 109 | | | |
| NHET[8] | E18 | 112 | E18 | 112 | | | |
| NHET[9] | V7 | 57 | V7 | 57 | | | |
| NHET[10] | D19 | 116 | D19 | 116 | | | |
| NHET[11] | E3 | 117 | E3 | 117 | | | |
| NHET[12] | B4 | 8 | B4 | 8 | | | |
| NHET[13] | N2 | 26 | N2 | 26 | | | |
| NHET[14] | A11 | 138 | A11 | 138 | | | |
| NHET[15] | N1 | 113 | N1 | 113 | | | |
| NHET[16] | A4 | 142 | A4 | 142 | | | |
| NHET[17] | A13 | | A13 | | | | |
| NHET[18] | J1 | 10 | J1 | 10 | | | |
| NHET[19] | B13 | | B13 | | | | |
| NHET[20] | P2 | 45 | P2 | 45 | | | |
| NHET[21] | H4 | 11 | H4 | 11 | | | |
| NHET[22] | B3 | 9 | B3 | 9 | | | |
| NHET[23] | J4 | 12 | J4 | 12 | | | |
| NHET[24] | P1 | 43 | P1 | 43 | | | |
| NHET[25] | M3 | | M3 | | | | |
| NHET[26] | A14 | | A14 | | | | |
| NHET[27] | A9 | | A9 | | | | |
| NHET[28] | K19 | 106 | K19 | 106 | | | |
| NHET[29] | A3 | | A3 | | | | |
| NHET[30] | B11 | 137 | B11 | 137 | | | |
| NHET[31] | J17 | | J17 | | | | |

Table 2-9. Terminal Functions (continued)

| Name | Terminal | | | | Type | Internal pullup/pulldown | Description | | |
|--|---------------|-----|---------------|-----|----------|--------------------------|-----------------------------------|--|------------------------------------|
| | TMS570LS20216 | | TMS570LS20206 | | | | | | |
| | 337 | 144 | 337 | 144 | | | | | |
| GENERAL-PURPOSE I/O (GIO) | | | | | | | | | |
| GIOA[0]/INT0 | A5 | 118 | A5 | 118 | 3.3V I/O | 2mA - z | Program mable IPD (20uA) | General-purpose input/output pin. GIOA[0]/INT[0] is an interrupt-capable pin. GIOA[0]/INT[0] is also connected to the NHET Pin Disable input of the NHET module. | |
| GIOA[1]/INT1 | C2 | 134 | C2 | 134 | | | | General-purpose input/output pins. GIOA[7:1]/INT[7:1] are interrupt-capable pins. | |
| GIOA[2]/INT2 | C1 | 141 | C1 | 141 | | | | | |
| GIOA[3]/INT3 | E1 | 144 | E1 | 144 | | | | | |
| GIOA[4]/INT4 | A6 | 110 | A6 | 110 | | | | | |
| GIOA[5]/INT5 | B5 | 111 | B5 | 111 | | | | | |
| GIOA[6]/INT6 | H3 | 27 | H3 | 27 | | | | | |
| GIOA[7]/INT7 | M1 | 51 | M1 | 51 | | | | | |
| GIOB[0] | M2 | | M2 | | | | | | General-purpose input/output pins. |
| GIOB[1] | K2 | | K2 | | | | | | |
| GIOB[2] | F2 | | F2 | | | | | | |
| GIOB[3] | W10 | | W10 | | | | | | |
| GIOB[4] | G1 | | G1 | | | | | | |
| GIOB[5] | G2 | | G2 | | | | | | |
| GIOB[6] | J2 | | J2 | | | | | | |
| GIOB[7] | F1 | | F1 | | | | | | |
| FlexRay Controller (FLEXRAY) | | | | | | | | | |
| NOTE: Devices with out the FlexRay option should leave all FlexRay pins unconnected (NC) | | | | | | | | | |
| FRAYRX1 | A15 | 126 | | | 3.3V I | | Program mable IPD (20uA) | FlexRay data receive (channel 1) pin | |
| FRAYTX1 | B15 | 124 | | | 3.3V O | 8mA | | FlexRay data transmit (channel 1) pin | |
| FRAYTXEN1 | B16 | 125 | | | | 8mA | | FlexRay transmit enable (channel 1) pin | |
| FRAYRX2 | A8 | 131 | | | 3.3V I | | Program mable IPD(20u A) | FlexRay data receive (channel 2) pin | |
| FRAYTX2 | B8 | 129 | | | 3.3V O | 8mA | | FlexRay data transmit (channel 2) pin | |
| FRAYTXEN2 | B9 | 130 | | | | 8mA | | FlexRay transmit enable (channel 2) pin | |
| CAN Controller (DCAN1) | | | | | | | | | |
| CAN1TX | A10 | 50 | A10 | 50 | 3.3V I/O | 2mA - z | Program mable IPU (20uA) | CAN1 transmit pin or GIO pin | |
| CAN1RX | B10 | 49 | B10 | 49 | | | | CAN1 receive pin or GIO pin | |
| CAN Controller (DCAN2) | | | | | | | | | |
| CAN2TX | H2 | 54 | H2 | 54 | 3.3V I/O | 2mA - z | Program mable IPU (20uA) | CAN2 transmit pin or GIO pin | |
| CAN2RX | H1 | 55 | H1 | 55 | | | | CAN2 receive pin or GIO pin | |
| CAN Controller (DCAN3) | | | | | | | | | |
| CAN3TX | M18 | | M18 | | 3.3V I/O | 2mA - z | program mable IPU (20uA) | CAN3 transmit pin or GIO pin | |
| CAN3RX | M19 | | M19 | | | | | CAN3 receive pin or GIO pin | |

Table 2-9. Terminal Functions (continued)

| Name | Terminal | | | | Type | Internal pullup/pulldown | Description | |
|--|---------------|-----|---------------|-----|----------|--------------------------|--------------------------|--|
| | TMS570LS20216 | | TMS570LS20206 | | | | | |
| | 337 | 144 | 337 | 144 | | | | |
| Serial Communications Interface (SCI)/Local Interconnect Network (LIN1) | | | | | | | | |
| LIN1RX | W12 | 53 | W12 | 53 | 3.3V I/O | 2mA - z | Program mable IPU (20uA) | LIN1 data receive pin or GIO pin |
| LIN1TX | V12 | 52 | V12 | 52 | | | | LIN1 data transmit pin or GIO pin |
| Serial Communications Interface (SCI)/Local Interconnect Network (LIN2) | | | | | | | | |
| LIN2RX | A7 | 140 | A7 | 140 | 3.3V I/O | 2mA - z | Program mable IPU (20uA) | LIN2 data receive pin or GIO pin |
| LIN2TX | B7 | 139 | B7 | 139 | | | | LIN2 data transmit pin or GIO pin |
| Multibuffered Serial Peripheral Interface (MIBSPI1) | | | | | | | | |
| MIBSPI1CLK | F18 | 17 | F18 | 17 | 3.3V I/O | 4mA | Program mable IPU (20uA) | MIBSPI1 clock pin or GIO pin |
| MIBSPI1CS[0] | R2 | 23 | R2 | 23 | | 2mA - z | | MIBSPI1 slave chip select pins or GIO pins |
| MIBSPI1CS[1] | F3 | 24 | F3 | 24 | | | | |
| MIBSPI1CS[2] | G3 | 25 | G3 | 25 | | | | |
| MIBSPI1CS[3] | J3 | | J3 | | | 2mA - z | | MIBSPI1 enable pin or GIO pin |
| MIBSPI1EN \bar{A} | G19 | 18 | G19 | 18 | | | | |
| MIBSPI1SIMO | F19 | 14 | F19 | 14 | | 4mA | | MIBSPI1 data stream - Slave in/master out pin or GIO pin |
| MIBSPI1SOMI | G18 | 13 | G18 | 13 | | | | MIBSPI1 data stream - Slave out/master in pin or GIO pin |
| Multibuffered Serial Peripheral Interface (MIBSPI3) | | | | | | | | |
| MIBSPI3CLK | V9 | 3 | V9 | 3 | 3.3V I/O | 4mA | Program mable IPU (20uA) | MIBSPI3 clock pin or GIO pin |
| MIBSPI3CS[0] | V10 | 7 | V10 | 7 | | 2mA - z | | MIBSPI3 slave chip select pins or GIO pins |
| MIBSPI3CS[1] | V5 | | V5 | | | | | |
| MIBSPI3CS[2] | B2 | | B2 | | | | | |
| MIBSPI3CS[3] | C3 | | C3 | | | 2mA - z | | MIBSPI3 enable pin or GIO pin |
| MIBSPI3EN \bar{A} | W9 | 6 | W9 | 6 | | | | |
| MIBSPI3SIMO | W8 | 4 | W8 | 4 | | 4mA | | MIBSPI3 data stream - Slave in/master out pin or GIO pin |
| MIBSPI3SOMI | V8 | 5 | V8 | 5 | | | | MIBSPI3 data stream - Slave out/master in pin or GIO pin |

Table 2-9. Terminal Functions (continued)

| Name | Terminal | | | | Type | Internal pullup/pulldown | Description | |
|---|---------------|-----|---------------|-----|----------|--------------------------|---|---|
| | TMS570LS20216 | | TMS570LS20206 | | | | | |
| | 337 | 144 | 337 | 144 | | | | |
| Multibuffered Serial Peripheral Interface - Parallel (MIBSPI5) | | | | | | | | |
| MIBSPI5CLK/DMMDATA[4] | H19 | 91 | H19 | 91 | 3.3V I/O | 4mA | MIBSPI5 clock pin or GIO pin; multiplexed with DMMDATA[4] pin | |
| MIBSPI5CS[0]/DMMDATA[5] | E19 | 92 | E19 | 92 | | 2mA - z | | MIBSPI5 slave chip select pins or GIO pins; multiplexed with DMMDATA pins |
| MIBSPI5CS[1]/DMMDATA[6] | B6 | 93 | B6 | 93 | | | | |
| MIBSPI5CS[2]/DMMDATA[2] | W6 | | W6 | | | | | |
| MIBSPI5CS[3]/DMMDATA[3] | T12 | | T12 | | | | | |
| MIBSPI5ENA/DMMDATA[7] | H18 | 94 | H18 | 94 | | | | |
| MIBSPI5SIMO[0]/DMMDATA[8] | J19 | 95 | J19 | 95 | | 4mA | Program mable IPU (20uA) | MIBSPI5 data stream - Slave in/master out pins or GIO pins; multiplexed with DMMDATA pins |
| DMMDATA[9]/MIBSPI5SIMO[1] | E16 | 96 | E16 | 96 | | | | |
| MIBSPI5SIMO[2]/DMMDATA[10] | H17 | 97 | H17 | 97 | | | | |
| MIBSPI5SIMO[3]/DMMDATA[11] | G17 | 98 | G17 | 98 | | | | |
| MIBSPI5SOMI[0]/DMMDATA[12] | J18 | 99 | J18 | 99 | | | | |
| MIBSPI5SOMI[1]/DMMDATA[13] | E17 | 100 | E17 | 100 | | | | |
| MIBSPI5SOMI[2]/DMMDATA[14] | H16 | 101 | H16 | 101 | | | | MIBSPI5 data stream - Slave out/master in pins or GIO pins; multiplexed with DMMDATA pins |
| MIBSPI5SOMI[3]/DMMDATA[15] | G16 | 102 | G16 | 102 | | | | |
| Multibuffered Analog-To-Digital Converter (MIBADC1) | | | | | | | | |
| AD1EVT | N19 | 84 | N19 | 84 | 3.3V I/O | 2 mA - z | Program mable IPD (20uA) | MibADC1 event input pin or GIO pin |
| AD1IN[0] | W14 | 83 | W14 | 83 | 3.3V I | | | MibADC1 analog input pins |
| AD1IN[1] | V17 | 82 | V17 | 82 | | | | |
| AD1IN[2] | V18 | 81 | V18 | 81 | | | | |
| AD1IN[3] | T17 | 80 | T17 | 80 | | | | |
| AD1IN[4] | U18 | 79 | U18 | 79 | | | | |
| AD1IN[5] | R17 | 78 | R17 | 78 | | | | |
| AD1IN[6] | T19 | 77 | T19 | 77 | | | | |
| AD1IN[7] | V14 | 76 | V14 | 76 | | | | |

Table 2-9. Terminal Functions (continued)

| Name | Terminal | | | | Type | Internal pullup/pulldown | Description | |
|--|---------------|-----|---------------|-----|-----------|--------------------------|--------------------------------------|---|
| | TMS570LS20216 | | TMS570LS20206 | | | | | |
| | 337 | 144 | 337 | 144 | | | | |
| Multibuffered Analog-To-Digital Converter (MIBADC2) | | | | | | | | |
| AD2EVT | W13 | 59 | W13 | 59 | 3.3V I/O | 2 mA - z | Program mable I _{PD} (20uA) | MibADC2 event input pin or GIO pin |
| AD2IN[0] | V13 | 60 | V13 | 60 | 3.3 V I | | | MibADC2 analog input pins |
| AD2IN[1] | U13 | 61 | U13 | 61 | | | | |
| AD2IN[2] | U14 | 62 | U14 | 62 | | | | |
| AD2IN[3] | U16 | 63 | U16 | 63 | | | | |
| AD2IN[4] | U15 | | U15 | | | | | |
| AD2IN[5] | T15 | | T15 | | | | | |
| AD2IN[6] | R19 | | R19 | | | | | |
| AD2IN[7] | R16 | | R16 | | | | | |
| Multibuffered Analog-To-Digital Converter - shared signals (MIBADC1, MIBADC2) | | | | | | | | |
| ADSIN[8] | P18 | 75 | P18 | 75 | 3.3 V I | | | MibADC1, MibADC2 shared analog input pins |
| ADSIN[9] | W17 | 74 | W17 | 74 | | | | |
| ADSIN[10] | U17 | 73 | U17 | 73 | | | | |
| ADSIN[11] | U19 | 72 | U19 | 72 | | | | |
| ADSIN[12] | T16 | 71 | T16 | 71 | | | | |
| ADSIN[13] | T18 | 70 | T18 | 70 | | | | |
| ADSIN[14] | R18 | 69 | R18 | 69 | | | | |
| ADSIN[15] | P19 | 68 | P19 | 68 | | | | |
| ADREFHI | V15 | 66 | V15 | 66 | 3.3-V REF | | | MibADC1, MibADC2 module high-voltage reference input |
| ADREFLO | V16 | 65 | V16 | 65 | GND REF | | | MibADC1, MibADC2 module low-voltage reference input |
| VCCAD | W15 | 67 | W15 | 67 | 3.3-V PWR | | | MibADC1, MibADC2 analog supply voltage |
| VSSAD | V19 | 64 | V19 | 64 | GND | | | MibADC1, MibADC2 analog ground reference |
| VSSAD | W16 | | W16 | | | | | |
| VSSAD | W18 | | W18 | | | | | |
| VSSAD | W19 | | W19 | | | | | |
| Oscillator (OSC) | | | | | | | | |
| OSCIN | K1 | 20 | K1 | 20 | 1.5V I | | | Oscillator input connection pin or external clock input pin |
| OSCOU | L1 | 21 | L1 | 21 | 1.5V O | | | Oscillator output connection pin |
| Kelvin_GND | L2 | | L2 | | GND | | | Kelvin_GND for oscillator |

Table 2-9. Terminal Functions (continued)

| Name | Terminal | | | | Type | Internal pullup/pulldown | Description |
|-------------------------------------|---------------|-----|---------------|-----|----------|--------------------------|--|
| | TMS570LS20216 | | TMS570LS20206 | | | | |
| | 337 | 144 | 337 | 144 | | | |
| System Module (SYS) | | | | | | | |
| $\overline{\text{PORRST}}$ | W7 | 28 | W7 | 28 | 3.3V I | | IPD (100 μ A) Power on Reset Pin. External power supply monitor circuitry must assert a power-on reset on this pin. |
| $\overline{\text{RST}}$ | B17 | 85 | B17 | 85 | 3.3V I/O | 4mA | IPU (100 μ A) Active Low Bidirectional Reset pin. An external device can assert a device reset on this pin. The output buffer on this pin is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this pin. |
| ECLK | A12 | 88 | A12 | 88 | | 8mA | IPD (20 μ A) External Clock Prescaler module output pin or GIO pin |
| Tset/Debug (T/D) | | | | | | | |
| TCK | B18 | 30 | B18 | 30 | 3.3V I | | IPD (100 μ A) JTAG test clock pin. Clocks the JTAG debug logic. |
| RTCK | A16 | 35 | A16 | 35 | 3.3V O | | IPD (100 μ A) JTAG return test clock pin. (JTAG) |
| TDI | A17 | 34 | A17 | 34 | 3.3V I/O | 8 mA | IPU (100 μ A) JTAG test data in pin. |
| TDO | C18 | 33 | C18 | 33 | | | IPD (100 μ A) JTAG test data out pin. |
| TMS | C19 | 36 | C19 | 36 | | | IPU (100 μ A) JTAG serial input pin for controlling the state of the CPU test access port (TAP) controller. |
| $\overline{\text{TRST}}$ | D18 | 29 | D18 | 29 | | | IPD (100 μ A) JTAG test hardware reset to TAP. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic |
| TEST | U2 | 58 | U2 | 58 | 3.3V I | | IPD (100 μ A) Test enable pin. Reserved for internal TI use only. For proper operation, this pin must be connected to ground, e.g. using an external resistor. |
| Error Signaling Module (ESM) | | | | | | | |
| $\overline{\text{ERROR}}$ | B14 | 143 | B14 | 143 | 3.3V I/O | 8mA | IPD (20 μ A) Error Signaling pin |
| Flash | | | | | | | |
| FLTP1 | J5 | 122 | J5 | 122 | | | Flash Test Pad 1 pin. For proper operation this pin must connect only to a test pad or not be connected at all [no connect (NC)]. The test pad must not be exposed in the final product where it might be subjected to an ESD event. |
| FLTP2 | H5 | 123 | H5 | 123 | | | Flash Test Pad 2 pin. For proper operation this pin must connect only to a test pad or not be connected at all [no connect (NC)]. The test pad must not be exposed in the final product where it might be subjected to an ESD event. |
| V _{CCP} | F8 | 128 | F8 | 128 | 3.3V PWR | | Flash pump voltage supply (3.3 V). This pin is required for Flash read, program and erase operations. |

Table 2-9. Terminal Functions (continued)

| Name | Terminal | | | | Type | Internal pullup/pulldown | Description | |
|------------------------------------|---------------|-----|---------------|-----|----------|--------------------------|--------------------------|--|
| | TMS570LS20216 | | TMS570LS20206 | | | | | |
| | 337 | 144 | 337 | 144 | | | | |
| RAM Trace Port Module (RTP) | | | | | | | | |
| RTPDATA[0] | V11 | | V11 | | 3.3V I/O | 8mA | Program mable IPU (20uA) | RAM Trace Port Output Data Signal pins or GIO pins |
| RTPDATA[1] | U11 | | U11 | | | | | |
| RTPDATA[2] | T10 | | T10 | | | | | |
| RTPDATA[3] | U10 | | U10 | | | | | |
| RTPDATA[4] | T9 | | T9 | | | | | |
| RTPDATA[5] | U9 | | U9 | | | | | |
| RTPDATA[6] | U8 | | U8 | | | | | |
| RTPDATA[7] | U7 | | U7 | | | | | |
| RTPDATA[8] | U6 | | U6 | | | | | |
| RTPDATA[9] | U5 | | U5 | | | | | |
| RTPDATA[10] | U4 | | U4 | | | | | |
| RTPDATA[11] | T4 | | T4 | | | | | |
| RTPDATA[12] | V3 | | V3 | | | | | |
| RTPDATA[13] | U3 | | U3 | | | | | |
| RTPDATA[14] | T3 | | T3 | | | | | |
| RTPDATA[15] | T2 | | T2 | | | | | |
| $\overline{\text{RTPEN}}_A$ | U12 | | U12 | | | | | |
| RTPSYNC | T11 | | T11 | | | 8mA | | Packet Synchronization Signal pin or GIO pin |
| RTPCLK | W11 | | W11 | | | | | Packet Clock Signal pin or GIO pin |

Table 2-9. Terminal Functions (continued)

| Terminal | | | | Type | Internal pullup/pulldown | Description | |
|---------------------------------------|---------------|-----|---------------|---------|--------------------------|------------------------------------|--|
| Name | TMS570LS20216 | | TMS570LS20206 | | | | |
| | 337 | 144 | 337 | | | | 144 |
| Data Modification Module (DMM) | | | | | | | |
| DMMDATA[0] | L19 | | L19 | | 3.3V I/O | DMM Data pins or GIO pins | |
| DMMDATA[1] | L18 | | L18 | | | | |
| DMMDATA[2]/MIBSPI5CS[2] | W6 | | W6 | 2mA - z | | Program mable IPU (20uA) | DMM Data pins or GIO pins; multiplexed with MIBSPI5 pins |
| DMMDATA[3]/MIBSPI5CS[3] | T12 | | T12 | | | | |
| DMMDATA[4]/MIBSPI5CLK | H19 | | H19 | 4mA | | | |
| DMMDATA[5]/MIBSPI5CS[0] | E19 | | E19 | | | | |
| DMMDATA[6]/MIBSPI5CS[1] | B6 | | B6 | 2mA - z | | | |
| DMMDATA[7]/MIBSPI5ENA | H18 | | H18 | | | | |
| DMMDATA[8]/MIBSPI5SIMO[0] | J19 | | J19 | | | | |
| DMMDATA[9]/MIBSPI5SIMO[1] | E16 | | E16 | | | | |
| DMMDATA[10]/MIBSPI5SIMO[2] | H17 | | H17 | | | | |
| DMMDATA[11]/MIBSPI5SIMO[3] | G17 | | G17 | 4mA | | | |
| DMMDATA[12]/MIBSPI5SOMI[0] | J18 | | J18 | | | | |
| DMMDATA[13]/MIBSPI5SOMI[1] | E17 | | E17 | | | | |
| DMMDATA[14]/MIBSPI5SOMI[2] | H16 | | H16 | | | | |
| DMMDATA[15]/MIBSPI5SOMI[3] | G16 | | G16 | | | | |
| DMMENA | F16 | | F16 | 8mA | | DMM Handshake pin or GIO pin | |
| DMMSYNC | J16 | | J16 | | | DMM Synchronization pin or GIO pin | |
| DMMCLK | F17 | | F17 | 2mA - z | | DMM Clock input pin or GIO pin | |

Table 2-9. Terminal Functions (continued)

| Name | Terminal | | | | Type | Internal pullup/pulldown | Description |
|--|---------------|-----|---------------|-----|----------|--------------------------|--|
| | TMS570LS20216 | | TMS570LS20206 | | | | |
| | 337 | 144 | 337 | 144 | | | |
| External Memory Interface Module (EMIF) | | | | | | | |
| EMIFBADD[0] | D13 | | D13 | | 3.3V I/O | 8mA | EMIF Byte Address pins |
| EMIFBADD[1] | D16 | | D16 | | | | |
| EMIFDATA[0] | K16 | | K16 | | 3.3V I/O | 8mA | Program mable IPU (20uA) EMIF Data pins |
| EMIFDATA[1] | L16 | | L16 | | | | |
| EMIFDATA[2] | M16 | | M16 | | | | |
| EMIFDATA[3] | N16 | | N16 | | | | |
| EMIFDATA[4] | E4 | | E4 | | | | |
| EMIFDATA[5] | F4 | | F4 | | | | |
| EMIFDATA[6] | G4 | | G4 | | | | |
| EMIFDATA[7] | K4 | | K4 | | | | |
| EMIFDATA[8] | L4 | | L4 | | | | |
| EMIFDATA[9] | M4 | | M4 | | | | |
| EMIFDATA[10] | N4 | | N4 | | | | |
| EMIFDATA[11] | P4 | | P4 | | | | |
| EMIFDATA[12] | T5 | | T5 | | | | |
| EMIFDATA[13] | T6 | | T6 | | | | |
| EMIFDATA[14] | T7 | | T7 | | | | |
| EMIFDATA[15] | T8 | | T8 | | | | |
| EMIFADD[0] | D4 | | D4 | | 3.3V I/O | 8mA | EMIF Address pins |
| EMIFADD[1] | D5 | | D5 | | | | |
| EMIFADD[2] | D6 | | D6 | | | | |
| EMIFADD[3] | D7 | | D7 | | | | |
| EMIFADD[4] | D8 | | D8 | | | | |
| EMIFADD[5] | D9 | | D9 | | | | |
| EMIFADD[6] | C4 | | C4 | | | | |
| EMIFADD[7] | C5 | | C5 | | | | |
| EMIFADD[8] | C6 | | C6 | | | | |
| EMIFADD[9] | C7 | | C7 | | | | |
| EMIFADD[10] | C8 | | C8 | | | | |
| EMIFADD[11] | C9 | | C9 | | | | |
| EMIFADD[12] | C10 | | C10 | | | | |
| EMIFADD[13] | C11 | | C11 | | | | |
| EMIFADD[14] | C12 | | C12 | | | | |
| EMIFADD[15] | C13 | | C13 | | | | |
| EMIFADD[16] | D14 | | D14 | | | | |
| EMIFADD[17] | C14 | | C14 | | | | |
| EMIFADD[18] | D15 | | D15 | | | | |
| EMIFADD[19] | C15 | | C15 | | | | |
| EMIFADD[20] | C16 | | C16 | | | | |
| EMIFADD[21] | C17 | | C17 | | | | |
| EMIFCS[0] | L17 | | L17 | | 3.3V I/O | 8mA | EMIF Chip Select pins |
| EMIFCS[1] | K17 | | K17 | | | | |
| EMIFCS[2] | M17 | | M17 | | | | |
| EMIFCS[3] | N17 | | N17 | | | | |

Table 2-9. Terminal Functions (continued)

| Name | Terminal | | | | Type | | Internal pullup/pulldown | Description |
|------------|---------------|-----|---------------|-----|----------|-----|--------------------------|-------------|
| | TMS570LS20216 | | TMS570LS20206 | | | | | |
| | 337 | 144 | 337 | 144 | | | | |
| EMIFWE | D17 | | D17 | | 3.3V I/O | 8mA | EMIF Write Enable pin | |
| EMIFOE | D12 | | D12 | | 3.3V I/O | 8mA | EMIF Output Enable pin | |
| EMIFDQM[0] | D10 | | D10 | | 3.3V I/O | 8mA | EMIF Byte Enable pins | |
| EMIFDQM[1] | D11 | | D11 | | | | | |

Table 2-9. Terminal Functions (continued)

| Name | Terminal | | | | Type | Internal pullup/pulldown | Description |
|------------------------------------|---------------|-----|---------------|-----|--------|--------------------------|-----------------------------------|
| | TMS570LS20216 | | TMS570LS20206 | | | | |
| | 337 | 144 | 337 | 144 | | | |
| Embedded Trace Module (ETM) | | | | | | | |
| ETMDATA[0] | R12 | | R12 | | 3.3V O | 8mA | ETM Trace Data output pins |
| ETMDATA[1] | R13 | | R13 | | | | |
| ETMDATA[2] | J15 | | J15 | | | | |
| ETMDATA[3] | H15 | | H15 | | | | |
| ETMDATA[4] | G15 | | G15 | | | | |
| ETMDATA[5] | F15 | | F15 | | | | |
| ETMDATA[6] | E15 | | E15 | | | | |
| ETMDATA[7] | E14 | | E14 | | | | |
| ETMDATA[8] | E9 | | E9 | | | | |
| ETMDATA[9] | E8 | | E8 | | | | |
| ETMDATA[10] | E7 | | E7 | | | | |
| ETMDATA[11] | E6 | | E6 | | | | |
| ETMDATA[12] | E13 | | E13 | | | | |
| ETMDATA[13] | E12 | | E12 | | | | |
| ETMDATA[14] | E11 | | E11 | | | | |
| ETMDATA[15] | E10 | | E10 | | | | |
| ETMDATA[16] | K15 | | K15 | | | | |
| ETMDATA[17] | L15 | | L15 | | | | |
| ETMDATA[18] | M15 | | M15 | | | | |
| ETMDATA[19] | N15 | | N15 | | | | |
| ETMDATA[20] | E5 | | E5 | | | | |
| ETMDATA[21] | F5 | | F5 | | | | |
| ETMDATA[22] | G5 | | G5 | | | | |
| ETMDATA[23] | K5 | | K5 | | | | |
| ETMDATA[24] | L5 | | L5 | | | | |
| ETMDATA[25] | M5 | | M5 | | | | |
| ETMDATA[26] | N5 | | N5 | | | | |
| ETMDATA[27] | P5 | | P5 | | | | |
| ETMDATA[28] | R5 | | R5 | | | | |
| ETMDATA[29] | R6 | | R6 | | | | |
| ETMDATA[30] | R7 | | R7 | | | | |
| ETMDATA[31] | R8 | | R8 | | | | |
| ETMTRACECTL | R11 | | R11 | | | | ETM Control pin |
| ETMTRACECLKOUT | R10 | | R10 | | 3.3V O | 8mA | ETM Clock output pin |
| ETMTRACECLKIN | R9 | | R9 | | 3.3V I | | IPU (20uA) ETM Clock input pin |

Table 2-9. Terminal Functions (continued)

| Name | Terminal | | | | Type | Internal pullup/pulldown | Description | | | |
|--|---------------|-----|---------------|-----|-------------|--------------------------|---|--|--|--|
| | TMS570LS20216 | | TMS570LS20206 | | | | | | | |
| | 337 | 144 | 337 | 144 | | | | | | |
| Supply Voltage Digital I/O (3.3V) and Core (1.5V) | | | | | | | | | | |
| V _{CCIO} | F6 | 1 | F6 | 1 | 3.3V PWR | | Digital I/O supply pins Note: All V _{CCIO} pads are connected to the BGA packages through the package substrate. There is not a direct ball to bond pad connection for this supply. | | | |
| V _{CCIO} | F7 | 15 | F7 | 15 | | | | | | |
| V _{CCIO} | F11 | 40 | F11 | 40 | | | | | | |
| V _{CCIO} | F12 | 90 | F12 | 90 | | | | | | |
| V _{CCIO} | F13 | 108 | F13 | 108 | | | | | | |
| V _{CCIO} | F14 | 119 | F14 | 119 | | | | | | |
| V _{CCIO} | G6 | 132 | G6 | 132 | | | | | | |
| V _{CCIO} | G14 | | G14 | | | | | | | |
| V _{CCIO} | H6 | | H6 | | | | | | | |
| V _{CCIO} | H14 | | H14 | | | | | | | |
| V _{CCIO} | J6 | | J6 | | | | | | | |
| V _{CCIO} | L14 | | L14 | | | | | | | |
| V _{CCIO} | M6 | | M6 | | | | | | | |
| V _{CCIO} | M14 | | M14 | | | | | | | |
| V _{CCIO} | N6 | | N6 | | | | | | | |
| V _{CCIO} | N14 | | N14 | | | | | | | |
| V _{CCIO} | P6 | | P6 | | | | | | | |
| V _{CCIO} | P7 | | P7 | | | | | | | |
| V _{CCIO} | P8 | | P8 | | | | | | | |
| V _{CCIO} | P9 | | P9 | | | | | | | |
| V _{CCIO} | P12 | | P12 | | | | | | | |
| V _{CCIO} | P13 | | P13 | | | | | | | |
| V _{CCIO} | P14 | | P14 | | | | | | | |
| V _{CCIO} | | | | | | | | | | |
| V _{CC} | F9 | 19 | F9 | 19 | 1.5V PWR | | Digital Core supply pins Note: All V _{CC} pads are connected to the BGA packages through the package substrate. There is not a direct ball to bond pad connection for this supply. | | | |
| V _{CC} | F10 | 31 | F10 | 31 | | | | | | |
| V _{CC} | H10 | 37 | H10 | 37 | | | | | | |
| V _{CC} | J14 | 47 | J14 | 47 | | | | | | |
| V _{CC} | K6 | 87 | K6 | 87 | | | | | | |
| V _{CC} | K8 | 104 | K8 | 104 | | | | | | |
| V _{CC} | K12 | 114 | K12 | 114 | | | | | | |
| V _{CC} | K14 | 135 | K14 | 135 | | | | | | |
| V _{CC} | L6 | | L6 | | | | | | | |
| V _{CC} | M10 | | M10 | | | | | | | |
| V _{CC} | P10 | | P10 | | | | | | | |
| V _{CC} | P11 | | P11 | | | | | | | |
| V _{CC} | | | | | | | | | | |
| V _{CC} | | | | | | | | | | |

Table 2-9. Terminal Functions (continued)

| Name | Terminal | | | | Type | Internal pullup/pulldown | Description |
|----------------------|---------------|-----|---------------|-----|------|--------------------------|---|
| | TMS570LS20216 | | TMS570LS20206 | | | | |
| | 337 | 144 | 337 | 144 | | | |
| Supply Ground | | | | | | | |
| V _{SS} | A1 | 2 | A1 | 2 | GND | | Digital supply ground reference pins Note: All V _{SS} pads are connected to the BGA packages through the package substrate. |
| V _{SS} | A2 | 16 | A2 | 16 | | | |
| V _{SS} | A18 | 22 | A18 | 22 | | | |
| V _{SS} | A19 | 32 | A19 | 32 | | | |
| V _{SS} | B1 | 38 | B1 | 38 | | | |
| V _{SS} | B19 | 39 | B19 | 39 | | | |
| V _{SS} | H8 | 46 | H8 | 46 | | | |
| V _{SS} | H9 | 86 | H9 | 86 | | | |
| V _{SS} | H11 | 89 | H11 | 89 | | | |
| V _{SS} | H12 | 103 | H12 | 103 | | | |
| V _{SS} | J8 | 107 | J8 | 107 | | | |
| V _{SS} | J9 | 115 | J9 | 115 | | | |
| V _{SS} | J10 | 120 | J10 | 120 | | | |
| V _{SS} | J11 | 127 | J11 | 127 | | | |
| V _{SS} | J12 | 133 | J12 | 133 | | | |
| V _{SS} | K9 | 136 | K9 | 136 | | | |
| V _{SS} | K10 | | K10 | | | | |
| V _{SS} | K11 | | K11 | | | | |
| V _{SS} | L8 | | L8 | | | | |
| V _{SS} | L9 | | L9 | | | | |
| V _{SS} | L10 | | L10 | | | | |
| V _{SS} | L11 | | L11 | | | | |
| V _{SS} | L12 | | L12 | | | | |
| V _{SS} | M8 | | M8 | | | | |
| V _{SS} | M9 | | M9 | | | | |
| V _{SS} | M11 | | M11 | | | | |
| V _{SS} | M12 | | M12 | | | | |
| V _{SS} | V1 | | V1 | | | | |
| V _{SS} | W1 | | W1 | | | | |
| V _{SS} | W2 | | W2 | | | | |
| V _{SS} | V4 | | V4 | | | | |
| V _{SS} | | | | | | | |
| V _{SS} | | | | | | | |
| V _{SS} | | | | | | | |
| V _{SS} | | | | | | | |
| V _{SS} | | | | | | | |

2.6 Device Support

2.6.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all devices and support tools. Each commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., TMS570LS20216ASGWTMEP). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

| | |
|------------|---|
| TMX | Experimental device that is not necessarily representative of the final device's electrical specifications. |
| TMP | Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification. |
| TMS | Fully-qualified production device. |

Support tool development evolutionary flow:

| | |
|-------------|--|
| TMDX | Development-support product that has not yet completed Texas Instruments internal qualification testing. |
| TMDS | Fully qualified development-support product. |

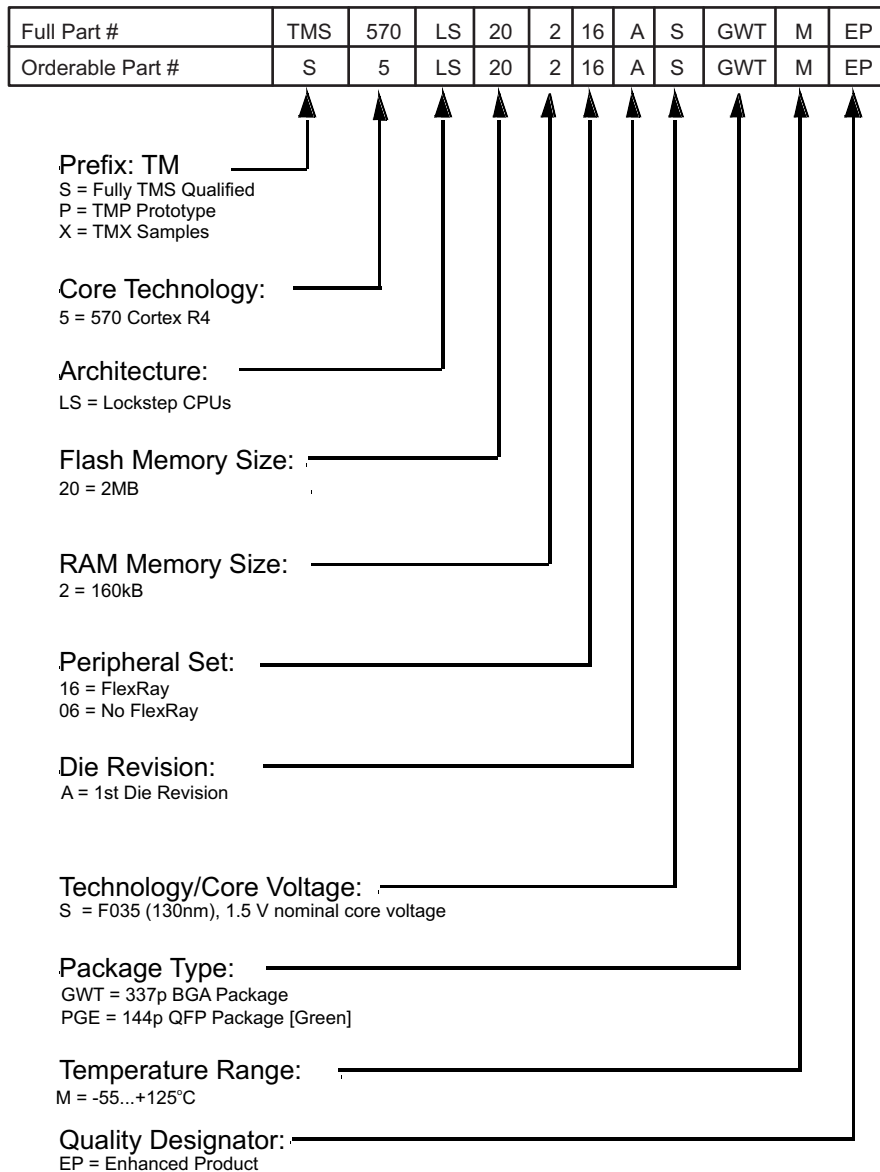
TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, GWT), the temperature range (for example, "Blank" is the commercial temperature range), and the device speed range in Mega Hertz.



A. For actual device part numbers (P/Ns) and ordering information, see the TI website (<http://www.ti.com>).

Figure 2-7. Device Numbering Conventions^(A)

3 Reset / Abort Sources

3.1 Reset / Abort Sources

The device Resets and Aborts are handled as shown in the following table. The table shows the source of the error, the system mode, the type of error response and the corresponding Error Signaling Module (ESM) channel. Only standard ARM exception handlers and ESM errors are used.

Table 3-1. Reset / Abort Sources

| Error Source | System Mode | Error Response | ESM Hookup group channel |
|--|----------------|---|--------------------------|
| 1) CPU transactions | | | |
| Precise write error (Strongly Ordered) | User/Privilege | Precise Abort (CPU) | n/a |
| Precise read error (Device or Normal) | User/Privilege | Precise Abort (CPU) | n/a |
| Imprecise write error (Device or Normal) | User/Privilege | Imprecise Abort (CPU) | n/a |
| Illegal instruction | User/Privilege | Undefined Instruction Trap (CPU) ⁽¹⁾ | n/a |
| MPU access violation | User/Privilege | Abort (CPU) | n/a |
| 2) SRAM | | | |
| B0 Tightly Coupled Memory (TCM) (even) ECC single error (correctable) | User/Privilege | ESM | 1.26 |
| B0 TCM (even) ECC double error (non-correctable) | User/Privilege | Abort (CPU), ESM => nERROR | 3.3 |
| B0 TCM (even) uncorrectable error (i.e. redundant address decode) | User/Privilege | ESM => NMI | 2.6 |
| B0 TCM (even) address bus parity error | User/Privilege | ESM => NMI | 2.10 |
| B1 TCM (odd) ECC single error (correctable) | User/Privilege | ESM | 1.28 |
| B1 TCM (odd) ECC double error (non-correctable) | User/Privilege | Abort (CPU), ESM => nERROR | 3.5 |
| B1 TCM (odd) uncorrectable error (i.e. redundant address decode) | User/Privilege | ESM => NMI | 2.8 |
| B1 TCM (odd) address bus parity error | User/Privilege | ESM => NMI | 2.12 |
| 3) Flash with ECC INTEGRATED INTO CPU | | | |
| ECC single error (correctable) | User/Privilege | ESM | 1.6 |
| ECC double error (non-correctable) | User/Privilege | Abort (CPU), ESM => nERROR | 3.7 |
| Uncorrectable error (i.e. redundant address tag, redundant syndrome compare, address bus parity, etc.) | User/Privilege | ESM => NMI | 2.4 |
| 4) DMA transactions | | | |
| External imprecise error on read (Illegal transaction with ok response) | User/Privilege | ESM | 1.5 |
| External imprecise error on write (Illegal transaction with ok response) | User/Privilege | ESM | 1.13 |

(1) The Undefined Instruction TRAP is NOT detectable outside the CPU. The trap is taken only if the Code reaches the execute stage of the CPU.

Table 3-1. Reset / Abort Sources (continued)

| Error Source | System Mode | Error Response | ESM Hookup group channel |
|--|----------------|------------------|--------------------------|
| Memory access permission violation | User/Privilege | ESM | 1.2 |
| Memory parity error | User/Privilege | ESM | 1.3 |
| 5) DMM transactions | | | |
| External imprecise error on read (Illegal transaction with ok response) | User/Privilege | ESM | 1.5 |
| External imprecise error on write (Illegal transaction with ok response) | User/Privilege | ESM | 1.13 |
| 6) AHB-AP transactions | | | |
| External imprecise error on read (Illegal transaction with ok response) | User/Privilege | ESM | 1.5 |
| External imprecise error on write (Illegal transaction with ok response) | User/Privilege | ESM | 1.13 |
| 7) HET TU | | | |
| NCNB (Strongly Ordered) transaction with slave error response | User/Privilege | Interrupt => VIM | n/a |
| External imprecise error (Illegal transaction with ok response) | User/Privilege | Interrupt => VIM | n/a |
| Memory access permission violation | User/Privilege | ESM | 1.9 |
| Memory parity error | User/Privilege | ESM | 1.8 |
| 8) NHET | | | |
| Memory parity error | User/Privilege | ESM | 1.7 |
| 9) MibSPI | | | |
| MibSPI1 memory parity error | User/Privilege | ESM | 1.17 |
| MibSPI3 memory parity error | User/Privilege | ESM | 1.18 |
| MibSPIP5 memory parity error | User/Privilege | ESM | 1.24 |
| 10) MibADC | | | |
| MibADC1 memory parity error | User/Privilege | ESM | 1.19 |
| MibADC2 memory parity error | User/Privilege | ESM | 1.1 |
| 11) DCAN | | | |
| DCAN1 memory parity error | User/Privilege | ESM | 1.21 |
| DCAN2 memory parity error | User/Privilege | ESM | 1.23 |
| DCAN3 memory parity error | User/Privilege | ESM | 1.22 |
| 12) PLL | | | |
| PLL slip error | User/Privilege | ESM | 1.10 |
| 13) Clock monitor | | | |
| Clock monitor interrupt | User/Privilege | ESM | 1.11 |
| 14) CCM | | | |
| Self test failure | User/Privilege | ESM | 1.31 |
| Compare failure | User/Privilege | ESM => NMI | 2.2 |
| 15) FlexRay | | | |
| Memory parity error | User/Privilege | ESM | 1.12 |
| 16) FlexRay TU | | | |
| NCNB (Strongly Ordered) transaction with slave error response | User/Privilege | Interrupt => VIM | n/a |

Table 3-1. Reset / Abort Sources (continued)

| Error Source | System Mode | Error Response | ESM Hookup group channel |
|---|----------------|------------------|--------------------------|
| External imprecise error (Illegal transaction with ok response) | User/Privilege | Interrupt => VIM | n/a |
| Memory access permission violation | User/Privilege | ESM | 1.16 |
| Memory parity error | User/Privilege | ESM | 1.14 |
| 17) VIM | | | |
| Memory parity error | User/Privilege | ESM | 1.15 |
| 18) voltage monitor | | | |
| VMON out of voltage range | n/a | Reset | n/a |
| 19) CPU Selftest (LBIST) | | | |
| CPU Selftest (LBIST) error | User/Privilege | ESM | 1.27 |
| 20) errors reflected in the SYSESR register | | | |
| Power-Up Reset; VCC out of voltage range | n/a | Reset | n/a |
| Oscillator fail / PLL slip ⁽²⁾ | n/a | Reset | n/a |
| Watchdog time limit exceeded | n/a | Reset | n/a |
| CPU Reset | n/a | Reset | n/a |
| Software Reset | n/a | Reset | n/a |
| External Reset | n/a | Reset | n/a |

(2) Oscillator fail/PLL slip can be configured in the system register PLLCTL1 to generate a reset.

4 Peripherals

4.1 Error Signaling Module (ESM)

The Error Signaling Module (ESM) is used to indicate a severe device failure via interrupts and the external $\overline{\text{ERROR}}$ pin. The error pin is normally used by an external device to either reset the controller and/or keep the system in a fail safe state.

The ESM module consists of three error groups with 32 inputs each. The generation of the interrupts and the activation of the $\overline{\text{ERROR}}$ Pin is shown in the following table. The next table shows the ESM error sources and their corresponding group and channel numbers.

Table 4-1. ESM Groups

| Error Group | Interrupt, Level | Influence on $\overline{\text{ERROR}}$ pin |
|-------------|--------------------|--|
| Group1 | maskable, low/high | configurable |
| Group2 | non-maskable, high | fixed |
| Group3 | none, none | fixed |

Table 4-2. ESM Assignments

| ERROR Sources | Group | Channels |
|---|--------|----------|
| Reserved | Group1 | 0 |
| MibADC2 - parity | Group1 | 1 |
| DMA - MPU | Group1 | 2 |
| DMA - parity | Group1 | 3 |
| Reserved | Group1 | 4 |
| DMA/DMM/AHB-AP - imprecise read error | Group1 | 5 |
| Flash (ATCM) - correctable error | Group1 | 6 |
| NHET - parity | Group1 | 7 |
| HET TU - parity | Group1 | 8 |
| HET TU - MPU | Group1 | 9 |
| PLL - slip | Group1 | 10 |
| Clock Monitor - interrupt | Group1 | 11 |
| FlexRay - parity | Group1 | 12 |
| DMA/DMM/AHB-AP - imprecise write error | Group1 | 13 |
| FlexRay TU - parity | Group1 | 14 |
| VIM RAM - parity | Group1 | 15 |
| FlexRay TU - MPU | Group1 | 16 |
| MibSPI1 - parity | Group1 | 17 |
| MibSPI3 - parity | Group1 | 18 |
| MibADC1 - parity | Group1 | 19 |
| Reserved | Group1 | 20 |
| DCAN1 - parity | Group1 | 21 |
| DCAN3 - parity | Group1 | 22 |
| DCAN2 - parity | Group1 | 23 |
| MibSPI5 - parity | Group1 | 24 |
| Reserved | Group1 | 25 |
| RAM even bank (B0TCM) - correctable error | Group1 | 26 |
| CPU - selftest | Group1 | 27 |
| RAM odd bank (B1TCM) - correctable error | Group1 | 28 |
| Reserved | Group1 | 29 |
| Reserved | Group1 | 30 |

Table 4-2. ESM Assignments (continued)

| ERROR Sources | Group | Channels |
|--|--------------|-----------------|
| CCM-R4 - selftest | Group1 | 31 |
| Reserved | Group2 | 0 |
| Reserved | Group2 | 1 |
| CCM-R4 - compare | Group2 | 2 |
| Reserved | Group2 | 3 |
| Flash (ATCM) - uncorrectable error | Group2 | 4 |
| Reserved | Group2 | 5 |
| RAM even bank (B0TCM) - uncorrectable error | Group2 | 6 |
| Reserved | Group2 | 7 |
| RAM odd bank (B1TCM) - uncorrectable error | Group2 | 8 |
| Reserved | Group2 | 9 |
| RAM even bank (B0TCM) - address bus parity error | Group2 | 10 |
| Reserved | Group2 | 11 |
| RAM odd bank (B1TCM) - address bus parity error | Group2 | 12 |
| Reserved | Group2 | 13 |
| Reserved | Group2 | 14 |
| Reserved | Group2 | 15 |
| Flash (ATCM) - ECC live lock detect | Group2 | 16 |
| Reserved | Group2 | 17 |
| Reserved | Group2 | 18 |
| Reserved | Group2 | 19 |
| Reserved | Group2 | 20 |
| Reserved | Group2 | 21 |
| Reserved | Group2 | 22 |
| Reserved | Group2 | 23 |
| Reserved | Group2 | 24 |
| Reserved | Group2 | 25 |
| Reserved | Group2 | 26 |
| Reserved | Group2 | 27 |
| Reserved | Group2 | 28 |
| Reserved | Group2 | 29 |
| Reserved | Group2 | 30 |
| Reserved | Group2 | 31 |
| Reserved | Group3 | 0 |
| Reserved | Group3 | 1 |
| Reserved | Group3 | 2 |
| RAM even bank (B0TCM) - ECC uncorrectable error | Group3 | 3 |
| Reserved | Group3 | 4 |
| RAM odd bank (B1TCM) - ECC uncorrectable error | Group3 | 5 |
| Reserved | Group3 | 6 |
| Flash (ATCM) - ECC uncorrectable error | Group3 | 7 |
| Reserved | Group3 | 8 |
| Reserved | Group3 | 9 |
| Reserved | Group3 | 10 |
| Reserved | Group3 | 11 |
| Reserved | Group3 | 12 |
| Reserved | Group3 | 13 |

Table 4-2. ESM Assignments (continued)

| ERROR Sources | Group | Channels |
|----------------------|--------------|-----------------|
| Reserved | Group3 | 14 |
| Reserved | Group3 | 15 |
| Reserved | Group3 | 16 |
| Reserved | Group3 | 17 |
| Reserved | Group3 | 18 |
| Reserved | Group3 | 19 |
| Reserved | Group3 | 20 |
| Reserved | Group3 | 21 |
| Reserved | Group3 | 22 |
| Reserved | Group3 | 23 |
| Reserved | Group3 | 24 |
| Reserved | Group3 | 25 |
| Reserved | Group3 | 26 |
| Reserved | Group3 | 27 |
| Reserved | Group3 | 28 |
| Reserved | Group3 | 29 |
| Reserved | Group3 | 30 |
| Reserved | Group3 | 31 |

4.2 Direct Memory Access (DMA)

The direct-memory access (DMA) controller transfers data to and from any specified location in the device memory map. The DMA supports data transfer for both on-chip memories and peripherals.

The DMA controller on this device supports 16 channels and 32 request lines. Each of the 32 DMA requests are assigned by default to one of the 16 available channels. For DMA requests multiplexed between multiple sources, the DMA controller cannot differentiate between the multiple sources and the user has to ensure that multiple sources are not enabled at the same time. Please refer to the DMA Specification in the TRM for more details.

The DMA request configuration is shown in the following table.

Table 4-3. DMA Request Line Connection

| Modules | DMA Request Sources | DMA Request |
|-------------------------------------|--|-------------|
| MIBSPI1 | MIBSPI1[1] ⁽¹⁾ | DMAREQ[0] |
| MIBSPI1 | MIBSPI1[0] ⁽²⁾ | DMAREQ[1] |
| Reserved | Reserved | DMAREQ[2] |
| Reserved | Reserved | DMAREQ[3] |
| MIBSPI1 / MIBSPI3 / DCAN2 | MIBSPI1[2] / MIBSPI3[2] / DCAN2 IF3 | DMAREQ[4] |
| MIBSPI1 / MIBSPI3 / DCAN2 | MIBSPI1[3] / MIBSPI3[3] / DCAN2 IF2 | DMAREQ[5] |
| MIBSPI5 / DCAN1 | MIBSPI5[2] / DCAN1 IF2 | DMAREQ[6] |
| MIBADC1 / MIBSPI5 | MIBADC1 event / MIBSPI5[3] | DMAREQ[7] |
| MIBSPI1 / MIBSPI3 / DCAN1 | MIBSPI1[4] / MIBSPI3[4] / DCAN1 IF1 | DMAREQ[8] |
| MIBSPI1 / MIBSPI3 / DCAN2 | MIBSPI1[5] / MIBSPI3[5] / DCAN2 IF1 | DMAREQ[9] |
| MIBADC1 / MIBSPI5 | MIBADC1 G1 / MIBSPI5[4] | DMAREQ[10] |
| MIBADC1 / MIBSPI5 | MIBADC1 G2 / MIBSPI5[5] | DMAREQ[11] |
| RTI / MIBSPI1 / MIBSPI3 | RTI DMAREQ0 / MIBSPI1[6] / MIBSPI3[6] | DMAREQ[12] |
| RTI / MIBSPI1 / MIBSPI3 | RTI DMAREQ1 / MIBSPI1[7] / MIBSPI3[7] | DMAREQ[13] |
| MIBADC2 / MIBSPI3 / MIBSPI5 | MIBADC2 event / MIBSPI3[1] ⁽¹⁾ / MIBSPI5[6] | DMAREQ[14] |
| MIBSPI3 / MIBSPI5 | MIBSPI3[0]† / MIBSPI5[7] | DMAREQ[15] |
| MIBADC2 / MIBSPI1 / MIBSPI3 / DCAN1 | MIBADC2 G1 / MIBSPI1[8] / MIBSPI3[8] / DCAN1 IF3 | DMAREQ[16] |
| MIBADC2 / MIBSPI1 / MIBSPI3 / DCAN3 | MIBADC2 G2 / MIBSPI1[9] / MIBSPI3[9] / DCAN3 IF1 | DMAREQ[17] |
| RTI / MIBSPI5 | RTI DMAREQ2 / MIBSPI5[8] | DMAREQ[18] |
| RTI / MIBSPI5 | RTI DMAREQ3 / MIBSPI5[9] | DMAREQ[19] |
| LIN2 / NHET / DCAN3 | LIN2 receive / NHET DMAREQ[4] / DCAN3 IF2 | DMAREQ[20] |
| LIN2 / NHET / DCAN3 | LIN2 transmit / NHET DMAREQ[5] / DCAN3 IF3 | DMAREQ[21] |
| MIBSPI1 / MIBSPI3 / MIBSPI5 | MIBSPI1[10] / MIBSPI3[10] / MIBSPI5[10] | DMAREQ[22] |
| MIBSPI1 / MIBSPI3 / MIBSPI5 | MIBSPI1[11] / MIBSPI3[11] / MIBSPI5[11] | DMAREQ[23] |
| NHET / MIBSPI5 | NHET DMAREQ[6] / MIBSPI5[12] | DMAREQ[24] |
| NHET / MIBSPI5 | NHET DMAREQ[7] / MIBSPI5[13] | DMAREQ[25] |
| CRC / MIBSPI1 / MIBSPI3 | CRC DMAREQ[0] / MIBSPI1[12] / MIBSPI3[12] | DMAREQ[26] |
| CRC / MIBSPI1 / MIBSPI3 | CRC DMAREQ[1] / MIBSPI1[13] / MIBSPI3[13] | DMAREQ[27] |
| LIN1 / MIBSPI5 | LIN1 receive / MIBSPI5[14] | DMAREQ[28] |
| LIN1 / MIBSPI5 | LIN1 transmit / MIBSPI5[15] | DMAREQ[29] |
| MIBSPI1 / MIBSPI3 / MIBSPI5 | MIBSPI1[14] / MIBSPI3[14] / MIBSPI5[1] ⁽¹⁾ | DMAREQ[30] |
| MIBSPI1 / MIBSPI3 / MIBSPI5 | MIBSPI1[15] / MIBSPI3[15] / MIBSPI5[0] ⁽²⁾ | DMAREQ[31] |

(1) SPI1, SPI3, SPI5 receive in standard SPI/compatibility mode

(2) SPI1, SPI3, SPI5 transmit in standard SPI/compatibility mode

4.3 High End Timer Transfer Unit (HET-TU)

The High End Timer Transfer Unit (HET-TU) is a local Direct Memory Access (DMA) module. It is specifically designed to transfer High End Timer (NHET) data to (or from) the CPU data SRAM. The HET software controls which HET instructions generate transfer requests to the transfer unit. More information about the NHET and the HET-TU can be found in the technical reference manual (TRM). The HET-TU supports 8 channels.

The HET-TU request assignment is shown in the following table.

Table 4-4. NHET Request Line Connection

| Modules | Request Source | HET TRANSFER UNIT Request |
|---------|----------------|---------------------------|
| NHET | HTUREQ[0] | HET TU DCP[0] |
| NHET | HTUREQ[1] | HET TU DCP[1] |
| NHET | HTUREQ[2] | HET TU DCP[2] |
| NHET | HTUREQ[3] | HET TU DCP[3] |
| NHET | HTUREQ[4] | HET TU DCP[4] |
| NHET | HTUREQ[5] | HET TU DCP[5] |
| NHET | HTUREQ[6] | HET TU DCP[6] |
| NHET | HTUREQ[7] | HET TU DCP[7] |

4.4 Vectored Interrupt Manager (VIM)

The Vectored Interrupt Manager (VIM) provides hardware assistance for prioritizing and controlling the many interrupt sources present on the device. Interrupt requests originating from the device modules (i.e., SPI, LIN, SCI, etc.) are assigned to channels within the 64-channel VIM. Programming multiple interrupt sources to the same VIM channel effectively shares the VIM channel between sources. The VIM request channels are maskable so that individual channels can be selectively disabled. All interrupt requests can be programmed in the VIM to be of either type:

- Fast interrupt request (FIQ)- The FIQ implemented in Cortex-R4F is Non-Maskable Fast Interrupts (NMFI).
- Normal interrupt request (IRQ)

The VIM prioritizes interrupts, whose precedence of request channels decrease with ascending channel order in the VIM (0 [highest] and 64[lowest] priority). For VIM default mapping, channel priorities, and their associated modules see the table below. More information on the VIM can be found in the technical reference manual (TRM).

Table 4-5. Interrupt Request Assignments

| Modules | Interrupt Sources | Default VIM Interrupt Request |
|------------------|--------------------------------|-------------------------------|
| ESM | ESM High level interrupt (NMI) | 0 |
| Reserved | (NMI) | 1 |
| RTI | RTI compare interrupt 0 | 2 |
| RTI | RTI compare interrupt 1 | 3 |
| RTI | RTI compare interrupt 2 | 4 |
| RTI | RTI compare interrupt 3 | 5 |
| RTI | RTI overflow interrupt 0 | 6 |
| RTI | RTI overflow interrupt 1 | 7 |
| RTI | RTI timebase | 8 |
| GIO | GIO interrupt A | 9 |
| NHET | NHET level 1 interrupt | 10 |
| HET TU | HET TU level 1 interrupt | 11 |
| MIBSPI1 | MIBSPI1 level 0 interrupt | 12 |
| LIN1 (incl. SCI) | LIN1 level 0 interrupt | 13 |
| MIBADC1 | MIBADC1 event group interrupt | 14 |
| MIBADC1 | MIBADC1 sw group 1 interrupt | 15 |
| DCAN1 | DCAN1 level 0 interrupt | 16 |
| Reserved | Reserved | 17 |
| FlexRay | FlexRay level 0 interrupt | 18 |
| CRC | CRC Interrupt | 19 |
| ESM | ESM Low level interrupt | 20 |
| SYSTEM | Software interrupt (SSI) | 21 |
| CPU | PMU Interrupt | 22 |
| GIO | GIO interrupt B | 23 |
| NHET | NHET level 2 interrupt | 24 |
| HET TU | HET TU level 2 interrupt | 25 |
| MIBSPI1 | MIBSPI1 level 1 interrupt | 26 |
| LIN1 (incl. SCI) | LIN1 level 1 interrupt | 27 |
| MIBADC1 | MIBADC1 sw group 2 interrupt | 28 |
| DCAN1 | DCAN1 level 1 interrupt | 29 |
| Reserved | Reserved | 30 |
| MIBADC1 | MIBADC1 magnitude interrupt | 31 |

Table 4-5. Interrupt Request Assignments (continued)

| Modules | Interrupt Sources | Default VIM Interrupt Request |
|------------------|--------------------------------------|-------------------------------|
| FlexRay | FlexRay level 1 interrupt | 32 |
| DMA | FTCA interrupt | 33 |
| DMA | LFSA interrupt | 34 |
| DCAN2 | DCAN2 level 0 interrupt | 35 |
| DMM | DMM level 0 interrupt | 36 |
| MIBSPI3 | MIBSPI3 level 0 interrupt | 37 |
| MIBSPI3 | MIBSPI3 level 1 interrupt | 38 |
| DMA | HBCA interrupt | 39 |
| DMA | BTCA interrupt | 40 |
| Reserved | Reserved | 41 |
| DCAN2 | DCAN2 level 1 interrupt | 42 |
| DMM | DMM level 1 interrupt | 43 |
| DCAN1 | DCAN1 IF3 interrupt | 44 |
| DCAN3 | DCAN3 level 0 interrupt | 45 |
| DCAN2 | DCAN2 IF3 interrupt | 46 |
| FPU | FPU interrupt | 47 |
| FlexRay TU | FlexRay TU Transfer Status interrupt | 48 |
| LIN2 (incl. SCI) | LIN2 level 0 interrupt | 49 |
| MIBADC2 | MIBADC2 event group interrupt | 50 |
| MIBADC2 | MIBADC2 sw group 1 interrupt | 51 |
| FlexRay | FlexRay T0C interrupt | 52 |
| MIBSPIP5 | MIBSPIP5 level 0 interrupt | 53 |
| LIN2 (incl. SCI) | LIN2 level 1 interrupt | 54 |
| DCAN3 | DCAN3 level 1 interrupt | 55 |
| MIBSPIP5 | MIBSPIP5 level 1 interrupt | 56 |
| MIBADC2 | MIBADC2 sw group 2 interrupt | 57 |
| FlexRay TU | FlexRay TU Error interrupt | 58 |
| MIBADC2 | MIBADC2 magnitude interrupt | 59 |
| DCAN3 | DCAN3 IF3 interrupt | 60 |
| Reserved | Reserved | 61 |
| FlexRay | FlexRay T1C interrupt | 62 |
| Reserved | Reserved | 63 |

Note: Address location 0x00000000 in the VIM RAM is reserved for the phantom interrupt ISR entry.

4.5 MIBADC Event Trigger Sources

All three conversion groups can be configured for event-triggered operation, providing up to three event triggered groups.

The trigger source and polarity can be selected individually for group 1, group 2 and the event group from the options identified in the first table following for MibADC1 and in the second table following for MibADC2.

Table 4-6. MIBADC1 Event Trigger Sources

| Event # | SOURCE SELECT BITS for G1, G2 or EVENT (G1SRC[2:0], G2SRC[2:0] or EVSRC[2:0]) | Hookup |
|---------|---|---------------|
| 1 | 000 | AD1EVT |
| 2 | 001 | NHET[8] |
| 3 | 010 | NHET[10] |
| 4 | 011 | RTI compare 0 |
| 5 | 100 | NHET[17] |
| 6 | 101 | NHET[19] |
| 7 | 110 | GIOB[0] |
| 8 | 111 | GIOB[1] |

NOTE

The Trigger is present, even if the pin is not available.

Table 4-7. MIBADC2 Event Trigger Sources

| Event # | SOURCE SELECT BITS for G1, G2 or EVENT (G1SRC[2:0], G2SRC[2:0] or EVSRC[2:0]) | Hookup |
|---------|---|---------------|
| 1 | 000 | AD2EVT |
| 2 | 001 | NHET[8] |
| 3 | 010 | NHET[10] |
| 4 | 011 | RTI compare 0 |
| 5 | 100 | NHET[17] |
| 6 | 101 | NHET[19] |
| 7 | 110 | GIOB[0] |
| 8 | 111 | GIOB[1] |

NOTE

The Trigger is present, even if the pin is not available.

The application can generate the trigger condition using these signals by configuring the corresponding device pins as input pins and driving them from an external source, or by configuring them as output pins and driving them by software. The pin doesn't have to be present on the package to be able to be used as a trigger.

The interrupt request signals (RTI compare 0) are driven HIGH when the interrupt condition occurs. So if the ADC is required to be triggered on the interrupt being asserted, select the rising edge for this trigger source. The ADC can be still triggered using the falling edge on the interrupt line. In this case, the falling edge occurs when the interrupt line is deasserted.

4.6 MIBSPI

4.6.1 MIBSPI Event Trigger Sources

The Multi-buffered Serial Peripheral Interfaces (MIBSPIs) have a programmable buffer memory that enables data transmission to be completed without CPU intervention. The buffers are combined in different Transfer Groups (TGs) that can be triggered by external events such as I/O activity, timers or by the internal tick counter. The internal tick counter supports the periodic trigger of events. Each buffer of the MibSPI can be associated with different DMA channels in different TGs, allowing the user to move data between internal memory and an external slave with minimal CPU interaction.

Table 4-8. MIBSPI1 Event Trigger Sources

| Event | TGxCTRL TRIGSRC[3:0] | Hookup |
|----------|----------------------|-----------------------|
| Disabled | 0000 | No trigger source |
| EVENT0 | 0001 | GIOA[0] |
| EVENT1 | 0010 | GIOA[1] |
| EVENT2 | 0011 | GIOA[2] |
| EVENT3 | 0100 | GIOA[3] |
| EVENT4 | 0101 | GIOA[4] |
| EVENT5 | 0110 | GIOA[5] |
| EVENT6 | 0111 | GIOA[6] |
| EVENT7 | 1000 | GIOA[7] |
| EVENT8 | 1001 | NHET[8] |
| EVENT9 | 1010 | NHET[10] |
| EVENT10 | 1011 | NHET[12] |
| EVENT11 | 1100 | NHET[14] |
| EVENT12 | 1101 | NHET[16] |
| EVENT13 | 1110 | NHET[18] |
| EVENT14 | 1111 | Internal Tick counter |

Table 4-9. MIBSPI3 Event Trigger Sources

| Event | TGxCTRL TRIGSRC[3:0] | Hookup |
|----------|----------------------|-----------------------|
| Disabled | 0000 | No trigger source |
| EVENT0 | 0001 | GIOA[0] |
| EVENT1 | 0010 | GIOA[1] |
| EVENT2 | 0011 | GIOA[2] |
| EVENT3 | 0100 | GIOA[3] |
| EVENT4 | 0101 | GIOA[4] |
| EVENT5 | 0110 | GIOA[5] |
| EVENT6 | 0111 | GIOA[6] |
| EVENT7 | 1000 | GIOA[7] |
| EVENT8 | 1001 | NHET[8] |
| EVENT9 | 1010 | NHET[10] |
| EVENT10 | 1011 | NHET[12] |
| EVENT11 | 1100 | NHET[14] |
| EVENT12 | 1101 | NHET[16] |
| EVENT13 | 1110 | NHET[18] |
| EVENT14 | 1111 | Internal Tick counter |

Table 4-10. MIBSPI5 Event Trigger Sources

| Event | TGxCTRL TRIGSRC[3:0] | Hookup |
|----------|----------------------|-----------------------|
| Disabled | 0000 | No trigger source |
| EVENT0 | 0001 | GIOA[0] |
| EVENT1 | 0010 | GIOA[1] |
| EVENT2 | 0011 | GIOA[2] |
| EVENT3 | 0100 | GIOA[3] |
| EVENT4 | 0101 | GIOA[4] |
| EVENT5 | 0110 | GIOA[5] |
| EVENT6 | 0111 | GIOA[6] |
| EVENT7 | 1000 | GIOA[7] |
| EVENT8 | 1001 | NHET[8] |
| EVENT9 | 1010 | NHET[10] |
| EVENT10 | 1011 | NHET[12] |
| EVENT11 | 1100 | NHET[14] |
| EVENT12 | 1101 | NHET[16] |
| EVENT13 | 1110 | NHET[18] |
| EVENT14 | 1111 | Internal Tick counter |

4.6.2 MIBSPI5/DMM Pin Multiplexing

The multiplexing of MIBSPI5 and DMM pins are controlled by the status of the MIBSPI5 module and the DMM module. The pins will have DMM functionality if the DMM module is enabled and the MIBSPI5 module is disabled; if the MIBSPI5 is enabled the pins will have MIBSPI functionality, regardless of the DMM module status. DMMCLK, DMMSYNC, DMMENA and DMMDATA[1:0] are always functional independent of the MIBSPI5 configuration because they are not multiplexed. The related pin numbers can be found in the MIBSPI5 and the DMM section of the Terminal Functions chapter. The following table shows the MIBSPI5 and DMM Data pin multiplexing.

Table 4-11. MIBSPI5 Pin Multiplexing

| MIBSPI5 enabled | DMM enabled & MIBSPI5 disabled |
|----------------------------------|--------------------------------|
| MIBSPI5CLK | DMMDATA[4] |
| $\overline{\text{MIBSPI5CS}}[0]$ | DMMDATA[5] |
| $\overline{\text{MIBSPI5CS}}[1]$ | DMMDATA[6] |
| $\overline{\text{MIBSPI5CS}}[2]$ | DMMDATA[2] |
| $\overline{\text{MIBSPI5CS}}[3]$ | DMMDATA[3] |
| MIBSPI5ENA | DMMDATA[7] |
| MIBSPI5SIMO[0] | DMMDATA[8] |
| MIBSPI5SIMO[1] | DMMDATA[9] |
| MIBSPI5SIMO[2] | DMMDATA[10] |
| MIBSPI5SIMO[3] | DMMDATA[11] |
| MIBSPI5SOMI[0] | DMMDATA[12] |
| MIBSPI5SOMI[1] | DMMDATA[13] |
| MIBSPI5SOMI[2] | DMMDATA[14] |
| MIBSPI5SOMI[3] | DMMDATA[15] |

4.7 ETM

The device contains an ARM Cortex™-R4F External Trace Macrocell (ETM-R4) with a 32bit data port. The ETM-R4 module is connected to a Test Port Interface Unit (TPIU) with a 32bit data bus. The ETM-R4 is CoreSight compliant and follows the ARM ETM v3 specification; for more details see ARM CoreSight™ ETM-R4 TRM specification Revr0p0. The ETM-R4 supports "half rate clocking" only.

The ETM clock source can be selected as either VCLK or the external ETMTRACECLKIN pin. The selection is done by the EXTCTRL0UT[1:0] control bits of the TPIU; the default is '00'.

Table 4-12. ETMTRACECLKIN Selection

| EXTCTRL0UT[1:0] | TPIU/TRACECLKIN |
|-----------------|-----------------|
| 00 | tied-zero |
| 01 | VCLK |
| 10 | ETMTRACECLKIN |
| 11 | tied-zero |

4.8 Debug Scan Chains

The device contains an ICEPICK module to access the debug scan chains. Debug scan chain #0 handles the access to the CPU, to the ETM-R4 (External Trace Macrocell), to the POM (Parameter Overlay Module) and to the TPIU (Test Port Interface Unit). Debug scan chain #1 handles the access to the Ram Trace Port (RTP) and the Data Modification Module (DMM) which each incorporate a dedicated TAP (Test Access Port) controller. Each module is selected via its scan chain number. The IcePick scan ID is 0x80206D05, which is the same number as the device ID.

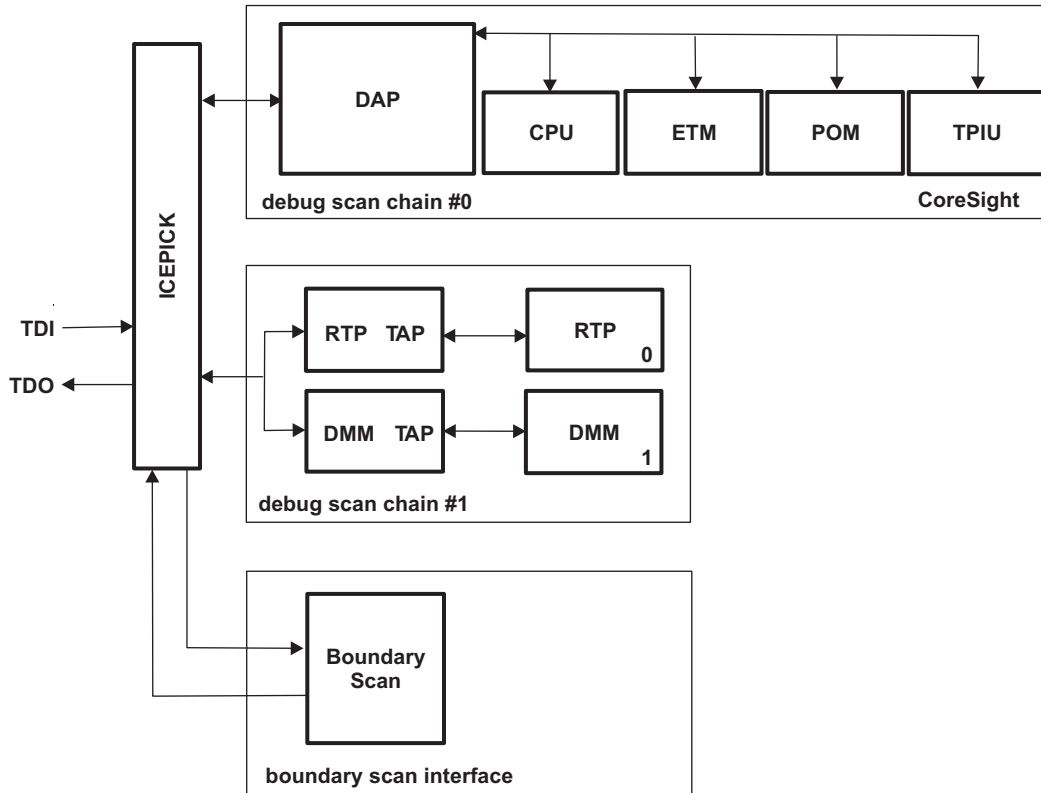


Figure 4-1. Debug Scan Chains

4.8.1 JTAG

The 32bit JTAG ID code for this device is 0x0B7B302F.

4.9 CCM

4.9.1 Dual Core Implementation

The microcontroller has two Cortex-R4 cores, where the output signals of both CPUs are compared in the CCM-R4 (Core Compare Module). To avoid common mode impacts the signals of the CPUs to be compared are delayed in a different way as shown in the following figure.

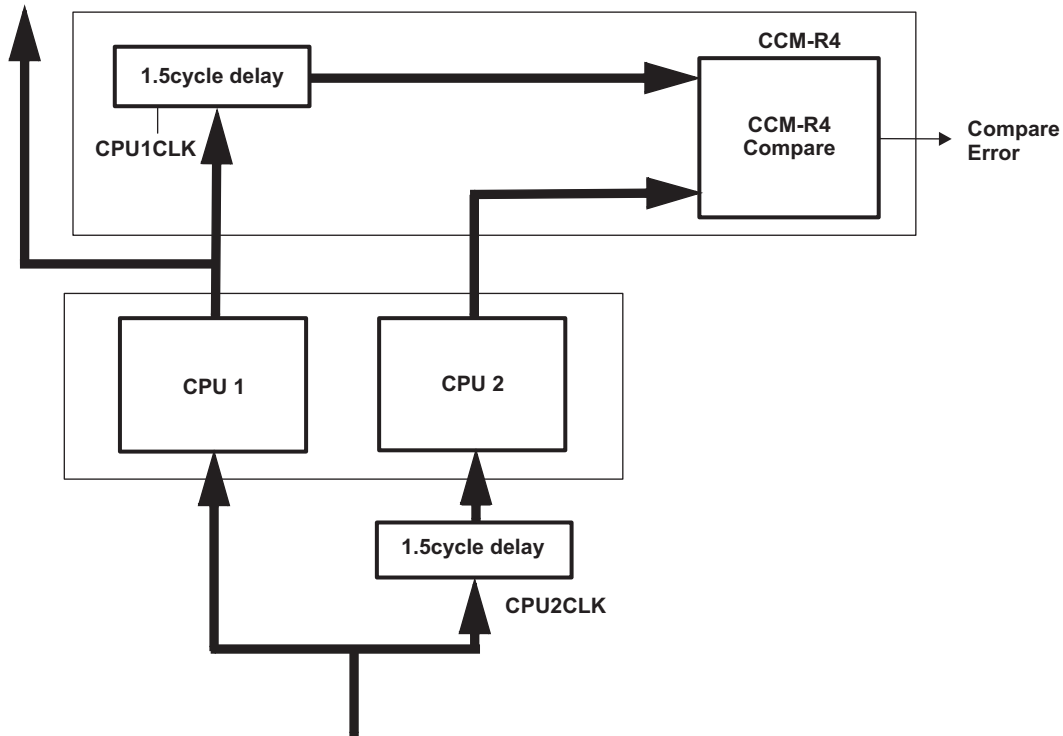


Figure 4-2. Dual Core Implementation

4.9.2 CCM-R4

To avoid an erroneous CCM-R4 compare error, the application software must ensure that the CPU registers of both CPUs are initialized with the same values before the 1st function call or other operation that pushes the CPU registers onto the stack. All CCM-R4 error forcing test modes are limited to 100MHz HCLK speed.

4.10 LPM

TMS570 Platform devices support multiple low power modes. These different modes allow the user to trade-off the amount of current consumption during low power mode versus functionality and wake-up time.

Supported Low Power modes on this devices are Doze, Snooze and Sleep; for detailed description please refer to the Architecture section of the Technical Reference Manual.

4.11 Voltage Monitor

A voltage monitor has been implemented on this device. The purpose of this voltage monitor is to eliminate the requirement for a specific sequence when powering up the core and I/O voltage supplies. It also reduces the risk of corrupting memory or glitches on I/O pins during power-up, power-down or brown outs. The voltage monitor does not eliminate the need of a voltage supervisor circuit to guarantee that the device is held in reset when the voltage supplies are out of range. The voltage monitor thresholds can be found in the Vmon section of the device electrical specifications.

When the voltage monitor detects a low voltage on the I/O supply, it will assert a reset. When the voltage monitor detects a low voltage on the core supply, it asynchronously makes all output pins high impedance, and asserts a reset. The voltage monitor is disabled when the device is in halt mode.

The voltage monitor has three filter functions:

- It rejects short low-going glitches on the $\overline{\text{PORRST}}$ pin
- It rejects noise on the VCCIO supply
- It rejects noise on the VCC supply

Please note that such glitches on VCC and VCCIO could still corrupt the system depending on many factors. The width of noise that can be filtered by the voltage monitor on the VCC and VCCIO supplies is shown in the table below. Glitches less than MIN will be filtered out, glitches greater than MAX are guaranteed to generate a reset. The duration of glitches that will be filtered on the $\overline{\text{PORRST}}$ pin can be found in [Table 7-6, Timing Requirements for \$\overline{\text{PORRST}}\$](#) .

Table 4-13. VMON Supply Glitch Filter Capability

| Parameter | Min | Max |
|---|-------|-----|
| Width of glitch on VCC that can be filtered out | 300ns | 1us |
| Width of glitch on VCCIO that can be filtered out | 300ns | 1us |

4.12 CRC

MCRC Controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a pre-determined good signature value. MCRC controller provides up to four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system. Channel 1 can also be put into data trace mode. In data trace mode, MCRC controller compresses each data being read through the CPU read data bus.

When using the MCRC module in PSA mode while ECC is enabled, bus masters (e.g. FTU, HTU, DMA or CPU) should not write to the data RAM (TCRAM) to avoid corrupting the PSA value.

4.13 System Module Access

The system module access modes and access rights are shown in the following table.

Table 4-14. System Module Access

| Domain | Module | Access Mode Used by Module | Access Rights Required to Access the Module RAMS |
|------------|--------|----------------------------|--|
| System | VIM | n/a | privilege mode (RWP) |
| System | RTP | n/a | privilege mode (RWP) |
| System | DMA | user mode | privilege mode (RWP) |
| Peripheral | HTU | privilege mode | privilege mode (RWP) |
| Peripheral | FTU | user & privilege mode | user & privilege mode (RW) |

4.14 Debug ROM

The Debug ROM stores the location of the components on the Debug APB bus.

Table 4-15. Debug ROM Table

| Address | Description | Value |
|-------------------------|----------------------|------------|
| Components Table | | |
| 0x000 | pointer to Cortex-R4 | 0x00001003 |
| 0x000 | ETM | 0x00002003 |
| 0x000 | TPIU | 0x00003003 |
| 0x000 | POM | 0x00004003 |
| 0x001 | end of table | 0x00000000 |

4.15 CPU Self Test Controller: STC / LBIST

The CPU Self Test Controller (STC) is used to test the ARM CPU core using a Deterministic Logic BIST (LBIST) Controller as the test engine. The STC has the capability of dividing the complete test run into smaller independent test sets (intervals). The test coverage and number of test execution cycles for each test interval is shown in the table below.

The maximum clock rate for the STC / LBIST is:

- 53.333MHz when HCLK = 160MHz / VCLK = 80MHz on BGA package
- 50MHz when HCLK = 100MHz / VCLK = 100MHz on QFP and BGA packages
- 46.666MHz when HCLK = 140MHz / VCLK = 70MHz on QFP and BGA packages

In order to achieve the proper clock rate during CPU self test a STC clock divider has been implemented. The clock divider is set by the CLKDIV bits in STCCCLKDIV register in the secondary system module frame at location 0xFFFF E108. The default value of the CPU Self Test LBIST clock divider is set to 'divide-by-1'.

NOTE

The supply current while performing CPU self test is different than the device operating mode current. These values can be found in the I_{cc} section of [Section 6.5](#).

Table 4-16. STC/LBIST Test Coverage and Duration

| Intervals | Test Coverage | Test Cycles (STC Clock Cycles) |
|-----------|---------------|--------------------------------|
| 0 | 0% | 0 |
| 1 | 57.14% | 1,555 |
| 2 | 65.82% | 3,108 |
| 3 | 70.56% | 4,661 |
| 4 | 73.56% | 6,214 |
| 5 | 76.06% | 7,767 |
| 6 | 78.07% | 9,320 |
| 7 | 79.62% | 10,873 |
| 8 | 80.92% | 12,426 |
| 9 | 82.1% | 13,979 |
| 10 | 82.94% | 15,532 |
| 11 | 83.76% | 17,085 |
| 12 | 84.51% | 18,638 |
| 13 | 85.12% | 20,191 |
| 14 | 85.62% | 21,744 |
| 15 | 86.19% | 23,297 |
| 16 | 86.56% | 24,850 |
| 17 | 86.97% | 26,403 |
| 18 | 87.33% | 27,956 |
| 19 | 87.67% | 29,509 |
| 20 | 88.01% | 31,062 |
| 21 | 88.31% | 32,615 |
| 22 | 88.58% | 34,168 |
| 23 | 88.87% | 35,721 |
| 24 | 89.11% | 37,274 |
| 25 | 89.34% | 38,827 |
| 26 | 89.59% | 40,380 |
| 27 | 89.82% | 41,933 |
| 28 | 90.05% | 43,486 |

Table 4-16. STC/LBIST Test Coverage and Duration (continued)

| Intervals | Test Coverage | Test Cycles (STC Clock Cycles) |
|-----------|---------------|--------------------------------|
| 29 | 90.26% | 45,039 |
| 30 | 90.46% | 46,592 |
| 31 | 90.64% | 48,145 |
| 32 | 90.84% | 49,698 |

5 Device Registers

5.1 Device Identification Code Register

The device identification code register identifies several aspects of the device including the silicon version. The details of the device identification code register are shown in [Figure 5-1](#). The device identification code register value for this device is:

- Rev 0 = 0x80206D05
- Rev A = 0x80206D0D

Figure 5-1. Device ID Bit Allocation Register

| | | | | | | | | | | | | | | | |
|-------|--------------------|--------------------|----------------------------------|-----------|----|------------|----|---------|----|----|----|----|-----|-----|-----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CP-15 | UNIQUE ID | | | | | | | | | | | | | | 16 |
| R-1 | R-00000 0000 10000 | | | | | | | | | | | | | | R-0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TECH | | I/O VOLT AGE | PERIP HERA L PARIT Y | FLASH ECC | | RAM ECC | | VERSION | | | | | 1 | 0 | 1 |
| R-011 | | R-0 | R-1 | R-10 | | R-1 | | R-1 | | | | | R-1 | R-0 | R-1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; D= *device dependent*

Table 5-1. Device ID Bit Allocation Register Field Descriptions

| Bit | Field | Value | Description |
|-------|--------------------------|--|---|
| 31 | CP15 | 0 1 | Indicates the presence of coprocessor 15 CP15 not present CP15 present |
| 30-17 | UNIQUE ID | 1 | Silicon version (revision) bits This bitfield holds a unique number for a dedicated device configuration (die). |
| 16-13 | TECH | 0000 0001 0010 0011 Others | Process technology on which the device is manufactured. C05 F05 C035 F035 Reserved |
| 12 | I/O VOLTAGE | 0 1 | I/O voltage of the device. I/O are 3.3v I/O are 5v |
| 11 | PERIPHERA L PARITY | 0 1 | Peripheral Parity No parity on peripherals Parity on peripherals |
| 10-9 | FLASH ECC | 00 01 10 11 | Flash ECC No error detection/correction Program memory with parity Program memory with ECC Reserved |
| 8 | RAM ECC | 0 1 | Indicates if RAM memory ECC is present. No ECC implemented ECC implemented |
| 7-3 | REVISION | | Revision of the Device. |

Table 5-1. Device ID Bit Allocation Register Field Descriptions (continued)

| Bit | Field | Value | Description |
|-----|-------|-------|--|
| 2-0 | 101 | | The platform family ID is always 0b101 |

5.2 Die-ID Registers

The two registers (DIEIDL and DIEIDH) form a 64-bit number that contains information about the device's die lot number, wafer number and X, Y wafer coordinates. The die identification information will vary from unit to unit. This information is programmed by TI as part of the initial device test procedure. The data format of the Die-ID registers is shown here.

Figure 5-2. DIEIDL Register (Location: 0xFFFF FF7C)

| | | | | | | | | | | | | | | | |
|---------------------|----|----|----|----|----|----|----|---------------------|----|---------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOT (LOWER 10 BITS) | | | | | | | | | | WAFER # | | | | | |
| R-D | | | | | | | | | | R-D | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Y WAFER COORDINATES | | | | | | | | X WAFER COORDINATES | | | | | | | |
| R-D | | | | | | | | R-D | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; D= device dependent

Figure 5-3. DIEIDH Register (Location: 0xFFFF FF80)

| | | | | | | | | | | | | | | | |
|----------|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-D | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | LOT # (UPPER 14 BITS) | | | | | | | | | | | | | | |
| R-D | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; D= device dependent

5.3 PLL Registers

The default values for the PLL (Phase Locked Loop) control registers are shown in this section. PLLCTL1 and PLLCTL2 are used to configure PLL1 (F035 FMzPLL) and PLLCTL3 is used to configure PLL2 (F035 FPLL).

Figure 5-4. PLLCTL1 Register (Location: 0xFFFF FF70)

| | | | | | | | | | | | | | | | |
|-----------------------|-----------|----|-------------|----|----|----|--------|------|----------------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ROS | BPOS[1:0] | | PLLDIV[4:0] | | | | ROF | RESV | REFCLKDIV[5:0] | | | | | | |
| R/WP-0 | R/WP-01 | | R/WP-01111 | | | | R/WP-0 | R-0 | R/WP-000010 | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PLL MUL[15:0] | | | | | | | | | | | | | | | |
| R/WP-0101111100000000 | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; D = device specific

PLLCTL1 Default = 0x2F025F00

Figure 5-5. PLLCTL2 Register (Location: 0xFFFF FF74)

| | | | | | | | | | | | | | | | |
|------------|--------------------|----|----------|----|----|----|-----------------|----|------|------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FMEN A | SPREADINGRATE[8:0] | | | | | | | | RESV | EWADJ[8:4] | | | | | |
| R/WP-0 | R/WP-111111111 | | | | | | | | R-0 | R/WP-00000 | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BWADJ[3:0] | | | ODPLL | | | | SPR_AMOUNT[8:0] | | | | | | | | |
| R/WP-0111 | | | R/WP-001 | | | | R/WP-000000000 | | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; D = device specific

PLLCTL2 Default = 0x7FC07200

NOTE

There are several combinations of the modulation depth and modulation frequency that are not allowed. Valid settings for this device include the list in [Table 7-2](#).

Figure 5-6. PLLCTL3 Register (Location: 0xFFFF E100)

| | | | | | | | | | | | | | | | |
|---------------|----|----|--------------|----|----|----|-----------|----|---------|---------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | OSC DIV | RESERVED | | | | | |
| R/W-000000000 | | | | | | | | | R/WP-0 | R/W-000000 | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | PLL_MUL[3:0] | | | | RESERVED | | | PLL_DIV [2:0] | | | | | |
| R/W-000000 | | | R/WP-011 | | | | R/W-00000 | | | R/WP 111 | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; D = device specific

PLLCTL3 Default = 0x00000307

6 Device Electrical Specifications

6.1 Operating Conditions

6.2 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)⁽¹⁾

| | | |
|--|---|------------------|
| Supply voltage ranges | V_{CC} ⁽²⁾ | - 0.3 V to 2.1V |
| | V_{CCIO} , V_{CCAD} , V_{CCP} (Flash pump) ⁽²⁾ | - 0.3 V to 4.1V |
| Input voltage range | All input pins | - 0.3 V to 4.1 V |
| Input clamp current | $I_{IK}(V_I < 0 \text{ or } V_I > V_{CCIO})$ | ±20 mA |
| | All pins except AD1IN[7:0], AD2IN[7:0], ADSIN[15:8] | |
| | $I_{IK}(V_I < 0 \text{ or } V_I > V_{CCAD})$ | |
| | AD1IN[7:0], AD2IN[7:0], ADSIN[15:8] | ±10 mA |
| | total | ±40 mA |
| Operating free-air temperature ranges, T_A | | -55°C to 125°C |
| Storage temperature range, T_{stg} | | -65°C to 150°C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

(2) All voltage values are with respect to their associated grounds.

6.3 Device Recommended Operating Conditions⁽¹⁾

| | | MIN | NOM | MAX | Unit |
|------------|-------------------------------------|------|-----|------|------|
| V_{CC} | Digital logic supply voltage (Core) | 1.35 | 1.5 | 1.65 | V |
| V_{CCIO} | Digital logic supply voltage (I/O) | 3 | 3.3 | 3.6 | V |
| V_{CCAD} | MibADC supply voltage | 3 | 3.3 | 3.6 | V |
| V_{CCP} | Flash pump supply voltage | 3 | 3.3 | 3.6 | V |
| V_{SS} | Digital logic supply ground | | 0 | | V |
| V_{SSAD} | MibADC supply ground | -0.1 | | 0.1 | V |
| T_A | Operating free-air temperature | -55 | | 125 | °C |

(1) All voltages are with respect to V_{SS} except V_{CCAD} is with respect to V_{SSAD} .

6.4 Thermal Information

| THERMAL METRIC | | TMS570LS20206 TMS570LS20216 | | UNITS |
|------------------|---|--------------------------------|----------|-------|
| | | GWT | PGE | |
| | | 337 BALL | 144 PINS | |
| θ_{JA} | Junction-to-ambient thermal resistance ⁽¹⁾ | 30.7 | 32.1 | °C/W |
| θ_{JcTop} | Junction-to-case (top) thermal resistance ⁽²⁾ | 4.7 | 3.3 | |
| θ_{JB} | Junction-to-board thermal resistance ⁽³⁾ | 15 | 13.7 | |
| ψ_{JT} | Junction-to-top characterization parameter ⁽⁴⁾ | 0.1 | 0.1 | |
| ψ_{JB} | Junction-to-board characterization parameter ⁽⁵⁾ | 15 | 13.3 | |
| θ_{JcBot} | Junction-to-case (bottom) thermal resistance ⁽⁶⁾ | N/A | N/A | |

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (5) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics Over Operating Free-Air Temperature Range⁽¹⁾

| Parameter | | | Test Conditions | MIN | TYP | MAX | Unit | |
|----------------------------------|------------------------------|---------------------------|--|---------------------------------------|------|-------------------------|------|----|
| V _{hys} | Input hysteresis | | | 0.15 | | | V | |
| V _{IL} | Low-level input voltage | All inputs ⁽²⁾ | | -0.3 | | 0.8 | V | |
| V _{IH} | High-level input voltage | All inputs | | 2 | | V _{CCIO} + 0.3 | V | |
| V _{OL} | Low-level output voltage | | I _{OL} = I _{OL} MAX | | | 0.2 V _{CCIO} | V | |
| | | | I _{OL} = 50 μA | | | 0.2 | | |
| V _{OH} | High-level output voltage | | I _{OH} = I _{OH} MAX | 0.8 V _{CCIO} | | | V | |
| | | | I _{OH} = 50 μA | V _{CCIO} - 0.2 | | | | |
| V _{ILoscIn} | Low-level input voltage | OSCIN | | -0.3 | | 0.2 V _{CC} | V | |
| V _{IHoscIn} | High-level input voltage | OSCIN | | 0.8 V _{CC} | | V _{CC} + 0.3 | V | |
| V _{MON} | Voltage monitoring threshold | | VCC low | 1.0 | 1.2 | 1.35 | V | |
| | | | VCC high | 1.7 | 2 | 2.38 | | |
| | | | VCCIO low | 2.0 | 2.4 | 3.0 | | |
| I _{IC} | Input clamp current | | V _I < V _{SSIO} - 0.3 or V _I > V _{CCIO} + 0.3 | -2 | | 2 | mA | |
| I _I | Input current (I/O pins) | | I _{IL} Pulldown | V _I = V _{SS} | -1 | | 1 | μA |
| | | | I _{IH} Pulldown 20 uA | V _I = V _{CCIO} | 5 | | 40 | |
| | | | I _{IH} Pulldown 100 uA | V _I = V _{CCIO} | 40 | | 195 | |
| | | | I _{IL} Pullup 20 uA | V _I = V _{SS} | -40 | | -3.6 | |
| | | | I _{IL} Pullup 100 uA | V _I = V _{SS} | -195 | | -40 | |
| | | | I _{IH} Pullup | V _I = V _{CCIO} | -1 | | 1 | |
| | | | All other pins | No pullup or pulldown | -1 | | 1 | |
| I _{OL} | Low-level output current | | TDO | V _{OL} = V _{OL} MAX | | | 8 | mA |
| | | | TDI | | | | | |
| | | | TMS | | | | | |
| | | | RTCK | | | | | |
| | | | ECLK | | | | | |
| | | | FRAYTX1 | | | | | |
| | | | FRAYTXEN1 | | | | | |
| | | | FRAYTX2 | | | | | |
| | | | FRAYTXEN2 | | | | | |
| | | | $\overline{\text{DMMENA}}$ | | | | | |
| | | | ETMTRACECTL | | | | | |
| | | | ETMTRACECLKOUT | | | | | |
| | | | ETMDATA[31:0] | | | | | |
| | | | RTPSYNC | | | | | |
| | | | RTPCLK | | | | | |
| | | | RTPDATA[15:0] | | | | | |
| | | | $\overline{\text{EMIFWE}}$ | | | | | |
| | | | $\overline{\text{EMIFOE}}$ | | | | | |
| | | | $\overline{\text{EMIFCS}}[3:0]$ | | | | | |
| | | | EMIFDATA[15:0] | | | | | |
| EMIFADD[21:0] | | | | | | | | |
| EMIFBADD[1:0] | | | | | | | | |
| $\overline{\text{EMIFDQM}}[1:0]$ | | | | | | | | |
| $\overline{\text{ERROR}}$ | | | | | | | | |

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.

(2) This does not apply to PORRST pin.

Electrical Characteristics Over Operating Free-Air Temperature Range⁽¹⁾ (continued)

| Parameter | | Test Conditions | MIN | TYP | MAX | Unit |
|-----------------|---------------------------|---|---------------------------------------|-----|-----|------|
| I _{OL} | Low-level output current | \overline{RST} MIBSPI1CLK MIBSPI1SIMO MIBSPI1SOMI MIBSPI3CLK MIBSPI3SIMO MIBSPI3SOMI MIBSPI5CLK MIBSPI5SIMO[3:0] MIBSPI5SOMI[3:0] DMMDATA[15:8] DMMDATA[4] | V _{OL} = V _{OL} MAX | | 4 | mA |
| | | All other output pins | | | 2 | |
| I _{OH} | High-level output current | TDO TDI TMS RTCK ECLK FRAYRX1 FRAYTX1 FRAYTXEN1 FRAYRX2 FRAYTX2 FRAYTXEN2 ETMTRACECTL ETMTRACECLKOUT ETMDATA[31:0] RTPSYNC RTPCLK RTPDATA[15:0] \overline{DMMENA} \overline{EMIFWE} \overline{EMIFOE} \overline{EMIFCS} [3:0] EMIFDATA[15:0] EMIFADD[21:0] EMIFBADD[1:0] $\overline{EMIFDQM}$ [1:0] \overline{ERROR} | V _{OH} = V _{OH} MIN | | -8 | mA |

Electrical Characteristics Over Operating Free-Air Temperature Range⁽¹⁾ (continued)

| Parameter | | Test Conditions | | MIN | TYP | MAX | Unit | |
|---|---|---|---|------|-----|-----|------|----|
| I _{OH} | High-level output current | RST | V _{OH} = V _{OH} MIN | | | -4 | mA | |
| | | MIBSPI1CLK MIBSPI1SIMO MIBSPI1SOMI MIBSPI3CLK MIBSPI3SIMO MIBSPI3SOMI MIBSPI5CLK MIBSPI5SIMO[3:0] MIBSPI5SOMI[3:0] DMMDATA[15:8] DMMDATA[4] | | | | | | |
| | | All other output pins | | | | -2 | | |
| I _{CC} ⁽¹⁾ | V _{CC} Digital supply current (Operating mode) | All packages | HCLK = 100MHz, VCLK = 100MHz | | | 350 | mA | |
| | | | HCLK = 140MHz, VCLK= 70MHz | | | 390 | mA | |
| | | BGA packages | HCLK = 160MHz, VCLK = 80MHz | | | 430 | mA | |
| | V _{CC} Digital supply current (CPU selftest mode: LBIST) ⁽²⁾⁽³⁾ | All packages | STCCLK = 46.666MHz | Peak | | | 510 | mA |
| | | | STCCLK = 50.0MHz | Peak | | | 540 | mA |
| | | BGA packages | STCCLK = 53.333MHz | Peak | | | 580 | mA |
| | V _{CC} Digital supply current (Mem selftest mode: PBIST) ⁽²⁾⁽⁴⁾ | All packages | HCLK=80MHz, VCLK=40MHz | Peak | | | 340 | mA |
| | | | HCLK=100MHz, VLCK=100MHz | Peak | | | 430 | mA |
| | V _{CC} Digital supply current (doze mode) | | OSCIN = 6 MHz, V _{CC} = 1.65 V ⁽⁵⁾ | | | | 35 | mA |
| | V _{CC} Digital supply current (snooze mode) | | All frequencies, V _{CC} = 1.65 V ⁽⁵⁾ | | | | 30 | mA |
| V _{CC} Digital supply current (sleep mode) | | All frequencies, V _{CC} = 1.65 V ⁽⁵⁾ | | | | 25 | mA | |
| I _{CCIO} | V _{CCIO} Digital supply current (operating mode) | | No DC load, V _{CCIO} = 3.6 V ⁽⁶⁾ | | | 15 | mA | |
| | V _{CCIO} Digital supply current (doze mode) | | No DC load, V _{CCIO} = 3.6 V ⁽⁶⁾ | | | 700 | μA | |
| | V _{CCIO} Digital supply current (snooze mode) | | No DC load, V _{CCIO} = 3.6 V ⁽⁶⁾ | | | 100 | μA | |
| | V _{CCIO} Digital supply current (sleep mode) | | No DC load, V _{CCIO} = 3.6 V ⁽⁶⁾ | | | 100 | μA | |
| I _{CCAD} | V _{CCAD} supply current (operating mode) | | All frequencies, V _{CCAD} = 3.6 V | | | 30 | mA | |
| | V _{CCAD} supply current (doze mode) | | All frequencies, V _{CCAD} = 3.6 V ⁽⁵⁾ | | | 200 | μA | |
| | V _{CCAD} supply current (snooze mode) | | All frequencies, V _{CCAD} = 3.6 V ⁽⁵⁾ | | | 200 | μA | |
| | V _{CCAD} supply current (sleep mode) | | All frequencies, V _{CCAD} = 3.6 V ⁽⁵⁾ | | | 200 | μA | |
| I _{CCP} | V _{CCP} pump supply current | | V _{CCP} = 3.6 V read operation | | | 25 | mA | |
| | | | V _{CCP} = 3.6 V program ⁽⁷⁾ | | | 90 | mA | |
| | | | V _{CCP} = 3.6 V erase | | | 90 | mA | |
| | | | V _{CCP} = 3.6 V doze mode ⁽⁵⁾ | | | 5 | μA | |
| | | | V _{CCP} = 3.6 V snooze mode ⁽⁵⁾ | | | 5 | μA | |
| | | | V _{CCP} = 3.6 V sleep mode ⁽⁵⁾ | | | 5 | μA | |
| C _I | Input capacitance ⁽⁸⁾ | | | | | 2 | pF | |
| C _O | Output capacitance | | | | | 3 | pF | |

(1) Typical values are at V_{CC}=1.5V and maximum values are at V_{CC}=1.65V

(2) The peak current is measured on the TI EVM board with two 10μF and thirteen 100nF capacitors on VCC domain. Running at a lower frequency consumes less current.

(3) LBIST currents specified are for execution of LBIST with a certain STC clock. Lower current consumption can be achieved by configuring a slower STC Clock frequency. The current peak duration can last for the duration of 1 LBIST test interval.

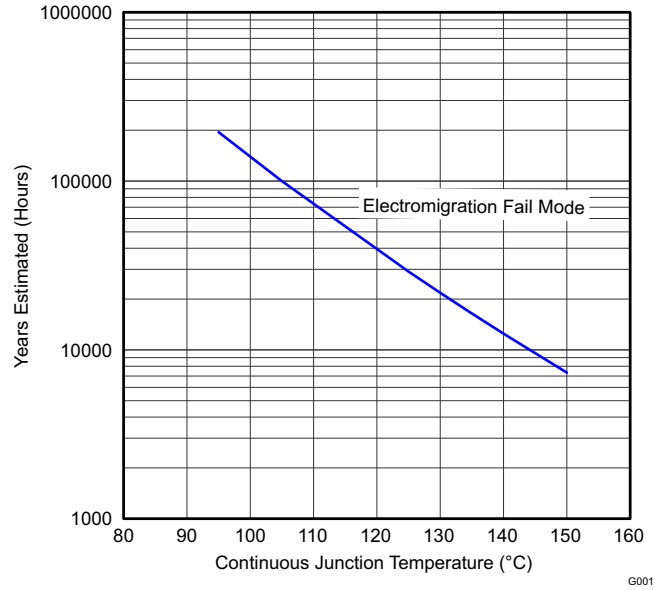
(4) PBIST currents specified are for execution of PBIST on all RAMs(Group 1- 14) and all the algorithms. Lower current consumption can be achieved by configuring a slower HCLK frequency. Different algorithms consume different current. For more information, please refer to *Basic PBIST Configuration and influence on current consumption (SPNA128)*.

(5) For Flash banks/pumps in sleep mode.

(6) I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ V_{CCIO} - 0.2 V.

(7) This assumes reading from one bank while programming a different bank.

(8) The maximum input capacitance C_I of the FlexRay RX pin(s) is 10pF.



- (1) See the absolute maximum ratings and the recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) The predicted operating lifetime vs junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 6-1. TMS570LS20206-EP and TMS570LS20216-EP Operating Life Derating Chart

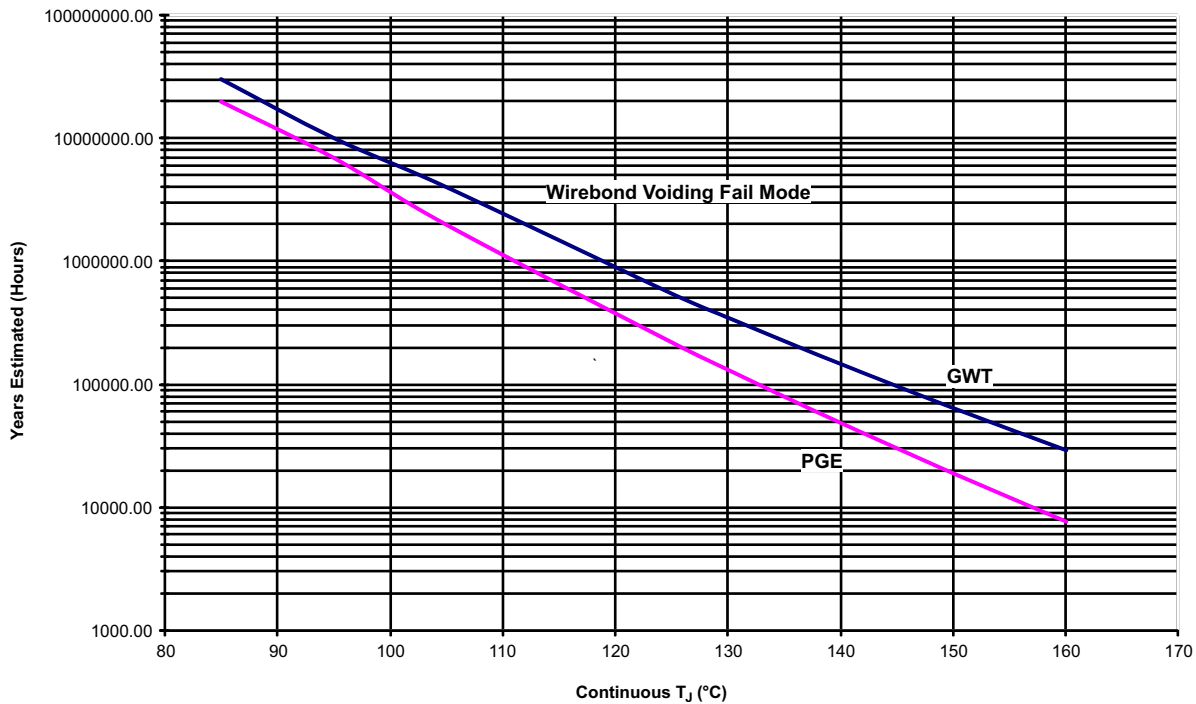


Figure 6-2. TMS570LS20206-EP and TMS570LS20216-EP Wirebond Voiding Fail Mode

7 Peripheral and Electrical Specifications

7.1 Clocks

7.1.1 PLL And Clock Specifications

Table 7-1. Timing Requirements For PLL Circuits Enabled Or Disabled

| | | MIN | MAX | Unit |
|----------------------|----------------------------------|-----|-----|------|
| $f_{(OSC)}^{(1)}$ | Input clock frequency | 5 | | MHz |
| $f_{(OSC)}$ | Input clock frequency | | 20 | MHz |
| $t_{c(OSC)}$ | Cycle time, OSCIN | 50 | | ns |
| $t_{w(OSCIL)}$ | Pulse duration, OSCIN low | 15 | | ns |
| $t_{w(OSCIH)}$ | Pulse duration, OSCIN high | 15 | | ns |
| $f_{(OSCRST)}^{(1)}$ | OSC FAIL frequency - upper level | 20 | 50 | MHz |
| $f_{(OSCRST)}^{(1)}$ | OSC FAIL frequency - lower level | 1.5 | 5 | MHz |

(1) This parameter is characterized from -40°C to 125°C only.

7.1.2 External Reference Resonator/Crystal Oscillator Clock Option

The oscillator is enabled by connecting the appropriate fundamental 5–20 MHz resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in section (a) of the figure below. The oscillator is a single stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and HALT mode.

NOTE

TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 1.5V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in section (b) of the figure below.

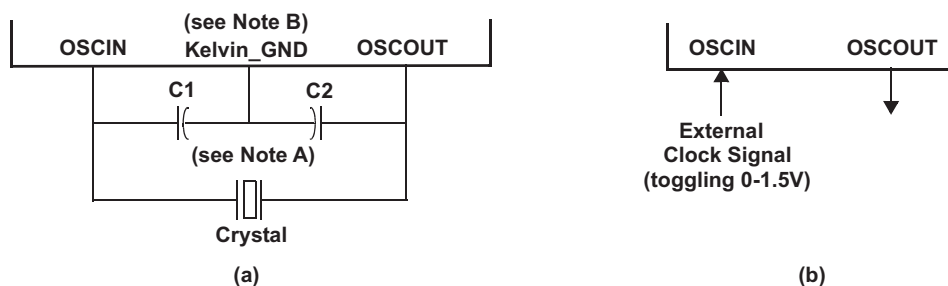


Figure 7-1. Recommended Crystal/Clock Connection

NOTE

In figure (a), The values of C1 and C2 should be provided by the resonator/crystal vendor.

In figure (b), Kelvin_GND should not be connected to any other GND.

7.1.3 Validated FMPLL Setting

The following table includes the validated FMPLL settings.

Table 7-2. Validated FMPLL Settings

| OSC_IN Frequency (MHz) | PLLCTL1 | PLLCTL2 | FMPLL Output Frequency(MHz) | Modulation Bandwidth (KHz) | Modulation Depth |
|------------------------|------------|------------|-----------------------------|----------------------------|------------------|
| 10 | 0x20049500 | 0x82409253 | 150 | 100 | 0.5% |
| 10 | 0x20049500 | 0x8300B240 | 150 | 77 | 0.5% |
| 10 | 0x20048600 | 0x8240925C | 135 | 100 | 0.5% |
| 10 | 0x20048600 | 0x8300B247 | 135 | 77 | 0.5% |
| 10 | 0x20048600 | 0x824092B9 | 135 | 100 | 1.0% |
| 10 | 0x20048D80 | 0x8300B443 | 95 | 77 | 0.5% |
| 10 | 0x20048D80 | 0x824094AF | 95 | 100 | 1.0% |
| 16 | 0x20079500 | 0x82409253 | 150 | 100 | 0.5% |
| 16 | 0x20079500 | 0x8300B240 | 150 | 77 | 0.5% |
| 16 | 0x20078600 | 0x8240925C | 135 | 100 | 0.5% |
| 16 | 0x20078600 | 0x8300B247 | 135 | 77 | 0.5% |
| 16 | 0x20078600 | 0x824092B9 | 135 | 100 | 1.0% |
| 16 | 0x20078D80 | 0x8300B443 | 95 | 77 | 0.5% |
| 16 | 0x20078D80 | 0x824094AF | 95 | 100 | 1.0% |
| 20 | 0x20099500 | 0x82409253 | 150 | 100 | 0.5% |
| 20 | 0x20099500 | 0x8300B240 | 150 | 77 | 0.5% |
| 20 | 0x20098600 | 0x8240925C | 135 | 100 | 0.5% |
| 20 | 0x20098600 | 0x8300B247 | 135 | 77 | 0.5% |
| 20 | 0x20098600 | 0x824092B9 | 135 | 100 | 1.0% |
| 20 | 0x20098D80 | 0x8300B443 | 95 | 77 | 0.5% |
| 20 | 0x20098D80 | 0x824094AF | 95 | 100 | 1.0% |

7.1.4 LPO And Clock Detection

The LPOCLKDET module consists of a clock monitor (CLKDET) and 2 low power oscillators (LPO) - a low frequency (LF) and a high frequency (HF) oscillator. The CLKDET is a supervisor circuit for an externally supplied clock signal. In case the externally supplied clock frequency falls out of a frequency window, the clock detector flags this condition and switches to the HF LPO clock (limp mode). The OSCFAIL flag and clock switch-over remain, regardless of the behavior of the oscillator clock signal. The only way OSCFAIL can be cleared (and re-enable OSCIN as the clock source) is a power-on-reset.

Table 7-3. LPO And Clock Detection

| Parameter | | MIN | Type | MAX | Unit |
|-----------------------------|-----------------|-----|------|------|------|
| Invalid frequency | lower threshold | 1.5 | | 5 | MHz |
| | upper threshold | 20 | | 50 | MHz |
| Limp mode frequency (HFosc) | | 7.9 | 10 | 14.4 | MHz |
| HFosc frequency | | 7.9 | 10 | 14.4 | MHz |
| LFosc frequency | | 62 | 80 | 113 | kHz |

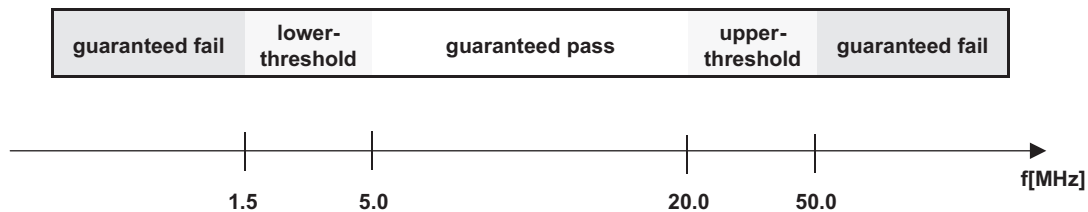


Figure 7-2. LPO And Clock Detection

7.1.5 Switching Characteristics Over Recommended Operating Conditions For Clocks

Table 7-4. Switching Characteristics Over Recommended Operating Conditions For Clocks

| Parameter | Test Conditions | MIN | MAX | Unit |
|-------------------------------------|--|------------------------|----------------------|------|
| f _(HCLK) | HCLK - System clock frequency (337 BGA packages) | Pipeline mode enabled | 160 | MHz |
| | | Pipeline mode disabled | 36 | MHz |
| f _(HCLK) | HCLK - System clock frequency (144pin QFP package) | Pipeline mode enabled | 140 | MHz |
| | | Pipeline mode disabled | 36 | MHz |
| f _(GCLK) | GCLK - CPU clock frequency (ratio GCLK : HCLK = 1:1) | | f _(HCLK) | MHz |
| f _(RCLK) | RCLK - Frequency out of PLL macro into R-divider | | 160 | MHz |
| f _(RTICK) ⁽¹⁾ | RTICK - clock frequency | | f _(VCLK) | MHz |
| f _(VCLK) | VCLK - Primary peripheral clock frequency | | f _(VCLK2) | MHz |
| f _(VCLK2) | VCLK2 - Secondary peripheral clock frequency | | 100 | MHz |
| f _(AVCLK1) | AVCLK1 - Primary asynchronous peripheral clock frequency | | f _(VCLK) | MHz |
| f _(AVCLK2) | AVCLK2 - Secondary asynchronous peripheral clock frequency | | f _(VCLK) | MHz |
| f _(ECLK) ⁽²⁾ | ECLK - External clock output frequency for ECP Module | | 80 | MHz |
| f _(PROG/ERASE) | System clock frequency - Flash programming/erase | | f _(HCLK) | MHz |

- (1) If the RTIx clock source is chosen to be anything other than the default VCLK, then the RTI clock needs to be at least three times slower than the VCLK.
- (2) (ECLK) = f(VCLK) / N, where N = {1 to 65536}. N is the ECP prescale value defined by the ECPCNTL.[15:0] register bits in the System module. Pipeline mode enabled or disabled is determined by the FRDCNTL[2:0].

7.1.5.1 Timing - Wait States

RAM



Flash

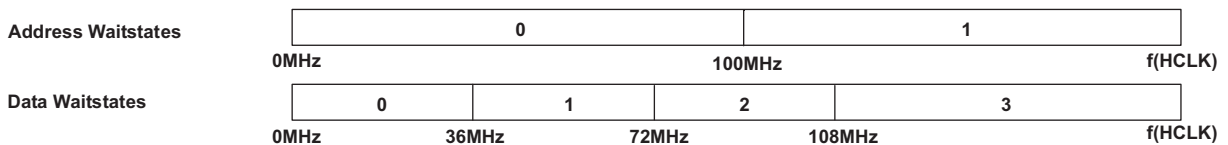


Figure 7-3. Wait States

NOTE

If FMzPLL frequency modulation is enabled, special care must be taken to ensure that the maximum system clock frequency f(HCLK) and peripheral clock frequency f(VCLK) are not exceeded. The speed of the device clocks may need to be derated to accommodate the modulation depth when FMzPLL frequency modulation is enabled.

7.2 ECLK Specification

7.2.1 Switching Characteristics Over Recommended Operating Conditions For External Clocks

Table 7-5. Switching Characteristics Over Recommended Operating Conditions For External Clocks⁽¹⁾⁽²⁾

| NO. | Parameter | | Test Conditions | MIN | MAX | Unit |
|-----|--------------|---------------------------|--|------------------------|-----|------|
| 3 | $t_{w(EOL)}$ | Pulse duration, ECLK low | under all prescale factor combinations (X and N) | $0.5t_{c(ECLK)} - t_f$ | | ns |
| 4 | $t_{w(EOH)}$ | Pulse duration, ECLK high | under all prescale factor combinations (X and N) | $0.5t_{c(ECLK)} - t_r$ | | ns |

(1) X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the VBUS interface clock divider ratio determined by the CLKCNTL.[19:16] bits in the SYS module.

(2) N = {1 to 65536}. N is the ECP prescale value defined by the ECPCNTL.[15:0] register bits in the System module.

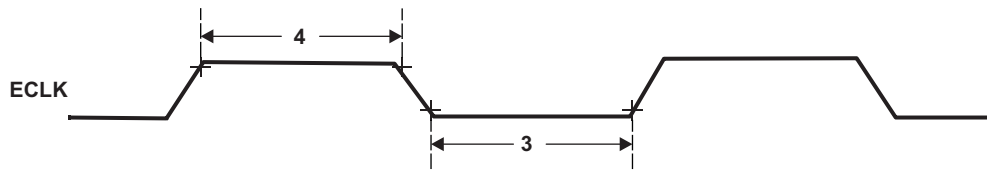


Figure 7-4. ECLK Timing Diagram

7.3 RST And PORRST Timings

7.3.1 Timing Requirements For PORRST

Table 7-6. Timing Requirements For PORRST

| NO. | | | MIN | MAX | Unit |
|-----|------------------------|--|------|----------------|---------|
| | $V_{CCPORL}^{(1)}$ | V_{CC} low supply level when \overline{PORRST} must be active during power up | | 0.5 | V |
| | $V_{CCPORH}^{(1)}$ | V_{CC} high supply level when \overline{PORRST} must remain active during power up and become active during power down | 1.35 | | V |
| | $V_{CCIOPORL}^{(1)}$ | V_{CCIO} / V_{CCP} low supply level when \overline{PORRST} must be active during power up | | 1.1 | V |
| | $V_{CCIOPORH}^{(1)}$ | V_{CCIO} / V_{CCP} high supply level when \overline{PORRST} must remain active during power up and become active during power down | 3 | | V |
| | $V_{IL(PORRST)}^{(1)}$ | Low-level input voltage of \overline{PORRST} $V_{CCIO} > 2.5V$ | | $0.2 V_{CCIO}$ | V |
| | | Low-level input voltage of \overline{PORRST} $V_{CCIO} < 2.5V$ | | 0.5 | V |
| 3 | $t_{su(PORRST)}^{(1)}$ | Setup time, \overline{PORRST} active before V_{CCIO} and $V_{CCP} > V_{CCIOPORL}$ during power up | 0 | | ms |
| 6 | $t_h(PORRST)^{(1)}$ | Hold time, \overline{PORRST} active after $V_{CC} > V_{CCPORH}$ | 1 | | ms |
| 7 | $t_{su(PORRST)}^{(1)}$ | Setup time, \overline{PORRST} active before $V_{CC} \leq V_{CCPORH}$ during power down | 8 | | μs |
| 8 | $t_h(PORRST)^{(1)}$ | Hold time, \overline{PORRST} active after V_{CCIO} and $V_{CCP} > V_{CCIOPORH}$ | 1 | | ms |
| 9 | $t_h(PORRST)^{(1)}$ | Hold time, \overline{PORRST} active after $V_{CC} < V_{CCPORL}$ | 0 | | ms |
| | $t_f(PORRST)^{(1)}$ | Filter time \overline{PORRST} , pulses less than MIN will be filtered out, pulses greater than MAX are guaranteed to generate a reset ⁽²⁾ | 20 | 150 | ns |
| | $t_f(RST)$ | Filter time \overline{RST} , pulses less than MIN will be filtered out, pulses greater than MAX are guaranteed to generate a reset | 20 | 150 | ns |

(1) This parameter is characterized from -40°C to 125°C only.

(2) A low pulse on the nPORRST pin which is just barely longer than the glitch filter implemented on this pin will result in a very short internal reset. This may result in unpredictable behavior as some parts of the device may be reset while other parts of the device are not.

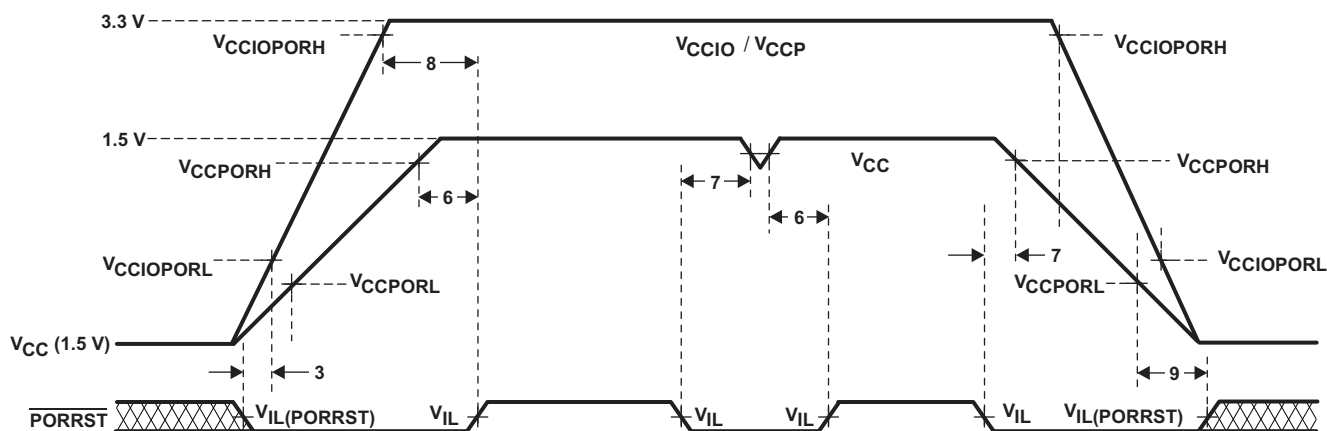


Figure 7-5. PORRST Timing Diagram

NOTE

There is no timing dependency between the ramp of the VCCIO and the VCC supply voltage; this is just an exemplary drawing. All requirements are to ensure \overline{PORRST} is active when VCCIO or VCC is out of the normal operating range.

7.3.2 Switching Characteristics Over Recommended Operating Conditions For \overline{RST}

Table 7-7. Switching Characteristics Over Recommended Operating Conditions For \overline{RST} ⁽¹⁾⁽²⁾

| | Parameter | MIN | MAX | Unit |
|--------------|--|----------------------------------|-----|------|
| $t_{v(RST)}$ | Valid time, \overline{RST} active after \overline{PORRST} inactive | 1048 _{c(OSC)} | | ns |
| | Valid time, \overline{RST} active (all others) | 8 _{t_{c(VCLK)}} | | |

- (1) Specified values do NOT include rise/fall times. For rise and fall timings, see the switching characteristics for output timings versus load capacitance table.
- (2) This parameter is characterized from -40°C to 125°C only.

7.3.3 IO Status During \overline{PORRST}

IO buffer condition during power-on-reset (nPORRST is low): All I/O pins, except nRST, are configured as High-impedance while nPORRST is low and immediately after nPORRST goes high. The FlexRay FRAYTX1 and FRAYTX2 pins are high impedance (high-Z) while nPORRST is low, and are output high at latest 1024 oscillator cycles after nPORRST goes high; the FlexRay FRAYTXEN1 and FRAYTXEN2 pins are high impedance (high-Z) while nPORRST is low, and output high immediately after nPORRST goes high.

IO pullup/pulldown condition during power-on-reset: all internal pullups and pulldowns on input pins are disabled when nPORRST is low, and become active immediately after nPORRST goes high. Pins that are listed with "programmable" have programmable pullups or pulldowns. The default value after reset is listed underneath "programmable" in the following table. The exceptions are nPORRST, nRST, nTRST and TEST pins. The pulls on these pins will be active during power-on-reset.

7.4 TEST Pin Timing

Table 7-8. TEST Pin Timing⁽¹⁾

| NO. | | Description | MIN | MAX | Unit |
|-----|----------------------|--|-----|-----|------|
| | $t_{f(\text{TEST})}$ | Filter time TEST, pulses less than MIN will be filtered out, pulses greater than MAX are guaranteed to enter TEST mode | 10 | 80 | ns |

(1) This parameter is characterized from -40°C to 125°C only.

7.5 DAP - JTAG Scan Interface Timing

7.5.1 JTAG clock specification 12-MHz and 50-pF load on TDO output

Table 7-9. JTAG Scan Interface Timing

| NO. | | | MIN | MAX | Unit |
|-----|-------------------------|---|-----|-----|------|
| | $f_{(TCK)}$ | TCK frequency (at HCLKmax) | | 12 | MHz |
| | $f_{(RTCK)}$ | RTCK frequency (at TCKmax and HCLKmax) | 10 | | MHz |
| 1 | $t_{d(TCK-RTCK)}$ | Delay time, TCK to RTCK | | 20 | ns |
| 2 | $t_{su(TDI/TMS-RTCKr)}$ | Setup time, TDI, TMS before RTCK rise (RTCKr) | 15 | | ns |
| 3 | $t_{h(RTCKr-TDI/TMS)}$ | Hold time, TDI, TMS after RTCKr | 0 | | ns |
| 4 | $t_{h(RTCKf-TDO)}$ | Hold time, TDO after RTCKf | 0 | | ns |
| 5 | $t_{d(RTCKf-TDO)}$ | Delay time, TDO valid after RTCK fall (RTCKf) | | 10 | ns |

Note: The timings in this table are measured with a 50pF and 50µA load. And they are measured at the 50% point, not 20% or 80% point.

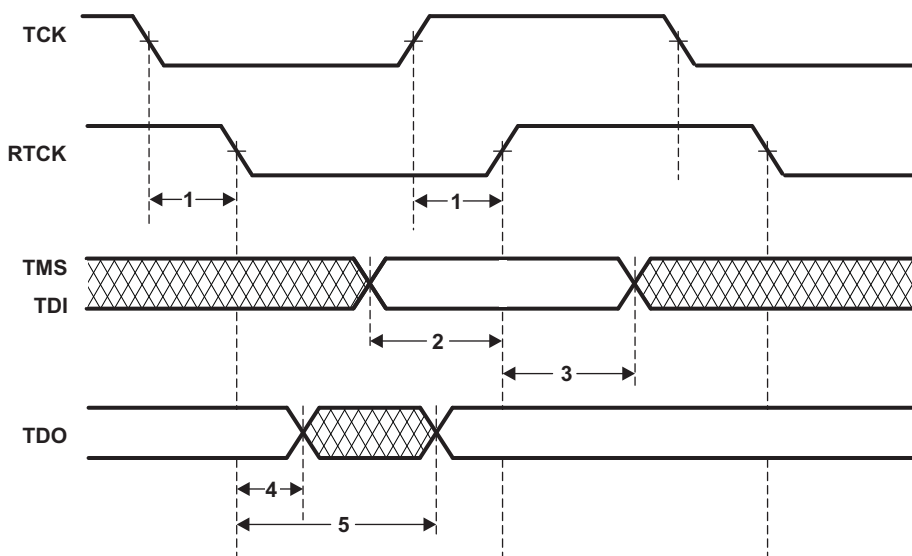


Figure 7-6. JTAG timing

7.6 Output Timings

7.6.1 Switching Characteristics For Output Timings Versus Load Capacitance (C_L)

Table 7-10. Switching Characteristics For Output Timings Versus Load Capacitance (C_L)

| Parameter | | MIN | TYP | MAX | Unit |
|-----------|------------|------------------------|-----|-----|------|
| t_r | 8mA pins | $C_L = 15 \text{ pF}$ | 2.5 | | ns |
| | | $C_L = 50 \text{ pF}$ | 5 | | |
| | | $C_L = 100 \text{ pF}$ | 9 | | |
| | | $C_L = 150 \text{ pF}$ | 12 | | |
| t_f | 8mA pins | $C_L = 15 \text{ pF}$ | 2.5 | | ns |
| | | $C_L = 50 \text{ pF}$ | 5 | | |
| | | $C_L = 100 \text{ pF}$ | 9 | | |
| | | $C_L = 150 \text{ pF}$ | 12 | | |
| t_r | 4mA pins | $C_L = 15 \text{ pF}$ | 7 | | ns |
| | | $C_L = 50 \text{ pF}$ | 13 | | |
| | | $C_L = 100 \text{ pF}$ | 21 | | |
| | | $C_L = 150 \text{ pF}$ | 29 | | |
| t_f | 4mA pins | $C_L = 15 \text{ pF}$ | 7 | | ns |
| | | $C_L = 50 \text{ pF}$ | 13 | | |
| | | $C_L = 100 \text{ pF}$ | 21 | | |
| | | $C_L = 150 \text{ pF}$ | 29 | | |
| t_r | 2mA-z pins | $C_L = 15 \text{ pF}$ | 10 | | ns |
| | | $C_L = 50 \text{ pF}$ | 17 | | |
| | | $C_L = 100 \text{ pF}$ | 25 | | |
| | | $C_L = 150 \text{ pF}$ | 35 | | |
| t_f | 2mA-z pins | $C_L = 15 \text{ pF}$ | 10 | | ns |
| | | $C_L = 50 \text{ pF}$ | 17 | | |
| | | $C_L = 100 \text{ pF}$ | 25 | | |
| | | $C_L = 150 \text{ pF}$ | 35 | | |

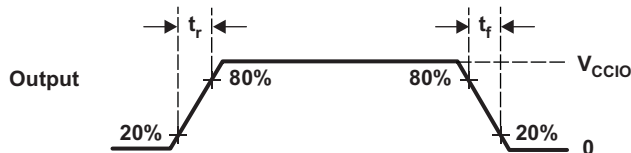


Figure 7-7. CMOS-Level Outputs

7.7 Input Timings

7.7.1 Timing Requirements For Input Timings

Table 7-11. Timing Requirements For Input Timings⁽¹⁾

| | | MIN | MAX | Unit |
|----------|---------------------------|--------------------------|-----|------|
| t_{pw} | Input minimum pulse width | $t_{c(VCLK)} + 10^{(2)}$ | | ns |

- (1) $t_{c(VCLK)}$ = peripheral VBUS clock cycle time = $1 / f_{(VCLK)}$
 (2) The timing shown above is only valid for pin used in GIO mode

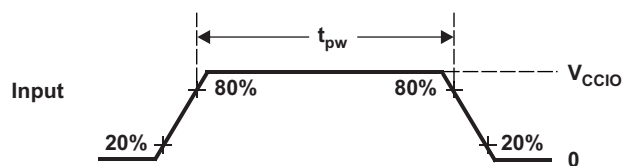


Figure 7-8. CMOS-Level Inputs

7.8 Flash Timings

Table 7-12. Timing Requirements For Program Flash

| | | | MIN | NOM | MAX | Unit |
|--------------------------------------|--|----------------------------------|------|-----|------|---------------|
| $t_{\text{prog}(32\text{-bit})}$ | Full word (32-bit) programming time | | | 33 | 300 | μs |
| $t_{\text{prog}(\text{Total})}$ | 2M-byte programming time ⁽¹⁾ | -40°C to 125°C | | 17 | 74 | s |
| | | 0°C to 60°C, for first 25 cycles | | 17 | 25 | s |
| $t_{\text{prog ECC}(16\text{-bit})}$ | ECC programming time | | | 33 | 300 | μs |
| $t_{\text{prog ECC}(\text{total})}$ | Total ECC bit programming time (256k-byte) | -40°C to 125°C | | 4.3 | 15 | s |
| | | 0°C to 60°C, for first 25 cycles | | 4.3 | 7 | s |
| $t_{\text{erase}(\text{sector})}$ | Sector erase time (including compaction) | -40°C to 125°C | | 2 | 15 | s |
| | | 0°C to 60°C, for first 25 cycles | | 1.5 | 10 | s |
| $t_{\text{erase}(\text{bank})}$ | Bank erase time (including compaction), 0°C to 60°C, for first 25 cycles | Bank 0 | | 7.5 | 20 | s |
| | | Bank 1 | | 5.5 | 12 | s |
| | | Bank 2 | | 5.5 | 12 | s |
| | | Bank 3 | | 5.5 | 12 | s |
| t_{wec} | Write/erase cycles at $T_A = -40$ to 125°C ⁽²⁾ | | | | 1000 | cycles |
| t_{ret} | Data Retention with continuous 150°C ⁽²⁾ | | 1000 | | | hours |

- (1) This programming time includes overhead of state machine, but does not include data transfer time.
- (2) Flash write/erase cycles and data retention specifications are based on a validated implementation of the TI flash API. Non-TI flash API implementation is not supported. For detailed description see the *F035 Flash Validation Procedure (SPNA127)*. The flash memory cells are qualified for data retention greater than 1000 hours at 150°C . Data retention at reduced temperatures can be estimated based on an Arrhenius model with activation energy of 1 eV.

7.9 SPI Master Mode Timing Parameters

7.9.1 SPI Master Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)

Table 7-13. SPI Master Mode External Timing Parameters⁽¹⁾⁽²⁾⁽³⁾

| NO. | | | MIN | MAX | Unit |
|------------------|----------------------|--|--|---|------|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK ⁽⁴⁾ | 50 | $256t_{c(VCLK)}$ | ns |
| 2 ⁽⁵⁾ | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - 3 - t_r$ | $0.5t_{c(SPC)M} + 5$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - 3 - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| 3 ⁽⁵⁾ | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - 3 - t_f$ | $0.5t_{c(SPC)M} + 5$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - 3 - t_r$ | $0.5t_{c(SPC)M} + 5$ | |
| 4 ⁽⁵⁾ | $t_{d(SIMO-SPCL)M}$ | Delay time, SPISIMO valid before SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - 10$ | | ns |
| | $t_{d(SIMO-SPCH)M}$ | Delay time, SPISIMO valid before SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - 10$ | | |
| 5 ⁽⁵⁾ | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - t_{f(SPC)} - 7$ | | ns |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - t_{r(SPC)} - 7$ | | |
| 6 ⁽⁵⁾ | $t_{su(SOMI-SPCL)M}$ | Setup time, SPISOMI before SPICLK low (clock polarity = 0) | $t_{f(SPC)}$ | | ns |
| | $t_{su(SOMI-SPCH)M}$ | Setup time, SPISOMI before SPICLK high (clock polarity = 1) | $t_{r(SPC)} + 4$ | | |
| 7 ⁽⁵⁾ | $t_{h(SPCL-SOMI)M}$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0) | 10 | | ns |
| | $t_{h(SPCH-SOMI)M}$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1) | 10 | | |
| 8 ⁽⁶⁾ | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high, assumes that SPInENA is low at t_{SPIENA} (clock polarity = 0) | $(C2TDELAY + CSHOLD + 2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 9$ | $(C2TDELAY + CSHOLD + 2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5$ | ns |
| | | Setup time CS active until SPICLK low, assumes that SPInENA is low at t_{SPIENA} (clock polarity = 1) | $(C2TDELAY + CSHOLD + 2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 9$ | $(C2TDELAY + CSHOLD + 2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5$ | ns |
| 9 ⁽⁶⁾ | $t_{T2CDELAY}$ | Hold time SPICLK low until CS inactive (clock polarity = 0) | $0.5 * t_{c(SPC)M} + T2CDELAY * t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 5$ | $0.5 * t_{c(SPC)M} + T2CDELAY * t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 10$ | ns |
| | | Hold time SPICLK high until CS inactive (clock polarity = 1) | $0.5 * t_{c(SPC)M} + T2CDELAY * t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} - 5$ | $0.5 * t_{c(SPC)M} + T2CDELAY * t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 10$ | ns |
| 10 | t_{SPIENA} | SPIENAn Sample point | $C2TDELAY * t_{c(VCLK)} - t_{f(SPICS)} - 20$ | $C2TDELAY * t_{c(VCLK)}$ | ns |
| 11 | $t_{SPIENAW}^{(7)}$ | SPIENAn Sample point from write to buffer | | $(C2TDELAY + 2) * t_{c(VCLK)}$ | ns |

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.

(2) $t_{c(VCLK)}$ = interface clock cycle time = $1 / f(VCLK)$

(3) For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

(4) When the SPI is in Master mode, the following must be true:

For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(VCLK)} \geq 50$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.

For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 50$ ns. The external load on the SPICLK pin must be less than 60pF.

(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

(6) C2TDELAY and T2CDELAY are programmed in the SPIDELAY register

(7) Parameters characterized from -40°C to 125°C only.

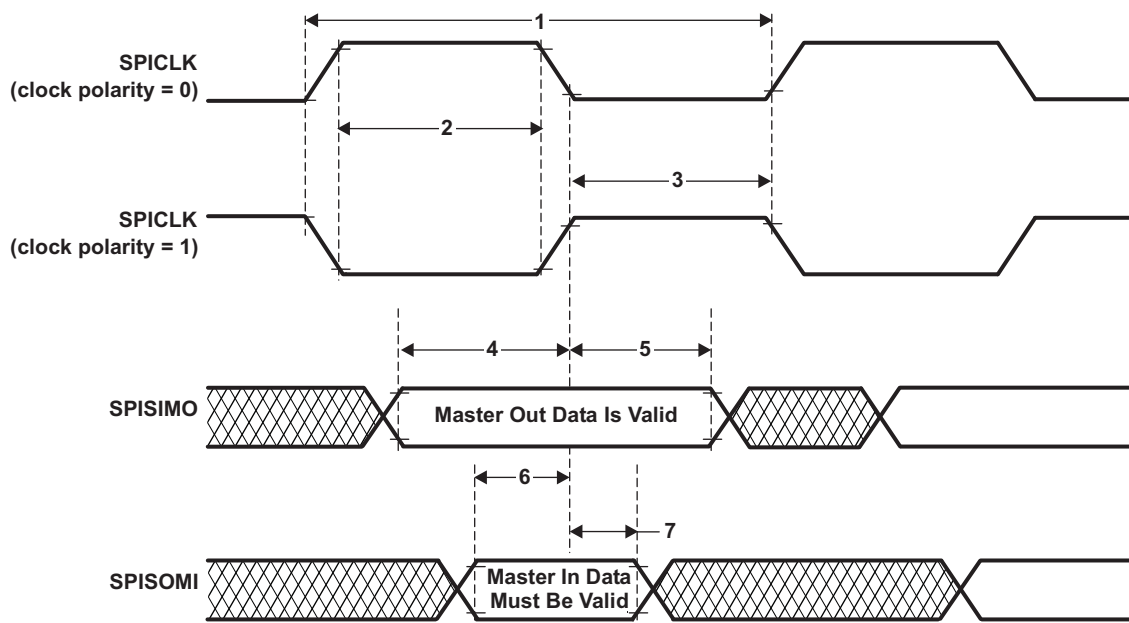


Figure 7-9. SPI Master Mode External Timing (CLOCK PHASE = 0)

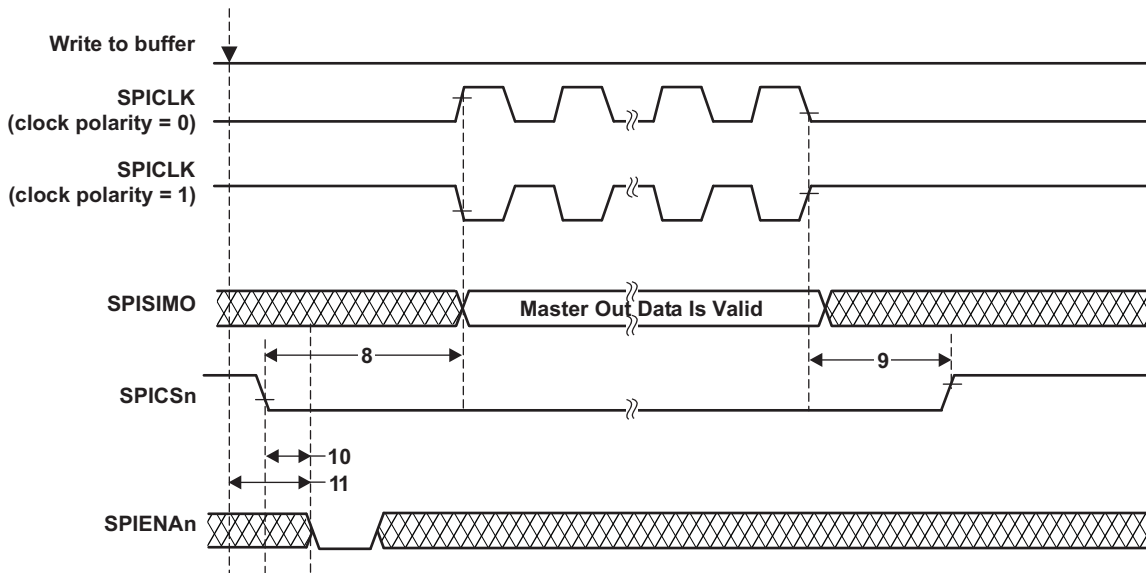


Figure 7-10. SPI Master Mode Chip Select timing (CLOCK PHASE = 0)

7.9.2 SPI Master Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)

Table 7-14. SPI Master Mode External Timing Parameters⁽¹⁾⁽²⁾⁽³⁾

| NO. | | | MIN | MAX | Unit |
|------------------|----------------------|--|---|---|------|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK ⁽⁴⁾ | 50 | $256t_{c(VCLK)}$ | ns |
| 2 ⁽⁵⁾ | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - 3 - t_r$ | $0.5t_{c(SPC)M} + 5$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - 3 - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| 3 ⁽⁵⁾ | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - 3 - t_r$ | $0.5t_{c(SPC)M} + 5$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - 3 - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| 4 ⁽⁵⁾ | $t_{d(SIMO-SPCH)M}$ | Delay time, SPICLK high after SPISIMO data valid (clock polarity = 0) | $0.5t_{c(SPC)M} - 10$ | | ns |
| | $t_{d(SIMO-SPCL)M}$ | Delay time, SPICLK low after SPISIMO data valid (clock polarity = 1) | $0.5t_{c(SPC)M} - 10$ | | |
| 5 ⁽⁵⁾ | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - t_r(SPC) - 7$ | | ns |
| | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - t_f(SPC) - 7$ | | |
| 6 ⁽⁵⁾ | $t_{su(SOMI-SPCH)M}$ | Setup time, SPISOMI before SPICLK high (clock polarity = 0) | $t_r(SPC) + 4$ | | ns |
| | $t_{su(SOMI-SPCL)M}$ | Setup time, SPISOMI before SPICLK low (clock polarity = 1) | $t_f(SPC)$ | | |
| 7 ⁽⁵⁾ | $t_{v(SPCH-SOMI)M}$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0) | 10 | | ns |
| | $t_{v(SPCL-SOMI)M}$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1) | 10 | | |
| 8 ⁽⁶⁾ | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high, assumes that SPInENA is low at t_{SPIENA} (clock polarity = 0) | $(C2TDELAY + CSHOLD + 2) * t_{c(VCLK)} + 0.5 * t_{c(SPC)M} - t_f(SPICS) + t_r(SPC) - 9$ | $(C2TDELAY + CSHOLD + 2) * t_{c(VCLK)} + 0.5 * t_{c(SPC)M} - t_f(SPICS) + t_r(SPC) + 5$ | ns |
| | | Setup time CS active until SPICLK low, assumes that SPInENA is low at t_{SPIENA} (clock polarity = 1) | $(C2TDELAY + CSHOLD + 2) * t_{c(VCLK)} + 0.5 * t_{c(SPC)M} - t_f(SPICS) + t_r(SPC) - 9$ | $(C2TDELAY + CSHOLD + 2) * t_{c(VCLK)} + 0.5 * t_{c(SPC)M} - t_f(SPICS) + t_r(SPC) + 5$ | ns |
| 9 ⁽⁶⁾ | $t_{T2CDELAY}$ | Hold time SPICLK low until CS inactive (clock polarity = 0) | $T2CDELAY * t_{c(VCLK)} + t_{c(VCLK)} - t_r(SPC) + t_r(SPICS) - 5$ | $T2CDELAY * t_{c(VCLK)} + t_{c(VCLK)} - t_r(SPC) + t_r(SPICS) + 10$ | ns |
| | | Hold time SPICLK high until CS inactive (clock polarity = 1) | $T2CDELAY * t_{c(VCLK)} + t_{c(VCLK)} - t_r(SPC) + t_r(SPICS) - 5$ | $T2CDELAY * t_{c(VCLK)} + t_{c(VCLK)} - t_r(SPC) + t_r(SPICS) + 10$ | ns |
| 10 | t_{SPIENA} | SPIENAn Sample Point | $C2TDELAY * t_{c(VCLK)} - t_f(SPICS) - 20$ | $C2TDELAY * t_{c(VCLK)}$ | ns |
| 11 | $t_{SPIENAW}$ | SPIENAn Sample point from write to buffer | | $(C2TDELAY + 2) * t_{c(VCLK)}$ | ns |

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.

(2) $t_{c(VCLK)}$ = interface clock cycle time = $1 / f(VCLK)$

(3) For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

(4) When the SPI is in Master mode, the following must be true:

For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(VCLK)} \geq 50$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.

For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 50$ ns. The external load on the SPICLK pin must be less than 60pF.

(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

(6) C2TDELAY and T2CDELAY are programmed in the SPIDELAY register

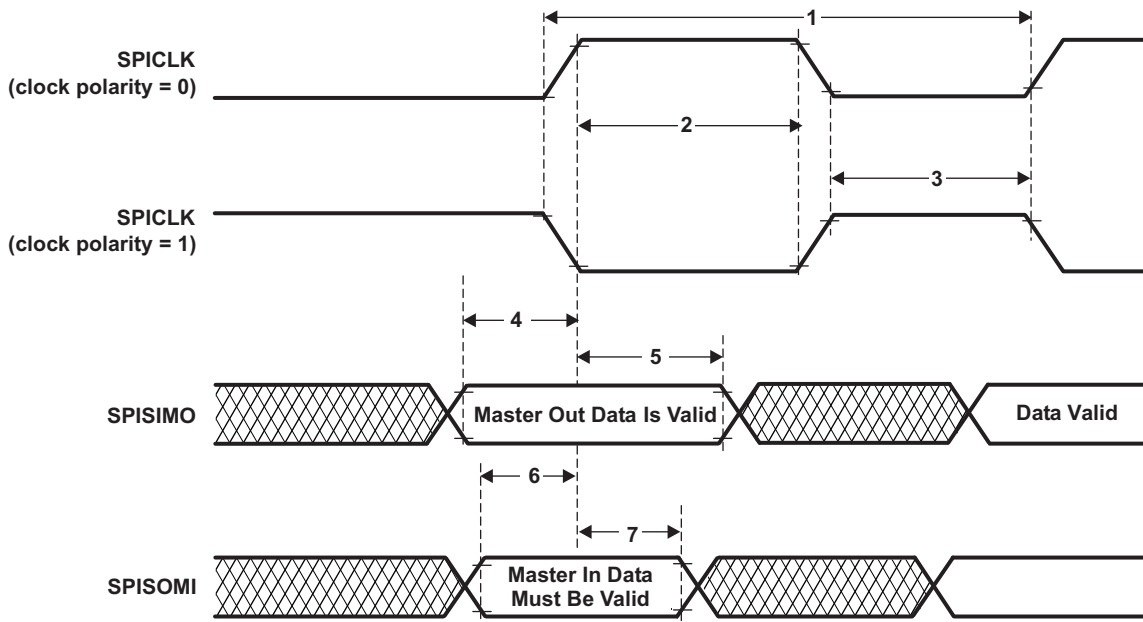


Figure 7-11. SPI Master Mode External Timing (CLOCK PHASE = 1)

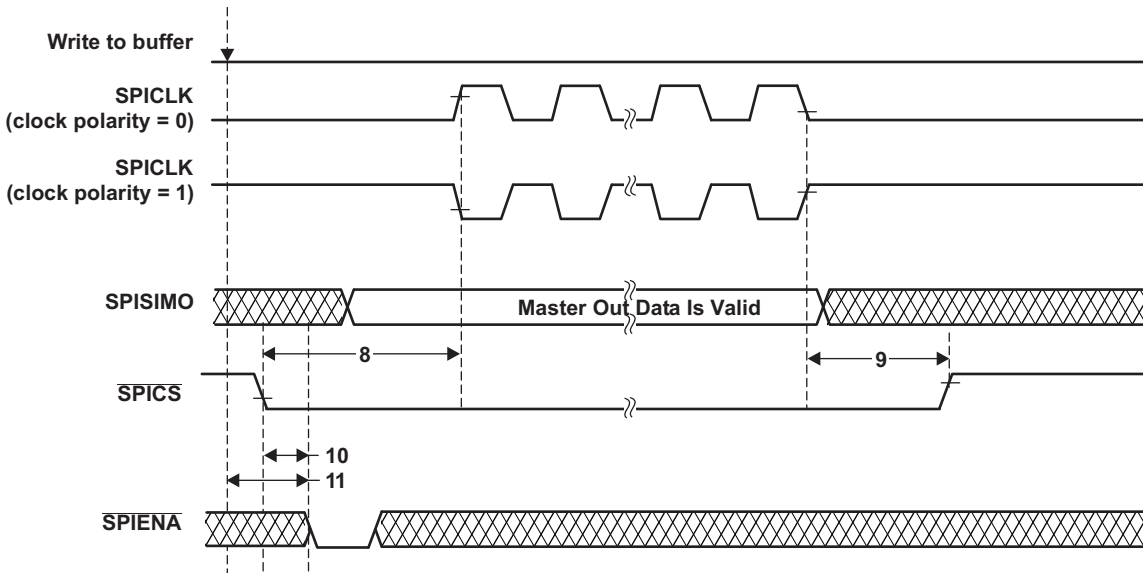


Figure 7-12. SPI Master Mode Chip Select timing (CLOCK PHASE = 1)

7.10 SPI Slave Mode Timing Parameters

7.10.1 SPI Slave Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = input, SPISIMO = input, and SPISOMI = output)

Table 7-15. SPI Slave Mode External Timing Parameters ⁽¹⁾⁽²⁾⁽³⁾

| NO. | | | MIN | MAX | Unit |
|------------------|----------------------|---|------------------|-------------------------------------|------|
| 1 | $t_{c(SPC)S}$ | Cycle time, SPICLK ⁽⁴⁾ | 90 | | ns |
| 2 ⁽⁵⁾ | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high(clock polarity = 0) | 30 | | ns |
| | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low(clock polarity = 1) | 30 | | |
| 3 ⁽⁵⁾ | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low(clock polarity = 0) | 30 | | ns |
| | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high(clock polarity = 1) | 30 | | |
| 4 ⁽⁵⁾ | $t_{d(SPCH-SOMI)S}$ | Delay time, SPISOMI valid after SPICLK high (clock polarity = 0) | | $t_{f(SOMI)} + 15$ | ns |
| | $t_{d(SPCL-SOMI)S}$ | Delay time, SPISOMI valid after SPICLK low (clock polarity = 1) | | $t_{f(SOMI)} + 15$ | |
| 5 ⁽⁵⁾ | $t_{v(SPCH-SOMI)S}$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0) | 0 | | ns |
| | $t_{v(SPCL-SOMI)S}$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1) | 0 | | |
| 6 ⁽⁵⁾ | $t_{su(SIMO-SPCL)S}$ | Setup time, SPISIMO before SPICLK low(clock polarity = 0) | 4 | | ns |
| | $t_{su(SIMO-SPCH)S}$ | Setup time, SPISIMO before SPICLK high(clock polarity = 1) | 4 | | |
| 7 ⁽⁵⁾ | $t_{h(SPCL-SIMO)S}$ | Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0) | 6 | | ns |
| | $t_{h(SPCH-SIMO)S}$ | Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1) | 6 | | |
| 8 | $t_{d(SPCL-SENAH)S}$ | Delay time, SPIENAn high after last SPICLK low (clock polarity = 0) | $1.5t_{c(VCLK)}$ | $2.5t_{c(VCLK)} + t_{f(ENAn)} + 26$ | ns |
| | $t_{d(SPCH-SENAH)S}$ | Delay time, SPIENAn high after last SPICLK high (clock polarity = 1) | $1.5t_{c(VCLK)}$ | $2.5t_{c(VCLK)} + t_{f(ENAn)} + 26$ | |
| 9 | $t_{d(SCSL-SENAL)S}$ | Delay time, SPIENAn low after SPICLK low (if new data has been written to the SPI buffer) | $t_{f(ENAn)}$ | $t_{c(VCLK)} + t_{f(ENAn)} + 18$ | ns |

- (1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) $t_{c(VCLK)}$ = interface clock cycle time = $1 / f_{(VCLK)}$
(3) For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
(4) When the SPI is in Slave mode, the following must be true:
 $t_{c(SPC)S} > 2t_{c(VCLK)}$ and $t_{c(SPC)S} \geq 90$ ns.
 $t_{w(SPCH)S} > t_{c(VCLK)}$ and $t_{w(SPCL)S} > t_{c(VCLK)}$.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

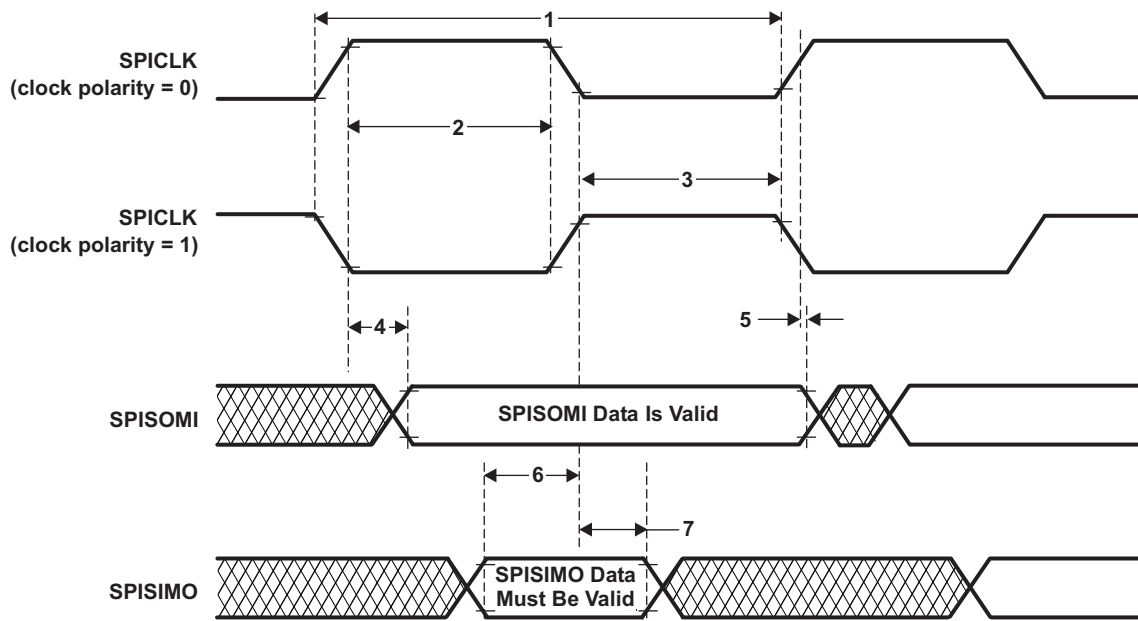


Figure 7-13. SPI Slave Mode External Timing (CLOCK PHASE = 0)

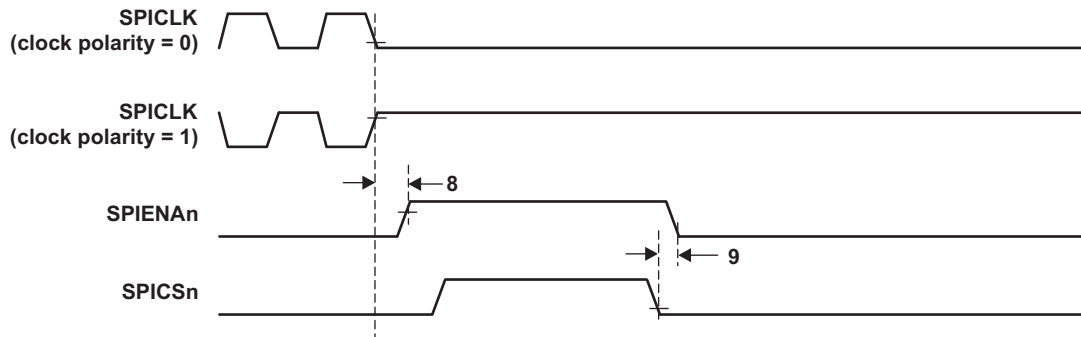


Figure 7-14. SPI Slave Mode Enable Timing (CLOCK PHASE = 0)

7.10.2 SPI Slave Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = input, SPISIMO = input, and SPISOMI = output)

Table 7-16. SPI Slave Mode External Timing Parameters⁽¹⁾⁽²⁾⁽³⁾

| NO. | | | MIN | MAX | Unit |
|------------------|----------------------|---|------------------|----------------------------------|------|
| 1 | $t_{c(SPC)S}$ | Cycle time, SPICLK ⁽⁴⁾ | 90 | | ns |
| 2 ⁽⁵⁾ | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high (clock polarity = 0) | 30 | | ns |
| | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low (clock polarity = 1) | 30 | | |
| 3 ⁽⁵⁾ | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low (clock polarity = 0) | 30 | | ns |
| | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high (clock polarity = 1) | 30 | | |
| 4 ⁽⁵⁾ | $t_{d(SOMI-SPCL)S}$ | Delay time, SPISOMI data valid after SPICLK low (clock polarity = 0) | | $t_{r(SOMI)}+15$ | ns |
| | $t_{d(SOMI-SPCH)S}$ | Delay time, SPISOMI data valid after SPICLK high (clock polarity = 1) | | $t_{r(SOMI)}+15$ | |
| 5 ⁽⁵⁾ | $t_{v(SPCL-SOMI)S}$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0) | 0 | | ns |
| | $t_{v(SPCH-SOMI)S}$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1) | 0 | | |
| 6 ⁽⁵⁾ | $t_{su(SIMO-SPCH)S}$ | Setup time, SPISIMO before SPICLK high (clock polarity = 0) | 4 | | ns |
| | $t_{su(SIMO-SPCL)S}$ | Setup time, SPISIMO before SPICLK low (clock polarity = 1) | 4 | | |
| 7 ⁽⁵⁾ | $t_{h(SPCH-SIMO)S}$ | Hold time, SPISIMO data valid after SPICLK high (clock polarity = 0) | 6 | | ns |
| | $t_{h(SPCL-SIMO)S}$ | Hold time, SPISIMO data valid after SPICLK low (clock polarity = 1) | 6 | | |
| 8 | $t_{d(SPCH-SENAH)S}$ | Delay time, SPIENAn high after last SPICLK high (clock polarity = 0) | $1.5t_{c(VCLK)}$ | $2.5t_{c(VCLK)}+t_{r(ENAn)}+ 26$ | ns |
| | $t_{d(SPCL-SENAH)S}$ | Delay time, SPIENAn high after last SPICLK low (clock polarity = 1) | $1.5t_{c(VCLK)}$ | $2.5t_{c(VCLK)}+t_{r(ENAn)}+ 26$ | |
| 9 | $t_{d(SCSL-SENAL)S}$ | Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer) | $t_{f(ENAn)}$ | $t_{c(VCLK)} + t_{f(ENAn)}+ 18$ | ns |
| 10 | $t_{d(SCSL-SOMI)S}$ | Delay time, SOMI valid after SPICSn low (if new data has been written to the SPI buffer) | $t_{c(VCLK)}$ | $2t_{c(VCLK)} + t_{r(SOMI)}+ 20$ | ns |

- (1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
- (2) $t_{c(VCLK)}$ = interface clock cycle time = $1 / f_{(VCLK)}$
- (3) For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
- (4) When the SPI is in Slave mode, the following must be true:
 $t_{c(SPC)S} > 2t_{c(VCLK)}$ and $t_{c(SPC)S} \geq 90$ ns.
 $t_{w(SPCH)S} > t_{c(VCLK)}$ and $t_{w(SPCL)S} > t_{c(VCLK)}$.
- (5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

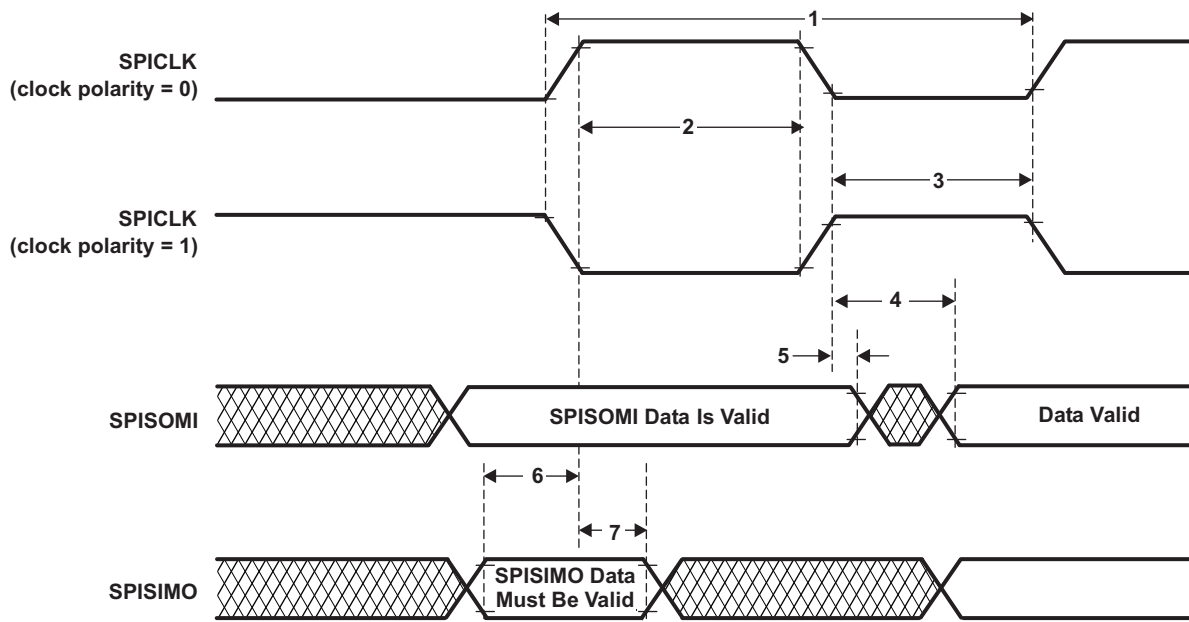


Figure 7-15. SPI Slave Mode External Timing (CLOCK PHASE = 1)

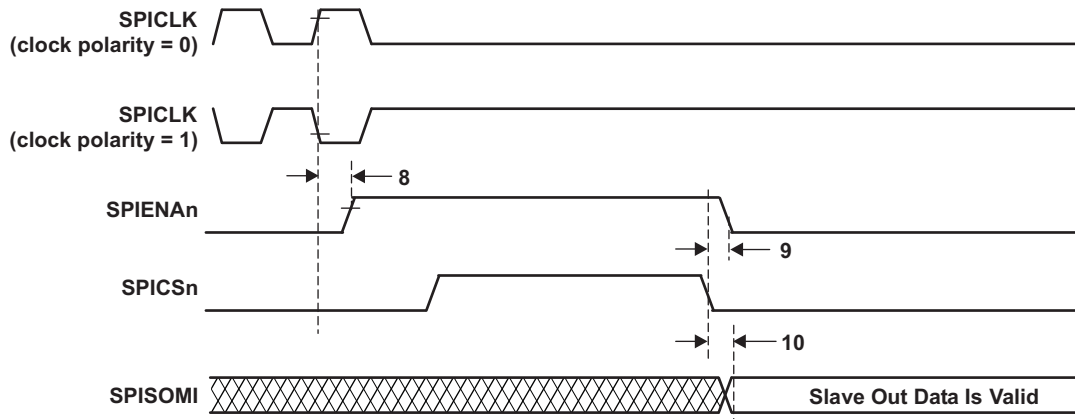


Figure 7-16. SPI Slave Mode Enable Timing (CLOCK PHASE = 1)

7.11 CAN Controller Mode Timings

7.11.1 Dynamic Characteristics For The CANnTX And CANnRX Pins

Table 7-17. Dynamic Characteristics For The CANnTX And CANnRX Pins⁽¹⁾

| Parameter | | MIN | MAX | Unit |
|----------------------|--|-----|-----|------|
| $t_d(\text{CANnTX})$ | Delay time, transmit shift register to CANnTX pin ⁽²⁾ | | 15 | ns |
| $t_d(\text{CANnRX})$ | Delay time, CANnRX pin to receive shift register | | 5 | ns |

(1) These parameters are characterized from -40°C to 125°C only.

(2) These values do not include rise/fall times of the output buffer.

7.12 SCI/LIN Mode Timings

At 100MHz Peripheral Clock, 3.125 Mb/s is the Max SCI Baud Rate achievable.

7.13 FlexRay Controller Mode Timings

7.13.1 Jitter Timing

Table 7-18. Jitter Timing⁽¹⁾

| Parameter | | MIN | MAX | Unit |
|-------------------|--|-------|--------|------|
| t_{Tx1bit} | clock jitter and signal symmetry | 98 | 102 | ns |
| $t_{Tx10bit}$ | FlexRay BSS (byte start sequence) to BSS | 999 | 1001 | ns |
| $t_{Tx10bitAvg}$ | average over 10000 samples | 999.5 | 1000.5 | ns |
| $t_{RxAsymDelay}$ | delay difference between rise and fall from Rx pin to sample point in FlexRay core | - | 2.5 | ns |

(1) Parameters characterized from -40°C to 125°C only.

7.14 EMIF Timings

Table 7-19. EMIF Read/Write Mode Switching Characteristics⁽¹⁾⁽²⁾

| NO | Parameter | Description | MIN | MAX | Unit |
|-------------------------|--------------------------------|--|--|--|------|
| Reads and Writes | | | | | |
| 1 | $t_d(\text{TURNAROUND})^{(3)}$ | Turn around time | $(TA + 1) * E - t_{r(\text{CS})} - 2$ | $(TA + 1) * E - t_{r(\text{CS})} + 3$ | ns |
| Reads | | | | | |
| 2 | $t_c(\text{EMRCYCLE})$ | EMIF read cycle time | $(RS + RST + RH + TA + 4) * E - t_{r(\text{CS})} - 3$ | $(RS + RST + RH + TA + 4) * E - t_{r(\text{CS})} + 3$ | ns |
| 3 | $t_{su}(\text{EMCSL-EMOEL})$ | Output setup time, $\overline{\text{EMIFCS}}[3:0]$ low to $\overline{\text{EMIFOE}}$ low (SS=0) | $(RS + 1) * E - t_{r(\text{CS})} + t_{r(\text{OE})} - 5$ | $(RS + 1) * E - t_{r(\text{CS})} + t_{r(\text{OE})} + 5$ | ns |
| | | Output setup time, $\overline{\text{EMIFCS}}[3:0]$ low to $\overline{\text{EMIFOE}}$ low (SS=1) | $- t_{r(\text{CS})} + t_{r(\text{OE})} - 5$ | $- t_{r(\text{CS})} + t_{r(\text{OE})} + 5$ | ns |
| 4 | $t_h(\text{EMOEEH-EMCSH})$ | Output hold time, $\overline{\text{EMIFOE}}$ high to $\overline{\text{EMIFCS}}[3:0]$ high (SS=0) | $(RH + 1) * E - t_{r(\text{OE})} + t_{r(\text{CS})} - 4$ | $(RH + 1) * E - t_{r(\text{OE})} + t_{r(\text{CS})} + 6$ | ns |
| | | Output hold time, $\overline{\text{EMIFOE}}$ high to $\overline{\text{EMIFCS}}[3:0]$ high (SS=1) | $- t_{r(\text{OE})} + t_{r(\text{CS})} - 4$ | $- t_{r(\text{OE})} + t_{r(\text{CS})} + 6$ | ns |
| 5 | $t_{su}(\text{EMBAV-EMOEL})$ | Output setup time, EMIFBADD[1:0] valid to $\overline{\text{EMIFOE}}$ low | $(RS + 1) * E - t_{r(\text{AD})} + t_{r(\text{OE})} - 5$ | $(RS + 1) * E - t_{r(\text{AD})} + t_{r(\text{OE})} + 5$ | ns |
| 6 | $t_h(\text{EMOEEH-EMBAIV})$ | Output hold time, $\overline{\text{EMIFOE}}$ high to EMIFBADD[1:0] invalid | $(RH + 1) * E - t_{r(\text{OE})} - 5$ | $(RH + 1) * E - t_{r(\text{OE})} + 5$ | ns |
| 7 | $t_{su}(\text{EMAV-EMOEL})$ | Output setup time, EMIFADD[21:0] valid to $\overline{\text{EMIFOE}}$ low | $(RS + 1) * E - t_{r(\text{AD})} + t_{r(\text{OE})} - 6$ | $(RS + 1) * E - t_{r(\text{AD})} + t_{r(\text{OE})} + 6$ | ns |
| 8 | $t_h(\text{EMOEEH-EMAIV})$ | Output hold time, $\overline{\text{EMIFOE}}$ high to EMIFADD[21:0] invalid | $(RH + 1) * E - t_{r(\text{OE})} - 5$ | $(RH + 1) * E - t_{r(\text{OE})} + 6$ | ns |
| 9 | $t_w(\text{EMOEL})^{(3)}$ | $\overline{\text{EMIFOE}}$ active low width | $(RST + 1) * E - t_{r(\text{OE})} - 1$ | $(RST + 1) * E - t_{r(\text{OE})} + 0$ | ns |
| 10 | $t_{su}(\text{EMDV-EMOEEH})$ | Setup time, EMIFD[15:0] valid before $\overline{\text{EMIFOE}}$ high | $t_{r(\text{OE})} + 9$ | | ns |
| 11 | $t_h(\text{EMOEEH-EMDV})$ | Hold time, EMIFD[15:0] valid after $\overline{\text{EMIFOE}}$ high | $- t_{r(\text{OE})} - 3$ | | |
| Writes | | | | | |
| 12 | $t_c(\text{EMWCYCLE})$ | EMIF write cycle time | $(WS + WST + WH + TA + 4) * E - t_{r(\text{CS})} - 3$ | $(WS + WST + WH + TA + 4) * E - t_{r(\text{CS})} + 2$ | ns |
| 13 | $t_{su}(\text{EMCSL-EMWEL})$ | Output setup time, $\overline{\text{EMIFCS}}[3:0]$ low to $\overline{\text{EMIFWE}}$ low (SS=0) | $(WS + 1) * E - t_{r(\text{CS})} + t_{r(\text{WE})} - 5$ | $(WS + 1) * E - t_{r(\text{CS})} + t_{r(\text{WE})} + 5$ | ns |
| | | Output setup time, $\overline{\text{EMIFCS}}[3:0]$ low to $\overline{\text{EMIFWE}}$ low (SS=1) | $- t_{r(\text{CS})} + t_{r(\text{WE})} - 5$ | $- t_{r(\text{CS})} + t_{r(\text{WE})} + 5$ | ns |
| 14 | $t_h(\text{EMWEH-EMCSH})$ | Output hold time, $\overline{\text{EMIFWE}}$ high to $\overline{\text{EMIFCS}}[3:0]$ high (SS=0) | $(WH + 1) * E - t_{r(\text{WE})} + t_{r(\text{CS})} - 4$ | $(WH + 1) * E - t_{r(\text{WE})} + t_{r(\text{CS})} + 5$ | ns |
| | | Output hold time, $\overline{\text{EMIFWE}}$ high to $\overline{\text{EMIFCS}}[3:0]$ high (SS=1) | $- t_{r(\text{WE})} + t_{r(\text{CS})} - 4$ | $- t_{r(\text{WE})} + t_{r(\text{CS})} + 5$ | ns |
| 15 | $t_{su}(\text{EMBAV-EMWEL})$ | Output setup time, EMIFBADD[1:0] valid to $\overline{\text{EMIFWE}}$ low | $(WS + 1) * E - t_{r(\text{AD})} + t_{r(\text{WE})} - 5$ | $(WS + 1) * E - t_{r(\text{AD})} + t_{r(\text{WE})} + 5$ | ns |
| 16 | $t_h(\text{EMWEH-EMBAIV})$ | Output hold time, $\overline{\text{EMIFWE}}$ high to EMIBADD[1:0] invalid | $(WH + 1) * E - t_{r(\text{WE})} - 5$ | $(WH + 1) * E - t_{r(\text{WE})} + 5$ | ns |
| 17 | $t_{su}(\text{EMAV-EMWEL})$ | Output setup time, EMIFADD[21:0] valid to $\overline{\text{EMIFWE}}$ low | $(WS + 1) * E - t_{r(\text{AD})} + t_{r(\text{WE})} - 6$ | $(WS + 1) * E - t_{r(\text{AD})} + t_{r(\text{WE})} + 6$ | ns |

(1) RS = Read setup, RST = Read Strobe, RH = Read Hold, WS = Write Setup, WST = Write Strobe, WH = Write Hold, TA = Turn Around, SS = Strobe Select Mode

(2) E = VCLK period in ns.

(3) Parameters characterized from -40°C to 125°C only.

Table 7-19. EMIF Read/Write Mode Switching Characteristics⁽¹⁾⁽²⁾ (continued)

| NO | Parameter | Description | MIN | MAX | Unit |
|----|----------------------|---|---|---|------|
| 18 | $t_{h(EMWEH-EMAIV)}$ | Output hold time, \overline{EMIFWE} high to EMIFADD[21:0] invalid | $(WH + 1) * E - t_{r(WE)} - 5$ | $(WH + 1) * E - t_{r(WE)} + 6$ | ns |
| 19 | $t_{w(EMWEL)}^{(1)}$ | \overline{EMIFWE} active low width | $(WST + 1) * E - t_{r(WE)} - 1$ | $(WST + 1) * E - t_{r(WE)} + 1$ | |
| 20 | $t_{su(EMDV-ENWEL)}$ | Output setup time, EMIFD[15:0] valid to \overline{EMIFWE} low | $(WS + 1) * E - t_{rf(DA)} + t_{r(WE)} - 6$ | $(WS + 1) * E - t_{rf(DA)} + t_{r(WE)} + 5$ | ns |
| 21 | $t_{h(EMWEH-EMDIV)}$ | Output hold time, EMIFD[15:0] valid after \overline{EMIFWE} high | $(WH + 1) * E - t_{r(WE)} - 5$ | $(WH + 1) * E - t_{r(WE)} + 5$ | ns |

(1) Parameters characterized from -40°C to 125°C only.

7.14.1 Read Timing (Asynchronous RAM)

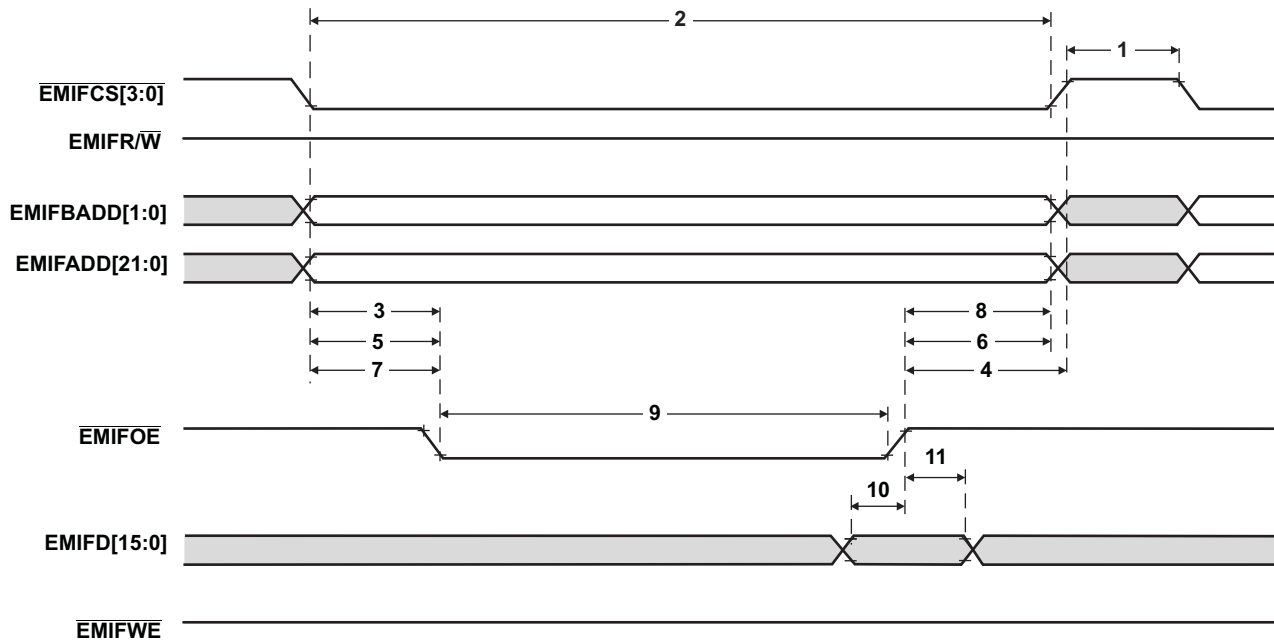


Figure 7-17. Asynchronous Memory Read Timing for EMIF

7.14.2 Write Timing (Asynchronous RAM)

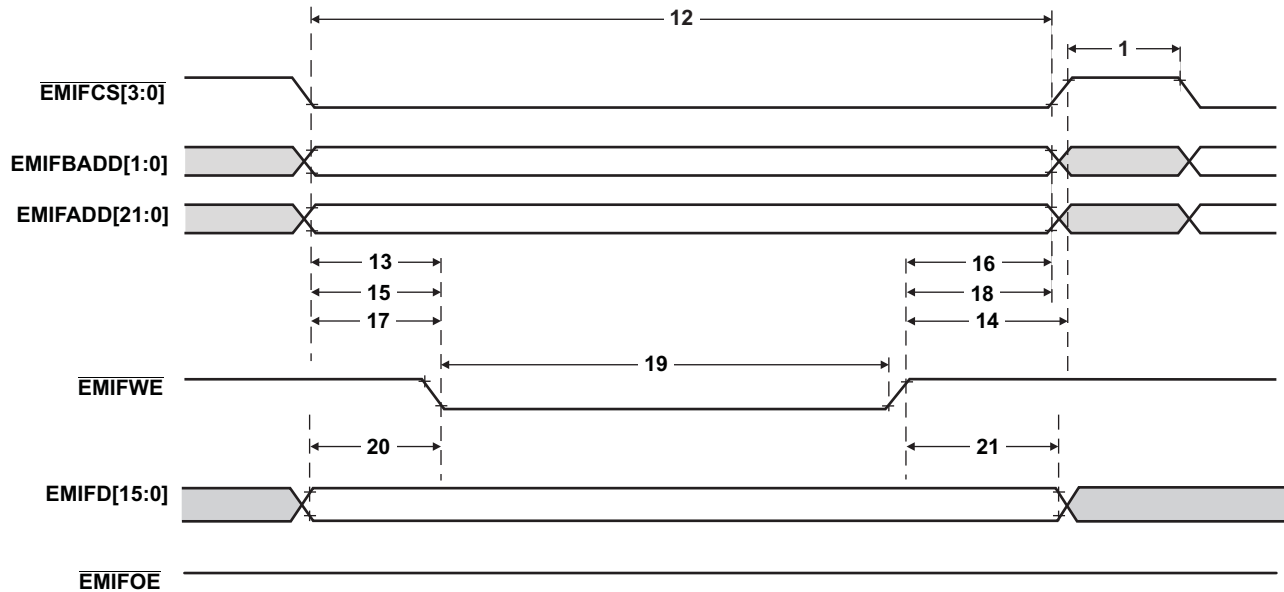


Figure 7-18. Asynchronous Memory Write Timing for EMIF

7.15 ETM Timings

7.15.1 ETMTRACECLK Timing

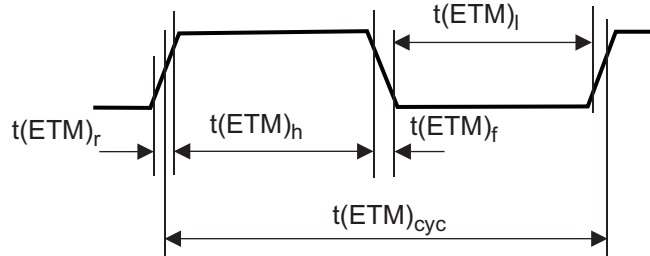


Figure 7-19. ETMTRACECLK Timing

Table 7-20. ETMTRACECLK Timing

| Parameter | Minimum | Maximum | Description |
|------------------------------|---------|---------|--------------------------|
| $f(\text{ETM})_{\text{cyc}}$ | | 40MHz | Clock frequency |
| $t(\text{ETM})_{\text{cyc}}$ | 25ns | | Clock period |
| $t(\text{ETM})_l$ | 2ns | | Low pulse width |
| $t(\text{ETM})_h$ | 2ns | | High pulse width |
| $t(\text{ETM})_r$ | 3ns | | Clock and data rise time |
| $t(\text{ETM})_f$ | 3ns | | Clock and data fall time |

7.15.2 ETMDATA Timing

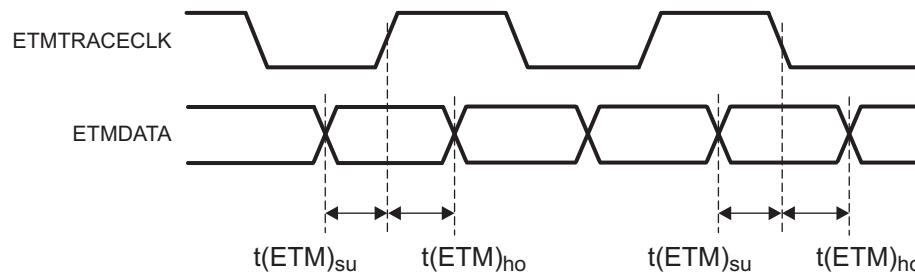


Figure 7-20. ETMDATA Timing

Table 7-21. ETMDATA Timing

| Parameter | Typical | Description |
|-----------------------------|---------|-----------------|
| $t(\text{ETM})_{\text{su}}$ | 2.5ns | Data setup time |
| $t(\text{ETM})_{\text{ho}}$ | 1.5ns | Data hold time |

Note: The timings in this table are measured with a 50pF and 50μA load. And they are measured at the 50% point, not 20% or 80% point. 'Typical' means 25°C and nominal voltage.

7.16 RTP Timings

7.16.1 RTPCLK Timing

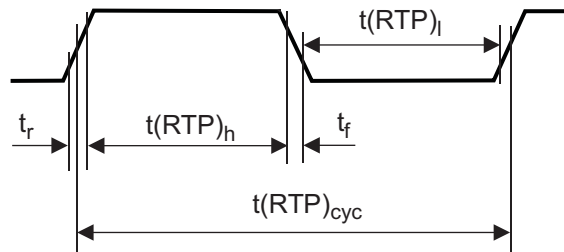


Figure 7-21. RTPCLK Timing

Table 7-22. RTPCLK Timing

| Parameter | Minimum | Description |
|------------------------------|--|---|
| $t(\text{RTP})_{\text{cyc}}$ | 10 ns | Clock period (depending on HCLK divide ratio) |
| $t(\text{RTP})_h$ | $(t(\text{RTP})_{\text{cyc}}/2) - ((t_r+t_f)/2) - 1.5$ | High pulse width (depending on HCLK divide ratio and load on pin) |
| $t(\text{RTP})_l$ | $(t(\text{RTP})_{\text{cyc}}/2) - ((t_r+t_f)/2) - 1.5$ | Low pulse width (depending on HCLK divide ratio and load on pin) |

7.16.2 RTPDATA Timing

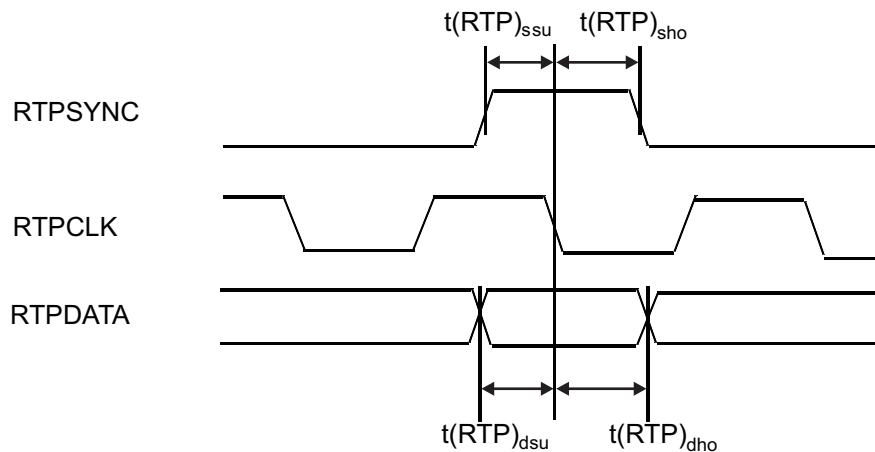


Figure 7-22. RTPDATA Timing

Table 7-23. RTPDATA Timing

| Parameter | Minimum | Description |
|------------------------------|---|-----------------|
| $t(\text{RTP})_{\text{dsu}}$ | $0.5 t(\text{RTP})_{\text{cyc}} - 3\text{ns}$ | Data setup time |
| $t(\text{RTP})_{\text{dho}}$ | $0.5 t(\text{RTP})_{\text{cyc}} - 2\text{ns}$ | Data hold time |
| $t(\text{RTP})_{\text{ssu}}$ | $0.5 t(\text{RTP})_{\text{cyc}} - 3\text{ns}$ | SYNC setup time |
| $t(\text{RTP})_{\text{sho}}$ | $0.5 t(\text{RTP})_{\text{cyc}} - 2\text{ns}$ | SYNC hold time |

Note: The timings in this table are measured with a 50pF and 50μA load. And they are measured at the 50% point, not 20% or 80% point.

7.16.3 RTPENABLE Timing

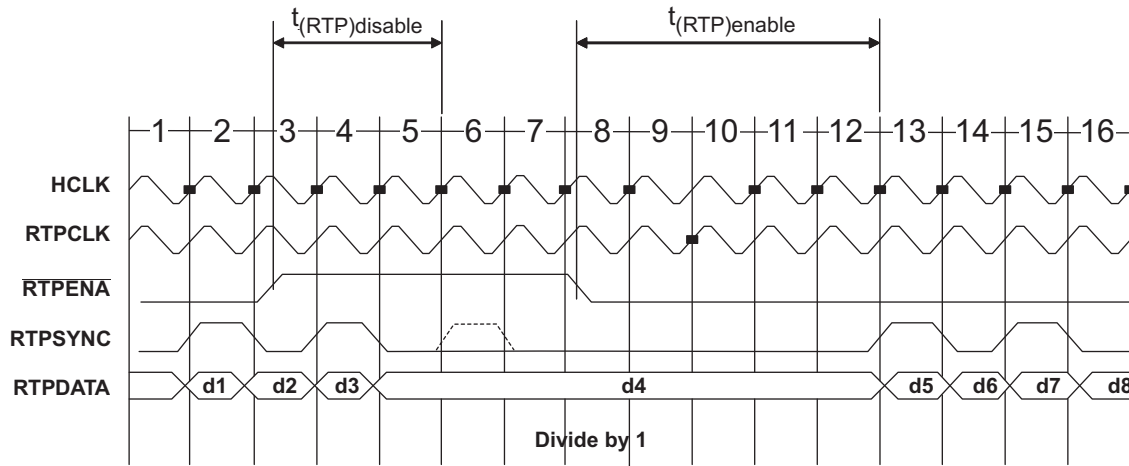


Figure 7-23. RTPENABLE Timing

Table 7-24. RTPENABLE Timing

| Parameter | Minimum | Maximum | Description |
|--------------------|--|--|---|
| $t_{(RTP)disable}$ | $1.5t_{c(HCLK)} + t_{r(RTPSYNC)} + 12ns$ | | Time that RTPEN \bar{A} must go high before the next scheduled RTPSYNC in order to suspend transmission for the packet following the scheduled RTPSYNC. |
| $t_{(RTP)enable}$ | $4.5t_{c(HCLK)} + t_{r(RTPSYNC)}$ | $5.5t_{c(HCLK)} + t_{r(RTPSYNC)} + 12ns$ | Time after RTPEN \bar{A} goes low before a packet that has been halted, resumes. |

7.17 DMM Timings

7.17.1 DMMCLK Timing

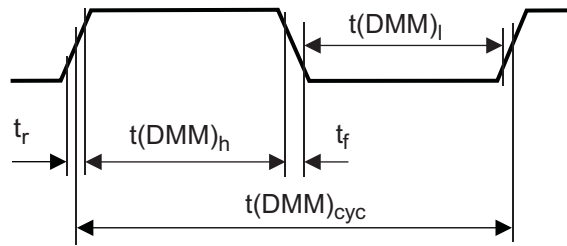


Figure 7-24. DMMCLK Timing

Table 7-25. DMMCLK Timing

| Parameter | Minimum | Description |
|------------------------------|--|------------------|
| $t(\text{DMM})_{\text{cyc}}$ | $t_{\text{c(HCLK)}} * 2$ | Clock period |
| $t(\text{DMM})_h$ | $t(\text{DMM})_{\text{cyc}}/2 - (t_r + t_f)/2$ | High pulse width |
| $t(\text{DMM})_l$ | $t(\text{DMM})_{\text{cyc}}/2 - (t_r + t_f)/2$ | Low pulse width |

7.17.2 DMMDATA Timing

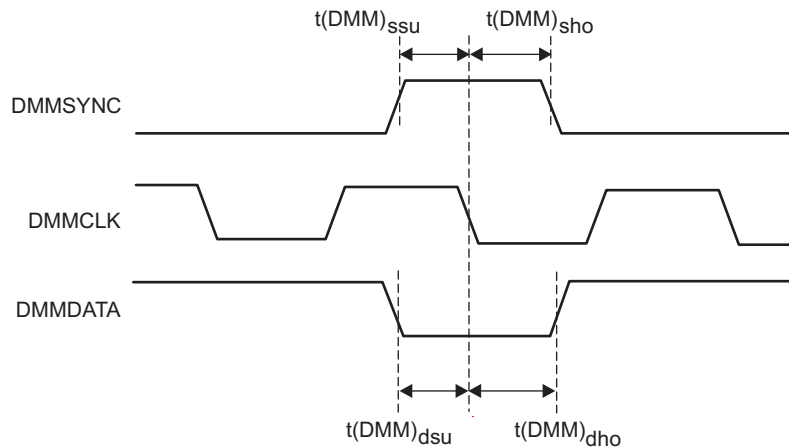


Figure 7-25. DMMDATA Timing

Table 7-26. DMMDATA Timing

| Parameter | Minimum | Description |
|------------------------------|---------|---|
| $t(\text{DMM})_{\text{ssu}}$ | 2ns | SYNC active to clk falling edge setup time |
| $t(\text{DMM})_{\text{sho}}$ | 3ns | clk falling edge to SYNC deactive hold time |
| $t(\text{DMM})_{\text{dsu}}$ | 2ns | DATA to clk falling edge setup time |
| $t(\text{DMM})_{\text{dho}}$ | 3ns | clk falling edge to DATA hold time |

7.17.3 DMMENA Timing

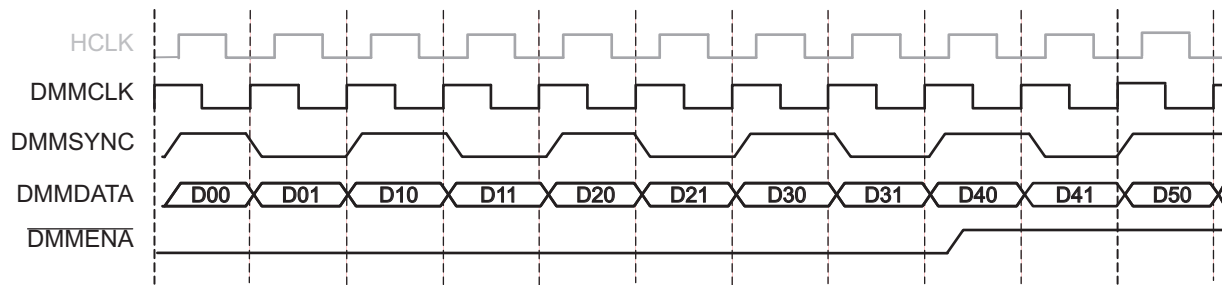


Figure 7-26. DMMENA Timing

The above figure shows a case with 1 DMM packet per 2 DMMCLK cycles (Mode = Direct Data Mode, data width = 8, portwidth = 4) where none of the packets received by the DMM are sent out, leading to filling up of the internal buffers. The DMMENA signal is shown asserted, after the first two packets have been received and synchronized to the HCLK domain. Here, the DMM has the capacity to accept packets D4, D5, D6, D7. Packet D8 would result in an overflow. Once DMMENA is asserted, the DMM expects to stop receiving packets after 4 HCLK cycles; once DMMENA is de-asserted, the DMM can handle packets immediately (after 0 HCLK cycles).

7.18 MibADC

7.18.1 MibADC

The multibuffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on VSS and VCC from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to ADREFLO unless otherwise noted.

Table 7-27. MibADC

| | |
|-------------------------------|---|
| Resolution | 12 bits (4096 values) |
| Monotonic | Assured |
| Output conversion ϕ code | 00h to FFFh [00 for $V_{AI} \leq AD_{REFLO}$; FFF for $V_{AI} \geq AD_{REFHI}$] |

7.18.2 MibADC Recommended Operating Conditions

Table 7-28. MibADC Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|---|---------------------|---------------------|------|
| AD _{REFHI} | A-to-D high-voltage reference source | 3 | 3.6 | V |
| AD _{REFLO} | A-to-D low-voltage reference source | 0 | 0.3 | V |
| V _{AI} | Analog input voltage | AD _{REFLO} | AD _{REFHI} | V |
| I _{AIC} | Analog input clamp current ⁽²⁾ ($V_{AI} < V_{SSAD} - 0.3$ or $V_{AI} > V_{CCAD} + 0.3$) | -2 | 2 | mA |

(1) For V_{CCAD} and V_{SSAD} recommended operating conditions, see the "device recommended operating conditions" table.

(2) Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

7.18.3 Operating Characteristics Over Full Ranges Of Recommended Operating Conditions

Table 7-29. Operating Characteristics Over Full Ranges Of Recommended Operating Conditions⁽¹⁾

| Parameter | | Description/Conditions | Min | TYP | Max | Unit |
|---------------------|--|--|---|-----|---------------|----------|
| $R_{mux}^{(2)}$ | Analog input mux on-resistance | | | | 250 | Ω |
| $R_{smp}^{(2)}$ | ADC sample switch on-resistance | | | 150 | 250 | Ω |
| C_{mux} | Input mux capacitance | | | | 16 | pF |
| C_{smp} | ADC sample capacitance | | 11 | 12 | 13 | pF |
| I_{AIL} | Analog input leakage current | Input leakage per ADC input pin | -200 | | 200 | nA |
| $I_{ADREFHI}^{(2)}$ | ADREFHI input current | $AD_{REFHI} = 3.6\text{ V}$, $AD_{REFLO} = V_{SSAD}$ | | | 5 | mA |
| CR | Conversion range over which specified accuracy is maintained | $AD_{REFHI} - AD_{REFLO}$ | 3 | | 3.6 | V |
| E_{DNL} | Differential nonlinearity error | Difference between the actual step width and the ideal value. | | | ± 3.8 | LSB |
| E_{INL} | Integral nonlinearity error | Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error. | | | ± 3.7 | LSB |
| E_{TOT} | Total error/Absolute accuracy | Maximum value of the difference between an analog value and the ideal midstep value. | Executing periodic internal calibration | | $\pm 8^{(3)}$ | LSB |
| | | | No calibration | | ± 15 | LSB |

(1) 1 LSB = $(AD_{REFHI} - AD_{REFLO}) / 2^{12}$ for the MibADC

(2) This parameter is characterized from -40°C to 125°C only.

(3) An periodic internal offset calibration is required to achieve the absolute accuracy. Please refer to the *Analog To Digital Converter (ADC) Module* chapter of the *TMS570LS Series Microcontroller Technical Reference Manual (SPNU489)* and *Interfacing the Embedded 12-bit ADC (SPNA129)* for more information.

7.18.4 MibADC Input Model

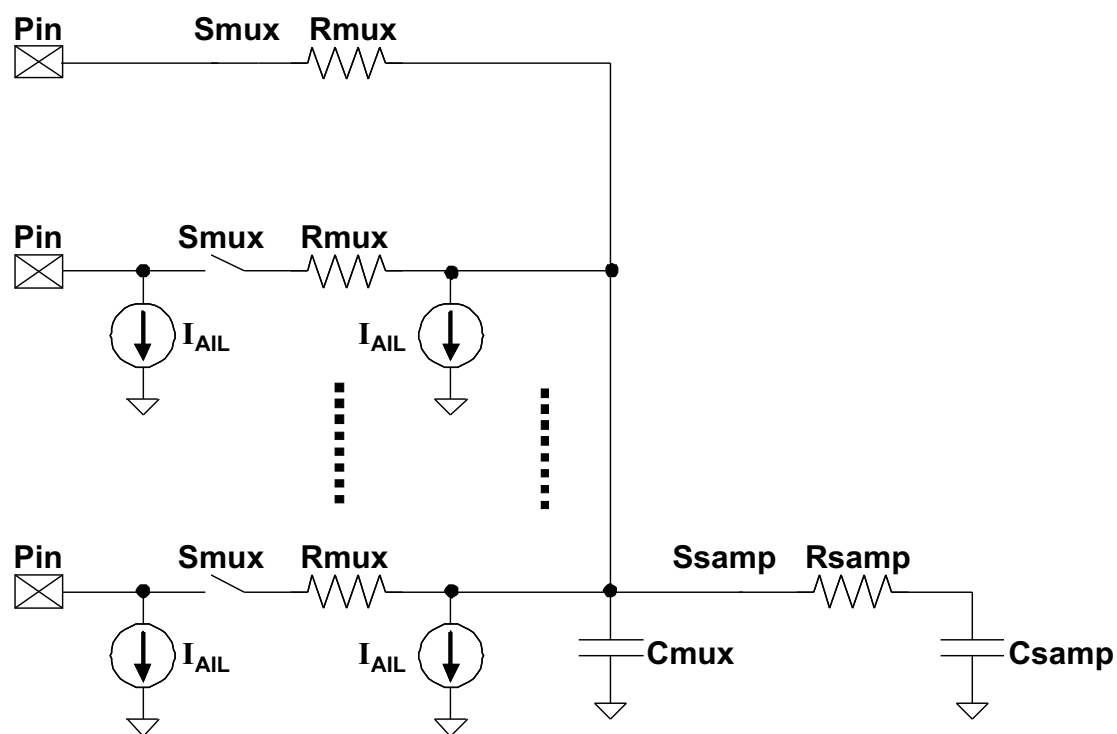


Figure 7-27. MibADC Input Equivalent Circuit

7.18.5 MibADC Timings

Table 7-30. MibADC Timings⁽¹⁾

| | | Min | NOM | MAX | Unit |
|--------------------|---|------------|------------|------------|-------------|
| $t_{c(ADCLK)}$ | Cycle time, MibADC clock | 33 | | | ns |
| $t_{d(SH)}$ | Delay time, sample and hold time | 200 | | | ns |
| $t_{d(C)}$ | Delay time, conversion time | 400 | | | ns |
| $t_{d(SHC)}^{(2)}$ | Delay time, total sample/hold and conversion time | 600 | | | ns |

(1) These parameters are characterized from -40°C to 125°C only.

(2) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors, e.g the prescale settings.

7.18.6 MibADC Nonlinearity Error

The differential nonlinearity error shown in the figure below (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.

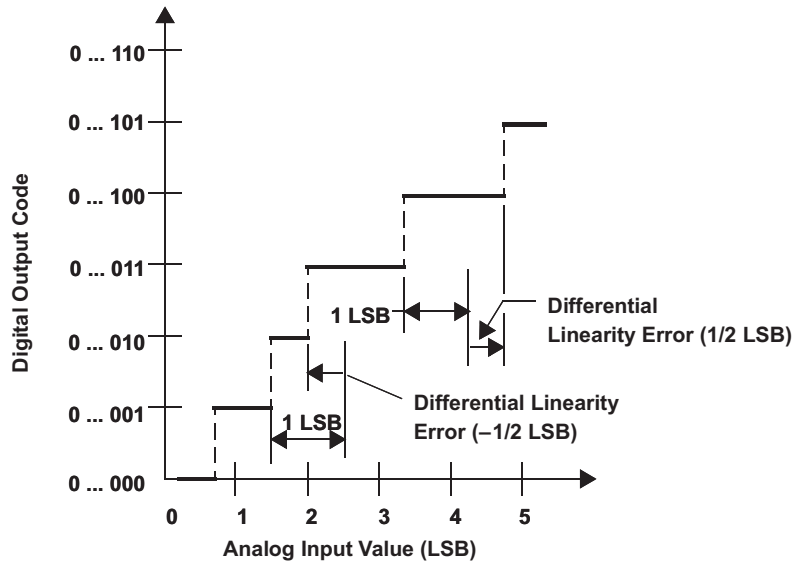


Figure 7-28. Differential Nonlinearity (DNL)

The integral nonlinearity error shown in the figure below (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.

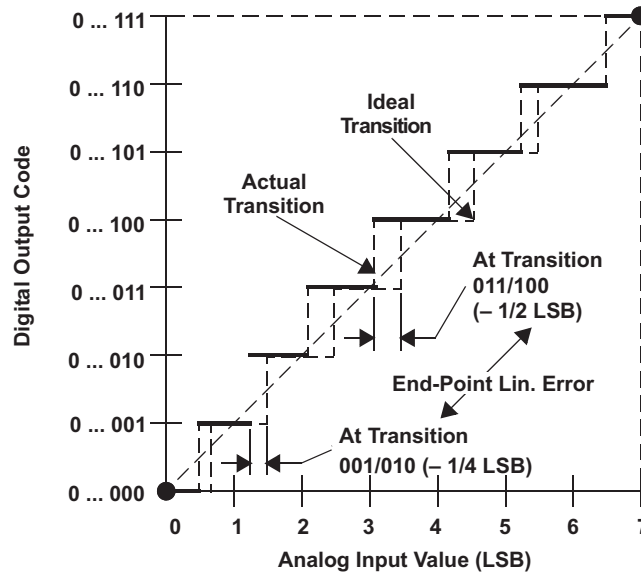


Figure 7-29. Integral Nonlinearity (INL) Error

7.18.7 MibADC Total Error

The absolute accuracy or total error of an MibADC as shown in the figure below is the maximum value of the difference between an analog value and the ideal midstep value.

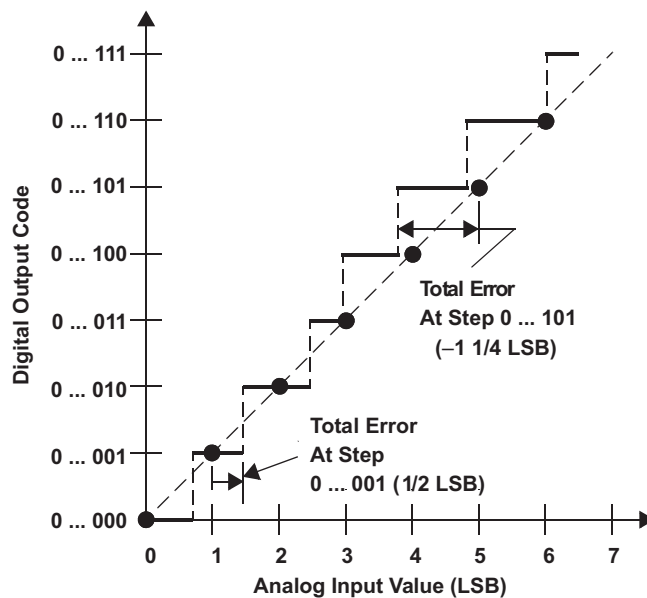


Figure 7-30. Absolute Accuracy (Total) Error

8 Mechanical Packaging and Orderable Information

8.1 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated device(s). The data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|----------------------------|-------------------------|
| S5LS20206ASGWTMEP | ACTIVE | NFBGA | GWT | 337 | 90 | TBD | SNPB | Level-3-220C-168 HR | -55 to 125 | TMS570 S20206ASGWTMEP | Samples |
| S5LS20206ASPGEMEP | ACTIVE | LQFP | PGE | 144 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -55 to 125 | S20206ASPGEMEP TMS570LS | Samples |
| S5LS20216ASGWTMEP | ACTIVE | NFBGA | GWT | 337 | 90 | TBD | SNPB | Level-3-220C-168 HR | -55 to 125 | TMS570 S20216ASGWTMEP | Samples |
| S5LS20216ASPGEMEP | ACTIVE | LQFP | PGE | 144 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -55 to 125 | S20216ASPGEMEP TMS570LS | Samples |
| V62/12622-01XE | ACTIVE | LQFP | PGE | 144 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -55 to 125 | S20206ASPGEMEP TMS570LS | Samples |
| V62/12622-01YE | ACTIVE | NFBGA | GWT | 337 | 90 | TBD | SNPB | Level-3-220C-168 HR | -55 to 125 | TMS570 S20206ASGWTMEP | Samples |
| V62/12622-02XE | ACTIVE | LQFP | PGE | 144 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -55 to 125 | S20216ASPGEMEP TMS570LS | Samples |
| V62/12622-02YE | ACTIVE | NFBGA | GWT | 337 | 90 | TBD | SNPB | Level-3-220C-168 HR | -55 to 125 | TMS570 S20216ASGWTMEP | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF TMS570LS20206-EP, TMS570LS20216-EP :

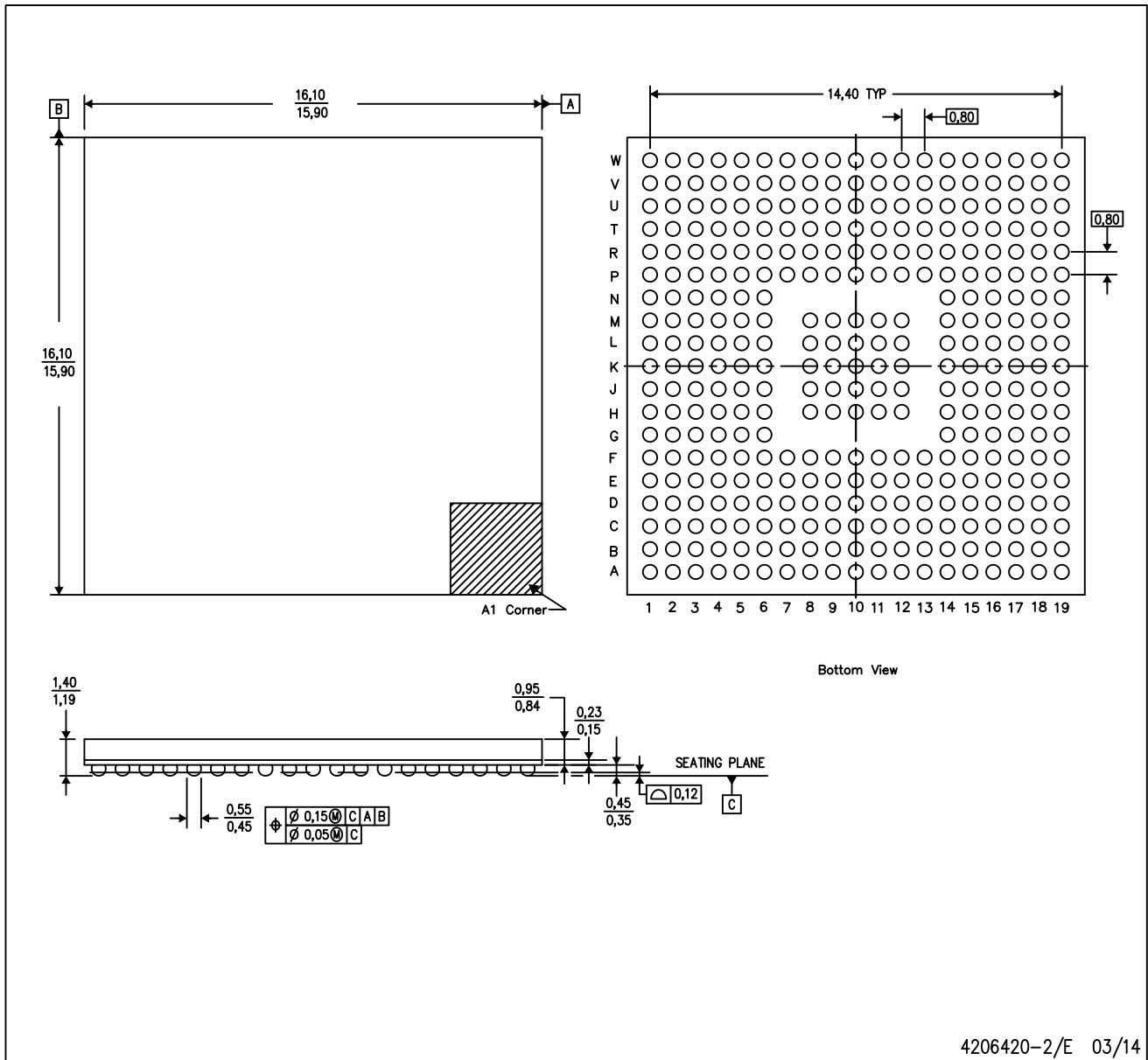
- Catalog: [TMS570LS20206](#), [TMS570LS20216](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GWT (S-PBGA-N337)

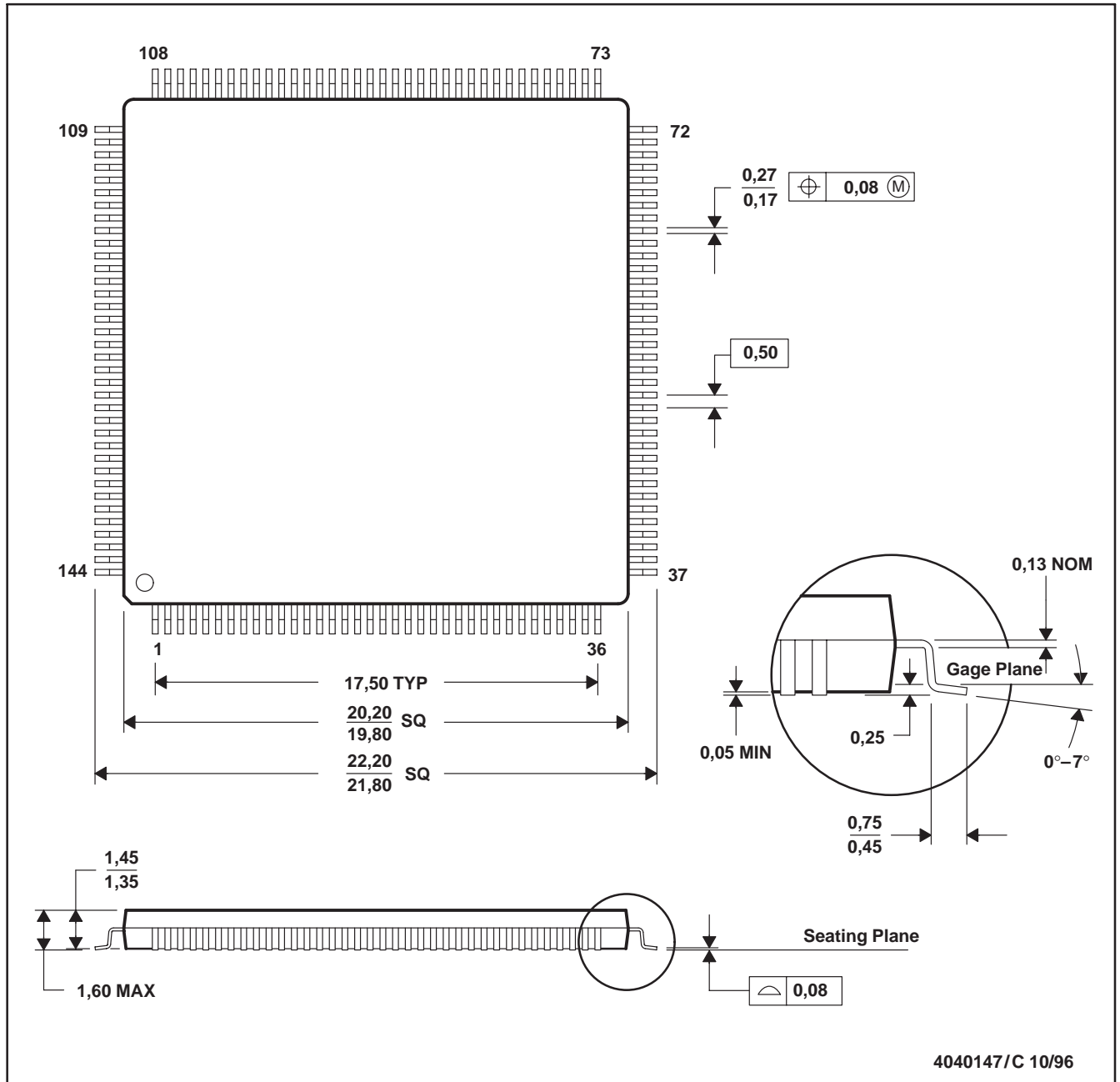
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.

PGE (S-PQFP-G144)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

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- Приемлемые сроки поставки, возможна ускоренная поставка.
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