Freescale Semiconductor
Technical Data

Document Number: A2T18H160-24S
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RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 28 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 1805 to 1880 MHz.

1800 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQA} = 400 mA, V_{GSB} = 0.65 Vdc, P_{out} = 28 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

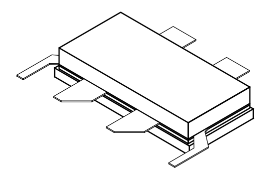
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1805 MHz	17.9	49.9	7.7	–32.0
1840 MHz	17.8	49.3	7.7	–33.8
1880 MHz	17.8	50.2	7.8	–34.7

Features

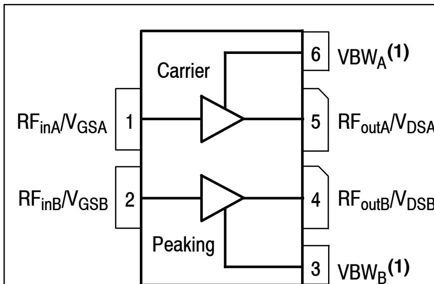
- Advanced High Performance In-Package Doherty
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems

A2T18H160-24SR3

1805–1880 MHz, 28 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



NI-780S-4L2L



(Top View)

Figure 1. Pin Connections

1. Device cannot operate with the V_{DD} current supplied through pin 3 and pin 6.

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range [1,2]	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case Case Temperature 75°C, 28 W Avg., W-CDMA, 28 Vdc, I_{DQA} = 400 mA, V_{GSB} = 0.65 Vdc, 1840 MHz	$R_{\theta JC}$	0.45	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics [4]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 60 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 400 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	1.4	1.8	2.2	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 0.6 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc
On Characteristics - Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2] (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 400 mA, V_{GSB} = 0.65 Vdc, P_{out} = 28 W Avg., f = 1805 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17.3	17.9	20.3	dB
Drain Efficiency	η_D	47.5	49.9	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.3	7.7	—	dB
Adjacent Channel Power Ratio	ACPR	—	–32.0	–29.5	dBc
Load Mismatch [2] (In Freescale Doherty Test Fixture, 50 ohm system) I_{DQA} = 400 mA, V_{GSB} = 0.65 Vdc, f = 1840 MHz					
VSWR 10:1 at 32 Vdc, 158 W CW Output Power (3 dB Input Overdrive from 100 W CW Rated Power)	No Device Degradation				
Typical Performance [2] (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 400 mA, V_{GSB} = 0.65 Vdc, 1805–1880 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	126	—	W
P_{out} @ 3 dB Compression Point [3]	P3dB	—	182	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz frequency range)	Φ	—	–10.3	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	135	—	MHz
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 28 W Avg.	G_F	—	0.04	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.008	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.003	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2T18H160-24SR3	R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel	NI-780S-4L2L

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

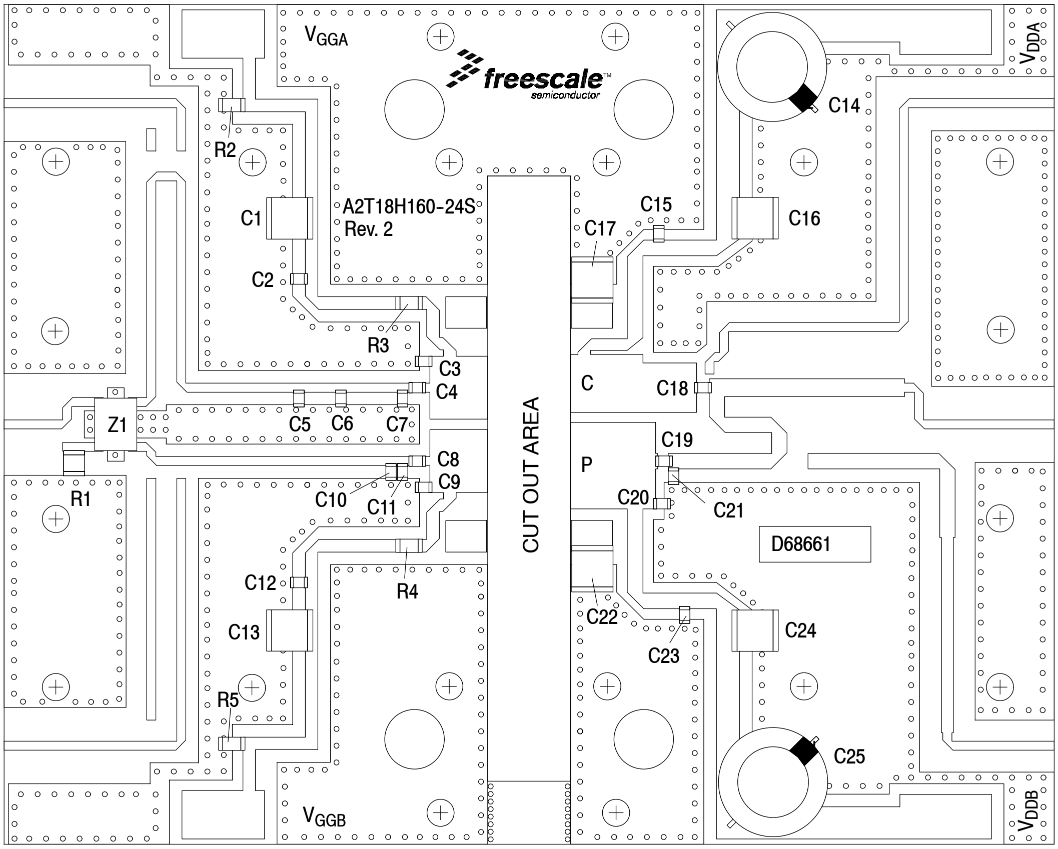


Figure 2. A2T18H160-24SR3 Test Circuit Component Layout

Table 6. A2T18H160-24SR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
PCB		D58628	MTL
C1, C13, C16, C17, C22, C24	10 µF Chip Capacitors	C5750X7S2A106M230KB	TDK
C2, C4, C8, C12, C15, C19, C23	12 pF Chip Capacitors	ATC600F120JT250XT	ATC
C3	1.8 pF Chip Capacitor	ATC600F1R8BT250XT	ATC
C5, C6	0.3 pF Chip Capacitors	ATC600F0R3BT250XT	ATC
C7	1.0 pF Chip Capacitor	ATC600F1R0BT250XT	ATC
C9	2.0 pF Chip Capacitor	ATC600F2R0BT250XT	ATC
C10, C11, C20	0.5 pF Chip Capacitors	ATC600F0R5BT250XT	ATC
C14, C25	220 µF, 50 V Electrolytic Capacitors	227CKS050M	Illinois Capacitor
C18	9.1 pF Chip Capacitor	ATC600F9R1BT250XT	ATC
C21	1.5 pF Chip Capacitor	ATC600F1R5BT250XT	ATC
R1	50 Ω, 4 W Chip Resistor	C10A50Z4	Anaren
R2, R5	20 KΩ, 1/4 W Chip Resistors	CRCW120620K0JNEA	Vishay
R3, R4	5.6 Ω, 1/4 W Chip Resistors	CRCW12065R60FKEA	Vishay
Z1	1700–2000 MHz Band, 90°, 5 dB Directional Coupler	X3C19P1-05S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D68661	MTL

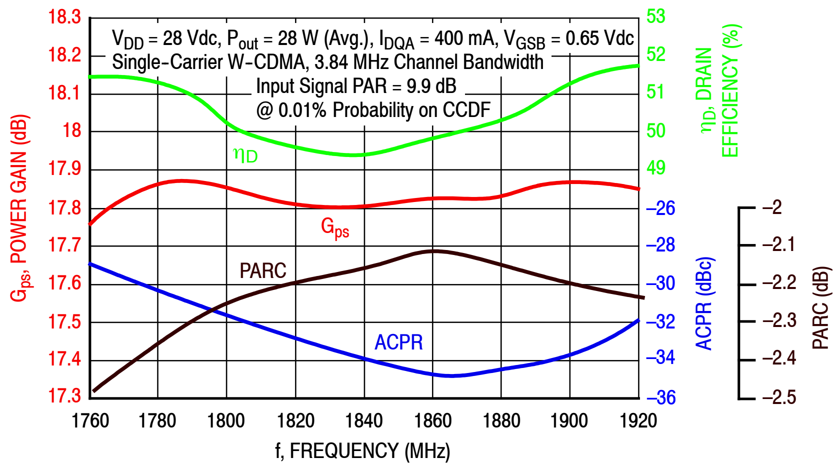


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 28 Watts Avg.

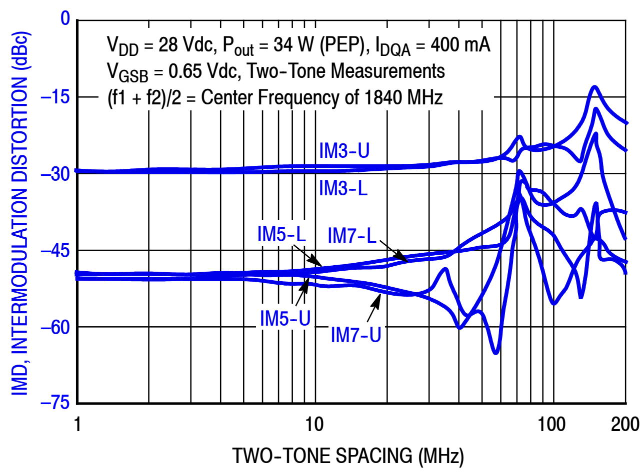


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

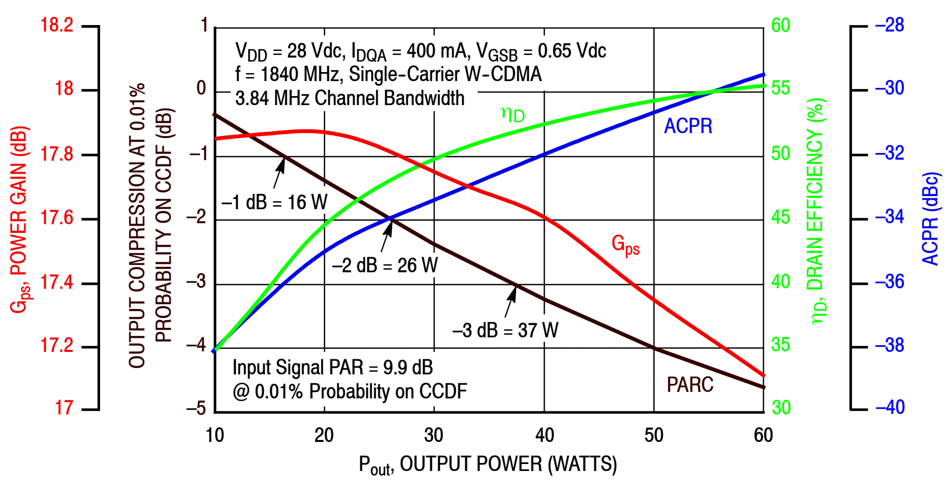


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

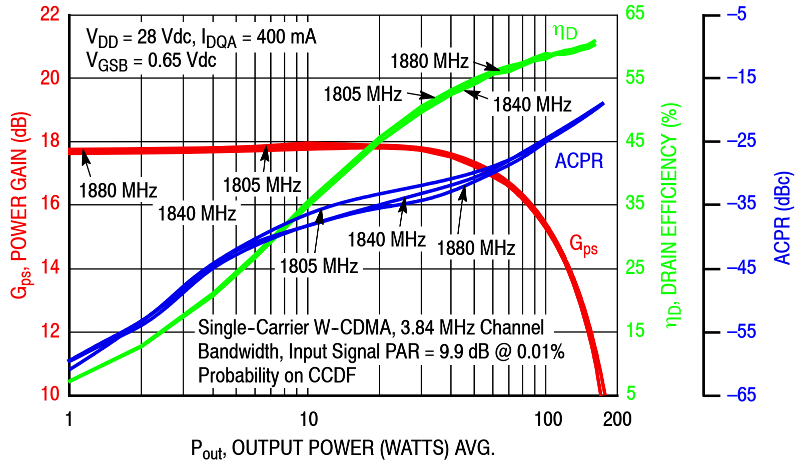


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

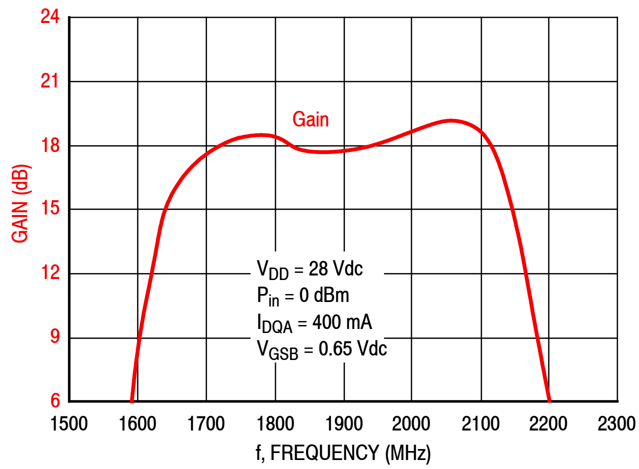


Figure 7. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 408 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	2.25 – j8.58	2.61 + j7.74	4.68 – j7.50	20.1	48.7	73	61.5	–15
1840	2.88 – j9.59	2.95 + j8.30	4.73 – j8.14	20.0	48.7	75	61.6	–15
1880	4.30 – j10.4	3.95 + j8.89	4.76 – j8.44	20.0	48.6	72	60.2	–15

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	2.25 – j8.58	2.53 + j8.36	4.68 – j8.41	18.0	49.4	87	62.3	–22
1840	2.88 – j9.59	2.91 + j9.02	4.71 – j8.78	17.9	49.4	87	62.6	–23
1880	4.30 – j10.4	4.06 + j9.90	4.89 – j9.14	18.0	49.3	85	61.3	–22

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQA} = 408 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	2.25 – j8.58	2.13 + j7.81	7.94 – j3.73	22.2	47.2	52	71.5	–27
1840	2.88 – j9.59	2.33 + j8.41	7.67 – j3.36	22.1	47.0	50	71.9	–29
1880	4.30 – j10.4	3.13 + j9.13	7.25 – j3.56	22.3	46.9	49	71.0	–29

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	2.25 – j8.58	2.17 + j8.29	7.63 – j6.11	19.8	48.4	70	72.0	–31
1840	2.88 – j9.59	2.41 + j8.94	7.53 – j5.64	19.7	48.3	67	72.3	–32
1880	4.30 – j10.4	3.27 + j9.86	6.95 – j5.06	19.8	48.0	63	71.1	–34

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

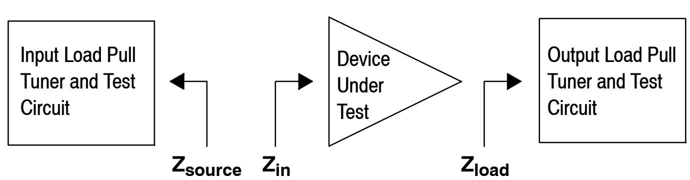


Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.65 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	2.70 – j9.87	2.49 + j9.58	3.97 – j9.45	15.5	50.5	112	56.5	–30
1840	3.29 – j10.6	2.89 + j10.3	3.81 – j9.81	15.4	50.5	113	55.7	–31
1880	5.01 – j11.4	4.06 + j11.3	4.09 – j10.1	15.5	50.5	111	56.0	–31

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	2.70 – j9.87	2.51 + j10.1	3.84 – j9.87	13.3	51.2	132	56.6	–38
1840	3.29 – j10.6	2.95 + j10.8	3.92 – j10.2	13.3	51.2	133	57.0	–39
1880	5.01 – j11.4	4.34 + j12.1	4.17 – j10.5	13.4	51.1	129	56.7	–39

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

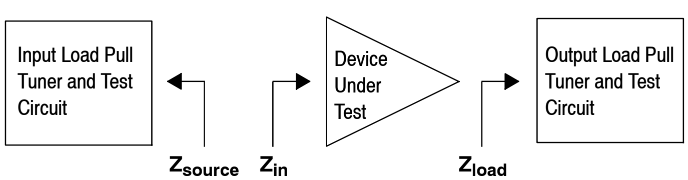
Table 10. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.65 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	2.70 – j9.87	2.08 + j9.49	8.64 – j6.58	16.8	48.9	78	69.4	–35
1840	3.29 – j10.6	2.35 + j10.1	8.17 – j6.08	16.8	48.9	77	69.8	–36
1880	5.01 – j11.4	3.22 + j11.2	7.22 – j5.33	16.8	48.7	73	69.7	–36

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	2.70 – j9.87	2.17 + j10.0	8.72 – j7.75	14.6	49.7	92	67.9	–43
1840	3.29 – j10.6	2.54 + j10.8	8.30 – j7.39	14.7	49.7	94	68.6	–44
1880	5.01 – j11.4	3.64 + j12.1	7.94 – j6.26	14.8	49.4	87	68.3	–45

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER LOAD PULL CONTOURS — 1840 MHz

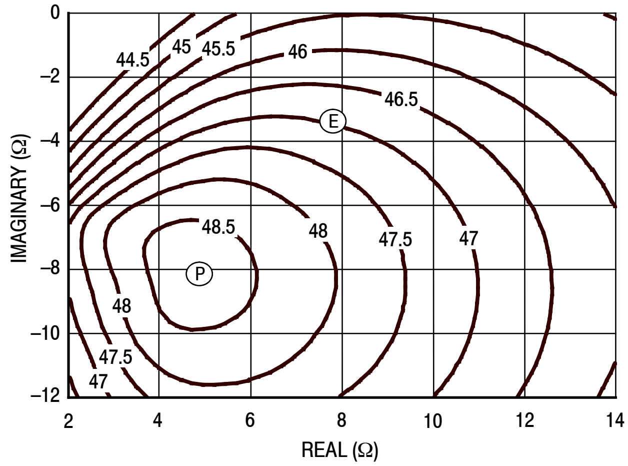


Figure 8. P1dB Load Pull Output Power Contours (dBm)

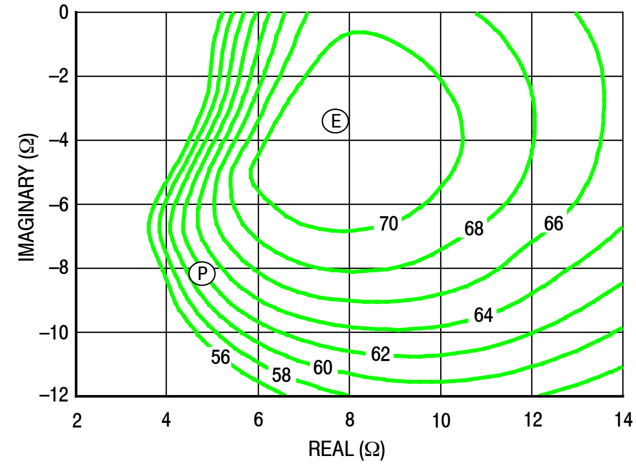


Figure 9. P1dB Load Pull Efficiency Contours (%)

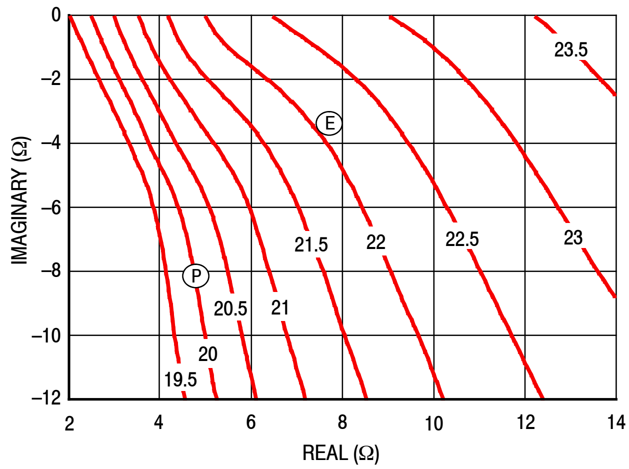


Figure 10. P1dB Load Pull Gain Contours (dB)

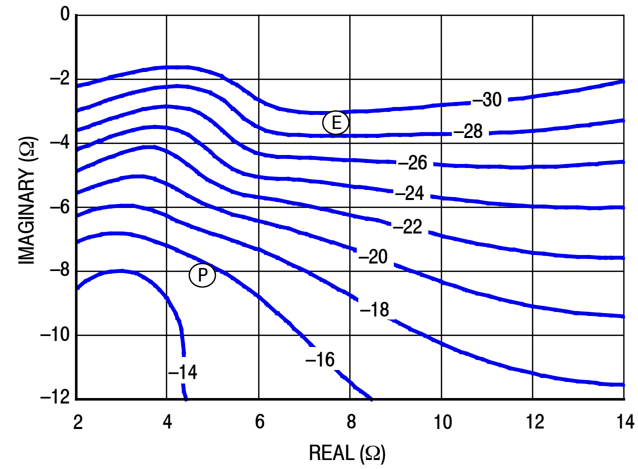


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

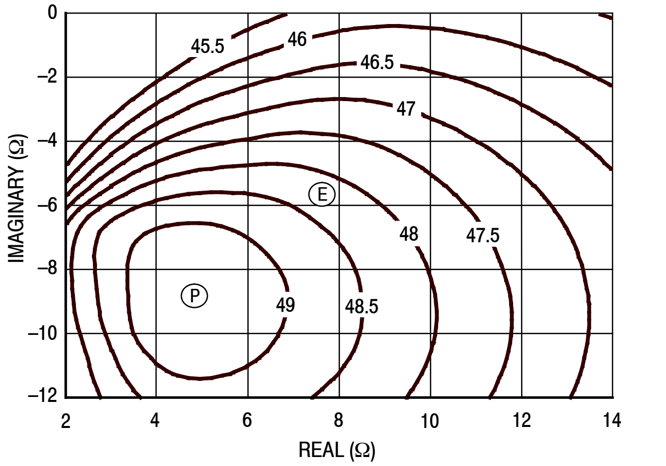


Figure 12. P3dB Load Pull Output Power Contours (dBm)

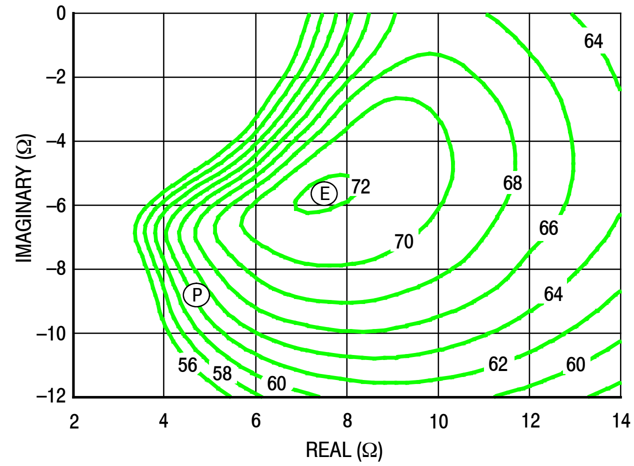


Figure 13. P3dB Load Pull Efficiency Contours (%)

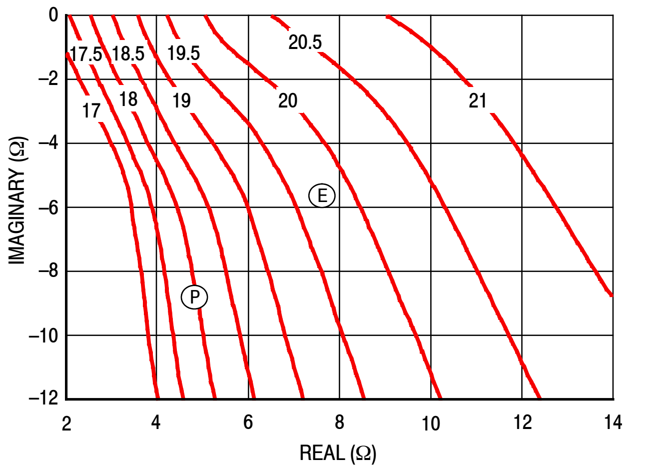


Figure 14. P3dB Load Pull Gain Contours (dB)

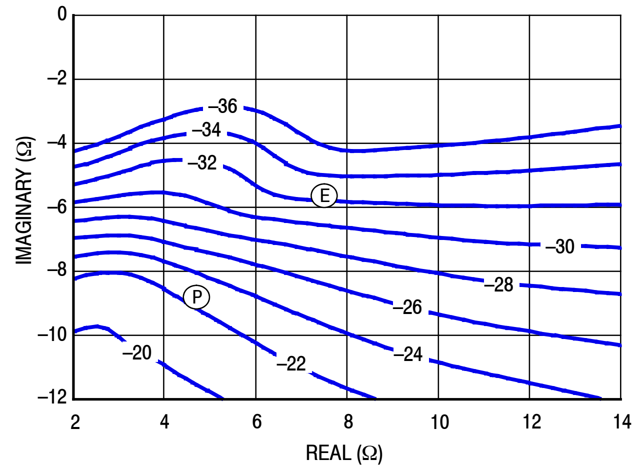
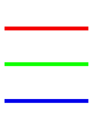


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency



P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 1840 MHz

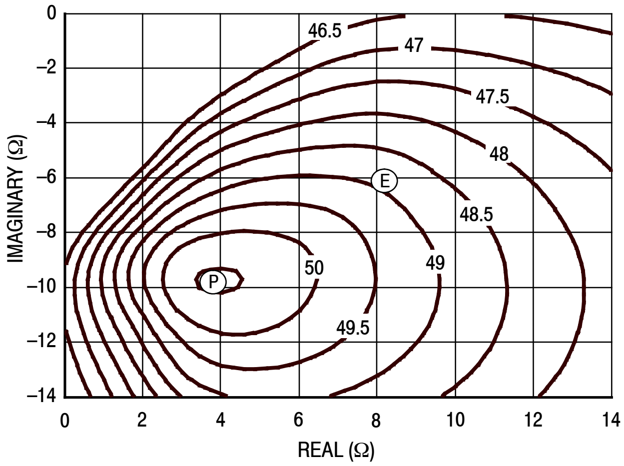


Figure 16. P1dB Load Pull Output Power Contours (dBm)

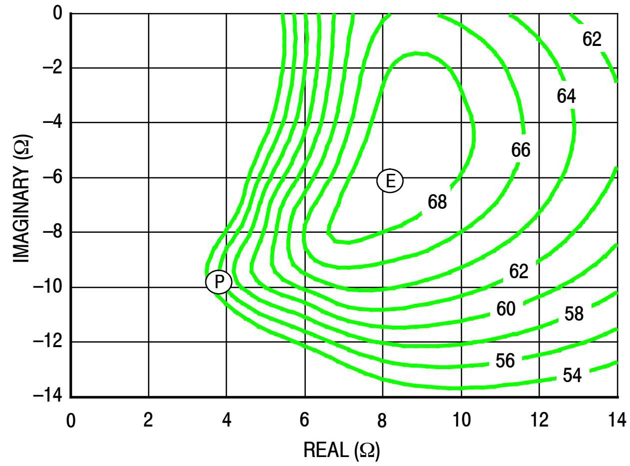


Figure 17. P1dB Load Pull Efficiency Contours (%)

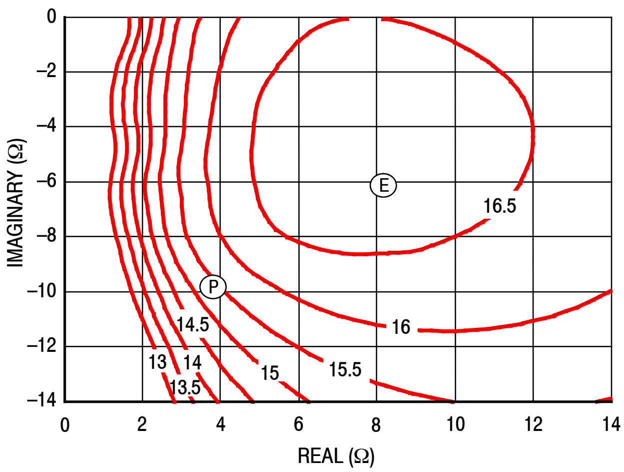


Figure 18. P1dB Load Pull Gain Contours (dB)

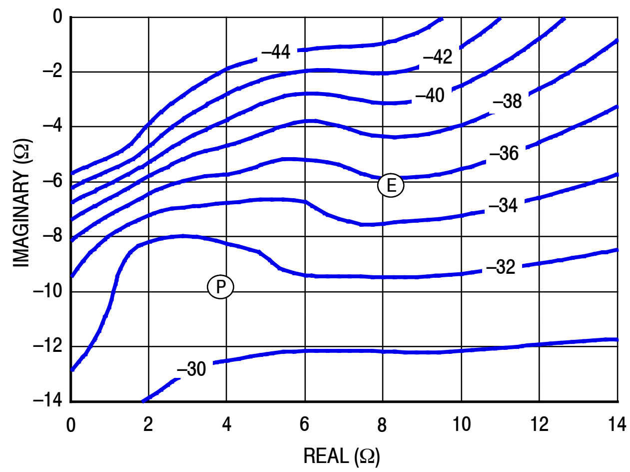


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL PEAKING LOAD PULL CONTOURS — 1840 MHz

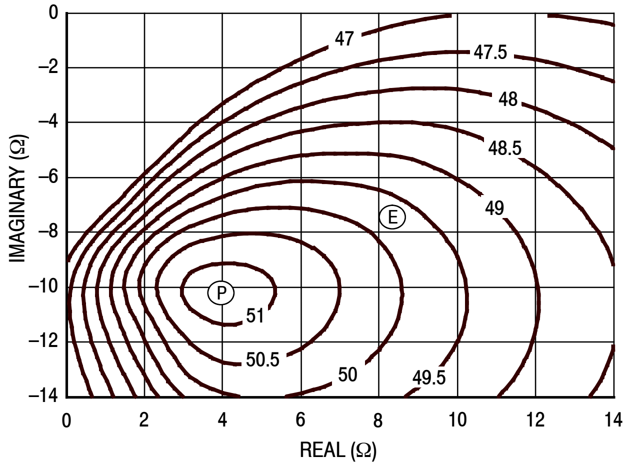


Figure 20. P3dB Load Pull Output Power Contours (dBm)

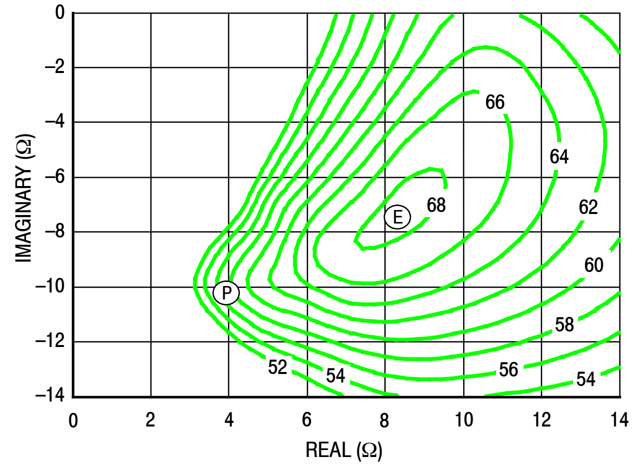


Figure 21. P3dB Load Pull Efficiency Contours (%)

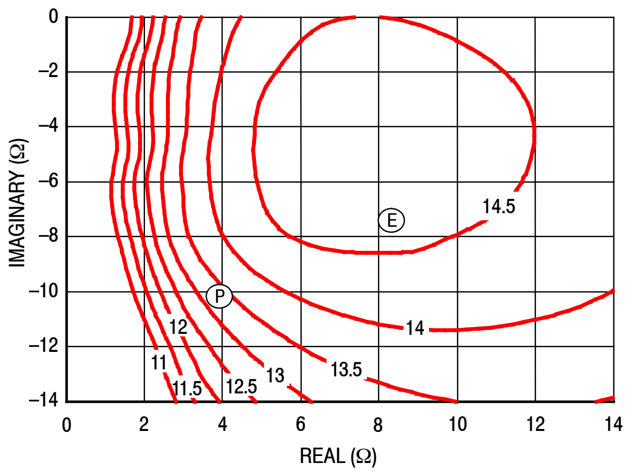


Figure 22. P3dB Load Pull Gain Contours (dB)

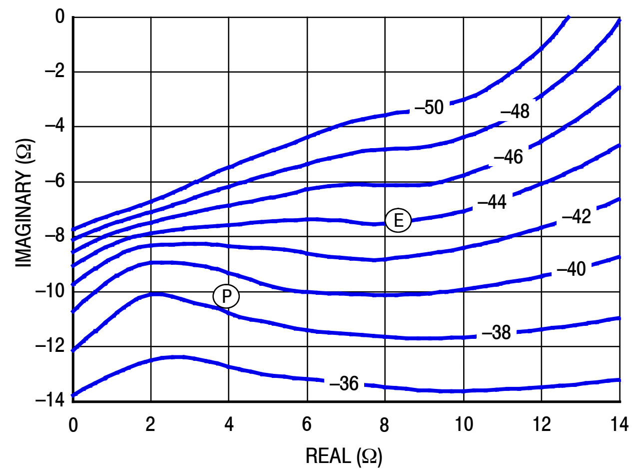


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

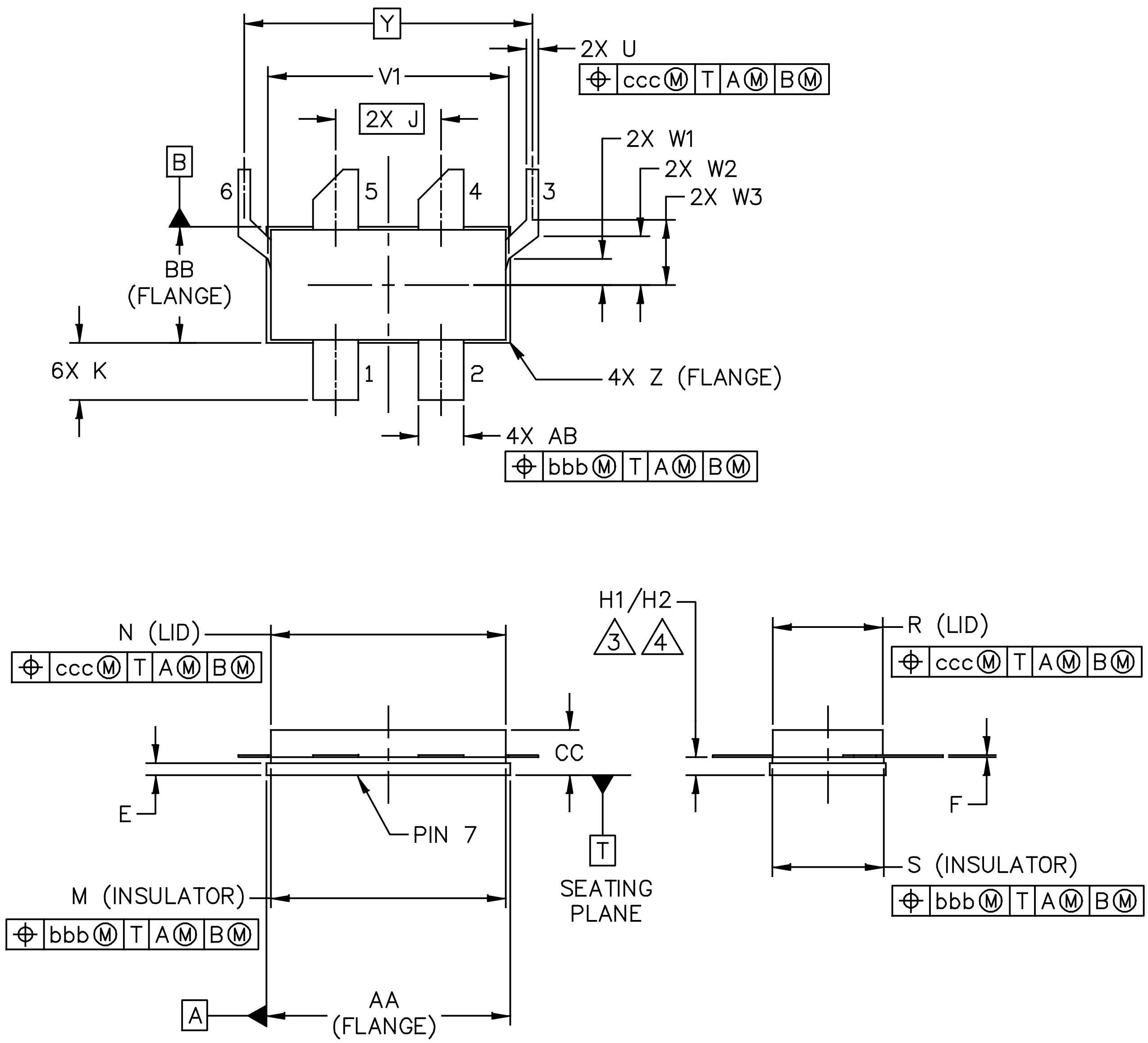
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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NOTES:

1. CONTROLLING DIMENSION: INCH.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
E	.035	.045	0.89	1.14	V1	.795	.805	20.19	20.45
F	.004	.007	0.10	0.18	W1	.080	.090	2.03	2.29
H1	.057	.067	1.45	1.70	W2	.155	.165	3.94	4.19
H2	.054	.070	1.37	1.78	W3	.210	.220	5.33	5.59
J	.350 BSC		8.89 BSC		Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R0.00	R1.02
M	.774	.786	19.66	19.96	AB	.145	.155	3.68	3.94
N	.772	.788	19.61	20.02	aaa	.005		0.13	
					bbb	.010		0.25	
					ccc	.015		0.38	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.freescale.com/rf
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Nov. 2015	• Initial Release of Data Sheet

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- *Приемлемые сроки поставки, возможна ускоренная поставка.*
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- *Комплексную поставку.*
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- *Тестирование поставляемой продукции.*
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- *Входной контроль качества.*
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