LTC2165, LTC2164, LTC2163 LTC2162, LTC2161, LTC2160, LTC2159, LTC2269 16-Bit, 20Msps to125Msps ADCs

DESCRIPTION

Demonstration circuit 1762A supports a family of 16-Bit 20Msps to 125Msps ADCs. Each assembly features one of the following devices: LTC®2165, LTC2164, LTC2163, LTC2162, LTC2161, LTC2160, LTC2159, or LTC2269 high speed, high dynamic range ADCs.

Demonstration circuit 1762A supports the LTC2165 family DDR LVDS output mode.

The versions of the 1762A demo board supporting the LTC2165 series of A/D converters are listed in Table 1.

Depending on the required resolution and sample rate, the DC1762A is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input frequencies from 5MHz to 140MHz. Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at http://www.linear.com/demo

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Table 1. DC1762A Variants

DC1762A VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1762A-A	LTC2165	16-Bit	125Msps	5MHz to 140MHz
1762A-B	LTC2164	16-Bit	105Msps	5MHz to 140MHz
1762A-C	LTC2163	16-Bit	80Msps	5MHz to 140MHz
1762A-D	LTC2162	16-Bit	65Msps	5MHz to 140MHz
1762A-E	LTC2161	16-Bit	40Msps	5MHz to 140MHz
1762A-F	LTC2160	16-Bit	25Msps	5MHz to 140MHz
1762A-G	LTC2159	16-Bit	20Msps	5MHz to 140MHz
1762A-H	LTC2269	16-Bit	20Msps	5MHz to 140MHz

PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage – DC1762A	Depending on Sampling Rate and the A/D Converter Provided, this Supply Must Provide up to 500mA.	4.5		6	V
Analog Input Range	Depending on SENSE Pin Voltage	1		2	V_{P-P}
Logic Input Voltages	Minimum Logic High Maximum Logic Low		1.3 0.6		V V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω Load, 3.5mA Mode) Common Mode Minimum Logic Levels (100Ω Load, 3.5mA Mode) Common Mode		350 1.25 247 1.25		mV V mV V
Sampling Frequency (Convert Clock Frequency)	See Table 1				
Convert Clock Level	Single-Ended Encode Mode (ENC^- Tied to GND) Differential Encode Mode (ENC^- Not Tied to GND)	0 0.2		3.6 3.6	V V
Resolution	See Table 1				
Input Frequency Range	See Table 1				
SFDR	See Applicable Data Sheet				
SNR	See Applicable Data Sheet				

QUICK START PROCEDURE

Demonstration circuit 1762A is easy to set up to evaluate the performance of the LTC2165 A/D converter family. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

Setup

If a DC890 USB demonstration circuit was supplied with the DC1762A demonstration circuit, follow the DC890 Quick Start Guide to install the required software and for connecting the DC890 to the DC1762A and to a PC.

DC1762 Demonstration Circuit Board Jumpers

The DC1762A demonstration circuit board should have the following jumper settings as default positions: (as per Figure 1)

JP2 PAR/SER: Selects parallel or serial programming mode. (default: serial)

JP3 Duty Cycle Stabilizer: enables/disables duty cycle stabilizer. (default: enable)

JP4 SHDN: Enables and disables the LTC2165. (default: enable)

JP5 NAP: Enables and disables NAP mode. (default: enable)

JP6 LVDS/CMOS: Selects between LVDS and CMOS output signaling. (default: LVDS)

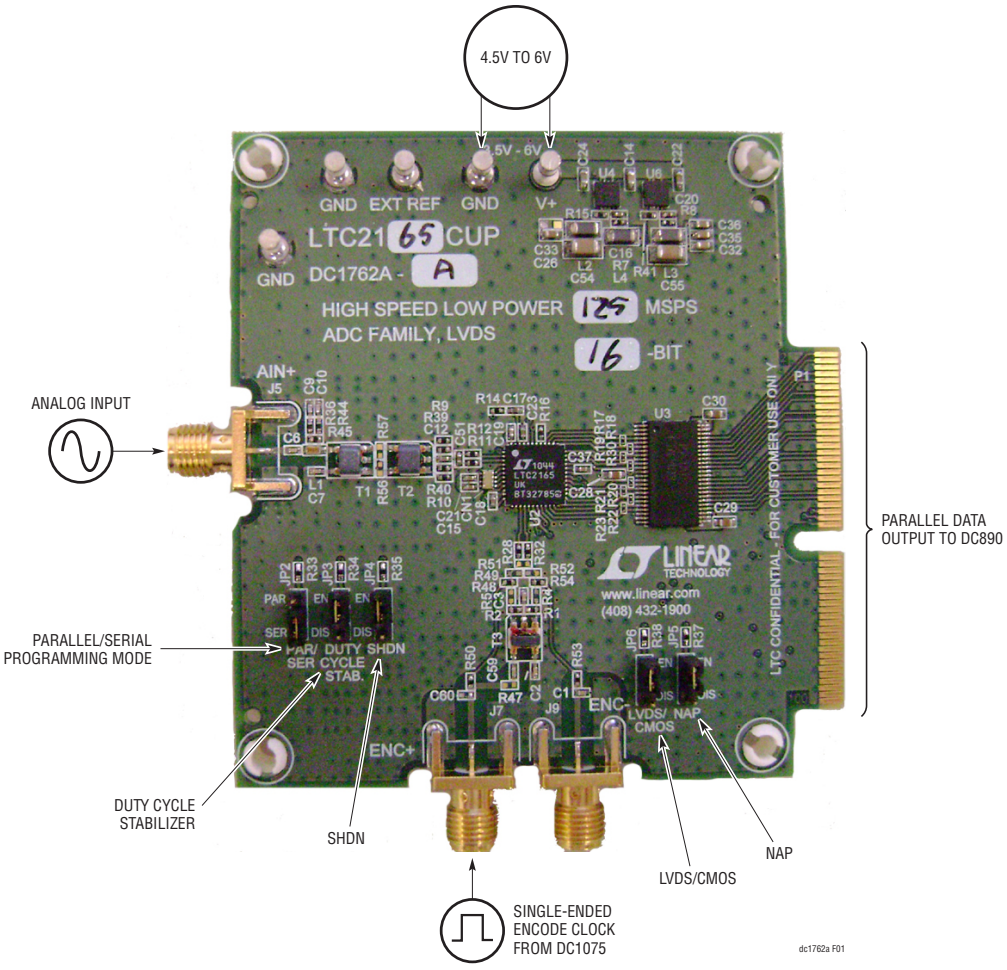


Figure 1. DC1762 Setup

QUICK START PROCEDURE

Applying Power and Signals to the DC1762A Demonstration Circuit

If a DC890 is used to acquire data from the DC1762A, the DC890 must FIRST be connected to a powered USB port or provided an external 6V to 9V BEFORE applying 4.5V to 6V across the pins marked V^+ and GND on the DC1762A. DC1762A requires 4.5V for proper operation. Regulators on the board produce the voltages required for the ADC. The DC1762A demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

The DC890 data collection board is powered by the USB cable and does require an external power supply when collecting data from and LVDS demo board. It must be supplied an external 6V to 9V on turrets G7(+) and G1(–) or the adjacent 2.1mm power jack.

Analog Input Network

For optimal distortion and noise performance the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies above 140MHz, refer to the respective ADC data sheet for a proper input network. Other input networks may be more appropriate for input frequencies less than 5MHz, or above 140MHz.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR. In the case of the DC1762A, a bandpass filter used for the clock should be used prior to the DC1075 clock divider board.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

Apply the analog input signal of interest to the SMA connector on the DC1762A demonstration circuit board marked J5 AIN^+. This input is capacitively coupled to a Balun transformer ETC1-1-13 (lead free part number: MABA007159-000000).

Encode Clock

NOTE: Apply an encode clock to the SMA connector on the DC1762A demonstration circuit board marked J3 ENC^+. As a default the DC1762A is populated to have a single-ended input.

For the best noise performance, the encode input must be driven with a very low jitter, square wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm. When using a sinusoidal signal generator a squaring circuit can be used. Linear Technology also provides demo board DC1075 that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTC2165.

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1762A a bandpass filter used for the clock should be used prior to the DC1075. Datasheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used with TTE bandpass filters for both the clock input and the analog input.

An internally generated conversion clock output is available on J1 which could be collected via a logic analyzer, or other data collection system if populated with a SAMTEC MEC8-150 type connector or collected by the DC890 QuikEval-II Data Acquisition Board using PScope™ software.

QUICK START PROCEDURE

Software

The DC890 is controlled by the PScope System Software provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a DC890 was provided, follow the DC890 Quick Start Guide and the instructions below.

To start the data collection software if PScope.exe, is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1762A demonstration circuit is properly connected to the DC890, PScope should automatically detect the DC1762A, and configure itself accordingly. If necessary the procedure below explains how to manually configure PScope.

Under the Configure menu, go to ADC Configuration… Check the Config Manually box and use the following configuration options, see Figure 2.

Manual Configuration settings:

Bits: 16

Alignment: 16

FPGA Ld: DDR LVDS

Channs: 2

Bipolar: Unchecked

Positive-Edge Clk: Unchecked

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the Collect button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC890 Quick Start Guide and in the online help available within the PScope program itself.

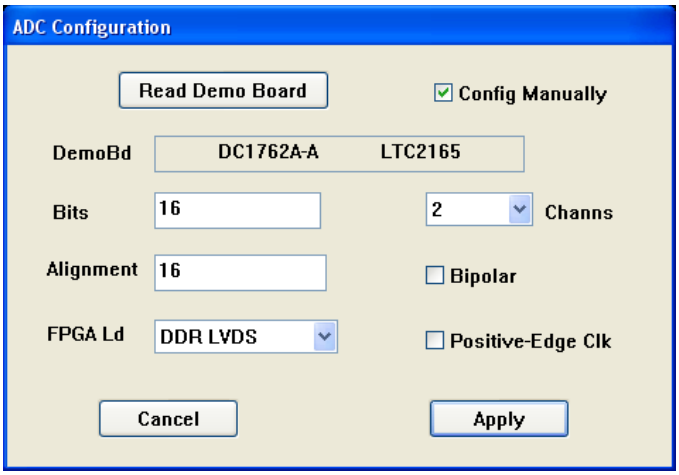


Figure 2: ADC Configuration

Serial Programming

PScope has the ability to program the DC1762A board serially through the DC890. There are several options available in the LTC2165 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the Set Demo Bd Options icon on the PScope toolbar (Figure 3).

This will bring up the menu shown in Figure 4.

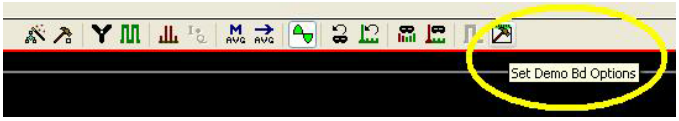


Figure 3: PScope Toolbar

QUICK START PROCEDURE

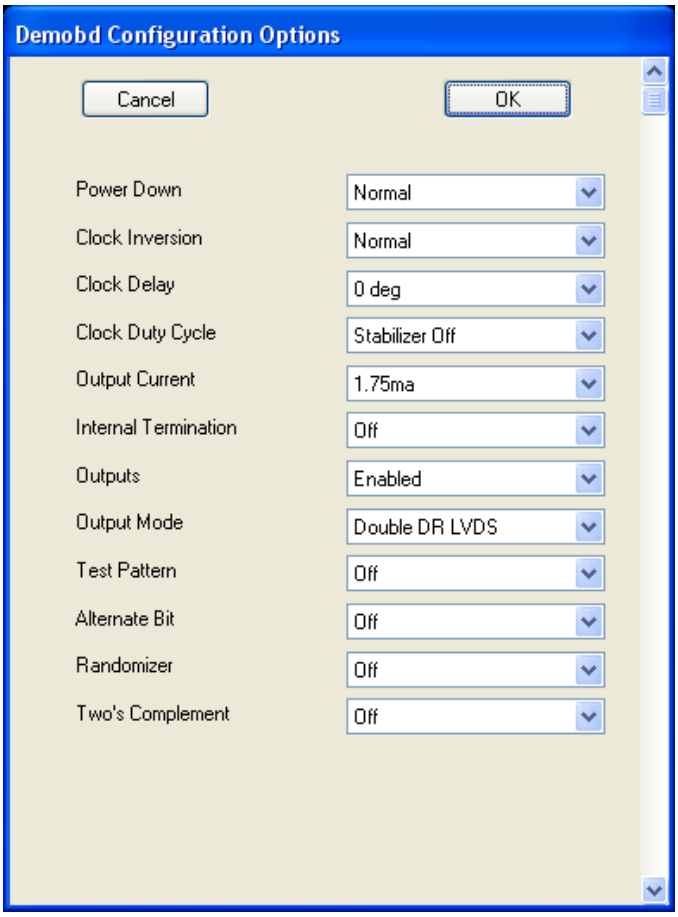


Figure 4: Demobd Configuration Options

This menu allows any of the options available for the LTC2165 family to be programmed serially. The LTC2165 family has the following options:

Power Down: Selects between normal operation, nap, and sleep modes:

- Normal (Default): Entire ADC is powered, and active.
- Nap: ADC core powers down while references stay active.
- Shutdown: The entire ADC is powered down.

Clock Inversion: Selects the polarity of the CLKOUT signal:

- Normal (Default): Normal CLKOUT polarity
- Inverted: CLKOUT polarity is inverted

Clock Delay: Selects the phase delay of the CLKOUT signal:

- None (Default): No CLKOUT delay
- 45 deg: CLKOUT delayed by 45 degrees
- 90 deg: CLKOUT delayed by 90 degrees
- 135 deg: CLKOUT delayed by 135 degrees

Clock Duty Cycle: Enables or disables duty cycle stabilizer

- Stabilizer off (Default): Duty cycle stabilizer disabled
- Stabilizer on: Duty cycle stabilizer enabled

Output Current: Selects the LVDS output drive current

- 1.75mA (Default): LVDS output driver current
- 2.1mA: LVDS output driver current
- 2.5mA: LVDS output driver current
- 3.0mA: LVDS output driver current
- 3.5mA: LVDS output driver current
- 4.0mA: LVDS output driver current
- 4.5mA: LVDS output driver current

Internal Termination: Enables LVDS internal termination

- Off (Default): Disables internal termination
- On: Enables internal termination

Outputs: Enables digital outputs

- Enabled (Default): Enables digital outputs
- Disabled: Disables digital outputs

QUICK START PROCEDURE

Output Mode: Selects digital output mode

- Full Rate: Full rate CMOS output mode (This mode is not supported by the DC1762A)
- Double LVDS (Default): Double data rate LVDS output mode
- Double CMOS: Double data rate CMOS output mode (This mode is not supported by the DC1762A)

Test Pattern: Selects digital output test patterns

- Off (Default): ADC data presented at output
- All out =1: All digital outputs are 1
- All out = 0: All digital outputs are 0
- Checkerboard: OF, and D13-D0 Alternate between 101 0101 1010 0101 and 010 1010 0101 1010 on alternating samples.
- Alternating: Digital outputs alternate between all 1's and all 0's on alternating samples.

Alternate Bit: Alternate Bit Polarity (ABP) Mode

- Off (Default): Disables alternate bit polarity
- On: Enables alternate bit polarity (Before enabling ABP, be sure the part is in offset binary mode)

Randomizer: Enables Data Output Randomizer

- Off (Default): Disables data output randomizer
- On: Enables data output randomizer

Two's complement: Enables two's complement mode

- Off (Default): Selects offset binary mode
- On: Selects two's complement mode

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1762A demo board.

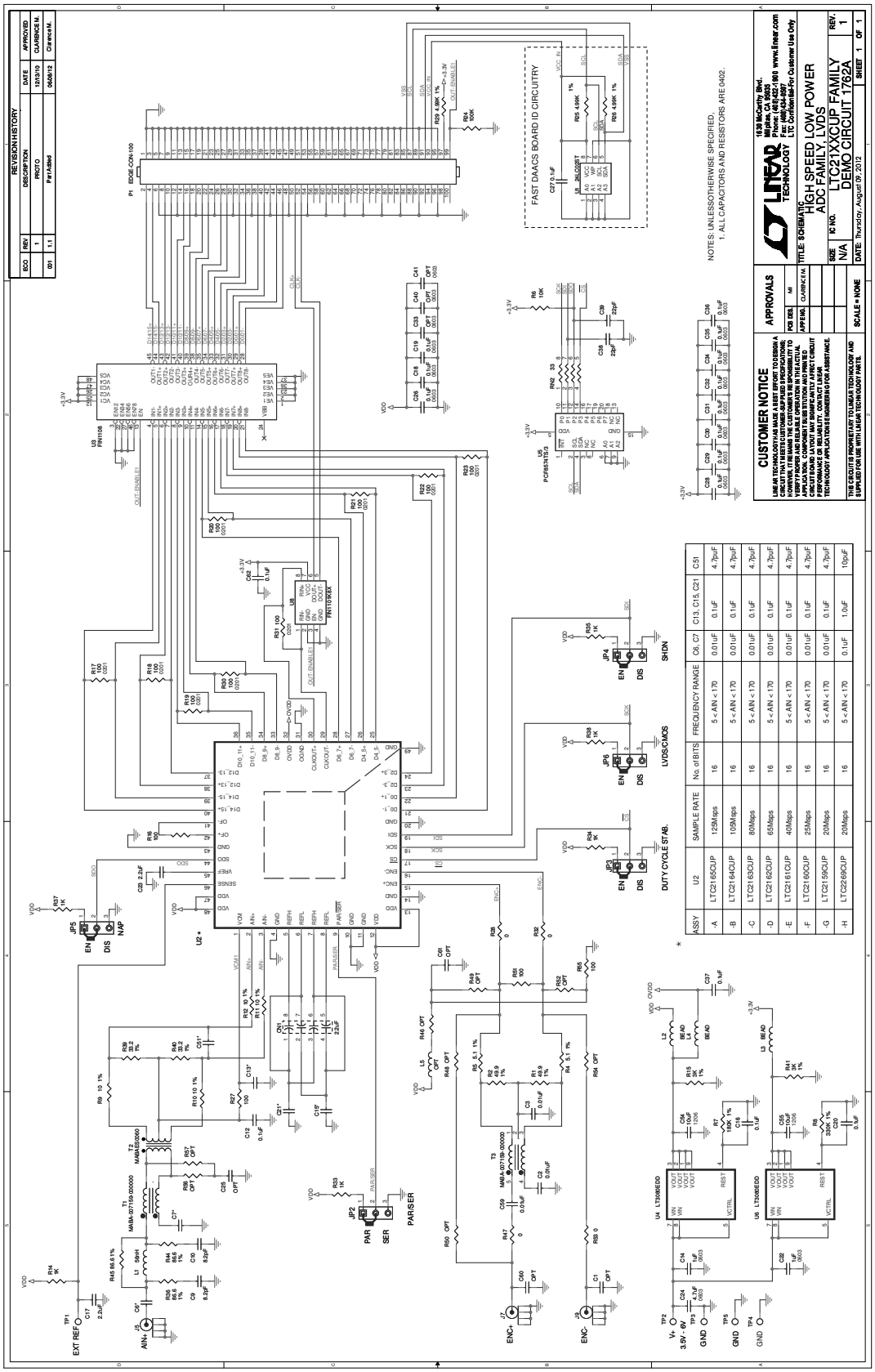
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CN1	Capacitor, Array, 0508, 2.2µF, 20%, 10V, X5R	AVX W2L14D225MAT1A
2	7	C1, R28, R32, R47, R48, R53, R54	Resistor, 0402, 0Ω, Jumper	Vishay CRCW04020000Z0ED
3	7	C2, C3, C6, C7, C8, C59, C60	Capacitor, 0402, 0.01µF, 10%, 16V, X7R	AVX 0402YC103KAT
4	2	C9, C10	Capacitor, 0402, 8.2pF, 5%, 50V, COG	AVX 04025A8R2JAT2A
5	8	C12, C13, C15, C18, C19, C21, C37, C61	Capacitor, 0402, 0.1µF, 10%, 10V, X5R	TDK C1005X5R1A104K
6	2	C14, C22	Capacitor, 0603, 1µF, 10%, 16V, X7R	TDK C1608X7R1C105K
7	2	C17, C23	Capacitor, 0402, 2.2µF, 20%, 6.3V, X5R	Taiyo Yuden JMK105BJ225MV-T
8	1	C24	Capacitor, 0603, 4.7µF, 20%, 6.3V, X5R	TDK C1608X5R0J475MT
9	11	C26-C32, C34-C36, C62	Capacitor, 0603, 0.1µF, 10%, 50V, X7R	TDK C1608X7R1H104K
10	0	C33, C40, C41	Capacitor, 0603, 0.1µF, 10%, 50V, X7R Option	TDK C1608X7R1H104K Option
11	2	C38, C39	Capacitor, 0402, 22pF, 5%, 16V, NPO	AVX 0402YA220JAT2A
12	1	C51	Capacitor, 0402, 4.7pF, ±0.25pF, 50V, NPO	AVX 04025A4R7CAT2A
13	2	C54, C55	Capacitor, 1206, 1µF, 10%, 16V, X7R	AVX 1206YC105KAT2A
14	5	JP2, JP3, JP4, JP5, JP6	Header, 3-Pin, 2mm	Samtec TMM-103-02-L-S
15	3	J5, J7, J9	Connector, BNC, SMA, 50Ω, Edge-Lanch	E. F. Johnson, 142-0701-851
16	2	L1, L5	Inductor, 0603, 56µH, 5%	Murata LQP18MN56NG02D
17	3	L2, L3, L4	Ferrite Bead, 1206	Murata BLM31PG330SN1L
18	1	RN2	Resistor, Array, 33Ω	Vishay CRA04SS08333R0JTD
19	2	R1, R2	Resistor, 0402, 49.9Ω, 1%, 1/16W	Vishay CRCW040249R9FKED
20	0	R4, R5	Resistor, 0402, 5.1Ω, 1%, 1/16W Option	Vishay CRCW04025R10FNED Option
21	1	R6	Resistor, 0402, 10kΩ, 5%, 1/16W	Vishay CRCW040210K0JNED
22	1	R7	Resistor, 0402, 180kΩ, 1%, 1/16W	Vishay CRCW0402180KFKED
23	1	R8	Resistor, 0402, 330kΩ, 1%, 1/16W	Vishay CRCW0402330KFKED
24	4	R9, R10, R11, R12	Resistor, 0402, 10Ω, 1%, 1/16W	Vishay CRCW040210R0FKED
25	6	R14, R33, R34, R35, R37, R38	Resistor, 0402, 1kΩ, 5%, 1/16W	Vishay CRCW04021K00JNTDE3
26	2	R15, R41	Resistor, 0402, 3kΩ, 1%, 1/16W	Vishay CRCW04023K00FKED
27	4	R16, R27, R46, R55	Resistor, 0402, 100Ω, 5%, 1/16W	Vishay CRCW0402100RJNED
28	9	R17-R23, R30, R31	Resistor, 0201, 100Ω, 5%, 1/16W	Vishay CRCW0201100RFNTD
29	1	R24	Resistor, 0402, 100kΩ, 5%, 1/16W	Vishay CRCW0402100KJNED
30	3	R25, R26, R29	Resistor, 0603, 4.99kΩ, 1%, 1/16W	AAC CR16-4991FM
31	3	R36, R44, R45	Resistor, 0402, 86.6Ω, 1%, 1/16W	Vishay CRCW040286R6FKED
32	2	R39, R40	Resistor, 0402, 33.2Ω, 1%, 1/16W	Vishay CRCW040233R2FKED
33	0	R49, R50, R51, R52	Resistor, 0402, 100Ω, 5%, 1/16W Option	Vishay CRCW0402100RJNED Option
34	5	TP1, TP2, TP3, TP4, TP5	Turrets	Millmax 2501-2-00-80-00-00-07-0

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
35	1	T1	XFMR, 1:1	Macom MABA-007159-000000
36	1	T2	XFMR, 1:1 CT	M/A-C0M MABAES0060
		T2 - Alternate	XFMR, 1:1 CT	Coilcraft WBC1-1LB
37	1	T3	XFMR, 1:1	Macom MABA-007159-000000
38	1	U1	IC, EEPROM	Microchip Tech. 24LC025-I/ST
39	1	U2	Refer to Schematic Table	Linear, Technology
40	1	U3	IC, FIN1108	Fairchild FIN1108
41	2	U4, U6	IC, Adjustable 1.1A Regulators	Linear, Technology LT3080EDD
42	1	U5	IC, 8-Bit I/0 Expander	Philips Semi PCF8574TS/3
43	1	U8	IC, LVDS Single Port High Speed Repeater	Fairchild FIN1101K8X
44	5	JP2, JP3, JP4, JP5, JP6	Shunt, 2mm	Samtec 2SN-BK-G
45	4		Standoff, Snap On	KEYSTONE_8831

SCHEMATIC DIAGRAM



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Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

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Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru