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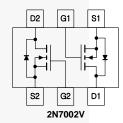
### January 2015

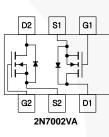
# 2N7002V / 2N7002VA N-Channel Enhancement Mode Field Effect Transistor

# Features

- Dual N-Channel MOSFET
- · Low On-Resistance
- · Low Gate Threshold Voltage
- Low Input Capacitance
- · Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- Lead Free by Design/RoHS Compliant







## **Ordering Information**

Part Number	Top Mark	Package	Packing Method	
2N7002V	AB	SOT-563F 6L	Tape and Reel	
2N7002VA	AC	SOT-563F 6L	Tape and Reel	

# **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^{\circ}$ C unless otherwise noted.

Symbol	Parameter		Value	Unit	
V <sub>DSS</sub>	Drain-Source Voltage		60	V	
V <sub>DGR</sub>	Drain-Gate Voltage ( $R_{GS} \le 1.0 \text{ M}\Omega$ )		60	V	
M	Cata Sauraa Valtaga	Continuous	±20	- V	
V <sub>GSS</sub> Gate-Source Vo	Gate-Source Voltage	Pulsed	±40		
I <sub>D</sub> Drain Cur	Drain Current	Continuous	280	mA	
	Jain Current	Pulsed	1.5	Α	
T <sub>J</sub> , T <sub>STG</sub>	T <sub>STG</sub> Junction and Storage Temperature Range		-55 to +150	°C	

# **Thermal Characteristics**

Values are at  $T_A = 25^{\circ}C$  unless otherwise noted.

Symbol	Parameter	Value	Unit
Total Device Dissipation		250	mW
PD	Derate Above T <sub>A</sub> = 25°C	2.0	mW/°C
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient <sup>(1)</sup>	500	°C/W

Note:

1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. Minimum land pad size.

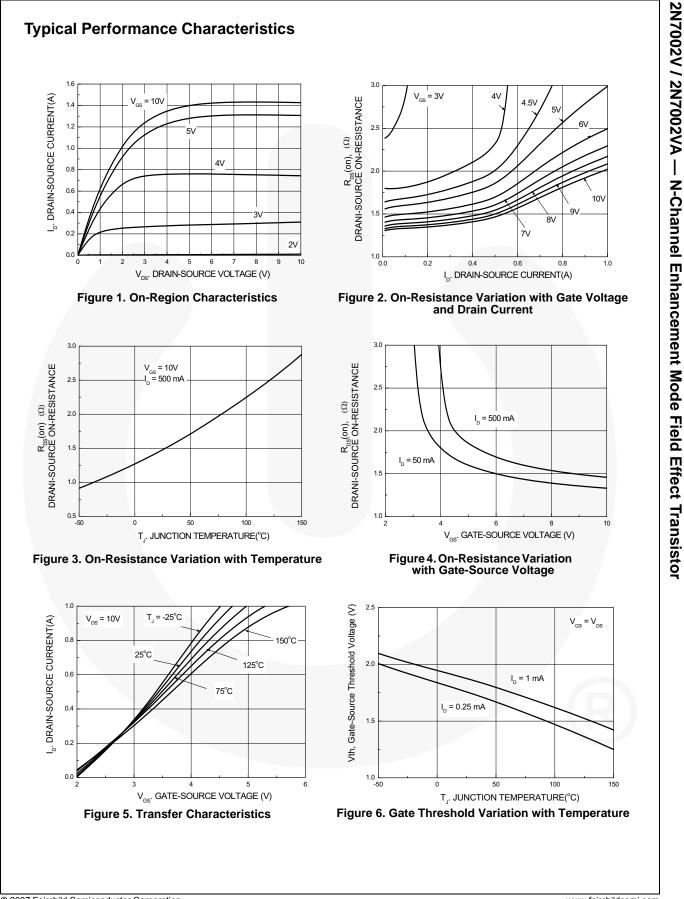
# **Electrical Characteristics**

Values are at  $T_A = 25^{\circ}C$  unless otherwise noted.

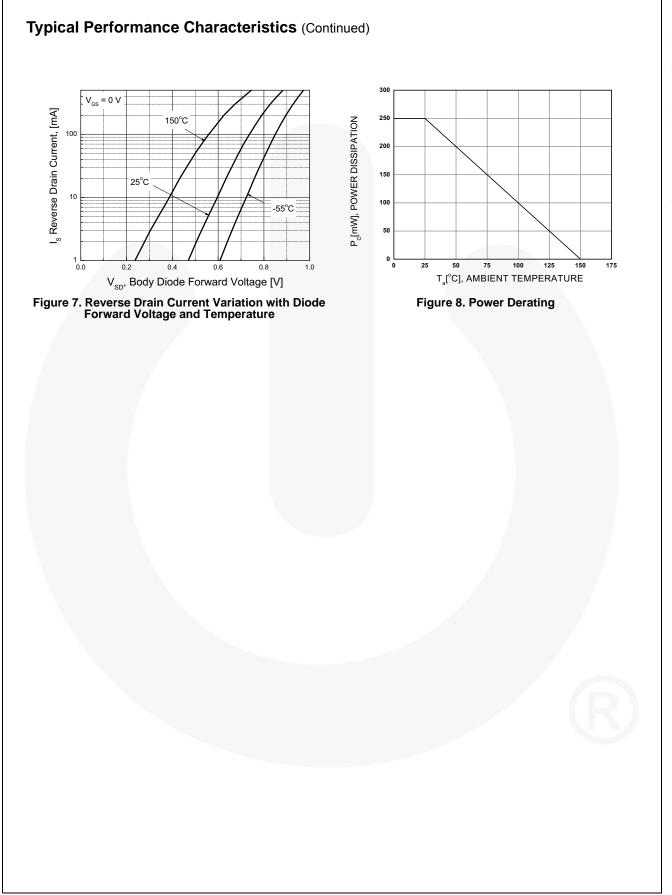
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Off Charact	teristics <sup>(2)</sup>			1		
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 μA	60	78		V
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V		0.001	1.0	
IDSS	Zero Gate Voltage Drain Current	in Current $V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, T_J = 125^{\circ}\text{C}$		7	500	μA
I <sub>GSS</sub>	Gate-Body Leakage	$V_{GS}$ = ±20 V, $V_{DS}$ = 0 V		0.2	±100	nA
On Charact	eristics <sup>(2)</sup>					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$	1.00	1.76	2.50	V
	Static Drain-Source On-Resistance	V <sub>GS</sub> = 5 V, I <sub>D</sub> = 0.05 A		1.6	7.5	Ω
R <sub>DS(ON)</sub>		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.5 A			2.0	
		$V_{GS}$ = 10 V, I <sub>D</sub> = 0.5 A, T <sub>J</sub> = 125°C		2.53	13.5	
I <sub>D(ON)</sub>	On-State Drain Current	$V_{GS}$ = 10 V, $V_{DS}$ = 7.5 V	1.50	1.43		А
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 0.2 A	80	356.5		mS
Dynamic C	haracteristics					
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		37.8	50	pF
C <sub>oss</sub>	Output Capacitance			12.4	25	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			6.5	7	pF
Switching (	Characteristics					
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 0.2 A,		5.85	20	ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time	V <sub>GEN</sub> = 10 V, R <sub>L</sub> = 150 Ω, R <sub>GEN</sub> = 25 Ω		12.5	20	ns

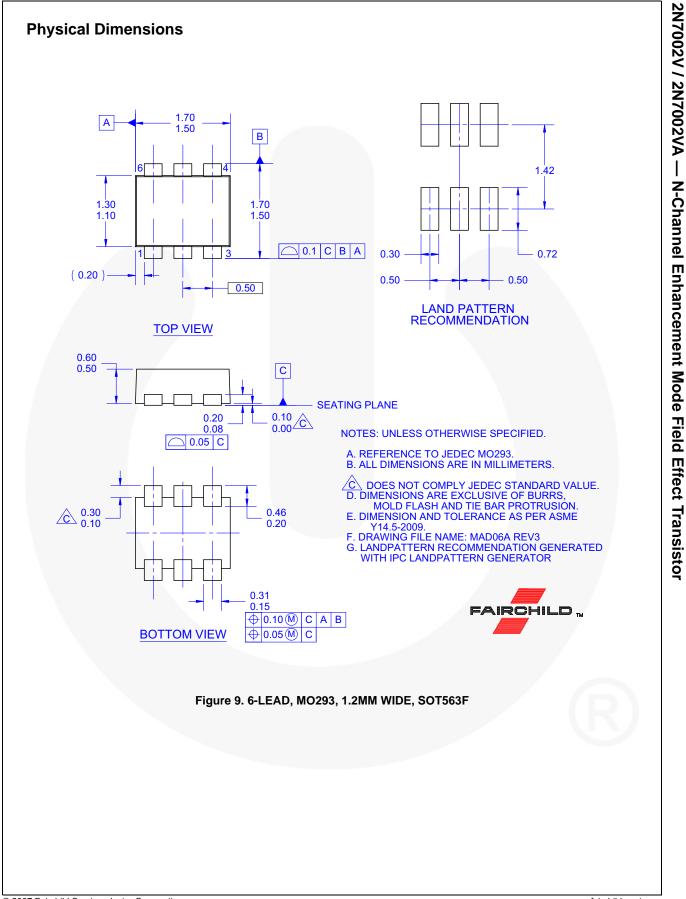
### Note:

2. Short duration test pulse used to minimize self-heating effect.



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