RoHS Compliant

4GB ECC DDR3 1.35V VLP Mini-DIMM

Product Specifications

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Version 1.2

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General Description

Apacer **78.B1GHC.4000C** is a 512M x 72 DDR3 SDRAM (Synchronous DRAM) Mini ECC DIMM. This high-density memory module consists of 9 pieces 512M x 8 bits with 8 banks DDR3 synchronous DRAMs in BGA packages and a 2K EEPROM. The module is a 244-pins dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM. The following provides general specifications of this module.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
78.B1GHC.4000C	12.8 GB/sec	1600 Mbps	800 MHz	CL11

Density	Organization	Component	Rank
4GB	512M x 72	512M x8*9	1

Key Parameters

MT/s	DDR3-1066	DDR3-1333	DDR3-1600	Unit
Grade	-CL7	-CL9	-CL11	
tCK (min)	1.875	1.5	1.25	ns
CAS latency	7	9	11	tCK
tRCD (min)	13.125	13.5	13.75	ns
tRP (min)	13.125	13.5	13.75	ns
tRAS (min)	37.5	36	35	ns
tRC (min)	50.625	49.5	48.75	ns
CL-tRCD-tRP	7-7-7	9-9-9	11-11-11	tCK

Specifications:

- Support ECC error detection and correction
- On-DIMM thermal sensor
- Organization: 512 words x 72 bits, 1 rank
- Integrating 9 pieces of 4G bits DDR3 SDRAM sealed FBGA
- Package: 244-pin socket type dual in-line memory module (Mini ECC DIMM)
- PCB: height 18.75 mm, lead pitch 0.6 mm (pin), lead-free (RoHS compliant)
- Power supply VDD: 1.35V (+0.1V ~ -0.067V)
- Backward compatible to VDD = VDDQ = 1.5V ± 0.075V

  -Supports DDR3L devices to be backward compatible in 1.5V applications
- Serial Presence Detect
- Eight Internal banks for concurrent operation
- Interface: SSTL_13
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- CAS Latency (CL): 6, 7, 8, 9, 10, 11
- CAS Write Latency (CWL): 5, 6, 7, 8
- Supports auto pre-charge option for each burst access
- Supports auto-refresh/self-refresh
- Refresh cycles: 7.8 μs at 0℃ < TC < +85℃
- PCB: 30µ gold finger

Features:

- Double-date-rate architecture: 2 data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted / received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Data mask (DM) for writing data
- Posted /CAS by programmable additive latency for enhanced command and data bus efficiency
- On-Die-Termination (ODT) for improved signal quality: Synchronous ODT/Dynamic ODT/Asynchronous ODT
- Multi-Purpose Register (MPR) for temperature read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /Reset pin for power-up sequence and reset function
- SRT range: normal/extended, auto/manual self-refresh
- Programmable output driver impedance control
- Commands entered at each positive clock input, while data and data mask are referenced to both edges of DQS

Pin Assignments

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VTT	31	DQ24	61	VDD	92	DQ40
2	VREFDQ	32	DQ25	62	A2	93	DQ41
3	VSS	33	VSS	63	VDD	94	VSS
4	DQ0	34	DQS3#	64	CK1	95	DQS5#
5	DQ1	35	DQS3	65	CK1#	96	DQS5
6	VSS	36	VSS	66	VDD	97	VSS
7	DQS0#	37	DQ26	67	VREFCA	98	DQ42
8	DQS0	38	DQ27	68	VDD	99	DQ43
9	VSS	39	VSS	69	NC	100	VSS
10	DQ2	40	CB0	70	VDD	101	DQ48
11	DQ3	41	CB1	71	A10	102	DQ49
12	VSS	42	VSS	72	BA0	103	VSS
13	DQ8	43	DQS8#	73	VDD	104	DQS6#
14	DQ9	44	DQS8	74	WE#	105	DQS6
15	VSS	45	VSS	75	CAS#	106	VSS
16	DQS1#	46	CB2	76	VDD	107	DQ50
17	DQS1	47	CB3	77	NC	108	DQ51
18	VSS	48	VSS	78	NC	109	VSS
19	DQ10	49	NC	79	VDD	110	DQ56
20	DQ11	50	RESET#	80	NC	111	DQ57
21	VSS	51	CKE0	81	NC	112	VSS
22	DQ16	52	VDD	82	VSS	113	DQS7#
23	DQ17	53	BA2	83	DQ32	114	DQS7
24	VSS	54	NC	84	DQ33	115	VSS
25	DQS2#	55	VDD	85	VSS	116	DQ58
26	DQS2	56	A11	86	DQS4#	117	DQ59
27	VSS	57	A7	87	DQS4	118	VSS
28	DQ18	58	VDD	88	VSS	119	SA0
29	DQ19	59	A5	89	DQ34	120	SCL
30	VSS	60	A4	90	DQ35	121	SA2
				91	VSS	122	VTT

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
123	VTT	153	DQ29	183	A3	214	DQ45
124	VSS	154	VSS	184	A1	215	VSS
125	DQ4	155	DM3	185	VDD	216	DM5
126	DQ5	156	NC	186	CK0	217	NC
127	VSS	157	VSS	187	CK0#	218	VSS
128	DM0	158	DQ30	188	VDD	219	DQ46
129	NC	159	DQ31	189	VDD	220	DQ47
130	VSS	160	VSS	190	EVENT#	221	VSS
131	DQ6	161	CB4	191	A0	222	DQ52
132	DQ7	162	CB5	192	VDD	223	DQ53
133	VSS	163	VSS	193	BA1	224	VSS
134	DQ12	164	DM8	194	VDD	225	DM6
135	DQ13	165	NC	195	RAS#	226	NC
136	VSS	166	VSS	196	CS0#	227	VSS
137	DM1	167	CB6	197	VDD	228	DQ54
138	NC	168	CB7	198	ODT0	229	DQ55
139	VSS	169	VSS	199	A13	230	VSS
140	DQ14	170	NC	200	VDD	231	DQ60
141	DQ15	171	NC	201	NC	232	DQ61
142	VSS	172	NC	202	NC	233	VSS
143	DQ20	173	VDD	203	VSS	234	DM7
144	DQ21	174	A15	204	DQ36	235	NC
145	VSS	175	A14	205	DQ37	236	VSS
146	DM2	176	VDD	206	VSS	237	DQ62
147	NC	177	A12	207	DM4	238	DQ63
148	VSS	178	A9	208	NC	239	VSS
149	DQ22	179	VDD	209	VSS	240	VDDSPD
150	DQ23	180	A8	210	DQ38	241	SA1
151	VSS	181	A6	211	DQ39	242	SDA
152	DQ28	182	VDD	212	VSS	243	VSS
				213	DQ44	244	VTT

*Unused pins in this module

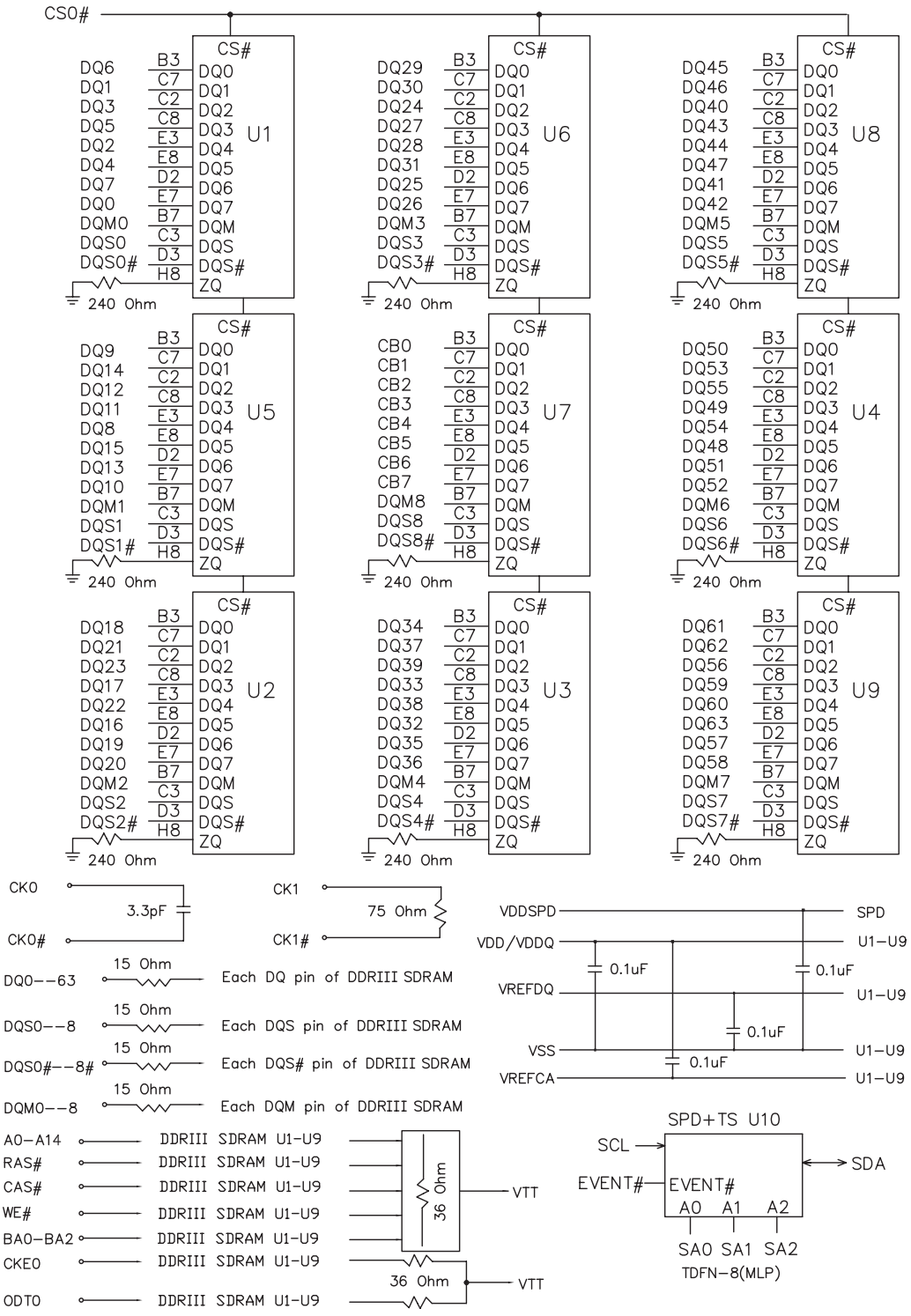
Pin Descriptions

Pin Name	Description
Ax	SDRAM address bus
BAx	SDRAM bank select
RAS#	SDRAM row address strobe
CAS#	SDRAM column address strobe
WE#	SDRAM write enable
CS0#	DIMM Rank Select Lines
CKE0	SDRAM clock enable lines
ODT0	On-die termination control lines
DQx	DIMM memory data bus
CBx	DIMM ECC check bits
DQSx	SDRAM data strobes(positive line of differential pair)
DQSx#	SDRAM data strobes(negative line of differential pair)
DMx	SDRAM data masks high data strobes(x8-based X72 DIMMs)
CKx	SDRAM clocks(positive line of differential pair)
CKx#	SDRAM clocks(negative line of differential pair)
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data line for EEPROM
SAx	I2C slave address select for EEPROM
VDD	SDRAM core power supply
VDDQ	SDRAM I/0 Driver power supply
VREFDQ	SDRAM I/O reference supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return(ground)
VDDSPD	Serial EEPROM positive power supply
NC	Spare pins(no connect)
RESET#	Set DRAMs to Known State
VTT	SDRAM I/O termination supply
EVENT#	An output of the thermal sensor to indicate critical module temperature

*IC Component Composition:

128Mx8	A0~A13
256Mx8	A0~A14
512Mx8	A0~A15
1024Mx8	A0~A15

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Description	Units
Voltage on VDD pin relative to Vss	V_{DD}	- 0.4 V ~ 1.975 V	V
Voltage on VDDQ pin relative to Vss	V_{DDQ}	- 0.4 V ~ 1.975 V	V
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.4 V ~ 1.975 V	V
Storage Temperature	TSTG	-55 to +100	℃

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

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DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Normal Operating Temperature Range	0 to 85	℃	1,2
	Extended Temperature Range	85 to 95	℃	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported during operation, the DRAM case temperature must be maintained between 0℃ - 85℃ under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85℃ and 95℃ case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs.
   b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

Operating Conditions

Recommended DC Operating Conditions - DDR3L (1.35V) operation

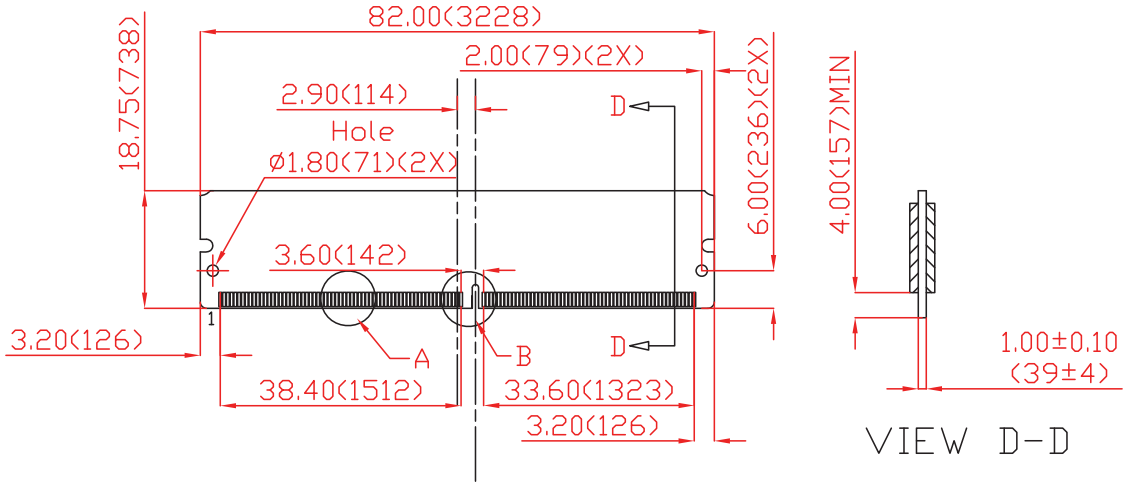
Symbol	Parameter	Rating			Units
		Min.	Typ.	Max.	
VDD	Supply Voltage	1.283	1.35	1.45	V
VDDQ	Supply Voltage for Output	1.283	1.35	1.45	V

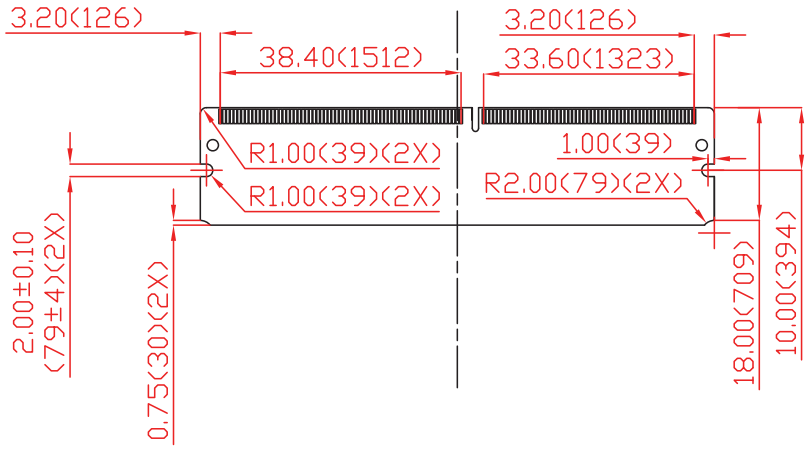
Notes:

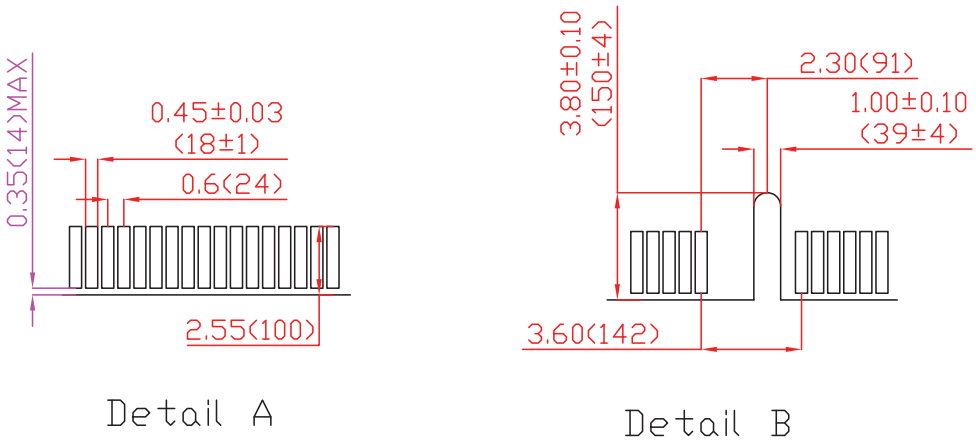
1. If minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
2. Under 1.5V operation, this DDR3L device operates to the DDR3 specifications under the same speed timings as defined for this device.
3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation.

Mechanical Drawing

Unit: mm







30µ gold finger

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Revision History

Revision	Date	Description	Remark
0.9	08/28/2012	Official release	
1.0	08/29/2012	release	
1.1	07/23/2013	1. Changed headquarters address 2. Added 30µ gold finger	
1.2	05/08/2015	Updated Mechanical Drawing	

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