1.5GHz–2.4GHz High Linearity Direct Quadrature Modulator

FEATURES

- **High Input Impedance Version of the LT5528**
- **Direct Conversion to 1.5GHz – 2.4GHz**
- **High OIP3: 22.8dBm at 2GHz**
- **Low Output Noise Floor at 20MHz Offset:**
  No RF: –158.2dBm/Hz
  P_{OUT} = 4dBm: –152.5dBm/Hz
- **4-Ch W-CDMA ACPR: –64dBc at 2.14GHz**
- **Integrated LO Buffer and LO Quadrature Phase Generator**
- **50Ω AC-Coupled Single-Ended LO and RF Ports**
- **Low Carrier Leakage: –49dBm at 2GHz**
- **High Image Rejection: 40dB at 2GHz**
- 16-Lead QFN 4mm × 4mm Package

APPLICATIONS

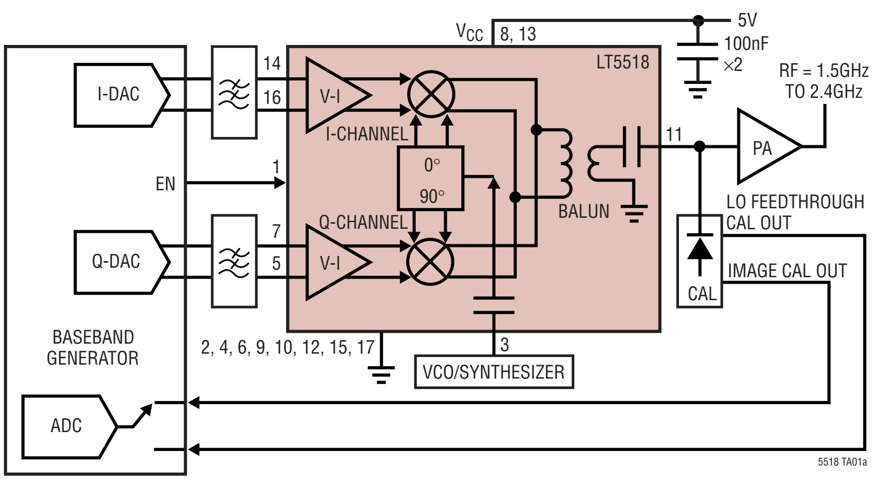
- Infrastructure Tx for DCS, PCS and UMTS Bands
- Image Reject Up-Converters for DCS, PCS and UMTS Bands
- Low Noise Variable Phase-Shifter for 1.5GHz to 2.4GHz Local Oscillator Signals

DESCRIPTION

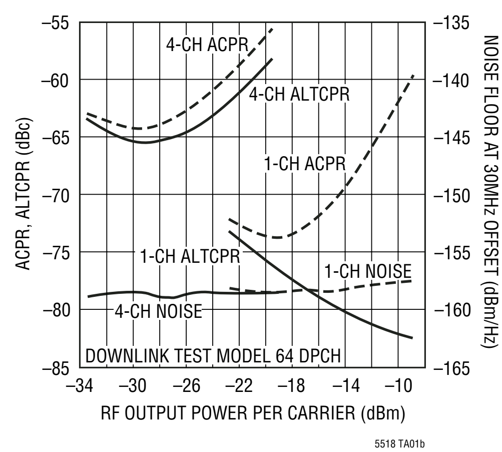
The LT®5518 is a direct I/Q modulator designed for high performance wireless applications, including wireless infrastructure. It allows direct modulation of an RF signal using differential baseband I and Q signals. It supports PHS, GSM, EDGE, TD-SCDMA, CDMA, CDMA2000, W-CDMA and other systems. It may also be configured as an image reject up-converting mixer, by applying 90° phase-shifted signals to the I and Q inputs. The high impedance I/Q baseband inputs consist of voltage-to-current converters that in turn drive double-balanced mixers. The outputs of these mixers are summed and applied to an on-chip RF transformer, which converts the differential mixer signals to a 50Ω single-ended output. The balanced I and Q baseband input ports are intended for DC coupling from a source with a common mode voltage level of about 2.1V. The LO path consists of an LO buffer with single-ended input, and precision quadrature generators that produce the LO drive for the mixers. The supply voltage range is 4.5V to 5.25V.

TYPICAL APPLICATION

1.5GHz to 2.4GHz Direct Conversion Transmitter Application with LO Feedthrough and Image Calibration Loop



W-CDMA ACPR, AltCPR and Noise vs RF Output Power at 2140MHz for 1 and 4 Channels



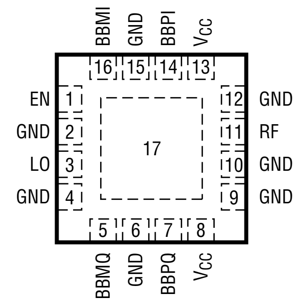
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 5.5V
Common Mode Level of BBPI, BBMI and
BBPQ, BBMQ 2.5V
Operating Ambient Temperature
(Note 2) .... –40°C to 85°C
Storage Temperature Range.................. –65°C to 125°C
Voltage on Any Pin
Not to Exceed...................... –500mV to V_{CC} + 500mV

PACKAGE/ORDER INFORMATION

TOP VIEW



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W

EXPOSED PAD (PIN 17) IS GND
MUST BE SOLDERED TO THE PCB

ORDER PART NUMBER	UF PART MARKING
LT5518EUF	5518

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 2GHz, f_{RF} = 2.002GHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 2.06V_{DC}, Baseband Input Frequency = 2MHz, I and Q 90° shifted (upper sideband selection). $P_{RF, OUT}$ = –10dBm, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Output (RF)						
f_{RF}	RF Frequency Range RF Frequency Range	–3dB Bandwidth –1dB Bandwidth		1.5 to 2.4 1.7 to 2.2		GHz GHz
$S_{22, ON}$	RF Output Return Loss	EN = High (Note 6)		–14		dB
$S_{22, OFF}$	RF Output Return Loss	EN = Low (Note 6)		–12		dB
NFloor	RF Output Noise Floor	No Input Signal (Note 8) P_{OUT} = 4dBm (Note 9) P_{OUT} = 4dBm (Note 10)		–158.2 –152.5 –151.1		dBm/Hz dBm/Hz dBm/Hz
G_P	Conversion Power Gain	P_{OUT}/P_{IN}, I&Q		10.6		dB
G_V	Conversion Voltage Gain	20 • log($V_{OUT, 50\Omega}/V_{IN, DIFF, I or Q}$)		–4		dB
P_{OUT}	Absolute Output Power	1$V_{P-P, DIFF}$ CW Signal, I and Q		0		dBm
$G_{3LO vs LO}$	3 • LO Conversion Gain Difference	(Note 17)		–28		dB
OP1dB	Output 1dB Compression	(Note 7)		8.5		dBm
OIP2	Output 2nd Order Intercept	(Notes 13, 14)		49		dBm
OIP3	Output 3rd Order Intercept	(Notes 13, 15)		22.8		dBm
IR	Image Rejection	(Note 16)		–40		dBc
LOFT	Carrier Leakage (LO Feedthrough)	EN = High, P_{LO} = 0dBm (Note 16) EN = Low, P_{LO} = 0dBm (Note 16)		–49 –58		dBm dBm
LO Input (LO)						
f_{LO}	LO Frequency Range			1.5 to 2.4		GHz
P_{LO}	LO Input Power		–10	0	5	dBm
$S_{11, ON}$	LO Input Return Loss	EN = High (Note 6)		–18		dB
$S_{11, OFF}$	LO Input Return Loss	EN = Low (Note 6)		–5		dB
NF_{LO}	LO Input Referred Noise Figure	(Note 5) at 2GHz		14		dB
G_{LO}	LO to RF Small Signal Gain	(Note 5) at 2GHz		23.8		dB
$IIP3_{LO}$	LO Input Linearity	(Note 5) at 2GHz		–9		dBm

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 2GHz, f_{RF} = 2.002GHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 2.06V_{DC}, Baseband Input Frequency = 2MHz, I and Q 90° shifted (upper sideband selection). $P_{RF, OUT}$ = –10dBm, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Baseband Inputs (BBPI, BBMI, BBPQ, BBMQ)						
BW_{BB}	Baseband Bandwidth	–3dB Bandwidth		400		MHz
V_{CMBB}	DC Common Mode Voltage	(Note 4)		2.06		V
$R_{IN, DIFF}$	Differential Input Resistance	Between BBPI and BBMI (or BBPQ and BBMQ)		2.9		kΩ
$R_{IN, CM}$	Common Mode Input Resistance	BBPX and BBMX Shorted Together		105		Ω
$I_{CM, COMP}$	Common Mode Compliance Current Range	BBPX and BBMX Shorted Together (Note 18)		–730 to 480		µA
P_{LO2BB}	Carrier Feedthrough on BB	P_{OUT} = 0 (Note 4)		–40		dBm
IP1dB	Input 1dB Compression Point	Differential Peak-to-Peak (Note 7)		2.7		$V_{P-P, DIFF}$
$\Delta G_{I/Q}$	I/Q Absolute Gain Imbalance			0.06		dB
$\Delta \phi_{I/Q}$	I/Q Absolute Phase Imbalance			1		deg
Power Supply (V_{CC})						
V_{CC}	Supply Voltage		4.5	5	5.25	V
$I_{CC, ON}$	Supply Current	EN = High		128	145	mA
$I_{CC, OFF}$	Supply Current, Sleep Mode	EN = 0V		0.05	50	µA
t_{ON}	Turn-On Time	EN = Low to High (Note 11)		0.2		µs
t_{OFF}	Turn-Off Time	EN = High to Low (Note 12)		1.3		µs
Enable (EN), Low = Off, High = On						
Enable	Input High Voltage Input High Current	EN = High EN = 5V	1.0	 240		V µA
Sleep	Input Low Voltage	EN = Low			0.5	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Specifications over the –40°C to 85°C temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Tests are performed as shown in the configuration of Figure 8.

Note 4: On each of the four baseband inputs BBPI, BBMI, BBPQ and BBMQ.

Note 5: V(BBPI) – V(BBMI) = 1V_{DC}, V(BBPQ) – V(BBMQ) = 1V_{DC}.

Note 6: Maximum value within –1dB bandwidth.

Note 7: An external coupling capacitor is used in the RF output line.

Note 8: At 20MHz offset from the LO signal frequency.

Note 9: At 20MHz offset from the CW signal frequency.

Note 10: At 5MHz offset from the CW signal frequency.

Note 11: RF power is within 10% of final value.

Note 12: RF power is at least 30dB lower than in the ON state.

Note 13: Baseband is driven by 2MHz and 2.1MHz tones. Drive level is set in such a way that the two resulting RF output tones are –10dBm each.

Note 14: IM2 measured at LO frequency + 4.1MHz.

Note 15: IM3 measured at LO frequency + 1.9MHz and LO frequency + 2.2MHz.

Note 16: Amplitude average of the characterization data set without image or LO feedthrough nulling (unadjusted).

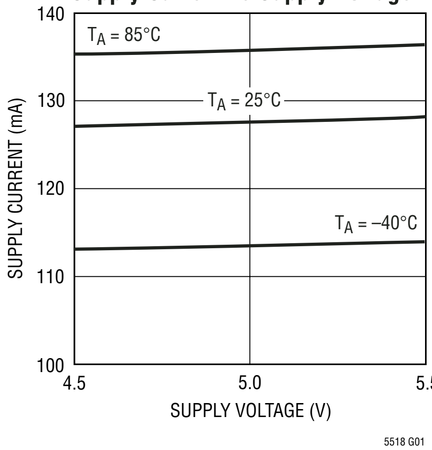
Note 17: The difference in conversion gain between the spurious signal at f = 3 • LO – BB versus the conversion gain at the desired signal at f = LO + BB for BB = 2MHz and LO = 2GHz.

Note 18: Common mode current range where the common mode (CM) feedback loop biases the part properly. The common mode current is the sum of the current flowing into the BBPI (or BBPQ) pin and the current flowing into the BBMI (or BBMQ) pin.

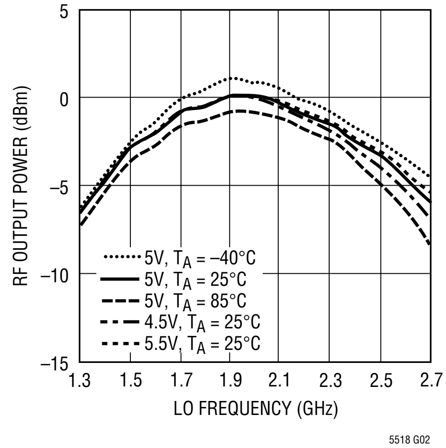
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 2.14GHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 2.06V_{DC}, Baseband Input Frequency f_{BB} = 2MHz, I and Q 90° shifted without image or LO feedthrough nulling. f_{RF} = f_{BB} + f_{LO} (upper sideband selection). $P_{RF, OUT}$ = –10dBm (–10dBm/tone for 2-tone measurements), unless otherwise noted. (Note 3)

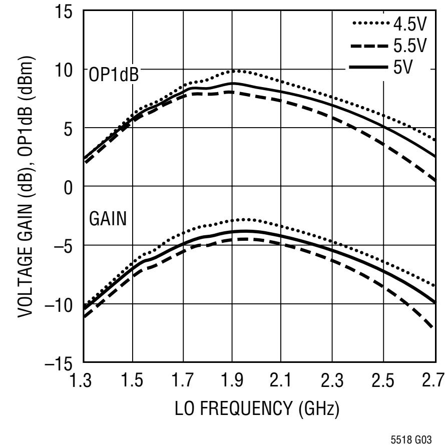
Supply Current vs Supply Voltage



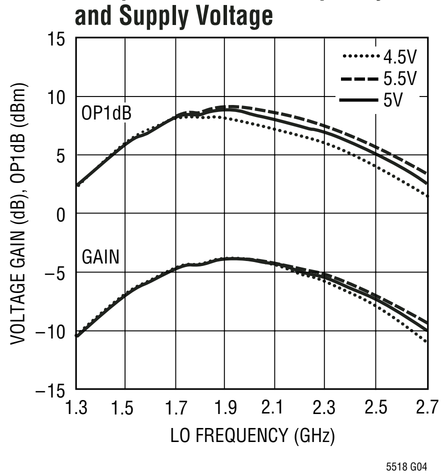
RF Output Power vs LO Frequency at 1V_{P-P} Differential Baseband Drive



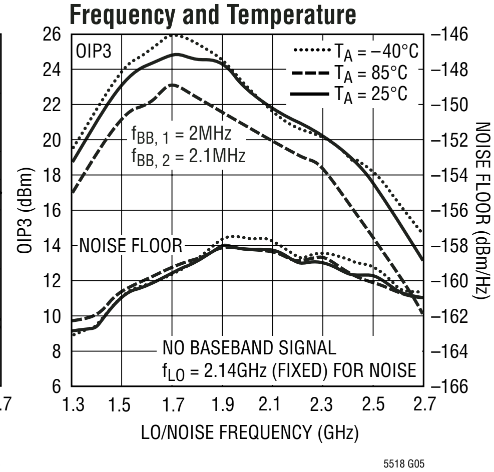
Voltage Gain and Output 1dB Compression vs LO Frequency and Temperature



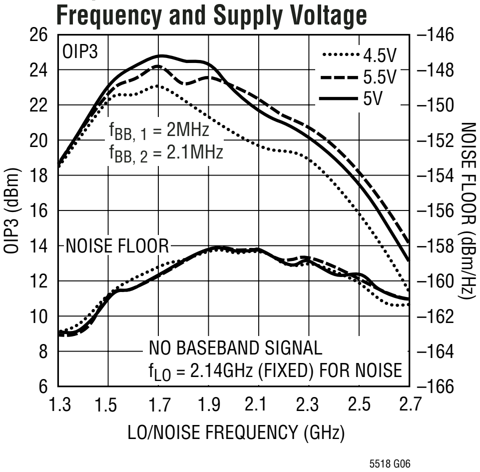
Voltage Gain and Output 1dB Compression vs LO Frequency and Supply Voltage



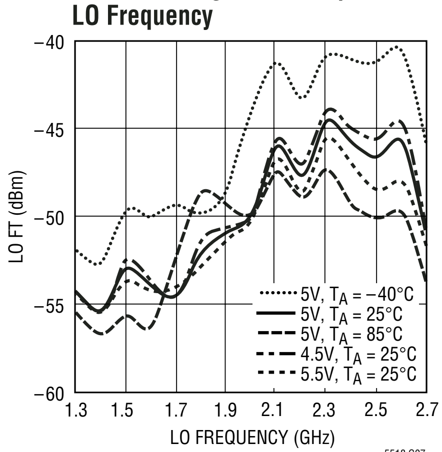
Output IP3 and Noise Floor vs LO Frequency and Temperature



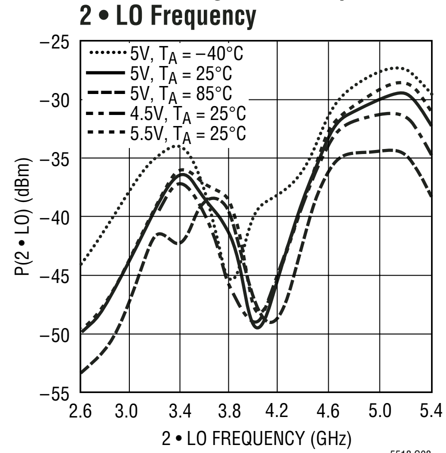
Output IP3 and Noise Floor vs LO Frequency and Supply Voltage



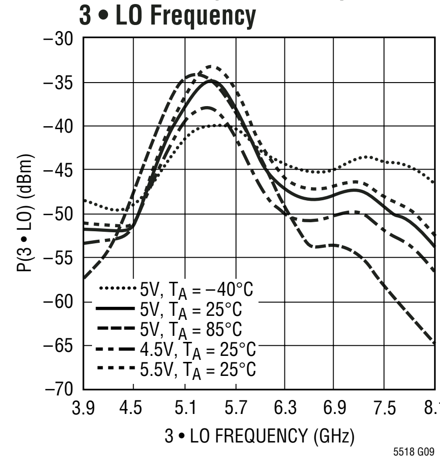
LO Feedthrough to RF Output vs LO Frequency



2 • LO Leakage to RF Output vs 2 • LO Frequency



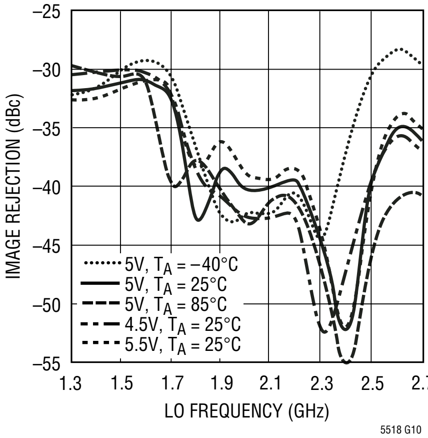
3 • LO Leakage to RF Output vs 3 • LO Frequency



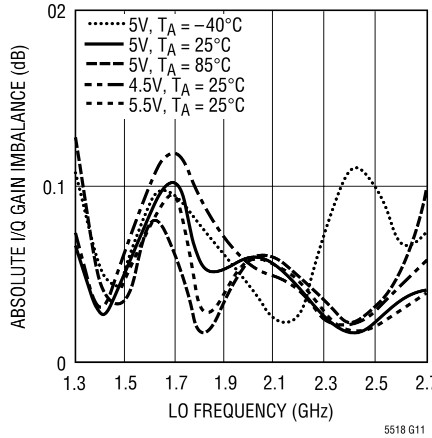
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 2.14GHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 2.06V_{DC}, Baseband Input Frequency f_{BB} = 2MHz, I and Q 90° shifted without image or LO feedthrough nulling. $f_{RF} = f_{BB} + f_{LO}$ (upper sideband selection). $P_{RF, OUT}$ = –10dBm (–10dBm/tone for 2-tone measurements), unless otherwise noted. (Note 3)

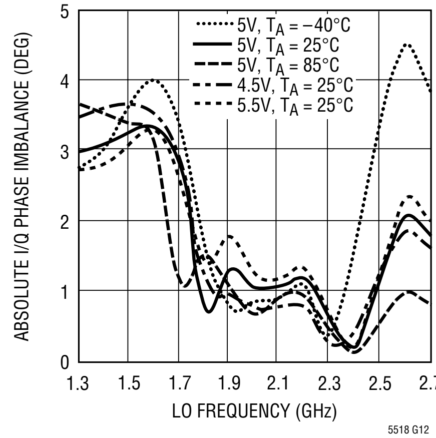
Image Rejection vs LO Frequency



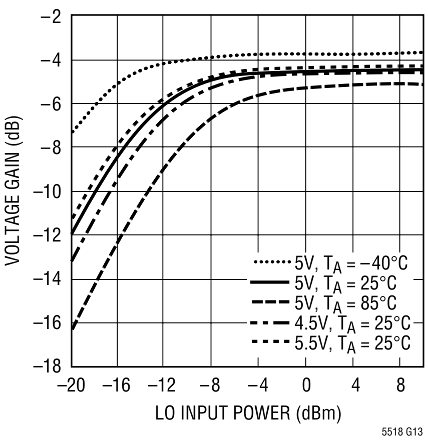
Absolute I/Q Gain Imbalance vs LO Frequency



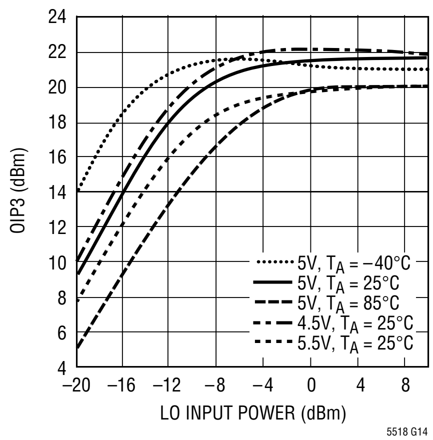
Absolute I/Q Phase Imbalance vs LO Frequency



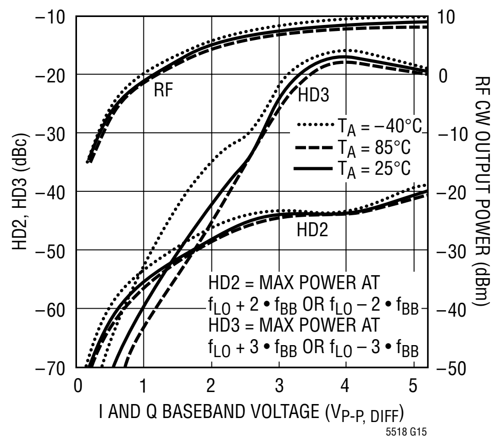
Voltage Gain vs LO Power



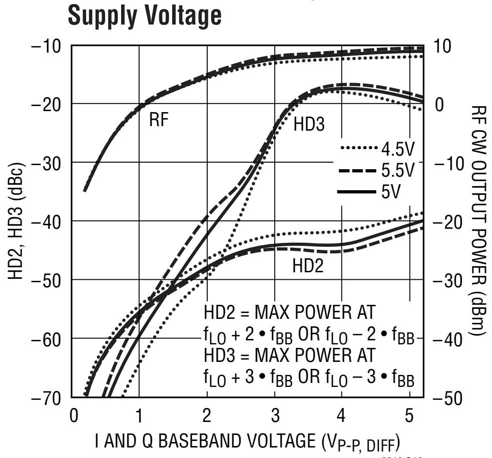
Output IP3 vs LO Power



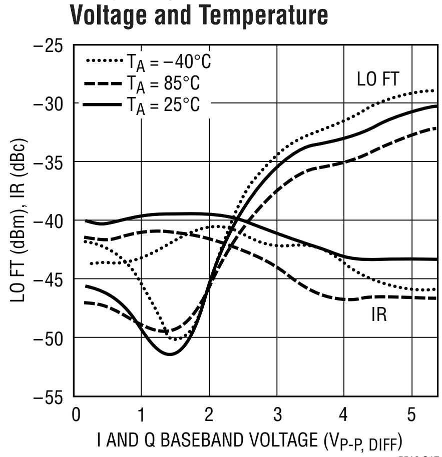
RF CW Output Power, HD2 and HD3 vs Baseband Voltage and Temperature



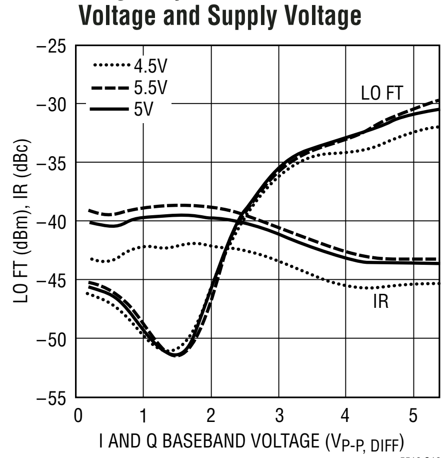
RF CW Output Power, HD2 and HD3 vs Baseband Voltage and Supply Voltage



LO Feedthrough to RF Output and Image Rejection vs Baseband Voltage and Temperature



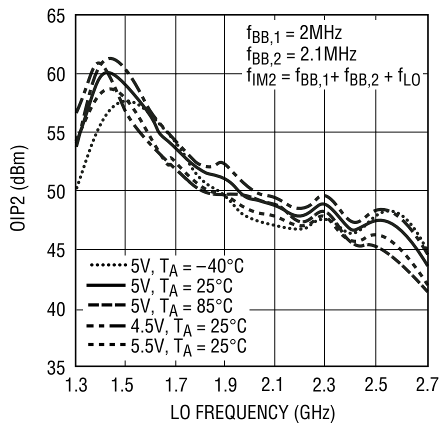
LO Feedthrough to RF Output and Image Rejection vs Baseband Voltage and Supply Voltage



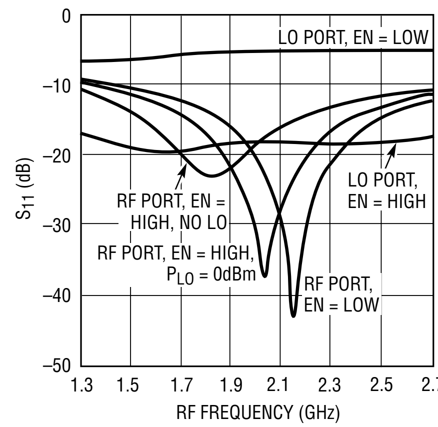
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 2.14GHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 2.06V_{DC}, Baseband Input Frequency f_{BB} = 2MHz, I and Q 90° shifted without image or LO feedthrough nulling. $f_{RF} = f_{BB} + f_{LO}$ (upper sideband selection). $P_{RF, OUT}$ = –10dBm (–10dBm/tone for 2-tone measurements), unless otherwise noted. (Note 3)

Output IP2 vs LO Frequency



LO and RF Port Return Loss vs RF Frequency



PIN FUNCTIONS

EN (Pin 1): Enable Input. When the enable pin voltage is higher than 1V, the IC is turned on. When the input voltage is less than 0.5V, the IC is turned off.

GND (Pins 2, 4, 6, 9, 10, 12, 15): Ground. Pins 6, 9, 15 and 17 (exposed pad) are connected to each other internally. Pins 2 and 4 are connected to each other internally and function as the ground return for the LO signal. Pins 10 and 12 are connected to each other internally and function as the ground return for the on-chip RF balun. For best RF performance, pins 2, 4, 6, 9, 10, 12, 15 and the Exposed Pad (Pin 17) should be connected to the printed circuit board ground plane.

LO (Pin 3): LO Input. The LO input is an AC-coupled single-ended input with approximately 50Ω input impedance at RF frequencies. Externally applied DC voltage should be within the range –0.5V to V_{CC} + 0.5V in order to avoid turning on ESD protection diodes.

BBPQ, BBMQ (Pins 7, 5): Baseband Inputs for the Q-Channel, with 2.9kΩ Differential Input Impedance. Internally biased at about 2.06V. Applied common mode voltage must stay below 2.5V.

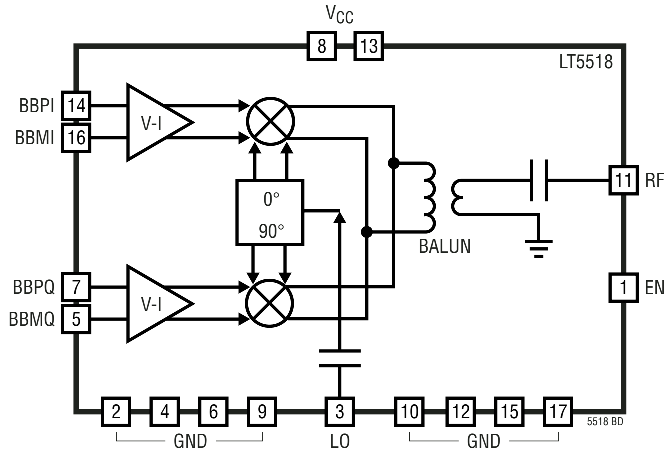
V_{CC} (Pins 8, 13): Power Supply. Pins 8 and 13 are connected to each other internally. It is recommended to use 0.1μF capacitors for decoupling to ground on each of these pins.

RF (Pin 11): RF Output. The RF output is an AC-coupled single-ended output with approximately 50Ω output impedance at RF frequencies. Externally applied DC voltage should be within the range –0.5V to V_{CC} + 0.5V in order to avoid turning on ESD protection diodes.

BBPI, BBMI (Pins 14, 16): Baseband Inputs for the I-Channel, with 2.9kΩ Differential Input Impedance. Internally biased at about 2.06V. Applied common mode voltage must stay below 2.5V.

Exposed Pad (Pin 17): Ground. This pin must be soldered to the printed circuit board ground plane.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT5518 consists of I and Q input differential voltage-to-current converters, I and Q up-conversion mixers, an RF output balun, an LO quadrature phase generator and LO buffers.

External I and Q baseband signals are applied to the differential baseband input pins, BBPI, BBMI, and BBPQ, BBMQ. These voltage signals are converted to currents and translated to RF frequency by means of double-balanced up-converting mixers. The mixer outputs are combined in an RF output balun, which also transforms the output impedance to 50Ω. The center frequency of the resulting RF signal is equal to the LO signal frequency. The LO input drives a phase shifter which splits the LO signal into in-phase and quadrature LO signals. These LO signals are then applied to on-chip buffers which drive the up-conversion mixers. Both the LO input and RF output are single-ended, 50Ω-matched and AC coupled.

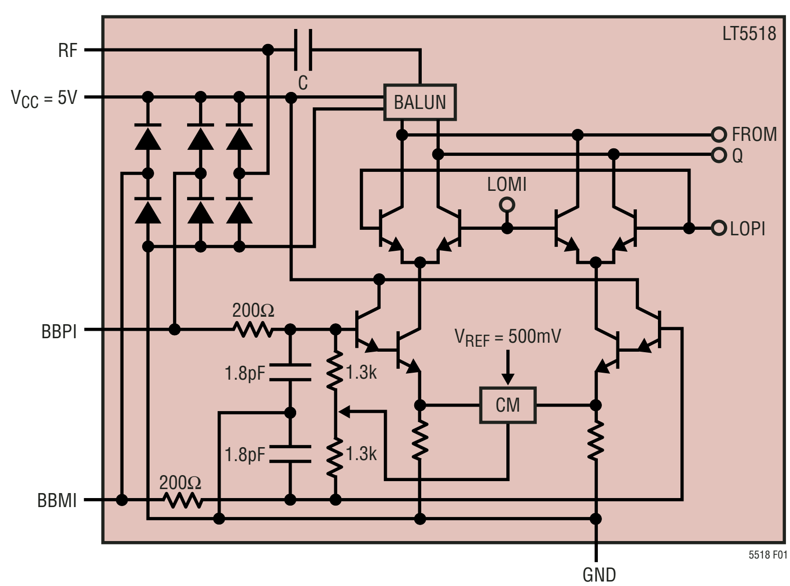


Figure 1. Simplified Circuit Schematic of the LT5518 (Only I-Half is Drawn)

APPLICATIONS INFORMATION

Baseband Interface

The baseband inputs (BBPI, BBMI), (BBPQ, BBMQ) present a differential input impedance of about 2.9kΩ. At each of the four baseband inputs, a lowpass filter using 200Ω and 1.8pF to ground is incorporated (see Figure 1), which limits the baseband bandwidth to approximately 250MHz (–1dB point). The common mode voltage is about 2.06V and is slightly temperature dependent. At $T_A = -40^oC$, the common mode voltage is about 2.19V and at $T_A = 85^oC$ it is about 1.92V.

If the I/Q signals are DC-coupled to the LT5518, it is important that the applied common mode voltage level of the I and Q inputs is about 2.06V in order to properly bias the LT5518. Some I/Q test generators allow setting the common mode voltage independently. In this case, the common mode voltage of those generators must be set to 1.03V to match the LT5518 internal bias, because for DC signals, there is no –6dB source-load voltage division (see Figure 2).

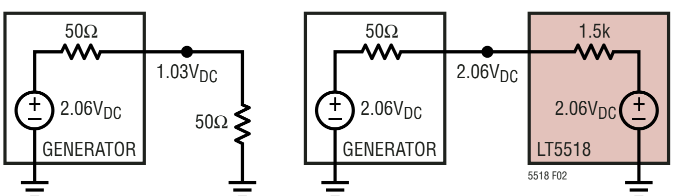


Figure 2. DC Voltage Levels for a Generator Programmed at $1.03V_{DC}$ for a 50Ω Load and for the LT5518 as a Load

The LT5518 should be driven differentially; otherwise, the even-order distortion products will degrade the overall linearity severely. Typically, a DAC will be the signal source for the LT5518. A reconstruction filter should be placed between the DAC output and the LT5518's baseband inputs. DC coupling between the DAC outputs and the LT5518 baseband inputs is recommended. Active level shifters may be required to adapt the common mode level of the DAC outputs to the common mode input voltage of the LT5518. It is also possible to achieve a DC level shift with passive components, depending on the application. For example, if flat frequency response to DC is not required, then the interface circuit of Figure 3 may be used. This figure shows a commonly used 0mA – 20mA DAC output followed by a passive 5th order lowpass filter. The DC-coupled interface allows adjustment of the DAC's differential output current to minimize the LO to RF feedthrough. Resistors R3A, R3B, R4A and R4B translate the DAC's output common mode level from about $0.5V_{DC}$ to the LT5518's input at about $2.06V_{DC}$. For these resistors, 1% accuracy is recommended. For different ambient temperatures, the LT5518 input common mode level varies with a temperature coefficient of about –2.7mV/°C. The internal common mode feedback loop will correct these level changes in order to bias the LT5518 at the correct operating point. Resistors R3 and R4 are chosen high enough that the LT5518 common mode compliance current value will not be exceeded at the inputs of the LT5518 as a result of temperature shifts. Capacitors C4A and C4B minimize the input signal attenuation caused by the network R3A, R3B, R4A and R4B. This results in a gain difference between low frequency and high frequency baseband signals. The high frequency baseband –3dB corner point is approximately given by:

$$f_{-3dB} = 1/[2\pi \bullet C4A \bullet (R3A||R4A||(R_{IN,\ DIFF}/2)]$$

In this example, f_{-3dB} = 58kHz.

This corner point should be set significantly lower than the minimum baseband signal frequency by choosing large enough capacitors C4A and C4B. For signal frequencies significantly lower than f_{-3dB}, the gain is reduced by approximately

$$G_{DC} = 20 \bullet \log [R3A||(R_{IN,\ DIFF}/2)]/[R3A||(R_{IN,\ DIFF}/2) + R4A]$$

In this example, G_{DC} = –11dB.

Inserting the network of R3A, R3B, R4A, R4B, C4A and C4B has the following consequences:

- Reduced LO feedthrough adjustment range. LO to RF feedthrough can be reduced by adjusting the differential DC offset voltage applied to the I and/or Q inputs. Because of the DC gain reduction, the range of adjustment is reduced. The resolution of the offset adjustment is improved by the same gain reduction factor.
- DC notch for uneven number of channels. The interface drawn in Figure 3 might not be practical for an uneven number of channels, since the gain at DC is lower and will appear in the center of (one of) the channel(s). In that case, a DC-coupled level shifting circuit is required, or the LT5528 might be a better solution.

APPLICATIONS INFORMATION

- Introduction of a (low frequency) time constant during startup. For TDMA-like systems the time constant introduced by C4A and C4B can cause some delay during start-up. The associated time constant is approximately given by $T_D = R_{IN,\ CM} \bullet (C4A + C4B)$. In this example it will result in a delay of about $T_D = 105 \bullet 6.6n = 693ns$.

The maximum sinusoidal single sideband RF output power is about 5.5dBm for a full 0mA to 20mA DAC swing. This maximum RF output level is usually limited by the compliance voltage range of the DAC (V_{COMPL}) which is assumed here to be 1.25V. When the DAC output voltage swing is larger than this compliance voltage, the baseband signal will distort and linearity requirements usually will not be met. The following situations can cause the DAC's compliance voltage limit to be exceeded:

1. Too high DAC load impedance. If the DC impedance to ground is higher than $V_{COMPL}/I_{MAX} = 1.25/0.02 = 62.5\Omega$, the compliance voltage is exceeded for a full DAC swing. In Figure 3, two 100Ω resistors in parallel are used, resulting in a DC impedance to ground of 50Ω.

2. Too much DC offset. In some DACs, an additional DC offset current can be set. For example, if the maximum offset current is set to $I_{MAX}/8 = 2.5mA$, then the maximum DC DAC load impedance to ground is reduced to $V_{COMPL}/I_{MAX} \bullet (1 + 1/8) = 1.25/0.0225 = 55\Omega$.

3. DC shift caused by R3A, R3B, R4A and R4B if used. The DC shift network consisting of R3A, R3B, R4A and R4B will increase the voltage on the DAC output by dumping an extra current into resistors R1A, R1B, R2A and R2B. This current is about $(V_{CC} - V_{DAC})/(R3A + R4A) = (5 - 0.5)/(3.01k + 5.63k) = 0.52mA$. Maximum impedance to ground will then be $V_{COMPL}/(I_{MAX} + I_{LS}) = 1.25/0.02052 = 60.9\Omega$.

4. Reflection of out-of-band baseband signal power. DAC output signal components higher than the cut-off frequency of the lowpass filter will not see R2A and R2B as load resistors and therefore will see only R1A, R1B and the filter components as a load. Therefore, it is important to start the lowpass filter with a capacitor (C1), in order to shunt the DAC higher frequency components and thereby, limit the required extra voltage headroom.

The LT5518's output 1dB compression point is about 8.5dBm, and with the interface network described above, a common DAC cannot drive the part into compression. However, it is possible to increase the driving capability by using a negative supply voltage. For example, if a –1V supply is available, resistors R1A, R1B, R2A and R2B can be made 200Ω each and connected with one side to the –1V supply instead of ground. Typically, the voltage compliance range of the DAC is –1V to 1.25V, so the DAC's output voltage will stay within this range. Almost 6dB extra voltage swing is available, thus enabling the DAC to drive the LT5518 beyond its 1dB compression point. Resistors R3A, R3B, R4A, R4B and the lowpass filter components must be adjusted for this case.

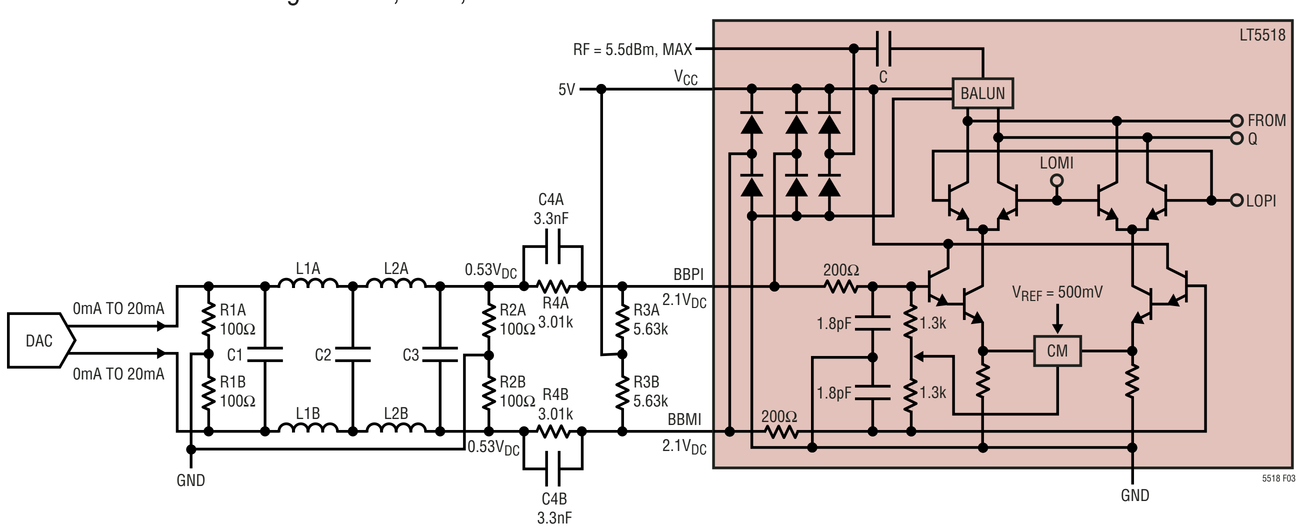


Figure 3. LT5518 5th Order Filtered Baseband Interface with Common DAC (Only I-Channel is Shown)

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Some DACs use an output common mode voltage of 3.3V. In that case, the interface circuit drawn in Figure 4 may be used. The performance is very similar to the performance of the DAC interface drawn in Figure 3, since the source and load impedances of the lowpass ladder filter are both 200Ω differential and the current drive is the same. There are some small differences:

- The baseband drive capability cannot be improved using an extra supply voltage, since the compliance range of the DACs in Figure 4 is typically 3.3V – 0.5V to 3.3V + 0.5V, so its range has already been fully used.
- G_{DC} and f_{-3dB} are a little different, since R3A (and R3B) is 4.99k instead of 5.6k to accommodate the proper DC level shift.

LO Section

The internal LO input amplifier performs single-ended to differential conversion of the LO input signal. Figure 5 shows the equivalent circuit schematic of the LO input.

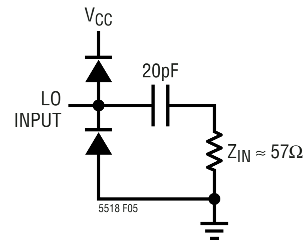

Figure 5. Equivalent Circuit Schematic of the LO Input

The internal, differential LO signal is split into in-phase and quadrature (90° phase shifted) signals that drive LO buffer sections. These buffers drive the double balanced I and Q mixers. The phase relationship between the LO input and the internal in-phase LO and quadrature LO signals is fixed, and is independent of start-up conditions. The phase shifters are designed to deliver accurate quadrature signals for an LO frequency near 2GHz. For frequencies significantly below 1.8GHz or above 2.4GHz, the quadrature accuracy will diminish, causing the image rejection to degrade. The LO pin input impedance is about 50Ω, and the recommended LO input power is 0dBm. For lower LO input power, the gain, OIP2, OIP3 and dynamic range will degrade, especially below –5dBm and at T_A = 85°C. For high LO input power (e.g. 5dBm), the LO feedthrough will increase, without improvement in linearity or gain. Harmonics present on the LO signal can degrade the image rejection, because they introduce a small excess phase shift in the internal phase splitter. For the second (at 4GHz) and third harmonics (at 6GHz) at –20dBc level, the introduced signal at the image frequency is about –55dBc or lower, corresponding to an excess phase shift much less than 1 degree. For the second and third harmonics at –10dBc, still the introduced signal at the image frequency is about –46dBc. Higher harmonics than the third will have less impact. The LO return loss typically will be better than 14dB over the 1.7GHz to 2.4GHz range. Table 1 shows the LO port input impedance vs frequency.

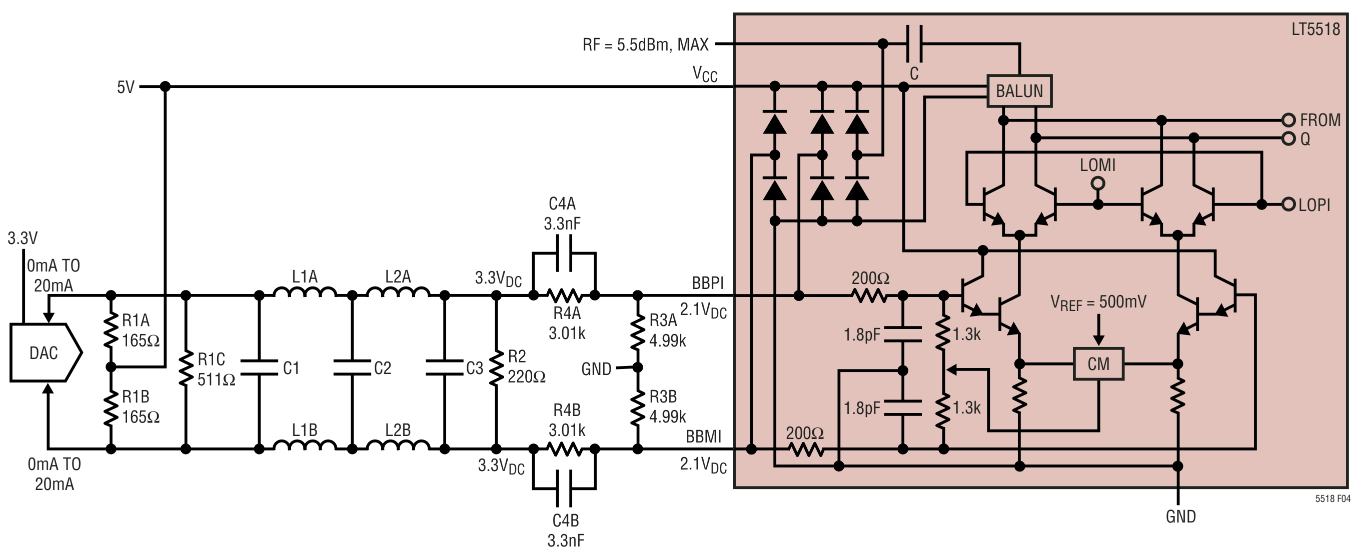

Figure 4. LT5518 5th Order Filtered Baseband Interface with 3.3V$_{CM}$ DAC (Only I-Channel is Shown).

APPLICATIONS INFORMATION

Table 1. LO Port Input Impedance vs Frequency for EN = High

Frequency MHz	Input Impedance Ω	S_{11} Mag	Angle
1000	44.5 + j18.2	0.197	95
1400	60.3 + j6.8	0.112	30
1600	62.8 – j0.6	0.113	–2.4
1800	62.4 – j9.0	0.136	–32
2000	56.7 – j15.6	0.157	–58
2200	50.9 – j16.5	0.161	–77
2400	46.6 – j15.2	0.159	–94
2600	42.9 – j13.9	0.165	–109

The input impedance of the LO port is different if the part is in shut-down mode. The LO input impedance for EN = Low is given in Table 2.

Table 2. LO Port Input Impedance vs Frequency for EN = Low

Frequency MHz	Input Impedance Ω	S_{11} Mag	Angle
1000	42.1 + j43.7	0.439	75
1400	121 + j34.9	0.454	15
1600	134 – j31.6	0.483	–11
1800	91.3 – j68.5	0.510	–33
2000	56.4 – j66.3	0.532	–53
2200	37.7 – j54.9	0.544	–70
2400	27.9 – j43.6	0.550	–87
2600	22.1 – j33.9	0.553	–104

RF Section

After up-conversion, the RF outputs of the I and Q mixers are combined. An on-chip balun performs internal differential to single-ended output conversion, while transforming the output signal impedance to 50Ω. Table 3 shows the RF port output impedance vs frequency.

Table 3. RF Port Output Impedance vs Frequency for EN = High and P_{LO} = 0dBm

Frequency MHz	Input Impedance Ω	S_{22} Mag	Angle
1000	21.3 + j9.7	0.421	153
1400	29.8 + j20.3	0.348	121
1600	39.1 + j23.5	0.280	100
1800	50.8 + j18.4	0.180	77.1
2000	52.1 + j5.4	0.057	65.5
2200	43.2 – j0.1	0.073	–179
2400	36.0 + j2.0	0.164	171
2600	32.1 + j5.6	0.228	159

The RF output S_{22} with no LO power applied is given in Table 4.

Table 4. RF Port Output Impedance vs Frequency for EN = High and No LO Power Applied

Frequency MHz	Input Impedance Ω	S_{22} Mag	Angle
1000	21.7 + j9.9	0.416	153
1400	32.3 + j19.5	0.312	119
1600	42.2 + j18.5	0.214	102
1800	46.8 + j9.6	0.104	103
2000	41.8 + j3.7	0.098	154
2200	36.1 + j4.3	0.170	160
2400	32.8 + j7.4	0.226	152
2600	31.2 + j10.5	0.264	144

For EN = Low the S_{22} is given in Table 5.

Table 5. RF Port Output Impedance vs Frequency for EN = Low

Frequency MHz	Input Impedance Ω	S_{22} Mag	Angle
1000	20.9+j9.6	0.428	154
1400	28.5 + j20.2	0.365	123
1600	36.7 + j24.5	0.311	103
1800	48.7 + j23.1	0.229	80.2
2000	55.7 + j11.0	0.116	56.7
2200	48.9 + j0.6	0.013	158.9
2400	39.8 – j0.02	0.115	–179
2600	34.2 + j3.2	0.193	167

To improve S_{22} for lower frequencies, a shunt capacitor can be added to the RF output. At higher frequencies, a shunt inductor can improve the S_{22}. Figure 6 shows the equivalent circuit schematic of the RF output.

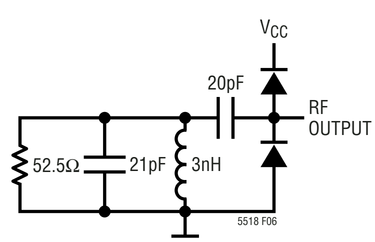

Figure 6. Equivalent Circuit Schematic of the RF Output

Note that an ESD diode is connected internally from the RF output to ground. For strong output RF signal levels (higher than 3dBm) this ESD diode can degrade the linearity performance if the 50Ω termination impedance is connected directly to ground. To prevent this, a

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coupling capacitor can be inserted in the RF output line. This is strongly recommended during a 1dB compression measurement.

Enable Interface

Figure 7 shows a simplified schematic of the EN pin interface. The voltage necessary to turn on the LT5518 is 1.0V. To disable (shutdown) the chip, the Enable voltage must be below 0.5V. If the EN pin is not connected, the chip is disabled. This EN = Low condition is guaranteed by the 75kΩ on-chip pull-down resistor. It is important that the voltage at the EN pin does not exceed V_{CC} by more than 0.5V. If this should occur, the full chip supply current could be sourced through the EN pin ESD protection diodes. Damage to the chip may result.

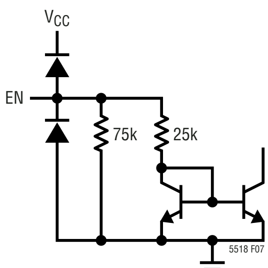

Figure 7. EN Pin Interface

Evaluation and Demo Boards

Figure 8 shows the schematic of the evaluation board that was used for the measurements summarized in the Electrical Characteristics tables and the Typical Performance Characteristic plots.

Figure 9 shows the demo board schematic. Resistors R3, R4, R10 and R11 may be replaced by shorting wires if a flat frequency response to DC is required. A good ground connection is required for the exposed pad of the LT5518 package. If this is not done properly, the RF performance will degrade. The exposed pad also provides heat sinking for the part and minimizes the possibility of the chip overheating. R7 (optional) limits the Enable pin current in the event that the Enable pin is pulled high while the V_{CC} inputs are low. In Figures 10, 11 and 12 the silk screen and the demo board PCB layouts are shown. If improved LO and Image suppression is required, an LO feedthrough calibration and an Image suppression calibration can be performed.

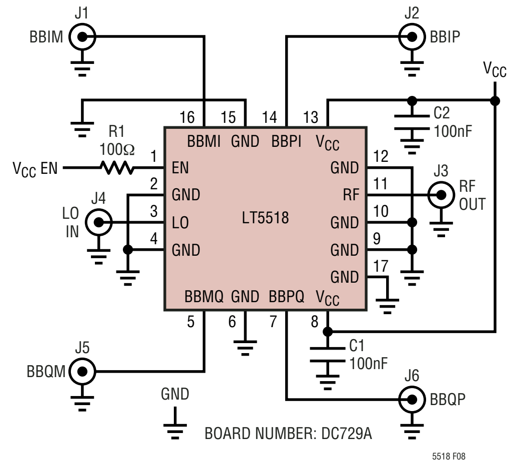

Figure 8. Evaluation Board Circuit Schematic

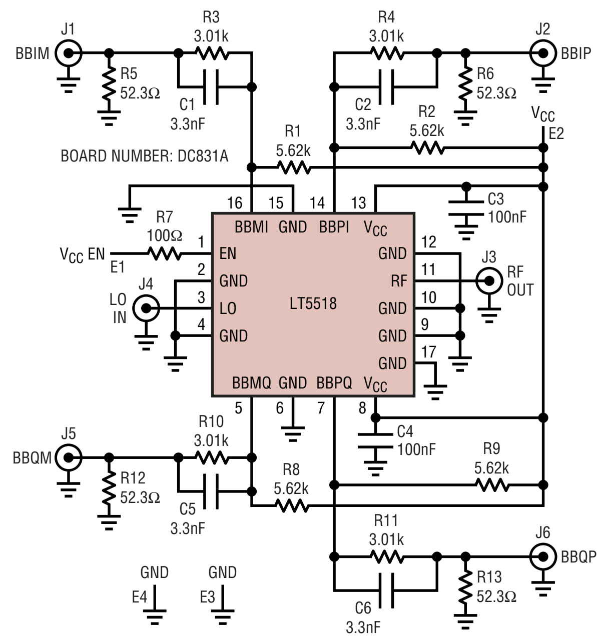

Figure 9. Demo Board Circuit Schematic

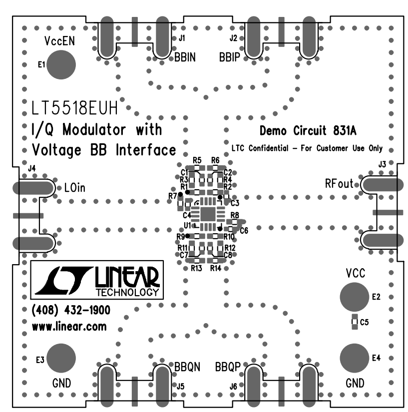

Figure 10. Component Side Silk Screen of Demo Board

LINEAR TECHNOLOGY

APPLICATIONS INFORMATION

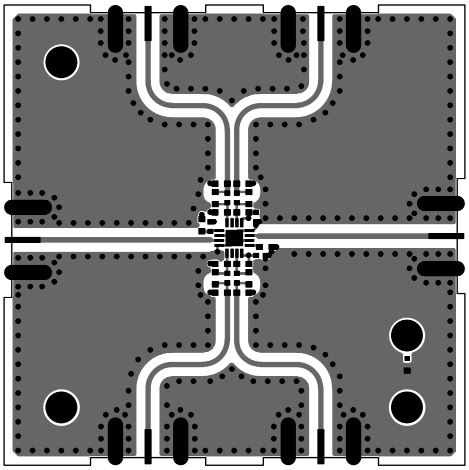

Figure 11. Component Side Layout of Demo Board

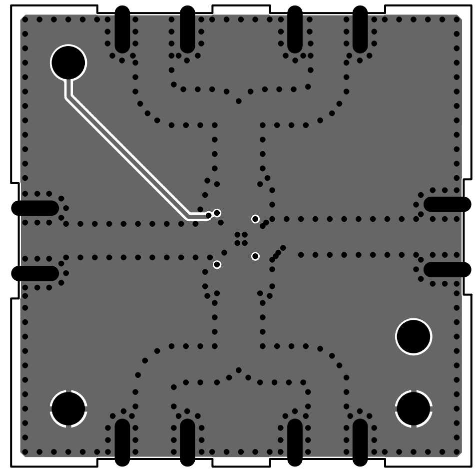

Figure 12. Bottom Side Layout of Demo Board

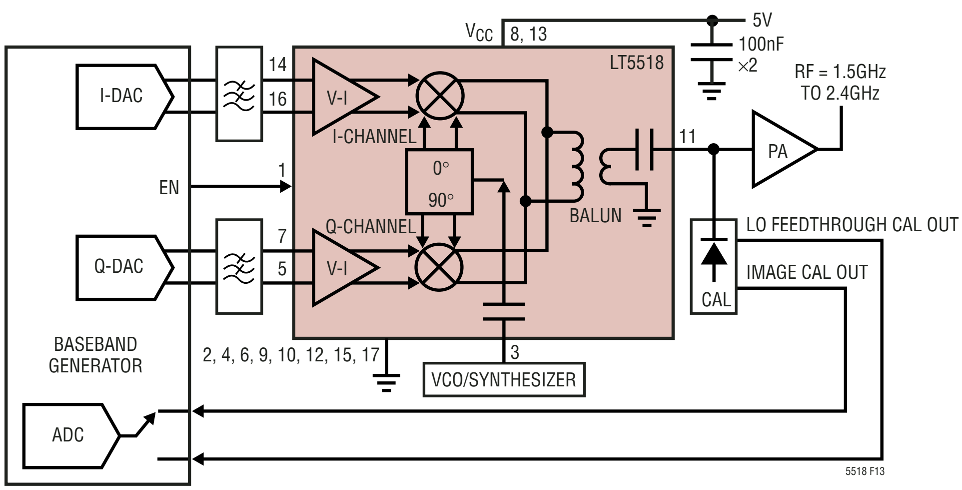

Figure 13. 1.5GHz to 2.4GHz Direct Conversion Transmitter Application with LO Feedthrough and Image Calibration Loop

Application Measurements

The LT5518 is recommended for base-station applications using various modulation formats. Figure 13 shows a typical application. The CAL box in Figure 13 allows for LO feedthrough and Image suppression calibration. Figure 14 shows the ACPR performance for W-CDMA using one or four channel modulation. Figures 15, 16 and 17 illustrate the 1, 2 and 4-channel W-CDMA measurement. To calculate ACPR, a correction is made for the spectrum analyzer noise floor.

If the output power is high, the ACPR will be limited by the linearity performance of the part. If the output power is low, the ACPR will be limited by the noise performance of the part. In the middle, an optimum ACPR is obtained.

Because of the LT5518's very high dynamic range, the test equipment can limit the accuracy of the ACPR measurement. Consult the factory for advice on ACPR measurement, if needed.

The ACPR performance is sensitive to the amplitude match of the BBIP and BBIM (or BBQP and BBQM) input voltage. This is because a difference in AC voltage amplitude will give rise to a difference in amplitude between the even-order harmonic products generated in the internal V-I converter. As a result, they will not cancel out entirely. Therefore, it

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is important to keep the amplitudes at the BBIP and BBIM inputs (or BBQP and BBQM) as equal as possible.

When the temperature is changed after calibration, the LO feedthrough and the Image Rejection performance will change. This is illustrated in Figure 18. The LO feedthrough and Image Rejection can also change as function of the baseband drive level, as is depicted in Figure 19. The RF output power, IM2 and IM3 vs two-tone baseband drive level are given in Figure 20.

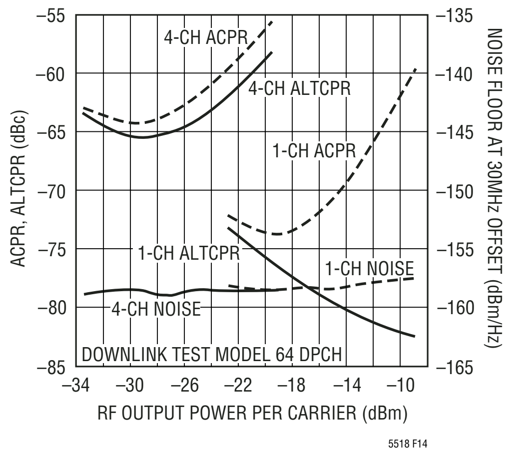


Figure 14. W-CDMA ACPR, ALTCPR and Noise vs RF Output Power at 2140MHz for 1 and 4 Channels

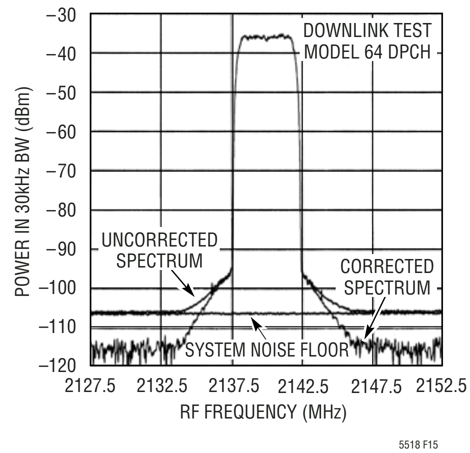


Figure 15. 1-Channel W-CDMA Spectrum

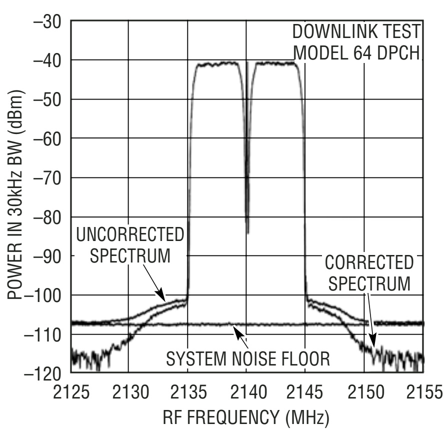


Figure 16. 2-Channel W-CDMA Spectrum

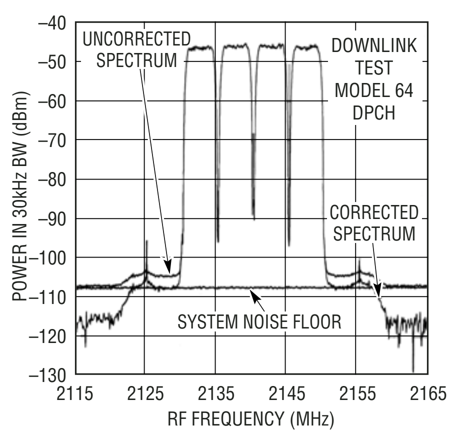


Figure 17. 4-Channel W-CDMA Spectrum

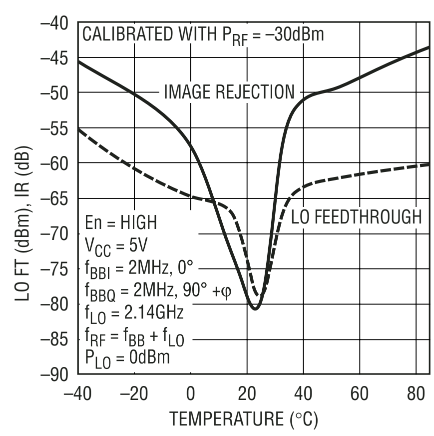


Figure 18. LO Feedthrough and Image Rejection vs Temperature after Calibration at 25°C

APPLICATIONS INFORMATION

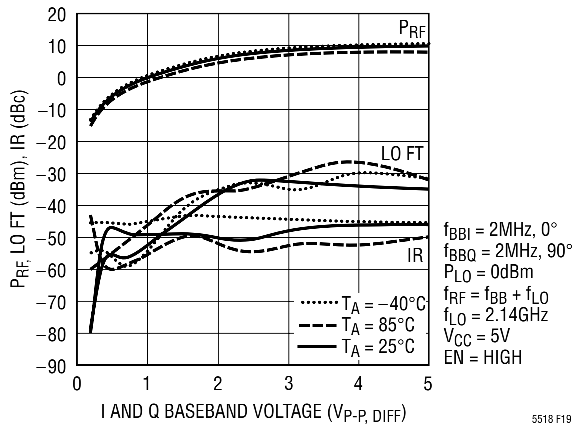


Figure 19. Image Rejection and LO Feedthrough vs Baseband Drive Voltage After Calibration at 25°C and V_{BBI} = 0.2$V_{P\text{-}P,\ DIFF}$

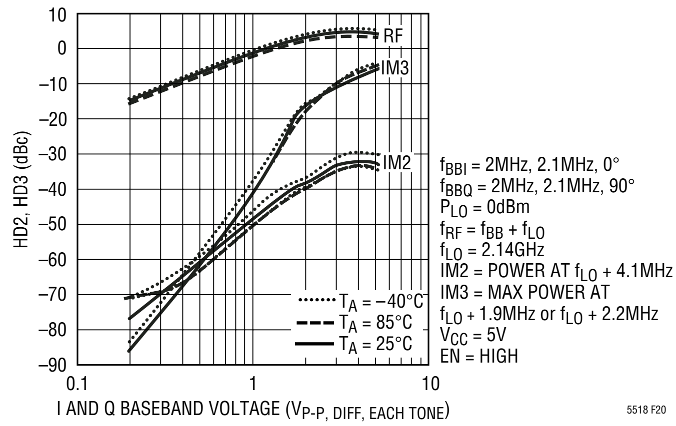
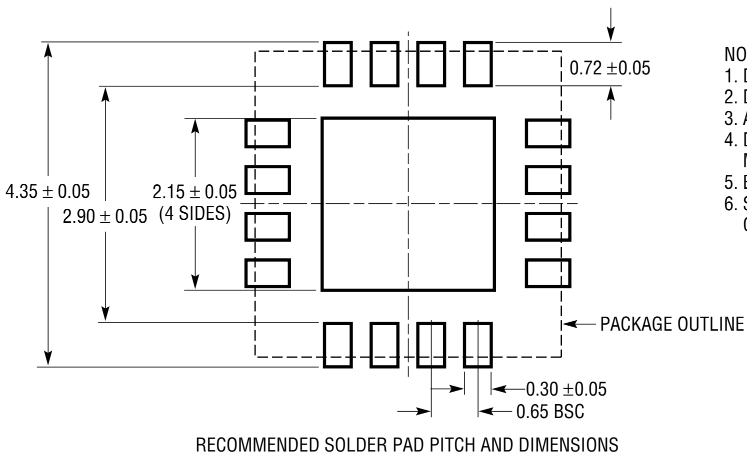


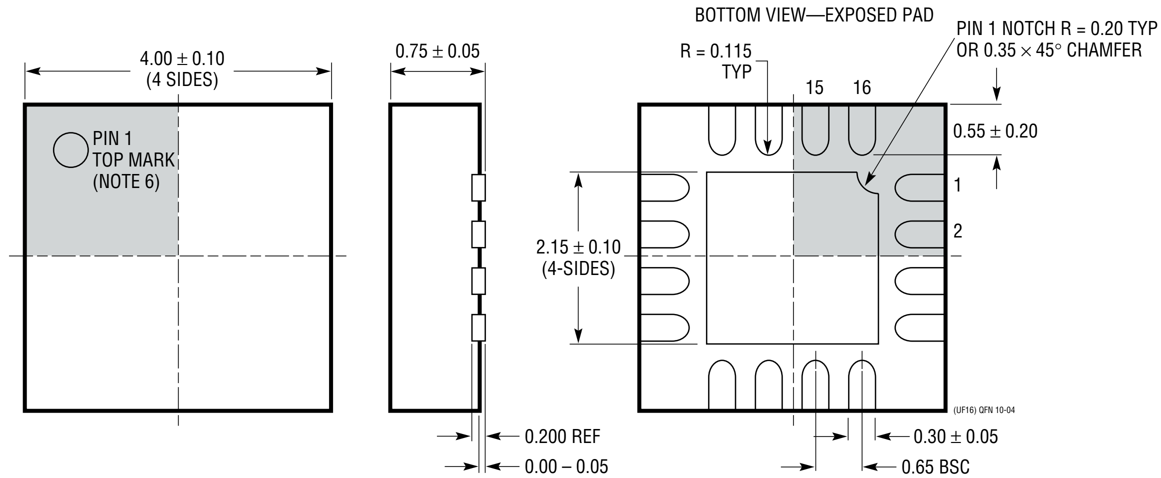
Figure 20. RF Two-Tone Power, IM2 and IM3 at 2140MHz vs Baseband Voltage

PACKAGE DESCRIPTION

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



5518f

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LT5511	High Linearity Up-Converting Mixer	RF Output to 3GHz, 17dBm IIP3, Integrated LO Buffer
LT5512	DC-3GHz High Signal Level Down-Converting Mixer	DC to 3GHz, 17dBm IIP3, Integrated LO Buffer
LT5514	Ultralow Distortion, IF Amplifier/ADC Driver with Digitally Controlled Gain	850MHz Bandwidth, 47dBm OIP3 at 100MHz, 10.5dB to 33dB Gain Control Range
LT5515	1.5GHz to 2.5GHz Direct Conversion Quadrature Demodulator	20dBm IIP3, Integrated LO Quadrature Generator
LT5516	0.8GHz to 1.5GHz Direct Conversion Quadrature Demodulator	21.5dBm IIP3, Integrated LO Quadrature Generator
LT5517	40MHz to 900MHz Quadrature Demodulator	21dBm IIP3, Integrated LO Quadrature Generator
LT5519	0.7GHz to 1.4GHz High Linearity Up-Converting Mixer	17.1dBm IIP3 at 1GHz, Integrated RF Output Transformer with 50Ω Matching, Single-Ended LO and RF Ports Operation
LT5520	1.3GHz to 2.3GHz High Linearity Up-Converting Mixer	15.9dBm IIP3 at 1.9GHz, Integrated RF Output Transformer with 50Ω Matching, Single-Ended LO and RF Ports Operation
LT5521	10MHz to 3700MHz High Linearity Up-Converting Mixer	24.2dBm IIP3 at 1.95GHz, NF = 12.5dB, 3.15V to 5.25V Supply, Single-Ended LO Port Operation
LT5522	600MHz to 2.7GHz High Signal Level Down-Converting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LT5524	Low Power, Low Distortion ADC Driver with Digitally Programmable Gain	450MHz Bandwidth, 40dBm OIP3, 4.5dB to 27dB Gain Control
LT5525	High Linearity, Low Power Downconverting Mixer	Single-Ended 50Ω RF and LO Ports, 17.6dBm IIP3 at 1900MHz, I_{CC} = 28mA
LT5526	High Linearity, Low Power Downconverting Mixer	3V to 5.3V Supply, 16.5dBm IIP3, 100kHz to 2GHz RF, NF = 11dB, I_{CC} = 28mA
LT5528	1.5GHz – 2.4GHz High Linearity Direct Quadrature Modulator	4.5V to 5.25V Supply, 22dBm OIP3 at 2GHz, NFloor = 159dBm/Hz, 50Ω Single-Ended BB, RF and LO Ports
RF Power Detectors		
LT5504	800MHz to 2.7GHz RF Measuring Receiver	80dB Dynamic Range, Temperature Compensated, 2.7V to 5.25V Supply
LTC®5505	RF Power Detectors with >40dB Dynamic Range	300MHz to 3GHz, Temperature Compensated, 2.7V to 6V Supply
LTC5507	100kHz to 1000MHz RF Power Detector	100kHz to 1GHz, Temperature Compensated, 2.7V to 6V Supply
LTC5508	300MHz to 7GHz RF Power Detector	44dB Dynamic Range, Temperature Compensated, SC70 Package
LTC5509	300MHz to 3GHz RF Power Detector	36dB Dynamic Range, Low Power Consumption, SC70 Package
LTC5530	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Shutdown, Adjustable Gain
LTC5531	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Shutdown, Adjustable Offset
LTC5532	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Adjustable Gain and Offset
LT5534	50MHz to 3GHz RF Power Detector with 60dB Dynamic Range	±1dB Output Variation Overtemperature, 38ns Response Time
Low Voltage RF Building Block		
LT5546	500MHz Quadrature Demodulator with VGA and 17MHz Baseband Bandwidth	17MHz Baseband Bandwidth, 40MHz to 500MHz IF, 1.8V to 5.25V Supply, –7dB to 56dB Linear Power Gain
Wide Bandwidth ADCs		
LT1749	12-Bit, 80Msps	500MHz BW S/H, 71.8dB SNR
LT1750	14-Bit, 80Msps	500MHz BW S/H, 75.5dB SNR

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- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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