TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

131,072-WORD BY 8-BIT STATIC RAM

DESCRIPTION

The TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI is a 1,048,576-bit static random access memory (SRAM) organized as 131,072 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5 V ± 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 5 mA/MHz (typ) and a minimum cycle time of 70 ns. It is automatically placed in low-power mode at 1 μA standby current (typ) when chip enable ($\overline{CE1}$) is asserted high or (CE2) is asserted low. There are three control inputs. $\overline{CE1}$ and CE2 are used to select the device and for data retention control, and output enable ($\overline{OE}$) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of − 40° to 85°C, the TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI can be used in environments exhibiting extreme temperature conditions. The TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI is available in a standard plastic 32-pin dual-in-line package (DIP), plastic 32-pin small-outline package (SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
  Operating: 27.5 mW/MHz (typical)
- Single power supply voltage of 5 V ± 10%
- Power down features using $\overline{CE1}$ and CE2.
- Data retention supply voltage of 2 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of − 40° to 85°C
- Standby Current (maximum) :

	TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI	
	-70, -85	-70L, -85L
5.5V	200 μA	40 μA
3.0V	100 μA	20 μA

- Access Times (maximum):

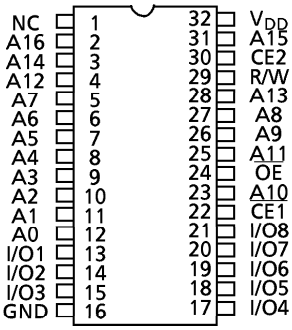
	TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI	
	-70, -70L	-85, -85L
Access Time	70 ns	85 ns
$\overline{CE1}$ Access Time	70 ns	85 ns
CE2 Access Time	70 ns	85 ns
$\overline{OE}$ Access Time	35 ns	45 ns

- Packages:

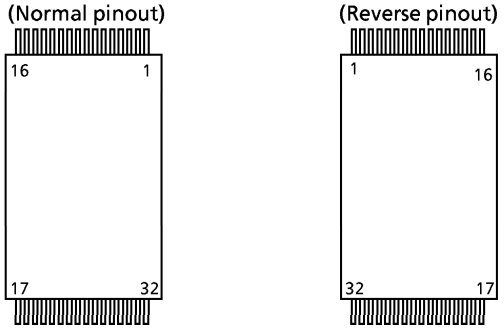
DIP32-P-600-2.54 (CPI)	(Weight: 4.45 g typ)
SOP32-P-525-1.27 (CFI)	(Weight: 1.04 g typ)
TSOP I 32-P-0820-0.50 (CFTI)	(Weight: 0.34 g typ)
TSOP I 32-P-0820-0.50A (CTRI)	(Weight: 0.34 g typ)
TSOP I 32-P-0.50 (CSTI)	(Weight: 0.24 g typ)
TSOP I 32-P-0.50A (CSRI)	(Weight: 0.24 g typ)

PIN ASSIGNMENT (TOP VIEW)

○ 32 PIN DIP & SOP



○ 32 PIN TSOP



PIN NAMES

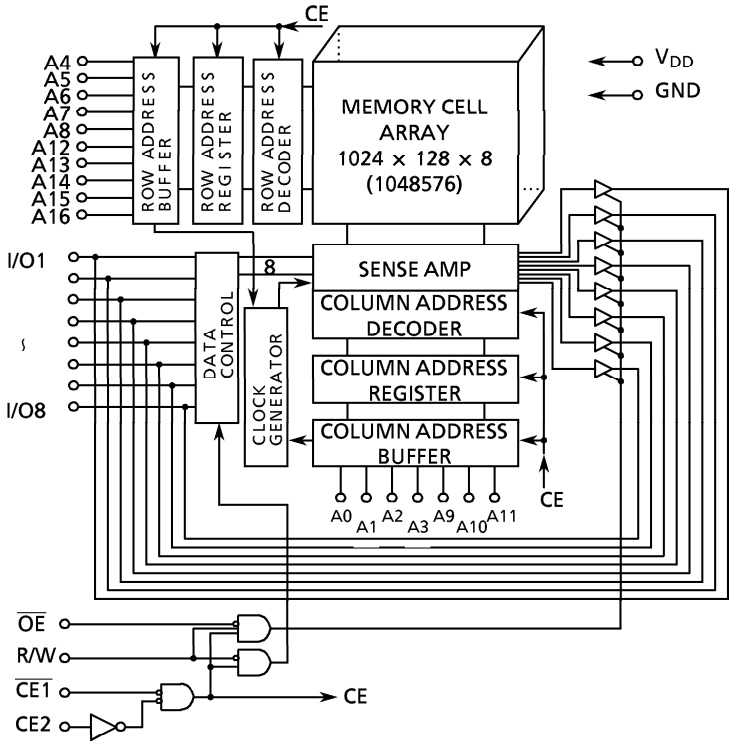
A0 to A16	Address Inputs
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{CE1}$, CE2	Chip Enable
I/O1 to I/O8	Data Input/Output
V_{DD}	Power (+ 5 V)
GND	Ground
NC	No Connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	NC	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

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BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 to I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	×	L	D_{IN}	I_{DDO}
Outputs Disabled	L	H	H	H	High-Z	I_{DDO}
Standby	H	×	×	×	High-Z	I_{DDS}
	×	L	×	×	High-Z	I_{DDS}

Note: × = don't care. H = logic high. L = logic low.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	− 0.3 to 7.0	V
V_{IN}	Input Voltage	− 0.3* to 7.0	V
$V_{I/O}$	Input and Output Voltage	− 0.5 to V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
Tsolder	Soldering Temperature (10 s)	260	°C
Tstrg.	Storage Temperature	− 55 to 150	°C
Topr.	Operating Temperature	− 40 to 85	°C

* − 3.0 V when measured at a pulse width of 50 ns ** SOP

DC RECOMMENDED OPERATING CONDITIONS (Ta = − 40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	− 0.3*	−	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	

* − 3.0 V when measured at a pulse width of 50 ns

DC CHARACTERISTICS (Ta = − 40° to 85°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{DD}			−	−	± 1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4 V			− 1.0	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V			4.0	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 V to V_{DD}			−	−	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH}, I_{OUT} = 0 mA Other Inputs = V_{IH}/V_{IL}	Tcycle	min	−	−	70	mA
				1 μs	−	−	20	
I_{DDO2}		$\overline{CE1}$ = 0.2 V and CE2 = V_{DD} − 0.2 V R/W = V_{DD} − 0.2 V, I_{OUT} = 0 mA Other Inputs = V_{DD} − 0.2 V/0.2 V	Tcycle	min	−	−	60	mA
				1 μs	−	−	10	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			−	−	3	mA
I_{DDS2} (Note)		$\overline{CE1}$ = V_{DD} − 0.2 V or CE2 = 0.2 V V_{DD} = 2.0 to 5.5 V	-70, -85	Ta = 25°C	−	1	−	μA
				Ta = −40° to 85°C	−	−	200	
			-70L, -85L	Ta = 25°C	−	1	2	
				Ta = −40° to 85°C	−	−	40	

Note: In standby mode with $\overline{CE1} \geqq V_{DD}$ − 0.2 V, these limits are assured for the condition CE2 $\geqq V_{DD}$ − 0.2 V or CE2 $\leqq$ 0.2 V.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = − 40° to 85°C, V_{DD} = 5 V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI				UNIT
		-70, -70L		-85, -85L		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	70	–	85	–	ns
t_{ACC}	Address Access Time	–	70	–	85	
t_{CO1}	Chip Enable ($\overline{CE1}$) Access Time	–	70	–	85	
t_{CO2}	Chip Enable (CE2) Access Time	–	70	–	85	
t_{OE}	Output Enable Access Time	–	35	–	45	
t_{COE}	Chip Enable Low to Output Active	5	–	5	–	
t_{OEE}	Output Enable Low to Output Active	0	–	0	–	
t_{OD}	Chip Enable High to Output High-Z	–	30	–	35	
t_{ODO}	Output Enable High to Output High-Z	–	30	–	35	
t_{OH}	Output Data Hold Time	10	–	10	–	

WRITE CYCLE

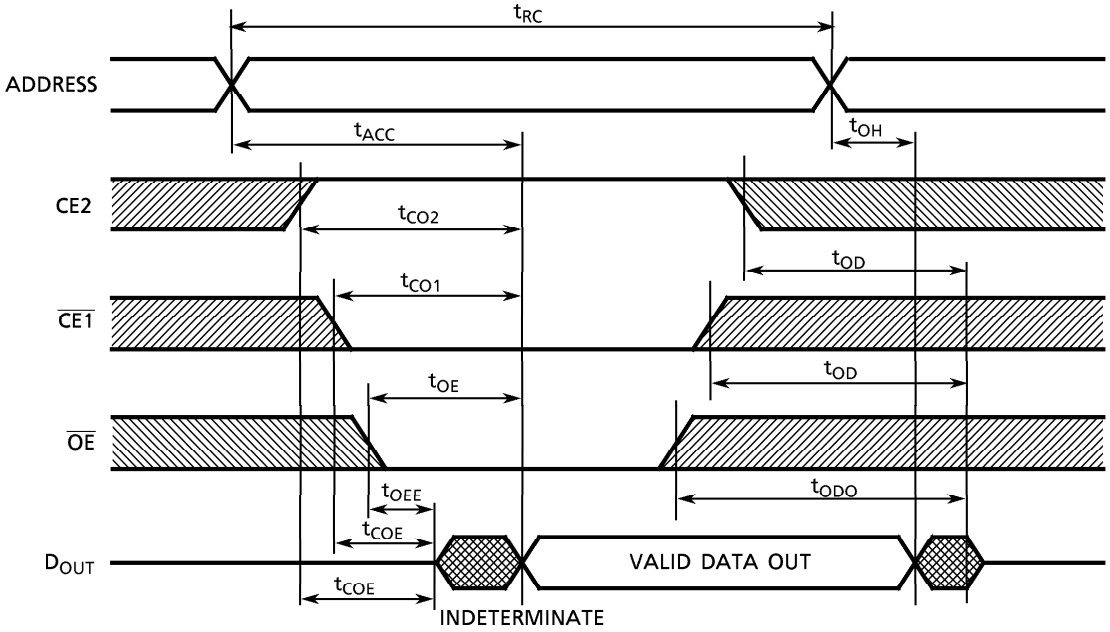
SYMBOL	PARAMETER	TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI				UNIT
		-70, -70L		-85, -85L		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	70	–	85	–	ns
t_{WP}	Write Pulse Width	50	–	60	–	
t_{CW}	Chip Enable to End of Write	60	–	75	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W Low to Output High-Z	–	30	–	35	
t_{OEW}	R/W High to Output Active	0	–	0	–	
t_{DS}	Data Setup Time	30	–	35	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC TEST CONDITIONS

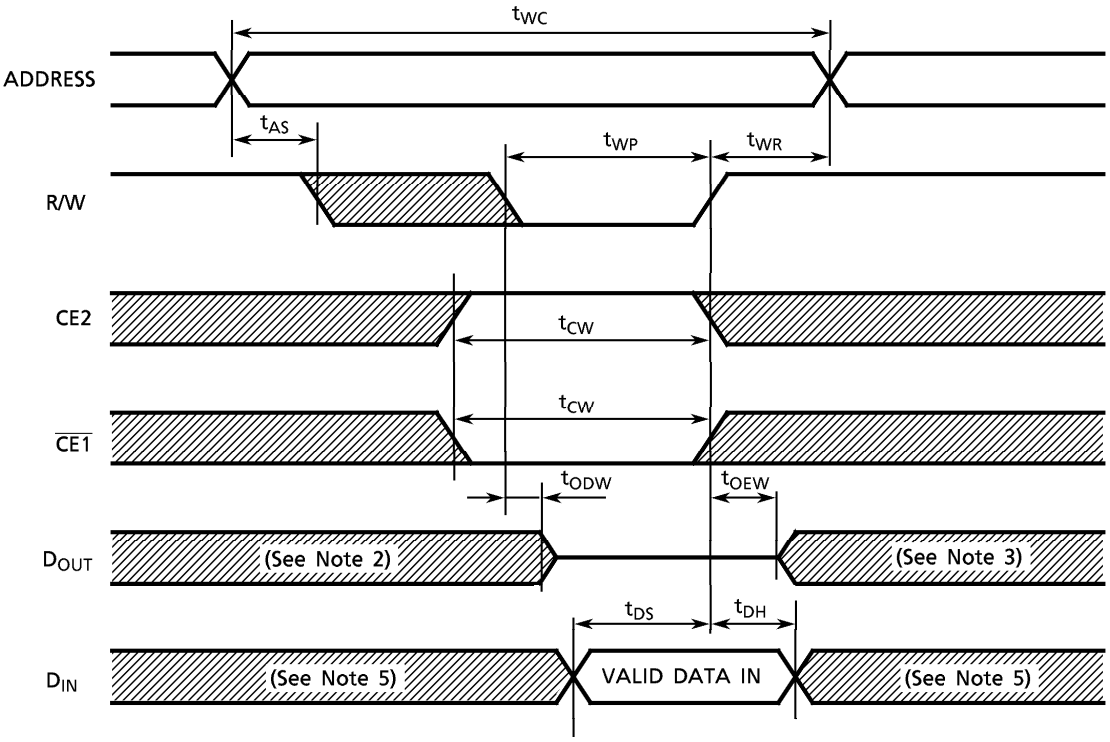
Output load: 100 pF + one TTL gate
Input pulse level: 0.4 V, 2.6 V
Timing measurements: 1.5 V
Reference level: 1.5 V
t_R, t_F: 5 ns

TIMING DIAGRAMS

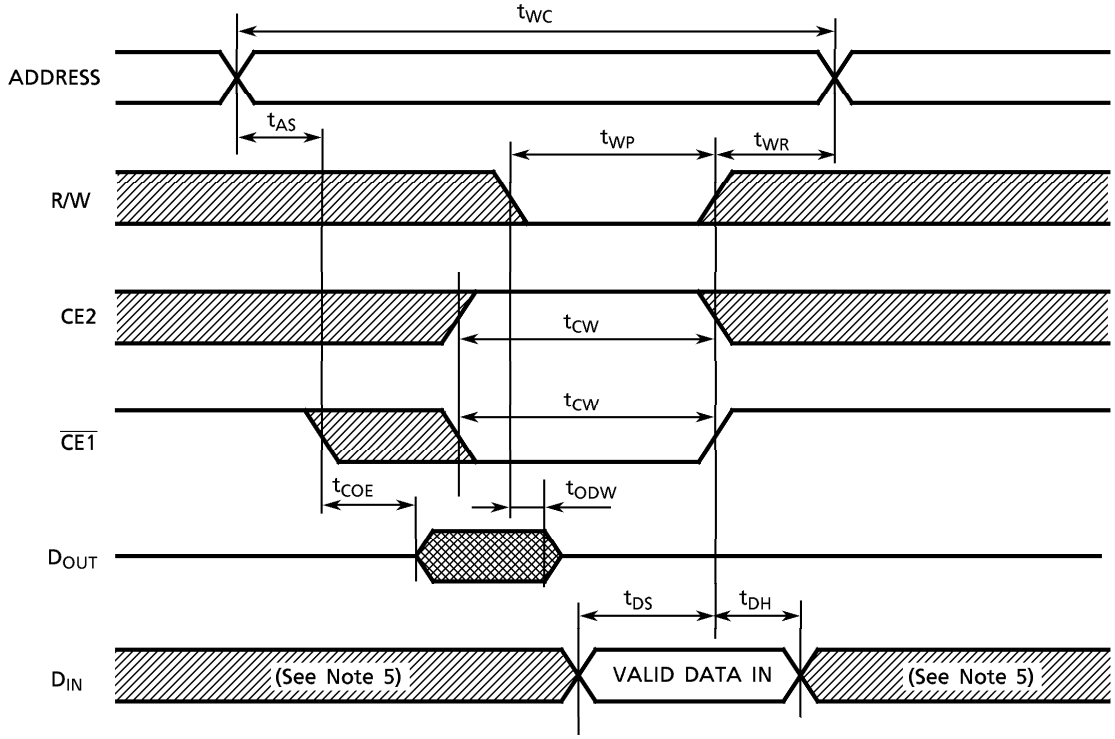
READ CYCLE (See Note 1)



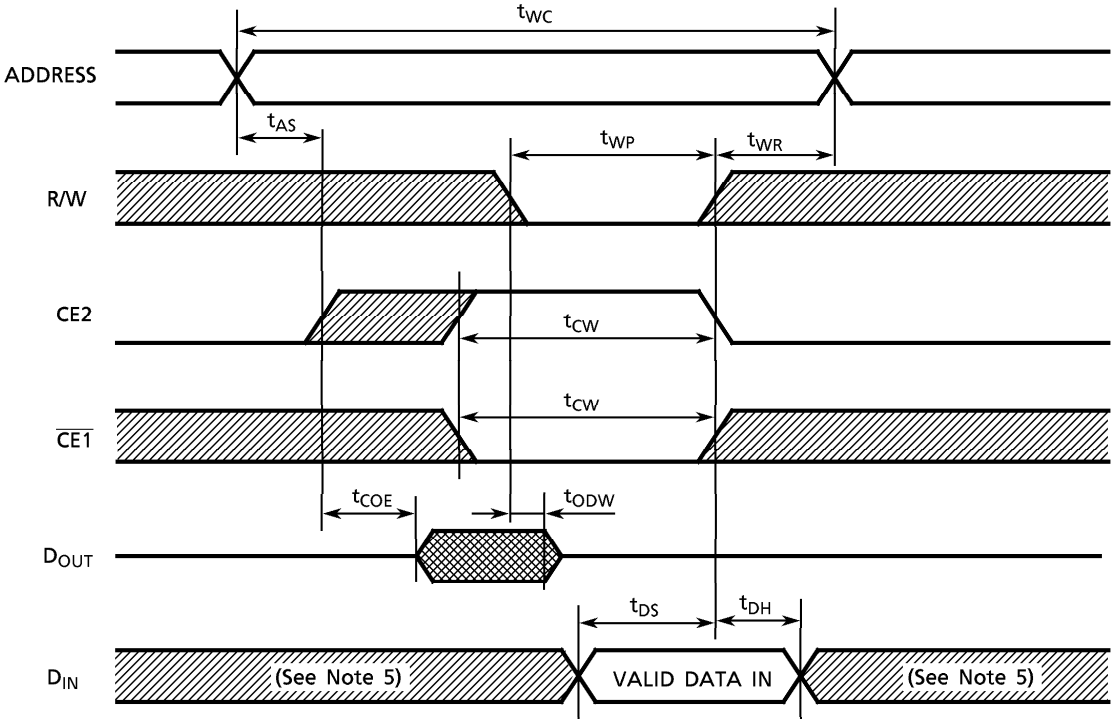
WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 ($\overline{CE1}$ CONTROLLED) (See Note 4)



WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)



Note: (1) R/W remains HIGH for the read cycle.

(2) If $\overline{CE1}$ goes LOW (or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If $\overline{CE1}$ goes HIGH (or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

(4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

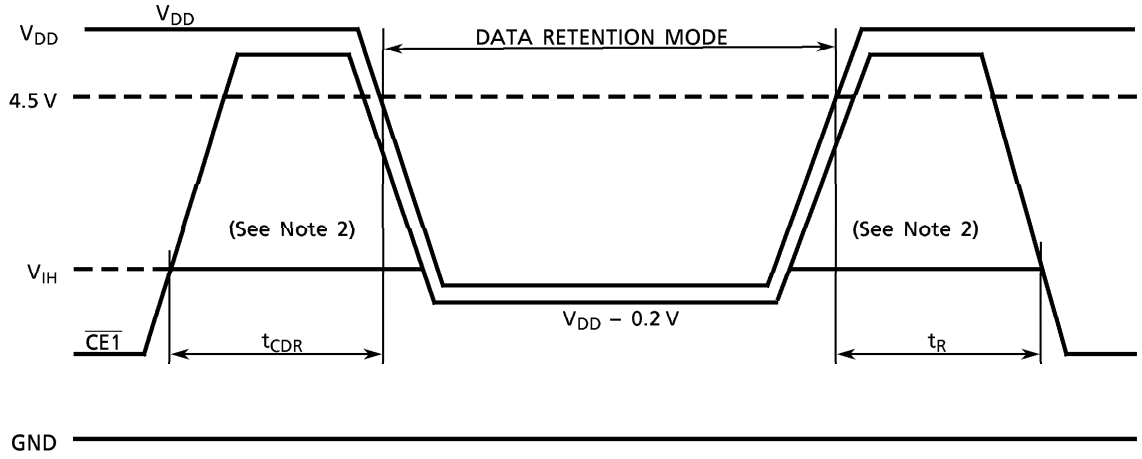
(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = – 40° to 85°C)

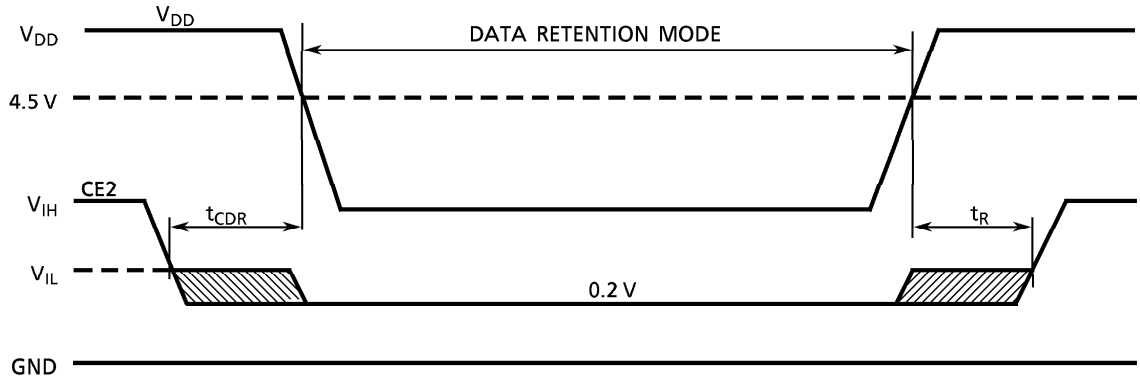
SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage			2.0	–	5.5	V
I_{DDS2}	Standby Current	-70, -85	V_{DH} = 3.0 V	–	–	100	μA
			V_{DH} = 5.5 V	–	–	200	
		-70L, -85L	V_{DH} = 3.0 V	–	–	20*	
			V_{DH} = 5.5 V	–	–	40	
t_{CDR}	Chip Deselect to Data Retention Mode Time			0	–	–	nS
t_R	Recovery Time			5	–	–	mS

* 2 μA (max) at Ta = – 40° to 40°C

$\overline{CE1}$ CONTROLLED DATA RETENTION MODE (See Note 1)



CE2 CONTROLLED DATA RETENTION MODE (See Note 3)



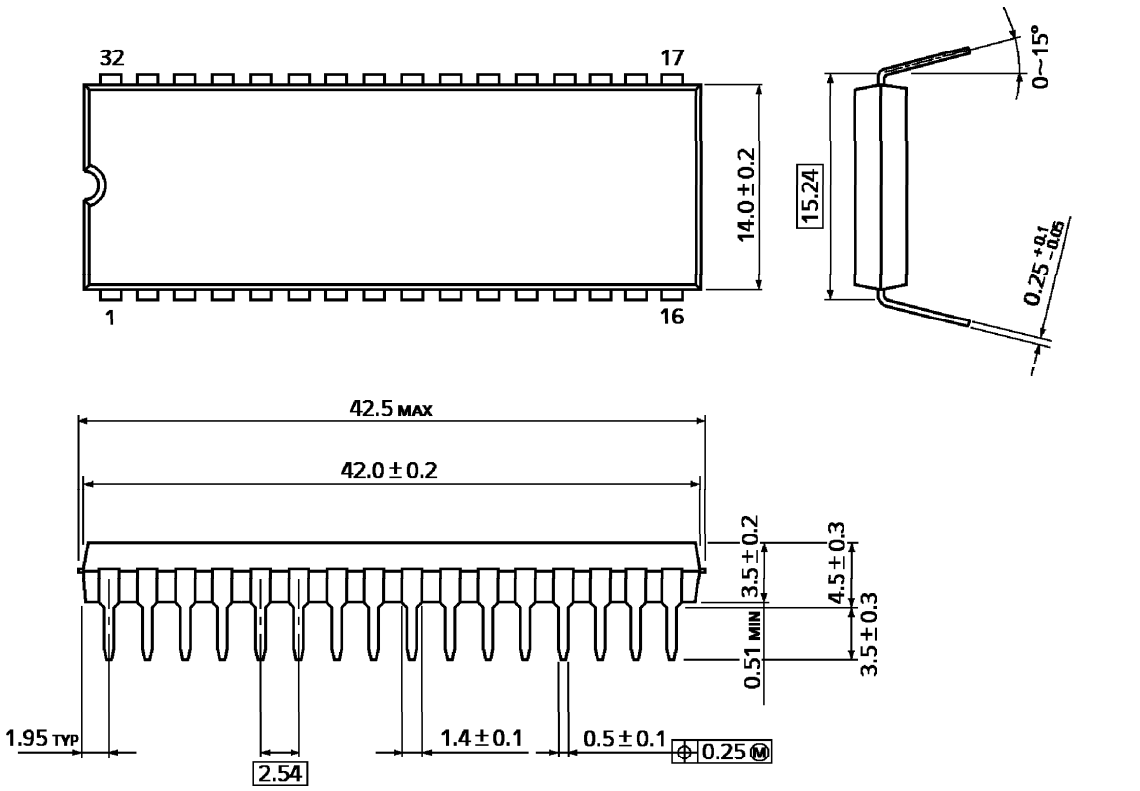
Note: (1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is entered when CE2 $\leqq$ 0.2 V or CE2 $\geqq$ V_{DD} − 0.2 V.

(2) When $\overline{CE1}$ is operating at the V_{IH} level (2.4 V), the operation current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.6 V.

(3) In CE2 controlled data retention mode, minimum standby current mode is entered when CE2 $\leqq$ 0.2 V.

PACKAGE DIMENSIONS (DIP32-P-600-2.54)

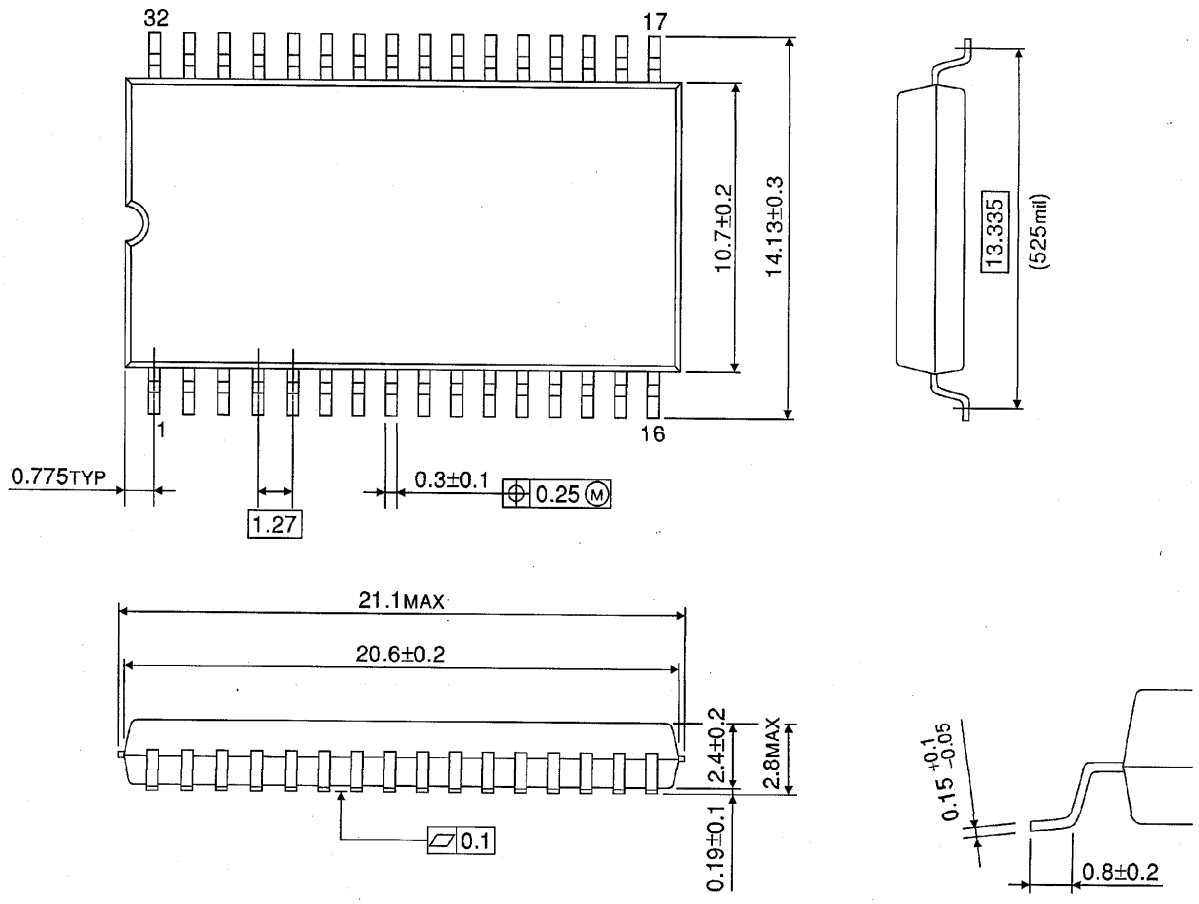
Units in mm



Weight: 4.45 g (typ)

PACKAGE DIMENSIONS (SOP32-P-525-1.27)

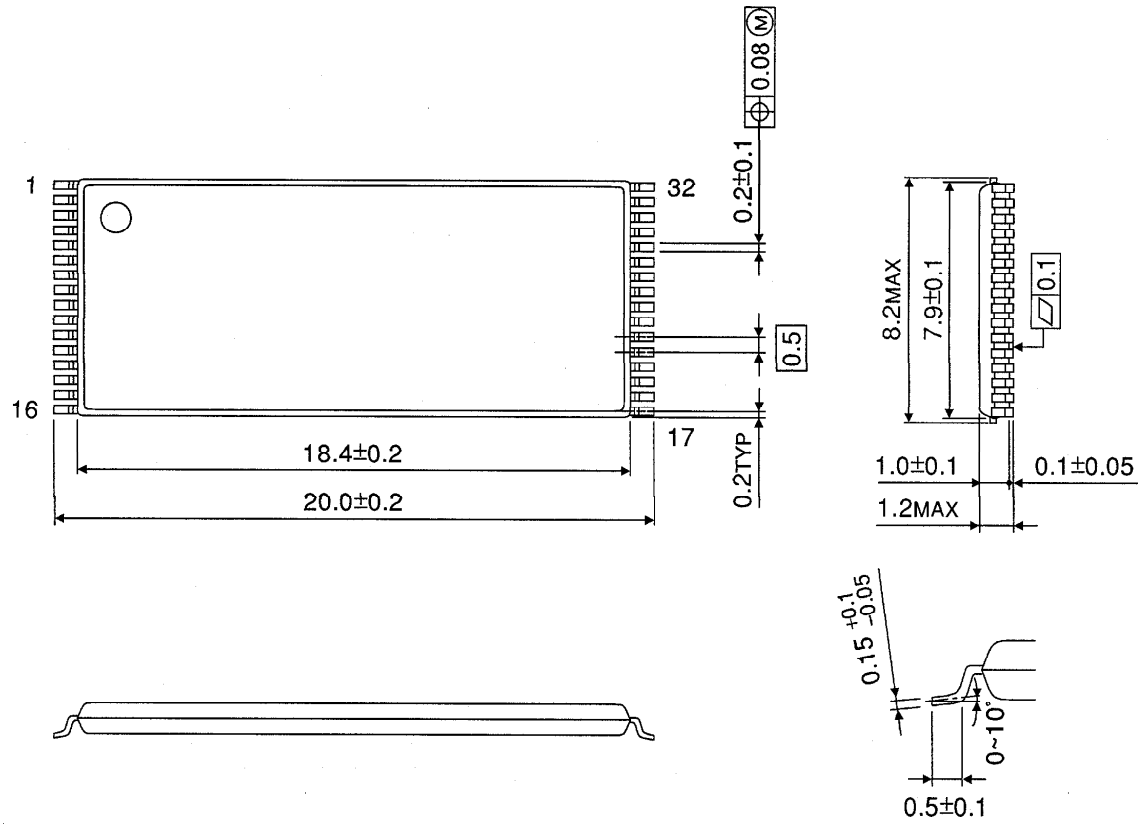
Units in mm



Weight: 1.04 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50)

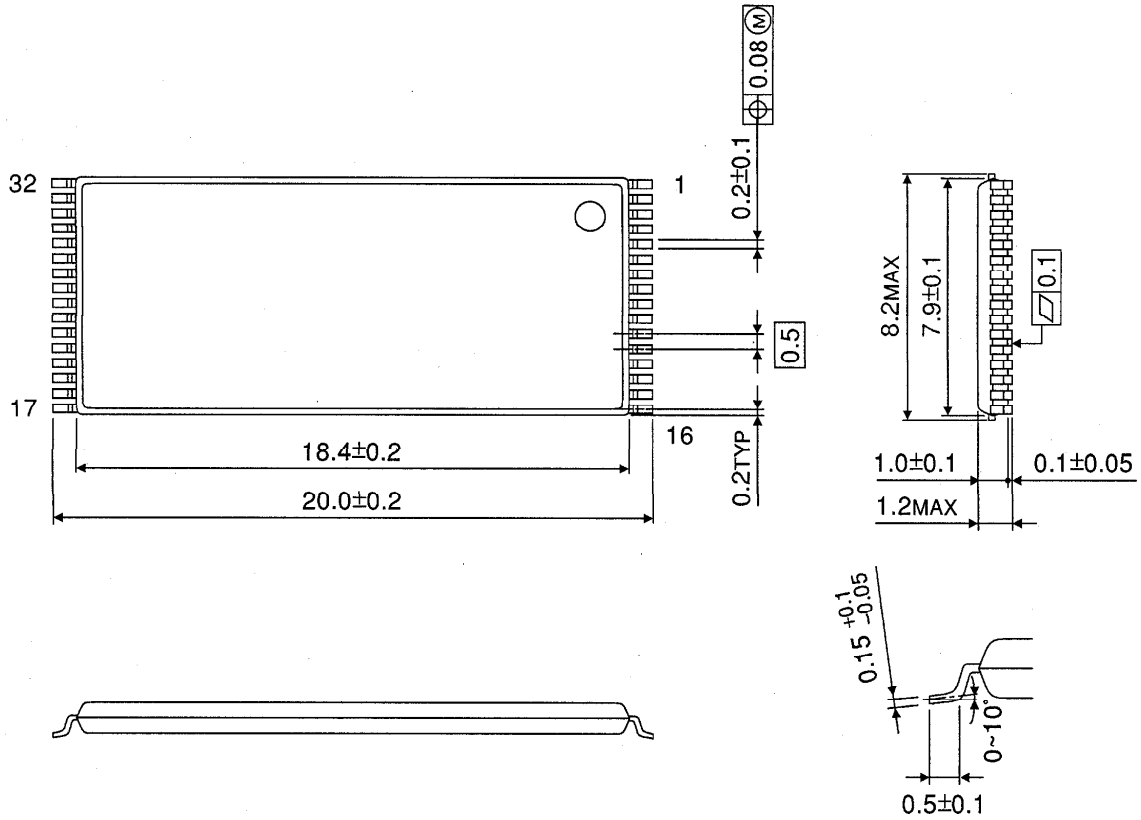
Units in mm



Weight: 0.34 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50A)

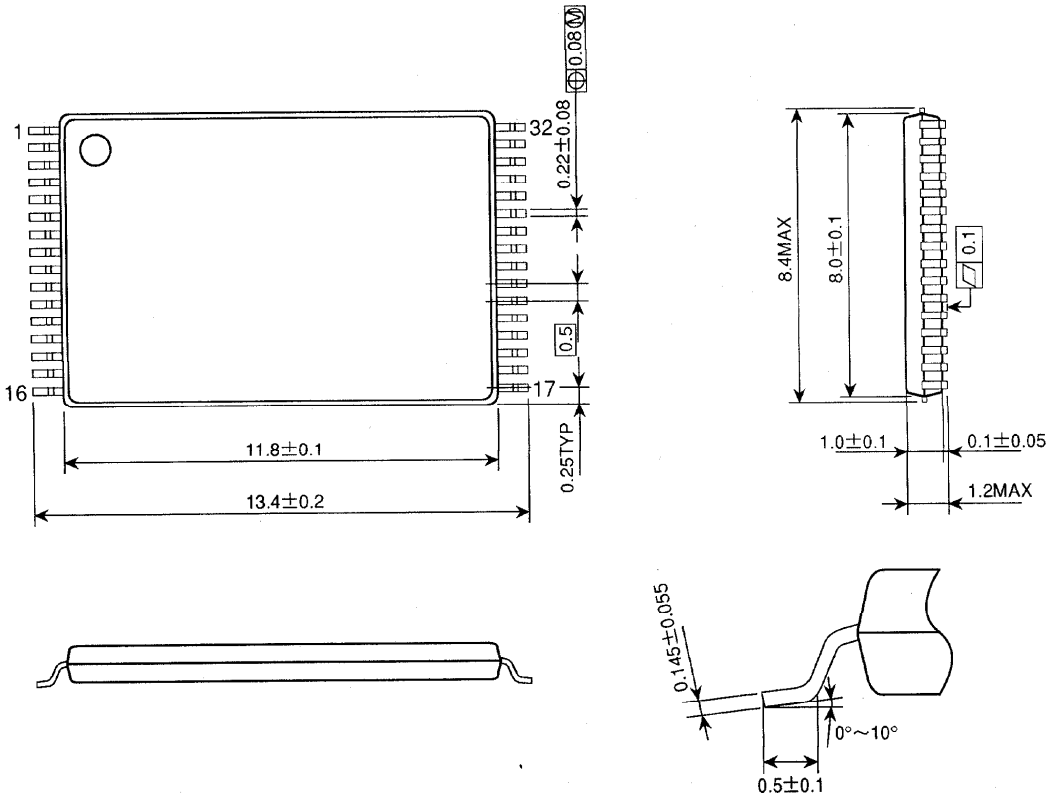
Units in mm



Weight: 0.34 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0.50)

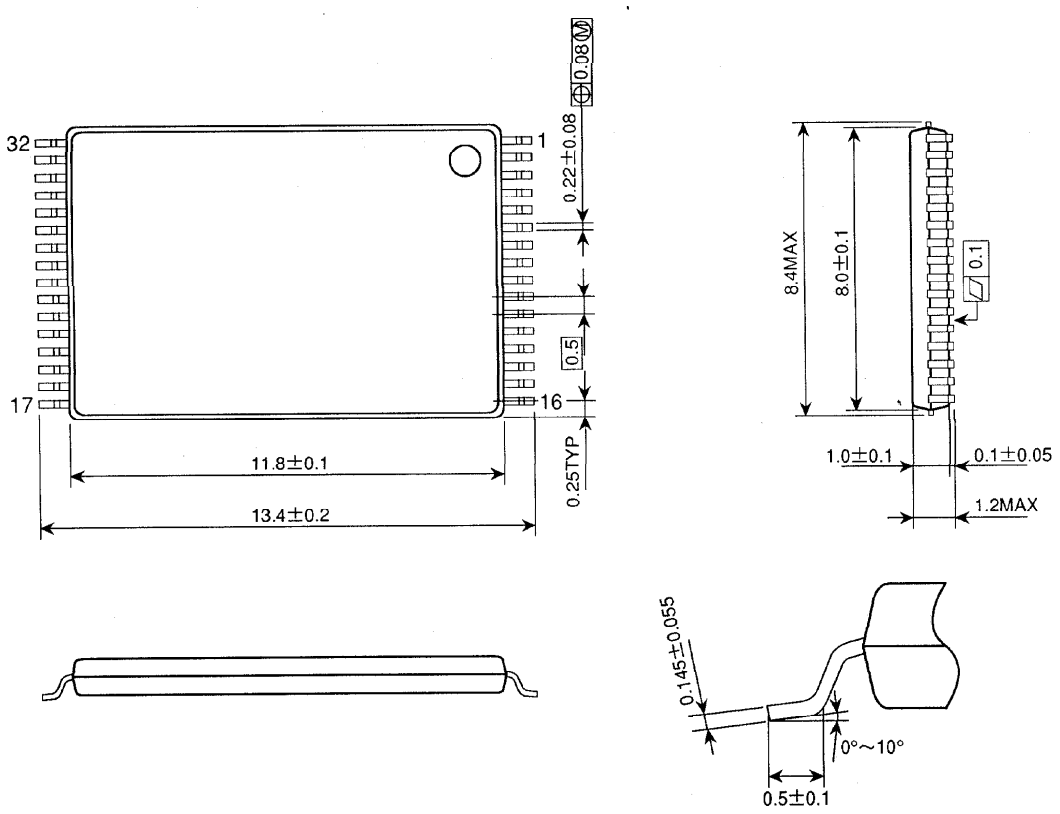
Units in mm



Weight: 0.24 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0.50A)

Units in mm



Weight: 0.24 g (typ)

LifeElectronics
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