Z86017/Z16017

PCMCIA Interface Solution

Reference Manual

RM001103-0901

ZiLOG Worldwide Headquarters • 910 E. Hamilton Avenue • Campbell, CA 95008
Telephone: 408.558.8500 • Fax: 408.558.8300 • www.ZiLOG.com

Z86017/Z16017 PCMCIA Interface Solution
Reference Manual

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact

ZiLOG Worldwide Headquarters
910 E. Hamilton Avenue
Campbell, CA 95008
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

Windows is a registered trademark of Microsoft Corporation.

Document Disclaimer

RM001103-0901

Preface

Thank you for your interest in Zilog's PCMCIA interface solution. This Reference Manual describes the programming and operation of the Z86017 and Z16017 PCMCIA adapter chips.

This Reference Manual is organized in the following way:

- **PCMCIA Interface Overview**
  This chapter is an introductory section that provides an overview of the architecture of the device.
- **Addressing Modes**
  This chapter describes the addressing modes supported by the Z86017/Z16017 architecture to ensure PCMCIA compatibility.
- **Programming Internal Registers**
  This chapter describes the serial interface modes.
- **Configuration Registers**
  This chapter describes the functions of the Z86017/Z16017 internal registers.
- **Appendix** A
  This appendix gives an overview of the Z86017/Z16017 multifunction pins.
- **Appendix B**
  This appendix provides Absolute Maximum Ratings, DC Electrical Characteristics, and Timing Specifications related to the Z86017/ Z1601.
- **Appendix C**
  This appendix provides various Z86017/Z16017 timing diagrams.

- **Appendix D**
  This appendix provides part numbers and ordering information.
- **Appendix E**
  This appendix provides a description of the Z8601700ZCO PCMCIA Interface Development Kit.

Table of Contents

List of Figures

List of Tables

PCMCIA Interface Overview

FEATURES

Table 1. Device Features

Device	RAM (Bytes)	Speed	Package
Z86017	256	20	100-Pin VQFP
Z86M17[1]	256	20	100-Pin VQFP
Z16017	256	20	100-Pin VQFP
Z16M17[1]	256	20	100-Pin VQFP

NOTES:
1.Mirror Image Bond-Out Options

- PCMCIA Configuration Registers
- Sequencer for programming attribute memory using EEPROM content, MASTER mode
- Serial Peripheral Interface (SPI) circuitry allows control through the local microprocessor, SLAVE mode
- PCMCIA to I/O peripheral
- PCMCIA to ATA/IDE translation
- ATA/IDE to ATA/IDE mapping, PASSHROUGH mode
- Operates from a 3.0V to 5.5V power supply
- Conforms to PCMCIA standards
- Low power dissipation
- Mirror image bond-out option (Z86M17/Z16M17)
- On-chip generation of IOIS16 in I/O mode (Z16017)

General Description

The Z86017/Z16017 (ZX6017) are general-purpose PCMCIA adapter chips used on the card side of the interface. For increased versatility, “mirror image” bond-out versions, the Z86M17 and Z16M17, are also available. These chips are easily configured to allow access to all types of memory or I/O-mapping peripherals, such as Ethernet controllers, Universal Asynchronous Receiver/Transmitters (UART), modems, rotating disk memory, and so on. The ZX6017 can be used in a stand-alone configuration without the use of a local processor when all necessary data for Attribute Memory, Card Configuration Registers (CCR), Memory/I/O maps, and so on, are being provided by a local serial EEPROM. The serial EEPROM is read automatically using an internal EEPROM sequencer. The ZX6017 can also be configured by a local microprocessor, when one is being used on the card.

Throughout this document, references to the ZX6017 device applies equally to the Z86017 and Z16017, unless otherwise specified.

Note: All Signals with an overline ($\overline{\ }$) are active Low, that is, B/$\overline{W}$ (WORD is active Low); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Table 2. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

The ZX6017 can be programmed by one of two ways: an external 256 byte serial EEPROM can be connected to the serial port interface, or a microprocessor can be connected to this port to provide a higher level of control. Figure 1 depicts the functional block diagram for the ZX6017.

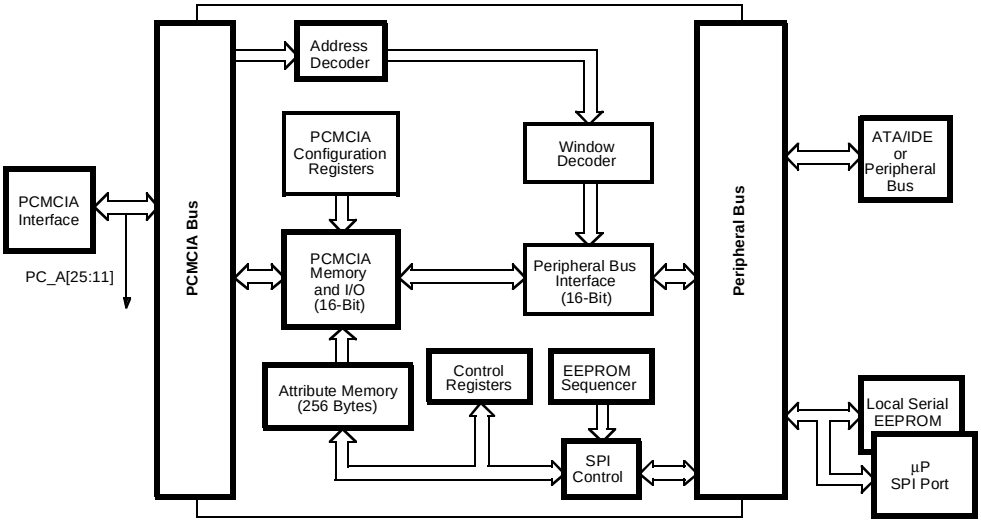


Figure 1. ZX6017 Functional Block Diagram

Power-On Reset

The ZX6017 defaults to the Memory Only interface as outlined in the PCMCIA specification upon deassertion of Power-On Reset (/POR). The hardware sets Busy on the PC_RDY/BSY pin and then addresses the EE_MASTER pin. If the EE_MASTER pin is unconnected or pulled High, the ZX6017 serial interface defaults to the Master mode and an external EEPROM is required. If this pin is pulled Low, the SLAVE mode is selected and an external microprocessor is required to configure the ZX6017 through the serial interface pins.

Next, the hardware addresses the PC_ATA//HOE pin. If the PC_ATA/HOE pin is held Low for 40 clocks (PC_MCLK_IN) after POR deassertion, the ZX6017 is enabled for ATA/IDE to ATA/IDE PASSTHROUGH mode. The PASSTHROUGH mode is for systems that

use the physical PCMCIA 68-pin connector but do not support PCMCIA protocol. If this pin is held High ($\overline{PC}$_ATA/$\overline{HOE}$), the device is placed into the PCMCIA mode. The override bits in register 00H determine what mode(s) the user can support.

Serial Port Operation (Master) Mode

After the ZX6017 determines that an external EEPROM is present (see Figure 2), the Ready/Busy pin on the PCMCIA interface is set to Busy. The ZX6017 internal sequencer starts up and reads EEPROM address 1eh. If EEPROM address 1Eh is loaded with a 1Ch then the EEPROM's data is considered to be valid. After that, the internal sequencer resets its address counter back to zero. Data from EEPROM's addresses [00-2F] is read out and put into the on-board registers of the ZX6017. The EEPROM sequencer then reads EEPROM addresses 30h to FFh and each byte is moved into the ZX6017 on-board attribute memory addresses 00-CFh. After loading the registers and attribute memory, the sequencer completes by clearing the Ready/Busy pin on the PCMCIA interface indicating 1 "Ready." If EEPROM address 1Eh does not contain 1Ch, then the sequencer stops. The PCMCIA Ready/Busy pin stays in the Busy state, the on-board registers of the ZX6017 remain in their default state, and attribute memory data is unknown. The user can program the off-board EEPROM through the PCMCIA interface by means of three special registers and ignore Busy.

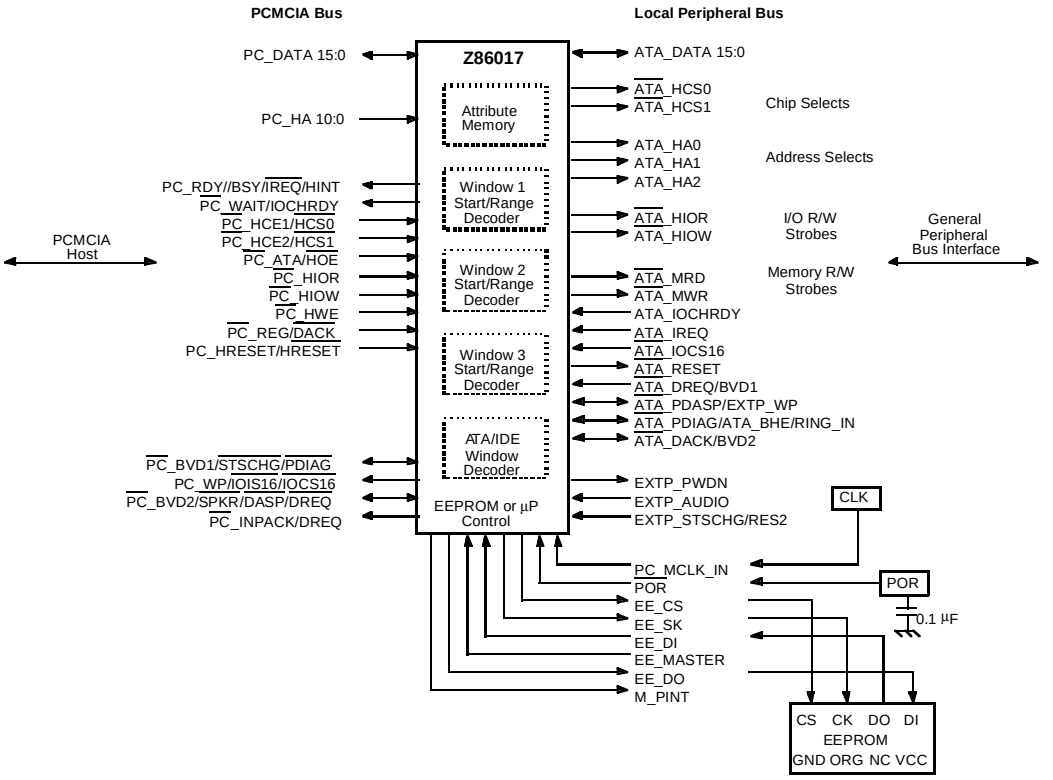


Figure 2. Serial Port Master Mode Control

Serial Port Operation (SLAVE) Mode

When the ZX6017 is placed in serial port SLAVE mode (EE_Master signal grounded on POR), the EEPROM sequencer is disabled and the user must provide external hardware (microprocessor) with serial interface to program CCRs and attribute memory. Additionally, if the

POR signal is deasserted, the user must provide a clock source on the PC_MCLK_IN pin in the range of 1-20MHz.

The external hardware can program the on-board registers and the attribute memory by selecting the ZX6017 and pulling the EE_CS pin High. The external hardware must set up the data to be sent to the ZX6017 on the EE_DI pin and strobe the EE_SK pin. The first byte of data is the address selected by the user, the second byte is the command byte and the third byte is the data. The external hardware must provide 24 clocks in order to read or write to a location in the ZX6017 (see Figure 26, Slave Interface Timing, in Appendix B).

To program the on-board attribute memory, the user must first write to it. Accomplish this programming by writing the address location of the attribute memory to be written (or read) in the attribute RAM data address register at location 08h. When this step has been accomplished, the user then writes (or reads) the attribute RAM data register 09h with the data to be read or written at that location.

Note: The attribute RAM address register auto-incriments after reading or writing to the attribute RAM data register.

Figure 3 demonstrates programming the ZX6017 in SLAVE Mode. The external user's hardware writes to register 00 and selects the clock divide by and the override mode (if needed). The READY/$\overline{\text{BUSY}}$ pin remains set to 0 to indicate BUSY, and a local µP interrupt polarity is selected.

The user programs registers 01-05, followed by registers 0Ah-2Fh. The user writes to the attribute memory by setting the address in the address register 08h and in the loop on data register 09h with the user's attribute memory data. The user completes the operation by writing back to register 00 to clear the READY/$\overline{\text{READY}}$ status.

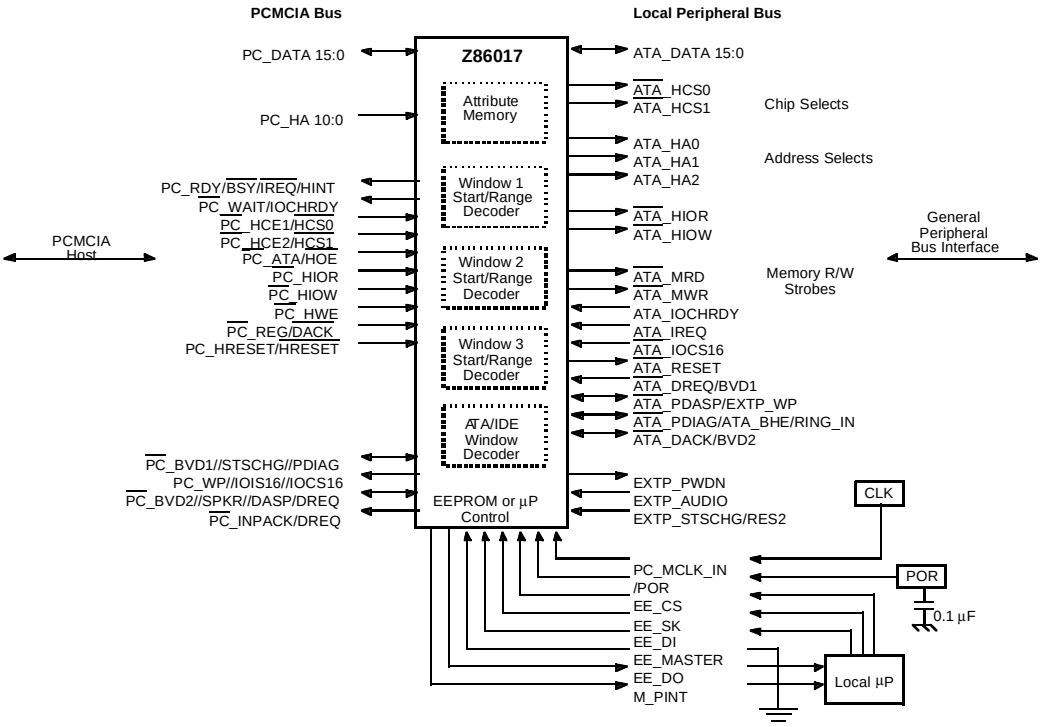


Figure 3. Serial Port Slave Mode Control

EEPROM Programming Through the PCMCIA Interface

The ZX6017 can program the serial EEPROM through the PCMCIA interface. EEPROM programming is accomplished by means of three special registers that are accessed identically to the CCR registers as defined by the PCMCIA specification (Figure 4). These registers are fixed at addresses 7F0, 7F2, and 7F4. The host software reads and writes each byte of the EEPROM through these registers and configures the

ZX6017 device. After the host writes new values to the EEPROM through these registers, the new values are loaded into the ZX6017 at Power-On Reset ($\overline{POR}$).

Note: The values written register 05h offset the CCR registers and the three special EEPROM programming registers on the next POR.

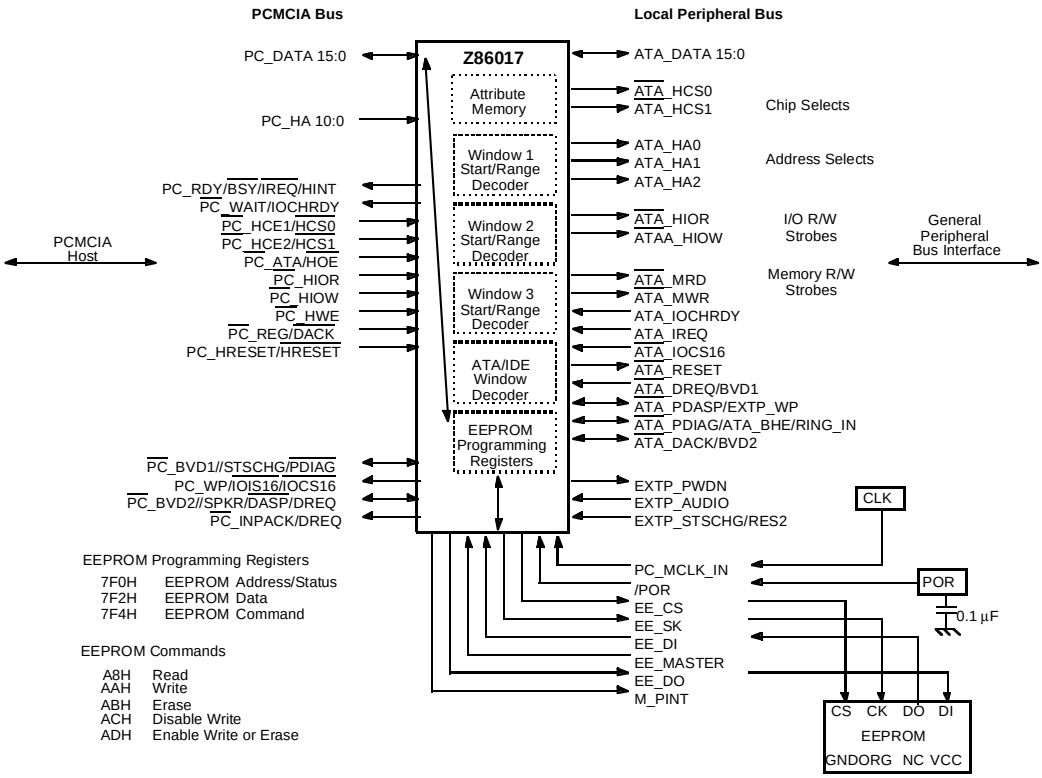


Figure 4. EEPROM Programming Through the PCMCIA Interface

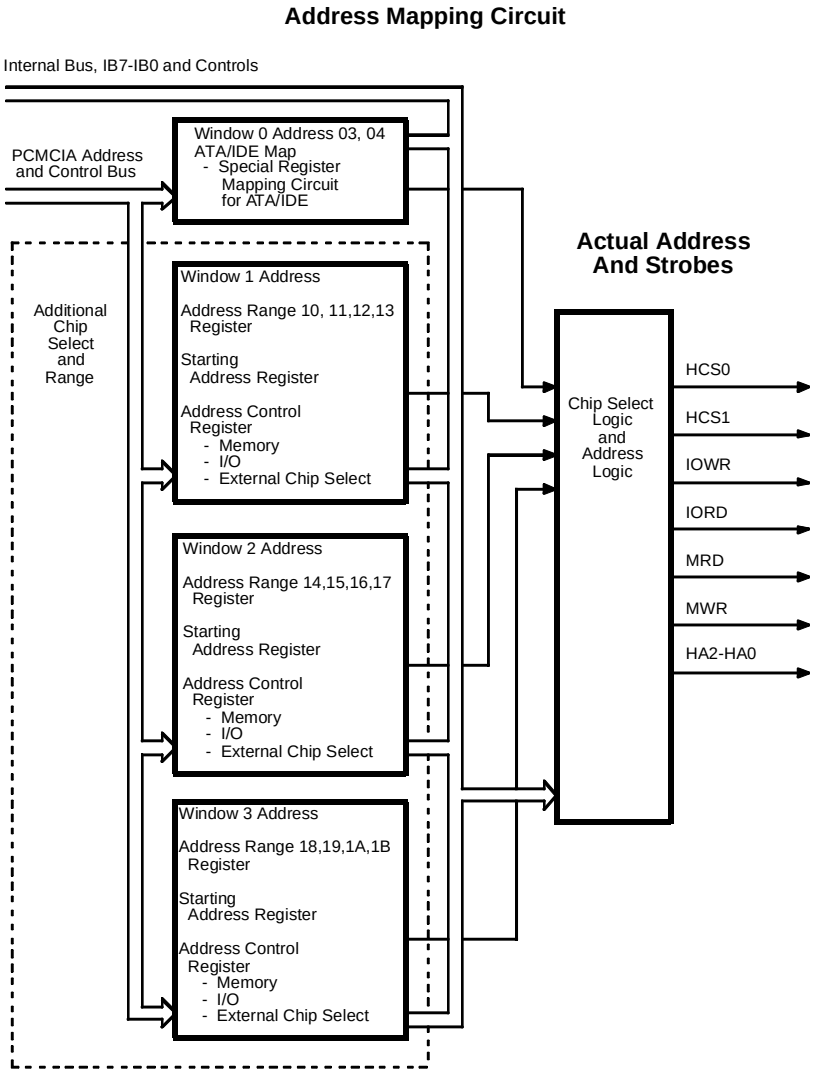


Figure 5. Connection Block Diagram

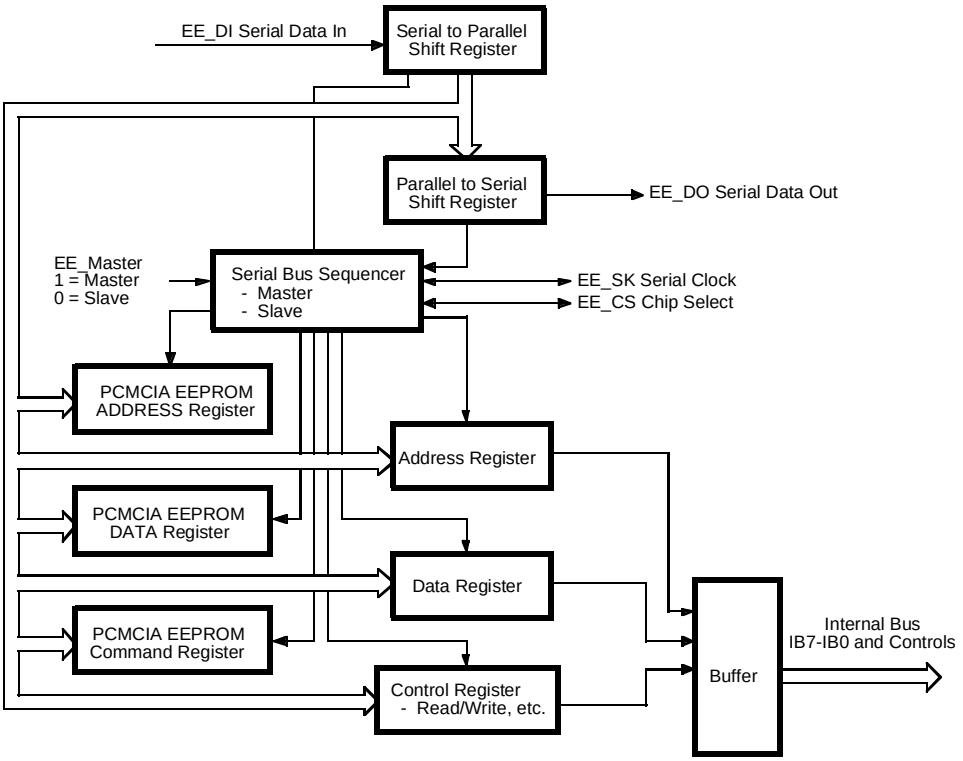


Figure 6. Serial Interface Diagram

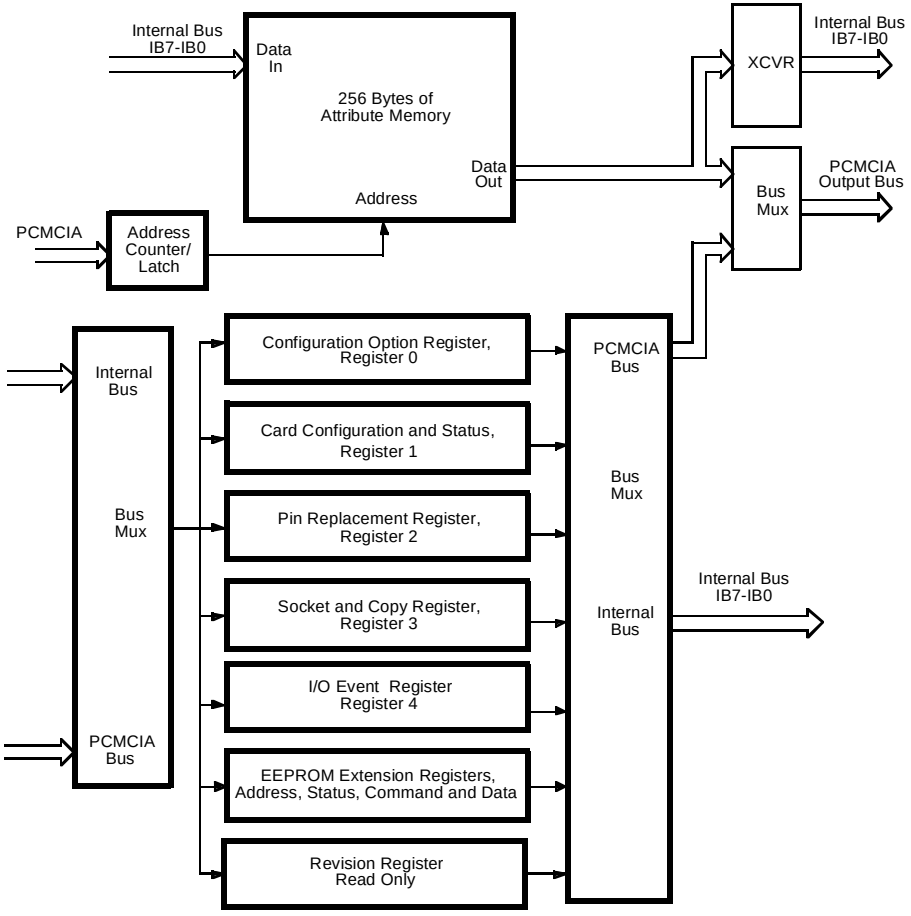


Figure 7. Attribute and Configuration Memory Diagram

PIN DESCRIPTION

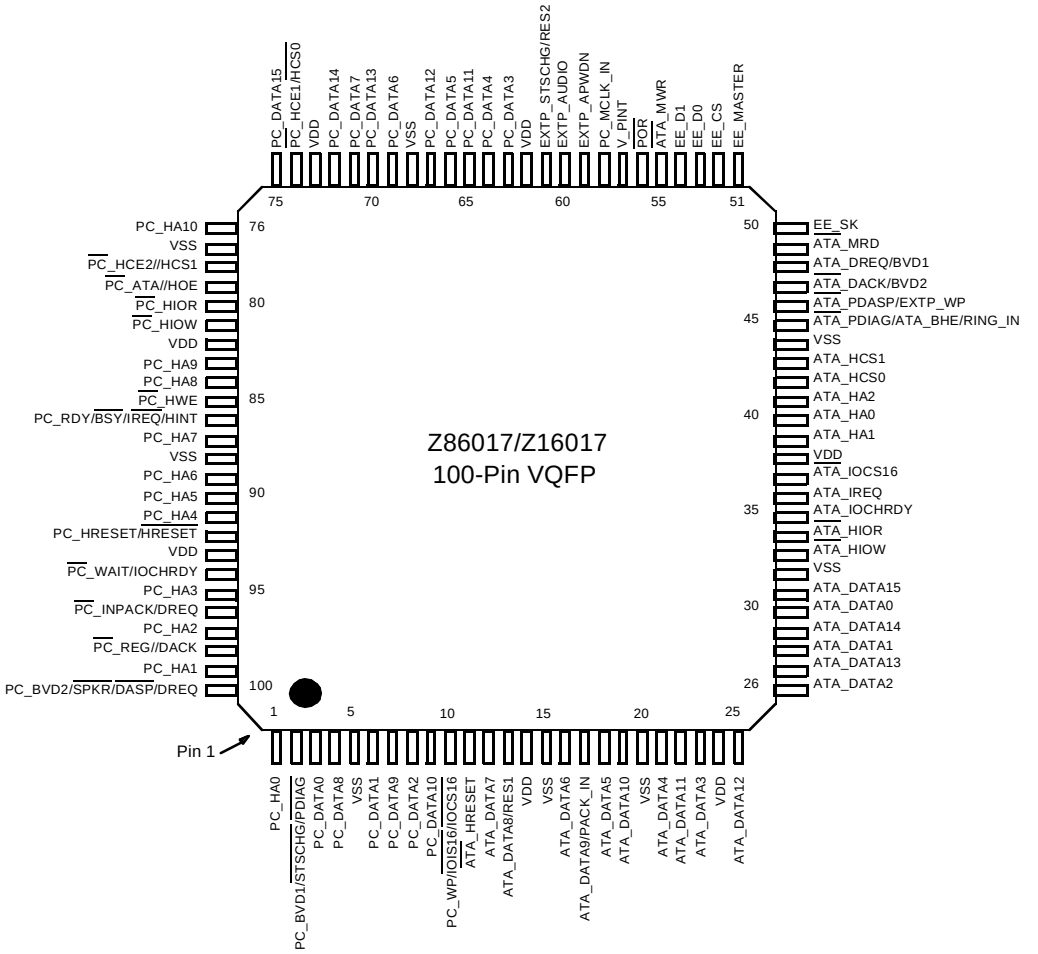


Figure 8. ZX6017 100-Pin VQFP Pin Configuration

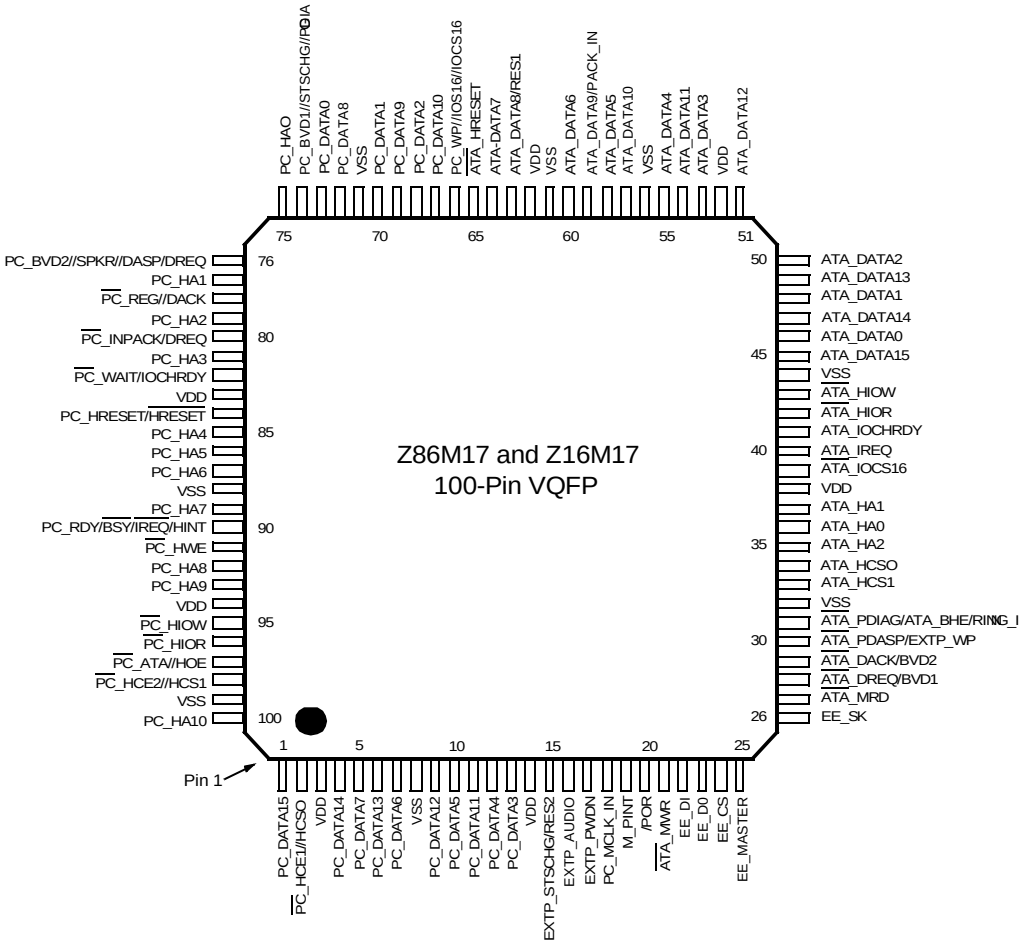


Figure 9. Z86M17 and Z16M17 (Mirror Image) 100-Pin VQFP Pin Configuration

PIN IDENTIFICATION

Table 3. 100-Pin VQFP Pin Identification

ZX6017	M17	Name	Description
1	75	PC_HA0	PCMCIA Address, Bit 0
2	74	PC_BVD1//STSCHG//PDIAG	Battery Voltage Detect 1, Status Change, PDiag
3	73	PC_DATA0	PCMCIA Data, Bit 0
4	72	PC_DATA8	PCMCIA Data, Bit 8
5	71	V_{SS}	Ground
6	70	PC_DATA1	PCMCIA Data, Bit 1
7	69	PC_DATA9	PCMCIA Data, Bit 9
8	68	PC_DATA2	PCMCIA Data, Bit 2
9	67	PC_DATA10	PCMCIA Data, Bit 10
10	66	PC_WP//IOIS16//IOCS16	Write Protect PCMCIA I/O Is 16-Bit Transfers
11	65	$\overline{\text{ATA\_HRESET}}$	AT Host RESET
12	64	ATA_DATA7	AT Host Data, Bit 7
13	63	ATA_DATA8/RES1	AT Host Data, Bit 8, Reserved Input 1
14	62	V_{DD}	Supply Voltage
15	61	V_{SS}	Ground
16	60	ATA_DATA6	AT Host Data, Bit 6
17	59	ATA_DATA9/PACK_IN	AT Host Data, Bit 9, PACK_IN
18	58	ATA_DATA5	AT Host Data, Bit 5
19	57	ATA_DATA10	AT Host Data, Bit 10
20	56	V_{SS}	Ground
21	55	ATA_DATA4	AT Host Data, Bit 4
22	54	ATA_DATA11	AT Host Data, Bit 11
23	53	ATA_DATA3	AT Host Data, Bit 3
24	52	V_{DD}	Supply Voltage
25	51	ATA_DATA12	AT Host Data, Bit 12
26	50	ATA_DATA2	AT Host Data, Bit 2
27	49	ATA_DATA13	AT Host Data, Bit 13
28	48	ATA_DATA1	AT Host Data, Bit 1

Table 3. 100-Pin VQFP Pin Identification (Continued)

ZX6017	M17	Name	Description
29	47	ATA_DATA14	AT Host Data, Bit 14
30	46	ATA_DATA0	AT Host Data, Bit 0
31	45	ATA_DATA15	AT Host Data, Bit 15
32	44	V_{SS}	Ground
33	43	$\overline{\text{ATA\_HIOW}}$	AT Host I/O Write Strobe
34	42	$\overline{\text{ATA\_HIOR}}$	AT Host I/O Read Strobe
35	41	ATA_IOCHRDY	AT Host I/O Channel Ready
36	40	ATA_IREQ	AT Host Interrupt Request
37	39	$\overline{\text{ATA\_IOCS16}}$	AT Host I/O Is 16 Bits Wide
38	38	V_{DD}	Supply Voltage
39	37	ATA_HA1	AT Host Address, Bit 1
40	36	ATA_HA0	AT Host Address, Bit 0
41	35	ATA_HA2	AT Host Address, Bit 2
42	34	ATA_HCS0	AT Host Chip Select 0
43	33	ATA_HCS1	AT Host Chip Select 1
44	32	V_{SS}	Ground
45	31	$\overline{\text{ATA\_PDIAG}}$/ATA_BHE/ Ring_IN	PDIAG I/O, Byte High Enable, RING_IN
46	30	$\overline{\text{ATA\_PDASP}}$/EXTP_WP	PDASP I/O or Write Protect In
47	29	$\overline{\text{ATA\_DACK}}$/BVD2	AT Host DMA Acknowledge, Battery Voltage Input 2
48	28	ATA_DREQ/BVD1	AT Host DMA Request, Battery Voltage Input 1
49	27	$\overline{\text{ATA\_MRD}}$	AT Host Memory Read Strobe
50	26	EE_SK	EEPROM Data Clock
51	25	EE_MASTER	EEPROM Is Master
52	24	EE_CS	EEPROM Data Chip Select
53	23	EE_DO	EEPROM Data Out
54	22	EE_DI	EEPROM Data In
55	21	$\overline{\text{ATA\_MWR}}$	AT Host Memory Write Strobe
56	20	POR	Power-On Reset
57	19	M_PINT	Local Processor Interrupt
58	18	PC_MCLK_IN	Master Clock In

Table 3. 100-Pin VQFP Pin Identification (Continued)

ZX6017	M17	Name	Description
59	17	EXTP_PWDN	Power Down Output
60	16	EXTP_AUDIO	Audio Input
61	15	EXTP_STSCHG/RES2	Status Change Input, Reserved Input 2
62	14	V_{DD}	Supply Voltage
63	13	PC_DATA3	PCMCIA Data, Bit 3
64	12	PC_DATA4	PCMCIA Data, Bit 4
65	11	PC_DATA11	PCMCIA Data, Bit 11
66	10	PC_DATA5	PCMCIA Data, Bit 5
67	9	PC_DATA12	PCMCIA Data, Bit 12
68	8	V_{SS}	Ground
69	7	PC_DATA6	PCMCIA Data, Bit 6
70	6	PC_DATA13	PCMCIA Data, Bit 13
71	5	PC_DATA7	PCMCIA Data, Bit 7
72	4	PC_DATA14	PCMCIA Data, Bit 14
73	3	V_{DD}	Supply Voltage
74	2	PC_HCE1//HCS0	PCMCIA Card Enable 1 $\overline{\text{ATA}}$ Chip Select 0
75	1	PC_DATA15	PCMCIA Data, Bit 15
76	100	PC_HA10	PCMCIA Address, Bit 10
77	99	V_{SS}	Ground
78	98	$\overline{\text{PC}}$_HCE2//HCS1	PCMCIA Card Enable 2 $\overline{\text{ATA}}$ Chip Select 1
79	97	$\overline{\text{PC}}$_ATA//HOE	Mode Select/PCMCIA Output Enable
80	96	$\overline{\text{PC}}$_HIOR	PCMCIA I/O Read Strobe
81	95	$\overline{\text{PC}}$_HIOW	PCMCIA I/O Write Strobe
82	94	V_{DD}	Supply Voltage
83	93	PC_HA9	PCMCIA Address, Bit 9
84	92	PC_HA8	PCMCIA Address, Bit 8
85	91	$\overline{\text{PC}}$_HWE	PCMCIA Write Enable
86	90	PC_RDY//BSY//IREQ/HINT	PCMCIA Ready/Busy, Interrupt Request
87	89	PC_HA7	PCMCIA Address, Bit 7
88	88	V_{SS}	Ground
89	87	PC_HA6	PCMCIA Address, Bit 6
90	86	PC_HA5	PCMCIA Address, Bit 5

Table 3. 100-Pin VQFP Pin Identification (Continued)

ZX6017	M17	Name	Description
91	85	PC_HA4	PCMCIA Address, Bit 4
92	84	PC_HRESET//HRESET	PCMCIA Reset
93	83	V_{DD}	Supply Voltage
94	82	$\overline{PC}$_WAIT/IOCHRDY	PCMCIA Wait, /IOCHRDY
95	81	PC_HA3	PCMCIA Address, Bit 3
96	80	$\overline{PC}$_INPACK/DREQ	PCMCIA Input Acknowledge, DREQ
97	79	PC_HA2	PCMCIA Address, Bit 2
98	78	$\overline{PC}$_REG//DACK	PCMCIA Register Signal, DACK
99	77	PC_HA1	PCMCIA Address, Bit 1
100	76	$\overline{PC}$_BVD2//SPKR//DASP/ DREQ	PCMCIA Battery Voltage Detect 2, Speaker Output, DASP, DREQ

PIN FUNCTIONS

PCMCIA Signals

- PC_DATA<15:0> *(I/O, Tristate, 8 mA)*
  PCMCIA Mode: 16-bit host Data bus.
  ATA/IDE Mode: 16-bit host Data bus.
- PC_HA<10:3> *(Input)*
  PCMCIA Mode: Host Address lines: 10,9,8,7,6,5,4,3.
  ATA/IDE Mode: Not used.
- PC_HA<2:0> *I(nput)*
  PCMCIA Mode: Host Address lines: 2,1,0.
  ATA/IDE Mode: Host Address lines: 2,1,0.
- $\overline{\text{PC}}$_HCE1//HCS0 *(Input, 100K Pull-Up)*
  PCMCIA Mode: This signal is Card Enable 1 (active Low).
  ATA/IDE Mode: Host Chip Select 0 (active Low).
- $\overline{\text{PC}}$_HCE2//HCS1 *(Input, 100K Pull-Up*)
  PCMCIA Mode: This signal is Card Enable 2 (active Low).
  ATA/IDE Mode: Host Chip Select 1 (active Low).
- $\overline{\text{PC}}$_REG/$\overline{\text{DACK}}$ *(Input, 100K Pull-Up)*
  PCMCIA Mode: (/REG), Register bit is asserted when the host selects I/O or Attribute Memory.
  ATA/IDE Mode: Data acknowledge (/DACK) defined in ATA. Issued during DMA data transfers on the data bus.
- $\overline{\text{PC}}$_ATA//HOE *(Input, 100K Pull-Up)*
  PCMCIA Mode: Memory Output Enable Strobe.
  ATA/IDE Mode: When pulled Low on Power-On Reset, this signal indicates ATA/IDE mode.
- $\overline{\text{PC}}$_HWE *(Input, 100K Pull-Up)*
  PCMCIA Mode: Memory Write Enable Strobe.
  ATA/IDE Mode: Not used.

- $\overline{PC}$_HIOR *(Input, 100K Pull-Up)*
  PCMCIA Mode: In PCMCIA I/O mode, this is the Input/Output Read Strobe.
  ATA/IDE Mode: Input/Output Read Strobe.
- $\overline{PC}$_HIOW *(Input, 100K Pull-Up)*
  PCMCIA Mode: In PCMCIA I/O mode, this is the Input/Output Write Strobe.
  ATA/IDE Mode: Input/Output Write Strobe.
- PC_HRESET/$\overline{HRESET}$*(Input, Schmitt-Triggered, 100K Pull-Up)*
  PCMCIA Mode: Active High input Reset signal.
  ATA/IDE Mode: Active Low input Reset signal.
- PC_RDY/$\overline{BSY}$/$\overline{IREQ}$/HINT *(Output, 8 mA)*
  PCMCIA Mode: In PCMCIA memory mode, this signal is READY/$\overline{BUSY}$. This signal will be asserted BUSY by the RESET logic. In PCMCIA I/O mode, this signal is /IREQ.
  ATA/IDE Mode: When enabled, the HINT signal is used to interrupt the host (active High).
- PC_WP//IOIS16//IOCS16 *(Output, Tri-State, 8 mA)*
  PCMCIA Mode: In PCMCIA memory mode, this signal is Write Protected. In PCMCIA I/O mode, this signal is IOIS16 and indicates that a 16-bit capable I/O device is being accessed on the PCMCIA bus.
  ATA/IDE Mode: I/O chip select 16 indicates that a 16- bit transfer is active on the bus.
- $\overline{PC}$_WAIT/IOCHRDY *(Output, Tri-State, 8 mA)*
  PCMCIA Mode: Insert Wait States when held active and the chip is being selected in I/O or memory mode.
  ATA/IDE Mode: Inserts Wait States when held active, and when the chip is being selected.
- $\overline{PC}$_INPACK/DREQ *(Output, Tri-State, 8 mA)*
  PCMCIA Mode: In PCMCIA I/O mode this signal is Input Acknowledge. It is asserted by the card when the card is selected and

can respond to an I/O cycle at the address on the address bus.
ATA/IDE Mode: This signal is Data request (DREQ), defined in ATA. It is issued during DMA data transfers on the data bus.

- PC_BVD1/$\overline{\text{STSCHG}}$/$\overline{\text{PDIAG}}$ *(I/O, 8 mA)*
  PCMCIA Memory Mode: Battery Voltage Detect 1, output.
  PCMCIA I/O Mode: Status Changed. This signal is used to indicate the change of status in the Pin Replacement Register (I/O Mode) or state of the BVD1 input when in Memory Mode.
  ATA/IDE Mode: Passed diagnostics.
- PC_BVD2/$\overline{\text{SPKR}}$/$\overline{\text{DASP}}$/DREQ (I/O, Tri-State, 10 mA)
  PCMCIA Memory Mode: Battery Voltage Detect 2, output.
  PCMCIA I/O Mode: SPKR, inverted AUDIO_EXTP signal, output;
  PCMCIA ATA Mode: ATA Data Request is the input pin for this signal, when DMA Enable bit is set in Window Start/Range Address registers.
  ATA/IDE Mode: Drive active/Slave present DASP.
- ATA_DATA<15:10> *(I/O, Tri-State, 8 mA*)
  ATA/IDE Mode: Host Data Bus, bits: 15,14,13,12,11,10.

Peripheral or ATA/IDE Signals

- ATA_DATA<15:10> *(I/O, Tri-State, 8 mA)*
  ATA/IDE Mode: Host Data Bus, bits: 15,14,13,12,11,10.
  Peripheral Mode: Peripheral data bus, bits: 15, 14, 13, 12, 11,10.
- ATA_DATA9/PACK_IN *(I/O, Tri-State, 8 mA)*
  ATA/IDE Mode: Host Data Bus, bit: 9.
  Peripheral Mode: When 8-bit mode is enabled (on the Local side) ATA_DATA9 can be used as a PACK_IN input.
- ATA_DATA8/RES1 *(I/O, Tri-State, 8 mA)*
  ATA/IDE Mode: Host Data Bus, bit: 8.
  Peripheral Mode: When 8-bit mode is enabled (on the Local side), ATA_DATA8 can be used as a RES1 input.
- ATA_DATA<7:0> *(I/O, Tri-State, 8 mA)*
  ATA/IDE Mode: Host Data Bus, bits: 7,6,5,4,3,2,1,0.
  Peripheral Mode: Peripheral Data Bus, bits: 7,6,5,4,3,2,1,0.
- ATA_HA<2:0> *(Output, 8 mA)*
  ATA/IDE Mode: ATA Host Address bits used to address the IDE interface chip.
  Peripheral Mode: Lower three bits offset from starting address.
- $\overline{\text{ATA}}$_HCS0 *(Output, 8 mA)*
  ATA/IDE Mode: ATA Host Chip Select 0, used to select the IDE interface chip.
  Peripheral Mode: Chip Select 0 used as a chip select for an external peripheral device as defined by the address range and offset register definition.
- $\overline{\text{ATA}}$_HCS1 *(Output, 8 mA)*
  ATA/IDE Mode: ATA Host Chip Select 1, used to select the IDE interface chip.
  Peripheral Mode: Chip Select 1 used as a chip select for an external peripheral device as defined by the address range and offset register definition.

- $\overline{\text{ATA}}$_HIOR *(Output, 8 mA)*
  ATA/IDE Mode: ATA Host I/O Read Strobe.
  Peripheral Mode: I/O read strobe or memory read strobe, depending on configuration.
- $\overline{\text{ATA}}$_HIOW *(Output, 8 mA)*
  ATA/IDE Mode: ATA Host I/O Write Strobe.
  Peripheral Mode: I/O Write Strobe or Memory Write Strobe, depending on configuration.
- $\overline{\text{ATA}}$_IOCS16 *(Input, 100K Pull-Up)*
  ATA/IDE Mode: I/O channel is 16 bits wide; input on the local ATA bus.
  Peripheral Mode: I/O access is 16 bits wide.
- ATA_IREQ *(Input)*
  ATA/IDE Mode: ATA/IDE host Interrupt Request.
  Peripheral Mode: Interrupt Request.
- ATA_IOCHRDY *(Input, 100K Pull-Up)*
  ATA/IDE Mode: ATA/IDE I/O Channel Ready-Input.
  Peripheral Mode: I/O Channel Ready.
- $\overline{\text{ATA}}$_HRESET *(Output, 8 mA)*
  ATA/IDE Mode: ATA Host Reset-Output to the ATA/IDE controller (programmable).
  Peripheral Mode: Host reset output to the peripheral device if PCMCIA signal is active (programmable).
- ATA_DREQ/BVD1 *(Input)*
  ATA/IDE Mode: ATA/IDE DMA request from the ATA/IDE controller.
  Peripheral Mode: Peripheral bus DMA Request or when in memory mode Battery Voltage 1 Detect input.
- $\overline{\text{ATA}}$_DACK/BVD2 *(I/O, 8 mA)*
  ATA/IDE Mode: ATA/IDE host DMA Acknowledge.
  Peripheral Mode: Peripheral Bus DMA Acknowledge. DMA

acknowledge is generated by the ZX6017 whenever DMA Acknowledge is enabled in the Window Start/Range Address registers and the address corresponds to the DMA address; or Battery Voltage 2 Detect input in memory mode.

- $\overline{\text{ATA}}$_PDASP/EXTP_WP *(I/O, Tri-State, 8 mA)*
  ATA/IDE Mode: ATA/IDE bus side PDASP signal controlled by internal bits ZEN_EXT_PDASP (Input) or ZEN_INT_PDASP (Output).
  Peripheral Mode: When configured as a Write Protect input, this pin will disable Write on the peripheral bus side.
- $\overline{\text{ATA}}$_PDIAG/ATA_BHE/RING_IN *(I/O, Tri-State, 8 mA*)
  ATA/IDE Mode: ATA/IDE bus side PDIAG signal controlled by internal bits ZEN_EXT_PDIAG (Input) or ZEN_INT_PDIAG (Output).
  Peripheral Mode: When configured as Byte High Enable for memory boards, ATA_BHE indicates High byte available, or it can be configured to be the RING_IN input signal for the I/O event indicator CCR4.
- $\overline{\text{ATA}}$_MRD *(Output, 8 mA)*
  ATA/IDE Mode: Not used.
  Peripheral Mode: External Memory Read Strobe.
- $\overline{\text{ATA}}$_MWR *(Output, 8 mA)*
  ATA/IDE Mode: Not used.
  Peripheral Mode: External Memory Write Strobe.

Serial Interface Signals

- EE_DO *(Output, 8 mA, Tri-State)*
  Master Mode: EEPROM data out Serial data, valid during EE_SK edge. In master mode, this signal is an output.
  Slave Mode: In slave mode, this signal is an output.
- EE_SK *(I/O, 8 mA)*
  Master Mode: EEPROM data clock. This signal is an output in master mode. It is active during R/W cycle only.
  Slave Mode: In slave mode, this signal is an input.
- EE_CS *(I/O, 8 mA)*
  Master Mode: EEPROM data chip select. This signal is an output in master mode.
  Slave Mode: In slave mode this signal is an input. This signal is active High.
- EE_DI *(Input, 100K Pull-Up)*
  Master Mode: EEPROM data in. This signal is an input in master mode.
  Slave Mode: In slave mode, this signal is an input.
- EE_MASTER (I*nput, Schmitt-Triggered, 100K Pull-Up)*
  Master/Slave mode detect: When set Low, no EEPROM is present. When set High EEPROM is present.

Peripheral Control Signals

- $\overline{\text{POR}}$ *(Input, Schmitt-Triggered, 100K Pull-Up)*
  Local Power-On Reset signal. A 0.1mF capacitor is recommended on this pin to GND to generate a POR.
- M_PINT (Output, Tri-State, 8 mA)
  Interrupt to local microprocessor
- PC_MCLK_IN *(Input, Schmitt-Triggered)*
  Master Clock In. This is an input signal. This clock signal is used to generate all internal timing. All local bus signals are asynchronous to this clock.
- EXTP_STSCHG/RES2 *(Input, 100K Pull-Up)*
  Status Change Input. This signal outputs the value of the status changed line on the PCMCIA bus if enabled in the CCR register, or it is an input for bit 7 (RSVDEVT3) in CCR4.
- EXTP_AUDIO *(Input 100K Pull-Up)*
  Audio Input. This input signal reflects the audio output. This signal is active High, and the Speaker output on the PCMCIA bus is active Low.
- EXTP_PWDN *(Output, 8 mA)*
  Power Down Output. This signal reflects the state of the Power Down bit in the CCR.
- V_{SS} *(Input)*
  Ground.
- V_{DD} *(Input)*
  Supply Voltage.

Addressing Modes

- The ZX6017 supports all PCMCIA Addressing Modes:
- PCMCIA Common Memory Mode
- PCMCIA I/O Mode
- PCMCIA ATA_IDE Mode
- Pass-through ATA/IDE-to-ATA/IDE Mode

Note: This mode is for users who have a 68-pin PCMCIA connector, but are using ATA/IDE protocol instead of PCMCIA protocol.

The overall ZX6017 mode of operation is controlled by the Interface Configuration Register (00h) bits 3,2. 00 in these two bits sets the device to ATA/IDE mode if the $\overline{PC}$_ATA/$\overline{HOE}$ pin is Low on power-up and into PCMCIA mode if the pin is High. The default for this register is 00 and the $\overline{PC}$_ATA/$\overline{HOE}$ pin determines the mode of operation, PCMCIA or ATA/IDE. Table 4 describes these addressing modes.

Table 4. ZX6017 Addressing Modes

Mode/Bus	PCMCIA	Peripheral Bus	Comments
Memory	Memory	Memory	
I/O	I/O	I/O	
PCMCIA_ATA_Memory	Memory	ATA	
PCMCIA_ATA_I/O	I/O	Primary ATA Secondary ATA Contiguous ATA	Contiguous block of at least 16 I/O registers is assigned to one card.
Pass-Through Mode	ATA/IDE	ATA/IDE	

To place the ZX6017 into proper Addressing mode, a set of Configuration Registers and Memory Maps reside on-chip.

The four on-chip address maps are:

- Memory_Map_1
- Memory_Map_2
- Memory_Map_3
- PCMCIA_ATA/IDE Map

Memory_Map_1, _2 and _3 support PCMCIA Memory/IO Mode. The chip can be configured in PCMCIA Mode either by:

- Pulling the $\overline{\text{PC}}$_ATA/HOE pin High during RESET;

or by

- Writing 10 in Override bits (bits 3, 2) in the Interface Configuration Register 0 (address 00h), and 0 in bits 0, 1, 2, 6 of the Interface Configuration Register 02 (address 03h).

After placing the device into PCMCIA Mode, each Map can be configured independently through its set of configuration registers.

Each Memory Map contains a set of Configuration Registers consisting of:

- Window Control Register
- Window Start Address LSB Register
- Window Start/Range Address MSB
- Window Range Address LSB

The PCMCIA_ATA/IDE Map enables chip operation in PCMCIA_ATA/IDE mode. When in this mode, the chip responds to different types of accesses, depending on the content of the following registers:

- Interface Configuration Register 02, address 03h (bits 0, 1, 6)
- Interface Configuration Register 03, address 04h (bits 0, 1, 2, 3)
- PCMCIA Exception Status Register, address 071h (bit 0)

Table 5 describes programming PCMCIA_ATA ZX6017 Configuration Registers.

Table 5. Programming PCMCIA_ATA ZX6017 Configuration Registers

ICR_2 [1:0] addr03	ICR_02[6] addr03	ICR_03[3:0] addr04	CICR_1[7:0] addr2DH	CICR_2[7:0] addr2EH	CCR0[5:0] addr0AH	addr 07[0}	Description
x	x	xxxx	xxxxxxxx	xxxxxxxx	xxxxx	1	Chip operates in ATA/IDE-to-ATA/IDE passthrough mode
11	0	xxxx	xxxxxxxx	xxxxxxxx	xxxxx	0	PCMCIA Mode
11	1	1111	FFH	FFH	00011	0	Enabled access to Primary set of IDE Task File Registers (1Fo-1F7)
11	1	1111	FFH	FFH	00011	0	Enabled access to Primary set of IDE Task File Registers (3F6-3F7)
11	1	1111	FFH	FFH	00010	0	Enabled access to Secondary set of IDE Task File Registers

Table 5. Programming PCMCIA_ATA ZX6017 Configuration Registers (Continued)

ICR_2 [1:0] addr03	ICR_02[6] addr03	ICR_03[3:0] addr04	CICR_1[7:0] addr2DH	CICR_2[7:0] addr2EH	CCR0[5:0] addr0AH	addr 07[0}	Description
11	1	1111	FFH	FFH	00001	0	PCMCIA_AA Independent IO Mode. Chip responds to any 1/0 access in the range 000 to 00Fh
11	1	1111	FFH	FFH	00000	0	PCMCIA Independent Memory Mode. Chip responds to any Memory access in the range 000-00Fh

Tables 6 through Table 9 provide ZX6017 addressing information in each mode.

Table 6. PCMCIA Common Memory Mode

Function Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{0E}$	WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High-Z	High-Z
Byte Access	H	H	L	L	L	H	High-Z	Even-Byte
	H	H	L	H	L	H	High-Z	Odd-Byte
Word Access	H	L	L	Z	L	H	Odd-Byte	Even-Byte
Odd-Byte only access	H	L	H	X	H	L	Odd-Byte	XX

Table 7. PCMCIA I/O Mode

Function Mode	REG	CE2	CE1	A0	OE	WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High-Z	High-Z
Byte Access	H	H	L	L	L	H	High-Z	Even-byte
	H	H	L	H	L	H	High-Z	Odd-byte
Word Access	H	L	L	Z	L	H	Odd-byte	Even-byte
I/O Inhibit	H	X	X	X	L	H	High-Z	High-Z
Odd-byte only access	L	L	H	X	L	H	Odd-byte	High-Z
Byte Access	L	H	L	L	H	L	X	Even-byte
	L	H	L	H	H	L	X	Odd-Byte
Word Access	L	L	L	L	H	L	Odd-byte	Even-byte
I/O Inhibit	H	X	X	X	H	L	X	X
Odd-byte only access	L	L	H	X	H	L	Odd-byte	X

Table 8. PCMCIA_ATA Memory Mapped Access

REG#	A10	A[9:4]	A3	A2	A1	A0	OE#	WE#
H	L	X	L	L	L	L	Read Data	Write Data
H	L	X	L	L	L	H	Error	Feature
H	L	X	L	L	H	L	Sector Count	Sector Count
H	L	X	L	L	H	H	Sector Number	Sector Number
H	L	X	L	H	L	L	Cylinder Low	Cylinder Low
H	L	X	L	H	L	H	Cylinder High	Cylinder High
H	L	X	L	H	H	L	Drive/Head	Drive/Head

Table 8. PCMCIA_ATA Memory Mapped Access

REG#	A10	A[9:4]	A3	A2	A1	A0	OE#	WE#
H	L	X	L	H	H	H	Status	Status
H	L	X	H	L	L	L	Duplicate Even Read Data	Duplicate Even Write Data
H	L	X	H	L	L	H	Duplicate Odd Read Data	Duplicate Odd Write Data
H	L	X	H	H	L	H	Duplicate Error	Duplicate Feature
H	L	X	H	H	H	L	Alt Status	Device Control
H	L	X	H	H	H	H	Drive Address	Reserved
H	H	X	X	X	X	L	Even Read Data	Even Write Data
H	H	X	X	X	X	H	Odd Read Data	Odd Write Data

Table 9. PCMCIA_ATA I/O Mapped Access

REG#	Primary A[9:0]	Secondary A[9:0]	Contiguous A[3:0]	IORD# = L	IOWR# = L
L	1F0H	170H	00H	Read Data	Write Data
L	1F1H	171H	01H	Error	Feature
L	1F2H	172H	02H	Sector Count	Sector Count
L	1F3H	173H	03H	Sector Number	Sector Number
L	1F4H	174H	04H	Cylinder Low	Cylinder Low
L	1F5H	175H	05H	Cylinder High	Cylinder High
L	1F6H	176H	06H	Drive/Head	Drive/Head
L	1F7H	177	07H	Status	Command
L	–	–	08H	Duplicate Even Read Data	Duplicate Even Write Data
L	–	–	09H	Duplicate Odd Read Data	Duplicate Odd Write Data
L	–	–	0DH	Duplicate Error	Duplicate Feature
L	1F6H	376H	0EH	Alt Status	Device Control
L	3F7H	377H	0FH	Drive Access	Reserved

Programming Internal Registers

INTRODUCTION

As stated in "Addressing Modes" on page 25, the ZX6017 devices feature a set of on-chip programmable registers that can be programmed either by using the on-board EEPROM Sequencer (MASTER Mode) or by Local Microprocessor (SLAVE Mode). A set of Card Configuration Registers can be accessed from the PCMCIA interface. Table 10 lists the programmable registers.

Table 10. ZX6017 Card Configuration Registers

EEPROM Address	PCMCIA Address	Register's Name	Access	POR Value	Comments
00h	NA	Interface Configuration Rg 0	R/W	00h	
01h	NA	Interrupt Enable Rg	R/W	00h	
02h	NA	Interface Configuration Rg 1	R/W	00h	
03h	NA	Interface Configuration Rg 2	R/W	00h	
04h	NA	Interface Configuration Rg 3	R/W	00h	
05h	NA	PCMCIA CCR's Base Rg	R/W	00h	
06h	NA	PCMCIA Interrupt Status Rg	R	00h	Note[1]
07h	NA	PCMCIA Exception Status Rg	R	00h	Note[1]
08h	NA	Attribute RAM Address Rg	W	XX	Note[1]
09h	NA	Attribute RAM Data Rg	R/W	XX	Note[1]
0Ah	XX0h	PCMCIA Configuration Option Rg (CCR0)	R/W	00h	Note[2]
0Bh	XX2h	PCMCIA Card Configuration and Status Rg (CCR1)	R/W	00h	Note[2]
0Ch	XX4h	PCMCIA Pin Replacement Rg (CCR2)	R/W	00h	Note[2]
0Dh	XX6h	PCMCIA Socket and Copy Rg (CCR3)	R/W	00h	Note[2]
0Eh–0Fh		Reserved		XX	
10h	NA	Window 1 Control Rg	R/W	01h	
11h	NA	Window 1 Start Address LSB Rg	R/W	00h	

Table 10. ZX6017 Card Configuration Registers (Continued)

EEPROM Address	PCMCIA Address	Register's Name	Access	POR Value	Comments
12h	NA	Window 1 Start/Range Address MSB Rg	R/W	00h	
13h	NA	Window 1 Range Address LSB Rg	R/W	00h	
14h	NA	Window 2 Control Rg	R/W	01h	
15h	NA	Window 2 Start Address LSB Rg	R/W	00h	
16h	NA	Window 2 Start/Range Address MSB Rg	R/W	00h	
17h	NA	Window 2 Range Address LSB Rg	R/W	00h	
18h	NA	Window 3 Control Rg	R/W	01h	
19h	NA	Window 3 Start Address LSB Rg	R/W	00h	
1Ah	NA	Window 3 Start/Range Address MSB Rg	R/W	00h	
1Bh	NA	Window 3 Range Address LSB Rg	R/W	00h	
1Ch–1Dh		Reserved		XX	
1Eh	NA	EEPROM Valid Flag Byte Rg (1Ch)	R/W	00h	Master Mode only
1Fh	XX8h	PCMCIA I/O Event Indication Rg (CCR4)	R/W	00h	Note[2], Note[3]
20h	7F0h	EEPROM Addr/Status Rg (CCR5) Back Door	R/W	00h	Note[1]
21h	7F2h	EEPROM Data Rg (CCR6) Back Door	R/W	00h	Note[1]
22h	7F4h	EEPROM Command Rg (CCR7) Back Door	R/W	00h	Note[1]
23h	NA	Revision Control Rg	R/W	00h	Note[3]
24h	7F6h	Revision Number Rg	R		Note[4]
25h		Reserved	R/W	XX	
26h	NA	Bus Control Rg 1	R/W	00h	Note[5]
27h	NA	IOIS16 Address Control Rg	R/W	00h	Note[5]

Table 10. ZX6017 Card Configuration Registers (Continued)

EEPROM Address	PCMCIA Address	Register's Name	Access	POR Value	Comments
28h	NA	ATA/IDE Dual Drive Control Rg	R/W	00h	Note[3]
29h		Reserved	R/W	00h	
2Ah	NA	Power Management Timer Count Value Rg	R/W	00h	Note[3]
2Bh	NA	Power Management Control Rg	R/W	00h	Note[3]
2Ch	NA	Interface Con•guration Rg 4	R/W	00h	Note[3]
2Dh	NA	Con•guration Index Compare Rg 1	R/W	00h	Note[3]
2Eh	NA	Con•guration Index Compare Rg 2	R/W	00h	Note[3]
2Fh	NA	Bus Control Rg 2	R/W	00h	Note[3]
30h–FFh		User-Definable Attribute Memory Location 00h–CFh (208-byte)	R/W	XXh	Note[6]

NOTES:
1. When the ZX6017 is in Master Mode, the user should program this location in EEPROM with 00h.
2. The PCMCIA base address for these registers could be set in the range of 000h–400h. At Power-On Reset (POR), the base is set to 000h.
3. User must write the Revision Number (see ZX6017 top mark) to the Revision Control register to unlock these registers.
4. The Z86017 BA Revision Number is 10h (see device top mark).
5. These registers are only available on the Z16017.
6. When the ZX6017 is in Master Mode, data at EEPROM addresses 30h–FFh are written locations 00h–CFh of the on-board Attribute Memory. In Slave Mode, Attribute Memory is programmed through registers 08h and 09h.

EEPROM REGISTER

EEPROM Register

Address: SELECT 00h
Name: Interface Configuration Register 0
Type: Read/Write

Table 11. Interface Configuration Register: Address 00h

Bit Placement	Bit Name	Description
Bits 1–0	Set Internal	Internal Clock Divider. On Power-On Reset, clock divide-by-32 selects the Master Clock. On Power-On Reset, set these bits to 0 0. Table 12 describes Master Clock Settings. Bit 1 Bit 0 0 0 Slowest Clock, Clock In divide-by-32 1 1 Clock In divide-by-16 1 0 Clock In divide-by-4 1 1 Clock In
Bits 3–2	EN_OVERIDE	Overrides PCMCIA ATA mode bits, /PC_ATA//HOE selection on the PCMCIA interface. On Power-On Reset, both bits are set to 0. Sample /PC_ATA//HOE. Bit 3 Bit 2 0 0 PC_ATA/$\overline{\text{HOE}}$ Sampled to Set Mode 0 1 Forces ATA/IDE Pass Through Mode 1 0 Forces PCMCIA Mode 1 1 Reserved

Table 11. Interface Configuration Register: Address 00h (Continued)

Bit Placement	Bit Name	Description
Bit 4	EN_RDY_BSY	When this bit is set to 1, the PC_RDY/$\overline{\text{BSY}}$/$\overline{\text{REQ}}$/$\overline{\text{HINT}}$ pin is configured as RDY//BSY. To con•gure this pin as an IREQ/HINT, set this bit to 0. On Power-On Reset, the ZX6017 automatically reads the EEPROM and also determines if a PCMCIA device is connected. After the entire attribute memory is loaded and the chip initialization is complete, the READY/$\overline{\text{BSY}}$ signal on the PCMCIA bus indicates READY. Without an EEPROM, the device indicates READY whenever this bit is set and the ZX6017 has determined a PCMCIA bus is connected.
Bit 5	EN_CTR_IRQ	Enables PCMCIA Interrupt Mode. Enables ATA_IREQ pin to control PC_IREQ in I/O Mode. This bit is active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 6	EN_INT_POL	Enable local (M_PINT) processor interrupt polarity active Low. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Interrupt is active High. M_PINT is a tri-state driven signal. Whenever an interrupt is present and enabled, M_PINT is driven. If the interrupt is programmed active High, then M_PINT is driven from tri-state to High. If the interrupt polarity selects active Low interrupts, then the interrupt is driven from tri-state to active Low. Also see Register 2Ch.
Bit 7	EN_ATA_BHE	When this bit is set to 1, it enables the ATA_PDIAG/ ATA_BHE/RING_IN pin to be used as a Byte High Enable pin on a local interface side. Byte High Enable is used to signify that a PCMCIA host is requesting or sending data on the high byte bus pins ATA_DATA[15-8] of the local bus. For ATA_BHE, also see Register 2Fh. When set to 0, ATA_PDIAG/ATA_BHE/RING_IN is used as a local bidirectional PDIAG pin. On Power-On Reset, this bit is set to 0.

Table 12. Master Clock

Register 0 Bit 1	Register 0 Bit 9	Clock In	EEPROM CLK Timing	Interrupt Pulse[1] Width	Comments
0	0	50 ns	6.4 µs	204 µs	
0	1	50 ns	3.2 µs	102 µs	
1	0	50 ns	800 ns	25 µs	Recommended
1	1	50 ns	200 ns	5.25 µs	
0	0	100 ns	12.8 µs	404 µs	
0	1	100 ns	6.4 µs	204 µs	
1	0	100 ns	1.6 µs	50 µs	
1	1	100 ns	400 ns	12.5 µs	Recommended

NOTES:

1. The pulse width of the /PC.IREQ signal in pulse mode is dependent on the clock period of the master clock input (TPMCKIN). The pulse width of the /PC.IREQ signal is equal to 192 x TPMCKIN.

EEPROM Register
Address: SELECT 01h
Name: Interrupt Enable Register
Type: Read/Write

Table 13. Interrupt Enable Register: Address 01h

Bit Placement	Bit Name	Description
Bit 0	EN_PC_INT0	Enables Local Processor interrupt when PCMCIA host has written CCR0, the Con•guration Option Register. This interrupt stays present until this bit is set to 0. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Also see Registers 06h, 2Ch.
Bit 1	EN_PC_INT1	Enables Local Processor interrupt when PCMCIA host has written CCR1, the Card Status Register. This interrupt stays present until this bit is set to 0. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Also see Registers 06h, 2Ch.
Bit 2	EN_PC_INT2	Enables Local Processor interrupt when PCMCIA host has written CCR2, the Pin Replacement Register. This interrupt stays present until this bit is set to 0. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Also see Registers 06h, 2Ch.
Bit 3	EN_PC_INT3	Enables Local Processor interrupt when PCMCIA host has written CCR3, the Socket and Copy Register. This interrupt stays present until this bit is set to 0. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Also see Registers 06h, 2Ch.
Bit 4	EN_PC_INT4	Enables Local Processor interrupt when ATA_IREQ is asserted. This interrupt stays present until this bit is set to 0. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Also see Registers 06h, 2Ch.
Bit 5	EN_EXTP_WP	Enables external write protect pin as an input when set to 1. When set to 0, this bit is DASP on the local AT bus side. On Power-On Reset, this bit is set to 0.

Table 13. Interrupt Enable Register: Address 01h (Continued)

Bit Placement	Bit Name	Description
Bit 6	CCR0_OVERIDE	ATA_DASP is used as a DASP pin. Also see Register 02h. Card Con•guration Register 0 is normally written after Power-On Reset by the PCMCIA host. If Interrupts are allowed by the local processor or EEPROM, then the PCMCIA READY/BSY signal is configured as an interrupt signal only when the Card Configuration Register is written. If the local processor does not require the PCMCIA host to write to CCR0, bit CCR0_OVERIDE can be set to force the internal logic to select the PCMCIA READY/BSY as the Interrupt pin, if interrupts are enabled. This bit is active when set to 1. On Power-On Reset, set this bit to 0, no override selected. PCMCIA host must select interrupts and write to the Card Con•guration Register 0.
Bit 7	EN_INPACK	Enable PCMCIA Input acknowledge when set to 1. On Power-On Reset, this bit is set to 0.

EEPROM Register

Address: SELECT 02h
Name: Interface Configuration Register 1
Type: Read/Write

Table 14. Interface Configuration Register 1: Address 02h

Bit Placement	Bit Name	Description
Bit 0	PDIAG_SET	When set to 1, this bit activates PDIAG on the PCMCIA bus side. On Power-On Reset, this bit is set to 0.
Bit 1	EN_PDIAG	When set to 1, this bit drives the PCMCIA pin on the PCMCIA side. On Power-On Reset, this bit is set to 0 (Table 15). Also see Registers 04h, 07h.
Bit 2	PDASP_SET	When set to 1, this bit sets the DASP pin on the PCMCIA side. On Power-On Reset, this bit is set to 0.
Bit 3	EN_DASP	When set to 1, this bit drives the DASP pin on the PCMCIA side. On Power-On Reset, this bit is set to 0 (Table 16).
Bit 4	EN_OR_CS01	When set to 1, this bit is active and ATA_HCS0 has the same level as ATA_HCS1. On Power-On Reset, this bit is set to 0 (Table 17). Also see Register 03h (Table 19).
Bit 5	EN_SPKR	When set to 1, this bit is active and connects EXTP_AUDIO (inverted) to the PC_BVD2//SPKR// DASP/DREQ pin. On Power-On Reset, this bit is set to 0 (Table 18).
Bit 6	EN_DASP_INT	When set to 1, DASP is generated internally. On Power-On Reset, this bit is set to 0.
Bit 7	EN_DASP_EXT	When set to 1, DASP is generated externally from the AT_DASP pin on the local AT bus side. On Power-On Reset, this bit is set to 0. Also see Register 01h (Table 13).

Table 15. PCMCIA PDIAG Pin Functions

Register2 Bit 1 EN_PDIAG	Register2 Bit 0 PDIAG_SET	Register 4 Bit 7 EN_PDIAG_EXT	Register4 Bit 6 EN_PDIAG_INT	ATA_PDIAG Pin I/O	PCMCIA PDIAG OUT I/O	Register 7 Bit5,PCMCIA PDIAG Input	Comments
0	X	X	X	X	Float - Z	PDIAG-OUT	Input mode
0	1	0	1	X	Float - Z	PDIAG-OUT	Input mode
1	1	0	1	X	1 (Output)	1	Output 1 (totem)
1	0	0	1	X	0 (Output)	0	Output 0 (totem)
1	0	1	0	0 (Input)	0 (Output)	0	Output generated from ATA-PDIAG.
1	0	1	0	1 (Input)	Float - Z	PDIAG-OUT	Output floated by ATA-PDIAG when set to 1.
0	0	0	1	0 (Output)	0 (Input)	0	ATA_PDIAG is sourced from PCMCIA side.
0	0	0	1	Float - Z	1 (Input)	1	

Table 16. PCMCIA DASP Pin Functions

Register2 Bit 3 EN_DASP	Register2 Bit 2 DASP_SET	Register2 Bit 7 EN_DASP_EXT	Register2 Bit 6 EN_DASP_INT	ATA_DASP Pin I/O	PCMCIA DASP OUT I/O	Register7 PCMCIA DASP Input	Comment
0	X	X	X	X	Float - Z	DASP-OUT	Input mode
0	1	0	1	X	Float- Z	DASP-OUT	Input mode
1	1	0	1	X	1 (Output)	1	Output 1 (totem)
1	0	0	1	X	0 (Output)	0	Output 0 (totem)
1	0	1	0	0 (Input)	0 (Output)	0	Output generated from ATA-DASP.
1	0	1	0	1 (Input)	Float- Z	DASP-OUT	Output floated when ATA-DASP is set to 1.
0	0	0	1	0 (Output)	0 (Input)	0	ATA_DASP is sourced from PCMCIA side.
0	0	0	1	Float - Z	1 (Input)	1	

Table 17. Host Chip Select Designations

Register 2 Bit 4 EN_OR_CS01	ATA_HCS0	Internal HCS1	ATA_HCS0 (External)
0	0	X	0
0	1	X	1
1	0	0	0
1	0	1	1
1	1	X	1

Table 18. Audio Pin Configurations

Register 2 Bit 5 EN_SPKR	EXTP_AUDIO	Register 7 Bit 0 ATA_MODE	Register 2 Bit 3 EN_DASP	PC_SPKR/ DASP//DREQ
0	X	0	0	Float - Z
1	0	0	0	1
1	1	0	0	0
1	0	0	0	AT_DREQ Input
0	0	0	0	AT_DREQ Input
0	0	1	x	DASP mode

EEPROM Register

Address: SELECT 03h
Name: Interface Configuration Register 2
Type: Read/Write

Table 19. Interface Configuration Register 2: Address 03h

Bit Placement	Bit Name	Description
Bit 0	EN_MEM_MODE	Enables PCMCIA memory access mode. This bit controls window0. It is active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 1	EN_INDP_MODE	Enables PCMCIA independent I/O access mode. This bit controls window0. It is active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 2	EN_ATT_MODE	Enables PCMCIA attribute memory access. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Also see Registers 08h and 09h (Table 28 and Table 29).
Bit 3	EN_INVERT_HCS0	Inverts the polarity of HCS0 output. HCS0 is active High when this bit is set. HCS0 is active Low when this bit is cleared. This bit is active when set to 1. On Power-On Reset, this bit is set to 0, active Low. Also see Register 02h (Table 14).
Bit 4	EN_INVERT_HCS1	Inverts the polarity of HCS1 output. HCS1 is active High when this bit is set. HCS1 is active Low when this bit is cleared. This bit is active when set to 1. On Power-On Reset, this bit is set to 0, active Low. Also see Register 02h (Table 14).
Bit 5	EN_INVERT_ATRST	Inverts the polarity of the ATA_HRESET output.
Bit 6	EN_IO_MODE	Enables PCMCIA/ATA/IDE access to 1Fx, 3Fx, 17x, 1Fx task Registers. This bit controls window0. This bit is active when set to 1. On Power-On-Reset, this bit is set to 0.
Bit 7	Reserved	

EEPROM Register

Address: SELECT 04h
Name: Interface Configuration Register 3
Type: Read/Write

Table 20. Interface Configuration Register 3: Address 04h

Bit Placement	Bit Name	Description
Bit 0	SEL_PRIMARY_1x	Enables IDE/PCMCIA access to primary task file addresses 1F<0-7>. This bit is active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 1	SEL_PRINARY_3x	Enables IDE/PCMCIA access to primary task file addresses 3F<6-7>. Active when set to 1. On Power-On Reset, this bit is set to 0 (Table 21).
Bit 2	SEL_SECOND_1x	Enables IDE/PCMCIA access to secondary task file addresses 17<0-7>. Active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 3	SEL_SECOND_3x	Enables IDE/PCMCIA access to secondary task file addresses 37<0-7>. Active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 4	STR_RST	Switching this bit from Low to High to Low again forces the ZX6017 to check the level on PC_ATA/HOE pin and latch the mode. This bit is active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 5	EN_DIS_RST	Disable PCMCIA reset. This bit is active when set to 1. Resets from the PCMCIA bus are not allowed. On Power-On Reset, this bit is set to 0 (Table 22).
Bit 6	EN_PDIAG_INT	When this bit is set to 1, PDIAG is generated internally. On Power-On Reset, this bit is set to 0. Also see Registers 02h and 07h (Table 14 and Table 26).
Bit 7	EN_PDIAG_EXT	When this bit is set to 1, PDIAG is generated externally through the AT_PDIAG pin on the local AT side. On Power-On Reset, this bit is set to 0. Also see Registers 02h and 07h (Table 14 and Table 26).

Table 21. ATA Register Selection Designations

Register 4 Bit 3 SEL_SECOND_3x	Register 4 Bit 2 SEL_SECOND_1x	Register 4 Bit 1 SEL_PRIMARY_3x	Register 4 Bit 0 SEL_PRIMARY_1x	Register 3 Bit 6 EN_IO_MODE	Address Range Response	Note
X	X	X	X	0	XX	Disabled
0	0	0	0	1	XX	Disabled
0	0	0	1	1	1F0-1F7	Primary HDD
0	0	1	1	1	1F0-1F7, 3F6, 3F7	Primary HDD
0	1	0	0	1	170-177	Secondary HDD
1	1	0	0	1	170- 177, 376, 377	Two drive system on local
1	1	1	1		170- 177, 376, 377, 1F0-1F7 3F6, 3F7	AT bus side

Table 22. Reset Conditions

Register 4 Bit 5 EN_DIS_RST	PC_HRESET	Register 7 Bit 0 ATA_MODE	ATA_HRESET	Notes:
1	X	X	1	PCMCIA Mode, Reset Disabled
0	0	0	1	PCMCIA Mode, No Reset
0	1	0	0	PCMCIA Mode, Asserted Reset
0	1	1	1	ATA Mode, No Reset.
0	0	1	0	ATA Mode, Asserted Reset.

EEPROM Register

Address: SELECT 05h
Name: BCMCIA CCR Base Address Register
Type: Read/Write

Table 23. PCMCIA CCR Base Address Register: Address 05h

Bit Placement	Bit Name	Description
Bit 0	EN_CRR_A4	Enables address bit 4 to be compared as High on PCMCIA when the PCMCIA Con•guration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 1	EN_CRR_A5	Enables address bit 5 to be compared as High on PCMCIA when the PCMCIA Con•guration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 2	EN_CRR_A6	Enables address bit 6 to be compared as High on PCMCIA when the PCMCIA Con•guration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 3	EN_CRR_A7	Enables address bit 7 to be compared as High on PCMCIA when the PCMCIA Con•guration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 4	EN_CRR_A8	Enables address bit 8 to be compared as High on PCMCIA when the PCMCIA Con•guration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 5	EN_CRR_A9	Enables address bit 9 to be compared as High on PCMCIA when the PCMCIA Con•guration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 6	EN_CRR_A10	Enables address bit 10 to be compared as High on PCMCIA when the PCMCIA Con•guration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 7	DIS_CRR_MODE	Disables PCMCIA host and allows access to the PCMCIA Con•guration Register's base address. This bit is active when set to 1. On Power-On Reset, this bit is set to 0.

Table 24. CCR Location Examples, Register 5

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CCR Base
EN	A10	A9	A8	A7	A6	A5	A4	Address
1	X	X	X	X	X	X	X	None
0	0	0	0	0	0	0	0	0000hx
0	0	0	0	0	0	0	1	0010hx
0	0	1	0	0	0	0	0	0200hx
0	1	0	0	0	0	0	0	0400hx

EEPROM Register

Address: SELECT 06h
Name: PCMCIA Interrupt Status Register
Type: Read

Table 25. PCMCIA Interrupt Status Register: Address 06h

Bit Placement	Bit Name	Description
Bit 0	PC_INT0	PCMCIA host write to CCR0, the Configuration Option Register has occurred. This bit is active when set to 1. Also see Register 01h (Table 13).
Bit 1	PC_INT1	PCMCIA host write to CCR1, the Card Configuration and Status Register has occurred. This bit is active when set to 1. Also see Register 01h (Table 13).
Bit 2	PC_INT2	PCMCIA host write to CCR2, the Pin Replacement Register has occurred. This bit is active when set to 1. Also see Register 01h (Table 13).
Bit 3	PC_INT3	PCMCIA host write to CCR3, the Socket and Copy Register has occurred. This bit is active when set to 1. Also see Register 01h (Table 13).
Bit 4	PC_INT4	External ATA_IREQ interrupt has occurred. This bit is active when set to 1. Also see Register 01h (Table 13).
Bit 5	PC_INT5	PCMCIA host write to CCR4, an I/O Event Indication Register has occurred. This bit is active when set to 1.
Bit 6	REV_BA	Set this bit to 1 after writing the revision number (see device top mark) to the revision control Register.
Bit 7	Reserved	

EEPROM Register

Address: SELECT 07h
Name: PCMCIA Exception Status Register
Type: Read

Table 26. PCMCIA Exception Status Register: Address 07h

Bit Placement	Bit Name	Description
Bit 0	ATA/IDE_MODE	When bit 7 of this register is set to 1, ATA mode has been selected by sampling the /PC_ATA//HOE signal on Power-On-Reset, or the override bits in Register 0 have set the ZX6017 to run in ATA/IDE mode. When set to 0, this bit indicates that the ZX6017 operates in PCMCIA mode (Table 27).
Bit 1	PCRST	PCMCIA reset status. Active when set to 1.
Bit 2	Reserved	
Bit 3	Reserved	
Bit 4	Reserved	
Bit 5	PDIAG	PDIAG is present. This bit is active when set to 1.
Bit 6	DASP	DASP is present. Drive Active/Slave Present. This bit is active when set
Bit 7	ATA_SAMPLED	When set to 1, this bit indicates that bit 0 of this register is valid to read.

Table 27. ATA Sample Mode Bit

Register 7 Bit 7 ATA_SAMPLED	Register 7 Bit 0 ATA_MODE	Comments
0	X	Not ready
1	0	PCMCIA Addressing Mode
1	1	ATA/IDE Addressing Mode

EEPROM Register

Address: SELECT 08h
Name: Attribute Memory Address Register
Type: Write

Table 28. Attribute Memory Address Register: Address 08h

Bit Placement	Bit Name	Description
Bits 7-0	Attribute Memory Address	After each access to the attribute RAM data register, the address is automatically incremented. Also see Register 03h.

EEPROM Register
Address: SELECT 09h
Name: Attribute Memory Data Register
Type: Write/Read

Table 29. Attribute Memory Data Register: Address 09h

Bit Placement	Bit Name	Description
Bits 7-0	Attribute Memory Data	The data read and written from this register is associated with the attribute memory location pointed to by the attribute RAM data address register. After each data write or read into this location, the address is automatically incremented by one. Also see Register 03h (Table 19).

EEPROM Register

Address: SELECT 10h
Name: Window 1 Control Register
Type: Write/Read

Table 30. Window 1 Control Register: Address 10h

Bit Placement	Bit Name	Description
Bit 0	DIS_PAC1	When this bit is set to 1, the Port 1 Address Control and decoder are disabled.
Bit 1	EN_PAC1_MEM	When this bit is set to 1, Memory Mode decoder is enabled. When cleared, I/O mode is enabled.
Bit 2	EN_PAC1_16	When this bit is set, data swapping is provided internal to the chip during data reads from the low byte of the ATA bus to the PCMCIA bus high byte, and from the high byte of the PCMCIA bus to the low byte of the ATA bus during data writes. When cleared, it is high byte to high byte and low byte to low byte.
Bit 3	READ_PROTECT	Allows two cards at the same address to be read. When this bit is set, it prevents the PCMCIA bus from going active.
Bit 4	EN_PAC1_ADDR_COMP	When this bit is set, use address compare logic; when it is cleared, acknowledge all PCMCIA chip selects.
Bit 5	EN_PAC1_HCS	When this bit is set, HCS1 is used as an external chip select. When this bit is cleared, HCS0 is used as an external chip select. Also see Registers 02h and 03h (Table 14 and Table 19).
Bits 7-6		Number of wait states (in Master Clock periods) inserted on the PCMCIA bus. 00 = 0xTpmclkin (no wait states) 01 = 3x Tpmclkin 10 = 5x Tpmclkin 11 = 7x Tpmclkin

EEPROM Register
Address: SELECT 11h
Name: Window 1 Start Address LSB
Type: Write/Read

Table 31. Window 1 Start Address LSB: Address 11h

Bit Placement	Bit Name	Description
Bits 7-0		LSB starting address for Port 1.

EEPROM Register
Address: SELECT 12h
Name: Window 1 Start/Range Address MSB
Type: Write/Read

Table 32. Window 1 Start/Range Address MSB: Address 12h

Bit Placement	Bit Name	Description
Bits 2-0		Bits 8, 9, and 10 of the starting address range of Port 1.
Bit 3	EN_WRITE_PROTECT	When this bit is set, the RWPROT bit in the pin replacement register is used to inhibit writing to the external peripherals. When these bits are cleared, PROT is ignored.
Bits 6-4		Bits 8, 9, and 10 of the starting address range of Port 1.
Bit 7	EN_DMA_ACK	When this bit is set, ATA_DMA_ACKNOWLEDGE is set when the address space is accessed, and Speaker Out on the PCMCIA interface is used as DREQ.

EEPROM Register
Address: SELECT 13h
Name: Window 1 Range Address LSB
Type: Write/Read

Table 33. Window 1 Range Address LSB: Address 13h

Bit Placement	Bit Name	Description
Bits 7-0		LSB range Address for Port 1

EEPROM Register
Address: SELECT 14h
Name: Window 2 Control Register
Type: Write/Read

Table 34. Window 2 Control Register: Address 14h

Bit Placement	Bit Name	Description
Bit 0	DIS_PAC2	When this bit is set to 1, it disables Port 2 address control and decoder.
Bit 1	EN_PAC2_MEM	When this bit is set to 1, Memory Mode decoder is enabled. When it is cleared, the I/O Mode decoder is enabled.
Bit 2	EN_PAC2_16	When this bit is set, data swapping is provided internal to the chip during data reads from the low byte of the ATA bus to the PCMCIA bus high byte, and from the high byte of the PCMCIA bus to the low byte of the ATA bus during data writes. When this bit is cleared, it is high byte to high byte and low byte to low byte.
Bit 3	READ_PROTECT	Allows two cards at the same address to be read from. When this bit is set, it prevents the PCMCIA bus from becoming active.

Table 34. Window 2 Control Register: Address 14h (Continued)

Bit Placement	Bit Name	Description
Bit 4	EN_PAC2_ADDR_COMP	When this bit is set, use address compare logic, when it is cleared, acknowledge all PCMCIA chip selects.
Bit 5	EN_PAC2_HCS	When this bit is set, HCS1 is used as an external chip select; when it is cleared, HCS0 is used as an external chip select. Also see Registers 02h and 03h.
Bits 7-6		Number of wait states (in Master Clock period) inserted on the

EEPROM Register

Address: SELECT 15h
Name: Window 2 Start Address LSB
Type: Write/Read

Table 35. Window 2 Start Address LSB: Address 15h

Bit Placement	Bit Name	Description
Bits 7-0		LSB starting address for Port 2.

EEPROM Register
Address: SELECT 16h
Name: Window 2 Start/Range Address MSB
Type: Write/Read

Table 36. Window 2 Start/Range Address MSB: Address 16h

Bit Placement	Bit Name	Description
Bits 2-0		Bits 8, 9, and 10 of the starting address range of Port 2.
Bit 3	EN_WRITE_PROTECT	When this bit is set, the RWPROT bit in the pin replacement register is used to inhibit writing to the external peripherals. When it is cleared, PROT is ignored. Bits 8, 9, and 10 of the starting address range of Port 2.
Bits 6-4		
Bit 7	EN_DMA_ACK	When this bit is set, ATA_DMA_ACKNOWLEDGE is set when the address space is accessed, and Speaker Out on the PCMCIA interface is used as DREQ.

EEPROM Register
Address: SELECT 17h
Name: Window 2 Range Address LSB
Type: Write/Read

Table 37. Window 2 Range Address LSB: Address 17h

Bit Placement	Bit Name	Description
Bits 7-0		LSB range address for Port 2.

EEPROM Register

Address: SELECT 18h
Name: Window 3 Control Register
Type: Write/Read

Table 38. Window 3 Control Register: Address 18h

Bit Placement	Bit Name	Description
Bit 0	DIS_PAC3	When set to 1, this bit disables Port 3 address control and decoder.
Bit 1	EN_PAC3_MEM	When this bit is set to 1, Memory mode decoder is enabled. When it is cleared, I/O mode decoder is enabled.
Bit 2	EN_PAC3_16+	When this bit is set, data swapping is provided internal to the chip during data reads from the low byte of the ATA bus to the PCMCIA bus high byte, and from the high byte of the PCMCIA bus to the low byte of the ATA bus during data writes. When this bit is cleared, it is high byte to high byte and low byte to low byte.
Bit 3	READ_PROTECT	This bit allows two cards to be read from the same address. When this bit is set, it prevents the PCMCIA bus from becoming active.
Bit 4	EN_PAC3_ADDR_COMP	When this bit is set, use address compare logic; when it is cleared, acknowledge all PCMCIA chip selects.
Bit 5	EN_PAC3_HCS	When this bit is set, HCS1 is used as an external chip select; when it is cleared, HCS0 is used as an external chip select.
Bits 7-6		Number of wait states (in Master Clock periods) inserted on the PCMCIA bus.

EEPROM Register
Address: SELECT 19h
Name: Window 3 Start Address LSB
Type: Write/Read

Table 39. Window 3 Start Address LSB: Address 19h

Bit Placement	Bit Name	Description
Bits 7-0		LSB starting Address for Port 3.

EEPROM Register
Address: SELECT 1Ah
Name: Window 3 Start/Range Address MSB
Type: Write/Read

Table 40. Window 3 Start/Range Address MSB: Address 1Ah

Bit Placement	Bit Name	Description
Bits 2-0		Bits 8, 9, and 10 of the starting address range of Port 3.
Bit 3	EN_WRITE_PROTECT	When this bit is set, the RWPROT bit in the pin replacement register is used to inhibit writing to the external peripherals. When this bit is cleared, PROT is ignored.
Bits 6-4		Bits 8, 9, and 10 of the starting address range of Port 3.
Bit 7	EN_DMA_ACK	When this bit is set, ATA_DMA_Acknowledge is set when the address space is accessed, and Speaker Out on the PCMCIA interface is used as DREQ.

EEPROM Register
Address: SELECT 1Bh
Name: Window 3 Range Address LSB
Type: Write/Read

Table 41. Window 3 Range Address LSB: Address 1Bh

Bit Placement	Bit Name	Description
Bits 7-0		LSB range address for Port 3.

EEPROM Register
Address: SELECT 1Eh
Name: EEPROM Valid Flag Byte Register
Type: Read

Table 42. EEPROM Valid flag Byte Register: Address 1Eh

Bit Placement	Bit Name	Description
Bits 7-0	Flag Byte	Read-Only Register used by the internal EEPROM Sequencer to determine if the contents of the EEPROM are valid. The valid Flag value is 1Ch.

EEPROM Register
Address: SELECT 20h
Name: EEPROM Address/Status CCR5 Back Door
Type: Write/Read

Table 43. EEPROM Address/Status CCR5 Back Door: Address 20h

Bit Placement	Bit Name	Description
Bits 7-0	Address/Status Bits	EEPROM address/status data.

EEPROM Register
Address: SELECT 21h
Name: EEPROM Data CCR6 Back Door
Type: Write/Read

Table 44. EEPROM Data CCR6 Back Door: Address 21h

Bit Placement	Bit Name	Description
Bits 7-0	Data Bits	EEPROM data.

EEPROM Register
Address: SELECT 22h
Name: EEPROM Command CCR7 Back Door
Type: Write/Read

Table 45. EEPROM Command CCR7 Back Door: Address 22h

Bit Placement	Bit Name	Description
Bits 7-0	Command Bits	Command value.

EEPROM Register
Address: SELECT 23h
Name: Revision Control Register
Type: Read/Write

Table 46. Revision Control Register: Address 23h

Bit Placement	Bit Name	Description
Bit 3-0	REV_MINOR	The lower four bits determine the minor revision number. This nibble must be written with the value read back from the lower nibble in Read-Only Register 24h to enable the minor revision functions.
Bit 7-4	REV_MAJOR	The upper four bits determine the major revision number. This nibble must be written with the value read back from the upper nibble in Read-Only Register 24h to enable the major revision functions.

EEPROM Register
Address: SELECT 24h
Name: Revision Number Register
Type: Read

Table 47. Revision Number Register: Address 24h

Bit Placement	Bit Name	Description
Bit 3-0	REV_NUM_MINOR	This is the Read-Only minor revision number of the chip.
Bit 7-4	REV_NUM_MAJOR	This is the Read-Only major revision number of the chip.

EEPROM Register

Address: SELECT 26h
Name: Bus Control 1 Register
Type: Read/Write
Reset: 00h

Table 48. Bus Control 1 Register: Address 26h

Bit Placement	Bit Name	Description
Bit 0	DISABLE_CLK	When this bit is set to 1, it turns off the PC_MCLK_IN pad. When it is cleared, it enables the PC_MCLK_IN pad. This bit is automatically cleared when in MASTER mode and at any access to the EEPROM command Register 7F4h as seen through the PCMCIA interface.
Bit 1	EN_IOIS_IN	When this bit is set to 1, it enables the IOIS16 signal to be generated internally (see Register 27, IOIS16 Address Control Register, Table 49). When it is cleared, the source for IOIS16 will be the ATA_IOIS16 input.
Bit 3-2	8-Bit_CNTRL	PCMCIA 8- to 16-bit control enable (see Table 51).

Table 48. Bus Control 1 Register: Address 26h (Continued)

Bit Placement	Bit Name	Description
Bit 4	EN_RW_LONG	Set this bit to 1 to enable the read/write long function when using the 8-bit to 16-bit mode or internal IOCS16 generation in ATA/IDE pass-through mode. PCMICA 8-Bit to 16-Bit Access After 512 bytes are transferred, each PC_IOR/IOW strobe to the data register will generate a ATA_IOR/IOW strobe on the ATA/IDE bus. 8-bit to 16-bit accesses of the data register will be continued after any write access to a task file register other than the data register. ATA/IDE PASSTHROUGH mode. When set in ATA/IDE PASSTHROUGH mode after 256 word accesses of the data register, the //IOCS16 signal on the host interface de-asserts until the next data transfer phase. The internal IOCS16 function must also be enabled. (EN_IOIS_IN=1) and the IOIS16 ADDR register set to 01 pointing to the ATA/IDE task file data Register 1F0, 170. Clearing this bit disables the read/write long function.
Bit 6-5	IOIS16_CTRL	IOIS16 source select (see Table 49)
Bit 7	BVD_CTRL	When set to 1, this bit enables the PC_BVD1/$\overline{\text{STSCHG}}$/$\overline{\text{PDIAG}}$ and PC_BVD2/$\overline{\text{SPKR}}$/$\overline{\text{DASP}}$/$\overline{\text{DREQ}}$ functions. When cleared, it sets both PC_BVD1/$\overline{\text{STSCHG}}$/$\overline{\text{PDIAG}}$ and PC_BVD2/$\overline{\text{SPKR}}$/$\overline{\text{DASP}}$ /DREQ pins High when in PCMCIA ATA/IDE memory mode. At Power-On Reset, set to 0.

Note: Registers 26h and 27h are only available on the Z16017 device.

EEPROM Register

Address: SELECT 27h
Name: IOIS16 Address Control Register
Type: Read/Write
Reset: 00h

The contents of this register determine which on-Host address IOIS16 is generated, but only when bit 1 of Register 26h is set to 1.

Table 49. IOIS16 Address Control Register: Address 27h

Register Content Bit <7-0>	Host Address PC_HA <3-0>	PC_WP/$\overline{\text{IOIS16}}$/$\overline{\text{IOIS16}}$	Comments
10000000 (80h)	1110 (Eh)	0	Must use this address to generate IOIS16.[1]
01000000 (40h)	1100 (Ch)	0	
00100000 (20h)	1010 (Ah)	0	
00010000 (10h)	1000 (8h)	0	
00001000 (08h)	0110 (6h)	0	
00000100 (04h)	0100 (4h)	0	
00000010 (02h)	0010 (2h)	0	
00000001 (01h)	0000 (0h)	0	

NOTES:
1. For IOIS16 to be generated on any even address, the register must contain 1 in all positions.

Table 50. 16-Bit_Control

Bit 6	Bit 5	Description
0	0	IOIS16 is being generated internally.
1	0	IOIS8 is the source for the IOIS16 in PCMCIA I/O Mode.[1]
1	1	IOIS16 is always High in PCMCIA I/O Mode

Note:
IOIS8 is bit 5 in CCR1 Card Configuration and Status Register.

NOTES:
1.

Table 51. 8-Bit _CTRL

Bit 3	Bit 2	Description
0	0	PCMCIA_8 to ATA_16 Mode is disabled.
0	1	
1	0	IOIS8 controls PCMCIA_8 to ATA_16 Mode.[1]
1	1	Forces the ZX6017 into PCMCIA_8 to ATA_16 Mode.

NOTES:
1. IOIS8 is bit 5 in CCR1 Card Configuration and Status Register.

EEPROM Register

Address: SELECT 28h
Name: ATA/IDE Dual Drive Control
Type: Read/Write

Bit Placement	Bit Name	Description
Bit 0	M_S_enable	This bit enables the Master/Slave mode control. When this bit is set to 1, the Master/Slave function is enabled. When it is set to 0, this function is disabled.
Bit 1	_select	When programmed, this bit determines when to drive the ATA/IDE bus. When set to 1, the ZX6017 drives the ATA bus when the host writes a 1 into Bit 4 of the "Drive/Head" task file register. Both primary and secondary addresses are compared. If this bit is set to 0, then the ZX6017 drives the bus if the host writes a 0 into Bit 4 of the "Drive/Head" task fie register.[1]
Bit 7-2	Reserved	Unused

NOTES:
1. Read Back Values: Z86017 00010000b = 10h
   Z16017 00100000b = 20h

EEPROM Register

Address: SELECT 2Ah
Name: Power Management Timer Count Value
Type: Read/Write

Table 52. Power Management Timer Count Value: Address 2Ah

Bit Placement	Bit Name	Description
Bit 7-0	TIMER_VAL	Power management timer count value. The timer reset during all PCMCIA activity. When the timer expires, it powers down all noncritical signals. TIMER intervals (sec.) = PC_MCLK (sec.) * 2(27) * timer_val. For example: PC_MCLK (20 MHz, 50 ns) * 2(27) * 1 = 6.67 sec. Also see Register 2Ch (Table 56).

EEPROM Register

Address: SELECT 2Bh
Name: Power Management Control Register
Type: Read/Write

Table 53. Power Management control Register: Address 2Bh

Bit Placement	Bit Name	Description
Bit 0	EN_8BIT_MODE	When set to 1, this bit enables the 8-bit mode on the local interface. When cleared, it enables the 16-bit interface.
Bit 1	EN_MODEM_ALT	When set to 1, this bit enables the alternate modem functions/pins. When cleared, it disables modem functions.
Bit 2	EN_CLK	When this bit is set to 1, all internal clocks are disabled after loading from the serial EEPROM. When this bit is cleared, all clocks are enabled.
Bit 3	EN_PADS[1]	When this bit is set to 1, the PCMCIA external pads are powered-down, unless PCMCIA(*) PC_HCE1 and PC_HCE2 are active. When this bit is cleared, all external pads are enabled.
Bit 4	EN_TIMER	When this bit is set to 1, the power management timer is enabled. The timer value is contained in Register 2A. When this bit is cleared, the power management timer is held reset and disabled.
Bit 5	EN_PM_RDY	When this bit is set to 1, the ZX6017 sets BUSY on the PCMCIA interface when the host sets the power down bit in CCR1.
Bit 6	EN_EXT_PD	When this bit is set to 1, the power management timer activates the external power down signal EXTP_PWND. When this bit is cleared, the external signal is not be activated. See also Register 0Bh (Table 67).
Bit 7	EN_EXPD_POL	When this bit is set to 1, the external power down signal EXTP_PWND is active Low. When this bit is cleared, EXTP_PWND is active High.

NOTES:
1. When the En_Pads bit is set, access to the CCR Registers is disabled.

EEPROM Register

Address: SELECT 2Ch
Name: Interface Configuration Register 4
Type: Read/Write

Table 54. Interface Configuration Register 4: Address 2Ch

Bit Placement	Bit Name	Description
Bit 2-0	TSTCLK	These power management clock select bits can be used to provide delay times in a number of different scales. Table 55 describes the different delay scale settings. Also see Register 2Ah (Table 53).
Bit 3	EN_POLL_BSY	This bit allows the ZX6017 to poll the Busy status bit in the local controller task file. When enabled in PCMCIA ATA I/O mode, the Busy status bit in the local controllers task file latches into the pin replacement register. In PCMCIA ATA Memory mode, the Busy status bit is placed on the Ready/Busy signal. Set this bit to 1 to enable auto polling. When this bit is cleared, auto polling is disabled. On Power-On Reset, it is set to 0.
Bit 4	EN_GLOB_INT	This is a Global Interrupt Enable for the M-PINT pin. When set to 1, this bit enables the local µP interrupts. When cleared, it disables the local µP interrupt. On Power-On Reset, it is set to 0.
Bit 5	EN_PC_INT5	This bit enables the local Processor interrupt when the PCMCIA host has written the I/O event indication Register CCR4. This interrupt source stays present until this bit is set to 0. When set to 1, this bit is active. On Power-On Reset, it is set to 0.
Bit 6	EN_BVD_INPUTS	When set to 1, this bit enables the two BVD inputs to be reflected either in Pin Replacement Register or on the corresponding pins of the ZX6017. On Power-On Reset, it is set to 0. See also Register 0Ch (Table 66).

Table 54. Interface Configuration Register 4: Address 2Ch (Continued)

Bit Placement	Bit Name	Description
Bit 7	EN_PULSE	When set, this bit enables auto busy status when the host sets reset. The busy status remains present until the internal time-out or when using a µP and the µP clears the busy status. When cleared, this bit disables auto busy on host resets. The pulse time for busy is 2(15)/PC_MCLK (MHz) = SEL.

Table 55. Power Management Clock Select

Bit 2	Bit 1	Bit 0	Timer/Count 6.7 sec./count	Input Clock PC_MCLK @ 20 MHz
0	0	1	6.4 µsec./count	@ 20 MHz
0	1	0	Disable counter	
0	1	1	12.8 µsec./count	@ 20 MHz
1	0	0	100 nsec./count	@ 20 MHz
1	0	1	6.4 µsec./count	@ 20 MHz
1	1	0	6.4 µsec./count	@ 20 MHz

EEPROM Register
Address: SELECT 2Dh
Name: Configuration Index Compare Register 1
Type: Read/Write

Table 56. Configuration Index Compare Register 1: Address 2Dh

Bit Placement	Bit Name	Description
Bit 2-0	IO_SEL_SEC	These bits are the configuration index for I/O secondary select.
Bit 3	EN_ IO_SEL_SEC	When set to 1, this bit enables the configuration index I/O secondary select; when cleared, it is disabled.
Bit 6-4	IO_SEL_PRI	These bits are the configuration index for I/O primary select.
Bit 7	EN_IO_SEL_PRI	When set to 1, this bit enables the configuration index I/O primary select; when cleared, it is disabled.

EEPROM Register
Address: :SELECT 2Eh
Name: Configuration Index Compare Register 2
Type: Read/Write

Table 57. Configuration Index Compare Register 2: Address 2Eh

Bit Placement	Bit Name	Description
Bit 2-0	MEM_INDX	These bits are the configuration index for memory select.
Bit 3	EN_MEM_INDX	When set to 1, this bit enables configuration index memory select; when cleared, it is disabled.
Bit 6-4	IO_INDP_INDX	These bits are the configuration index for I/O independent select.
Bit 7	EN_IO_INDP_INDX	When set to 1, this bit enables configuration index independent select; when cleared, it is disabled.

EN_IO_MODE bit 6 in Register 03h and Primary/Secondary enables in Register 04h bits 3, 2, 1, and 0 are globally enabled based on the values written into Register 2D and the Host writing into the configuration index bits in CCR0.

EN_MEM_MODE bit 0 and the EN_INDP_MODE bit 1 in Register 03h are globally enabled based on the values written into Register 2Eh and the Host writing into the configuration index bits in CCR0.

EEPROM Register

Address: SELECT 2Fh
Name: Bus Control
Type: Read/Write

Table 58. Bus Control Register: Address 2Fh

Bit Placement	Bit Name	Description
Bit 0	EN_BHE_POL	When this bit is cleared, it enables the polarity of the ATA_BHE output to be active High. When it is set, it enables the polarity to be active Low. At Power-On Reset, this bit defaults to clear. Also see Register 00h (Table 11).
Bit 1	EN_16_DUECE	When this bit is set, it enables word-to-byte access when in memory mode. This mode allows a 16-bit host to access 8-bit peripherals. When cleared, this bit disables word-to-byte access mode. When set, this bit enables the ZX6017 to generate two peripheral write or read strobes on the local peripheral side when the host writes or reads 16 bits of data. This mode allows a 16-bit host to read/write to 8-bit peripheral device registers with one 16-bit access. When this mode is enabled, and the ZX6017 is in memory mode, the host gains access to the peripheral's 8-bit registers by selecting an even address usingPC_HCE1. The ZX6017 asserts the $\overline{\text{PC\_WAIT}}$ pin, which allows the write or read strobe to the peripheral device to be controlled through the "DUECE_WIDTH" and "DUECE_ACCESS_DLY" bits in the Bus control Register 2Fh and the externals peripherals IOCHRDY signal if present (Figure 10). Figure 11 depicts the PCMCIA to local peripheral data path information.
Bit 2	EN_DIV_ADDR	When set, this bit indicates that PCMCIA host address lines A3, A2 and A1 are mapped to the local interface address lines A2, A1 and A0. When cleared, PCMCIA address lines A2, A1 and A0 are mapped to local interface A2, A1 and A0.

Table 58. Bus Control Register: Address 2Fh (Continued)

Bit Placement	Bit Name	Description
Bit 3	EN_MAP_IO_MEM	When this bit is set, all memory accesses are mapped to ATA_HIOR and ATA_HIOW. When it is cleared, all memory accesses are mapped to ATA_MRD and ATA_MWR.
Bit 5-4	DUECE_WIDTH	These bits set the $\overline{\text{ATA}}$_HIOR/HIOW strobe width and are clocked by PC_MCLK_IN /2. At Power-On Reset, they default to 00.
Bit 7-6	DUECE_ACCESS_DLY	These bits set the $\overline{\text{ATA}}$_HIOR/HIOW access delay and are clocked by PC_MCLK_IN /2. At Power-On Reset, they default to 00.

The $\overline{\text{ATA}}$_HIOR/HIOW strobe width is three cycles minimum (PC_MCLK_IN /2), plus IOCHRDY time (if any), plus width count programmed in bits 5, 4 (Table 59).

Table 59. Strobe Width and Access Delay[1]

Bits						Bits					
7	**6**	**5**	**4**	**Delay**	**Width**	**7**	**6**	**5**	**4**	**Delay**	**Width**
0	0	0	0	0	0	1	0	0	0	2	0
0	0	0	1	0	1	1	0	0	1	2	1
0	0	1	0	0	2	1	0	1	0	2	2
0	0	1	1	0	3	1	0	1	1	2	3
0	1	0	0	1	0	1	1	0	0	3	0
0	1	0	1	1	1	1	1	0	1	3	1
0	1	1	0	1	2	1	1	1	0	3	2
0	1	1	1	1	3	1	1	1	1	3	3

NOTES:
1. Each count equals PC_MCLK_IN /2.

WORD-TO-BYTE OPERATION

Figure 10 illustrates Word-to-Byte timing and Figure 11 depicts the Word-to-Byte Mode data path.

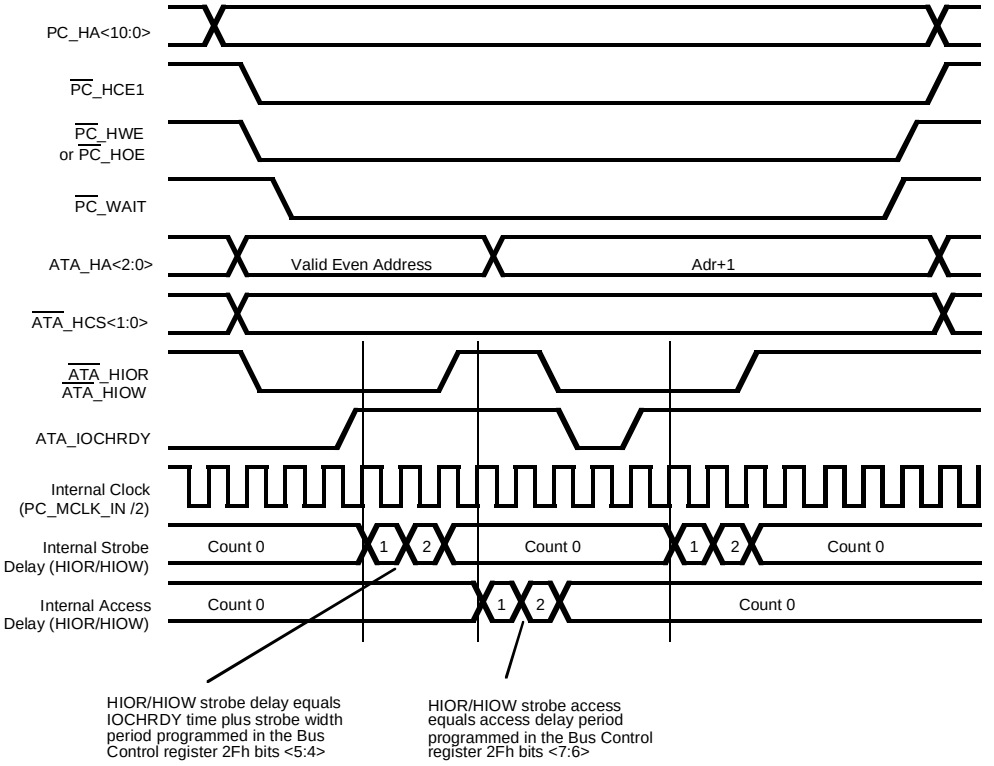


Figure 10. Word-to-Byte Timing

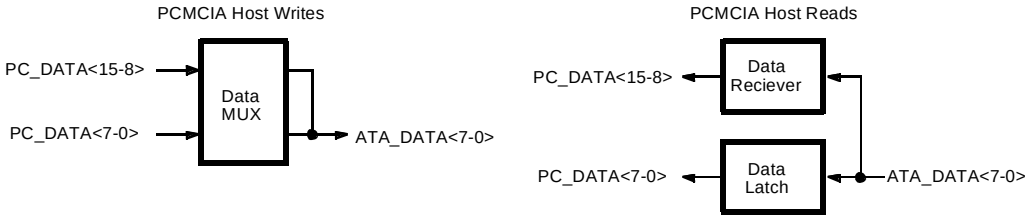


Figure 11. Word-to-Byte Mode Data Path

- PCMCIA Host Write
  PC_DATA<7–0> (Even Byte) written to ATA_DATA<7–0>
  PC_DATA<15–8> (Odd Byte) written to ATA_DATA<7–0>
- PCMCIA Host Read
  The PCMCIA selects an even address, then the ZX6017 pulls WAIT and reads the even register from the peripheral device, saves it in a latch, increments the local peripherals address bus, then reads the odd data byte and clears the PCMCIA WAIT pin.
  ATA_DATA<7–0> (Even Byte) put onto PC_DATA<7–0>
  ATA_DATA<7–0> (Odd Byte) put onto PC_DATA<15–8>

Table 60 describes the PCMCIA Host read and write address examples.

Table 60. PCMICA Host Read and Write Address Examples[1,2]

PCMCIA	ATA/IDE Memory Mode	General-Purpose	Maps
Host Address 0	Word Access Only	Host Address 0	Peripheral Address 0, then 1
Host Address 2	Peripheral Address 2, then 3	Host Address 2	Peripheral Address 2, then 3
Host Address 4	Peripheral Address 4, then 5	Host Address 4	Peripheral Address 4, then 5, and so on.

NOTES:
1. If the peripheral asserts the $\overline{\text{ATA}}$_IOCS16, then this feature is aborted.
2. The host accesses must be on even addresses.

Configuration Registers

INTRODUCTION

Support for the PCMCIA Configuration Registers is provided by the ZX6017. Table 62 lists register decodes.

Three additional registers have been added to the ZX6017 to provide an EEPROM link to support remote programming for attribute memory.

Table 62. PCMCIA Address xx0h to xx8h, Configuration Register Decode

$\overline{WE}$	$\overline{OE}$	$\overline{REG}$	$\overline{CE1}$	$\overline{CE2}$	Address	Action
1	0	0	0	1	xx0hx	Read Configuration Option Register
0	1	0	0	1	xx0hx	Write Configuration Option Register
1	0	0	0	1	xx2hx	Read Card Configuration and Status
0	1	0	0	1	xx2hx	Write Card Configuration and Status
1	0	0	0	1	xx4hx	Read Pin Replacement Register
0	1	0	0	1	xx4hx	Write Pin Replacement register
1	0	0	0	1	xx6hx	Read Socket and Copy Register
0	1	0	0	1	xx6hx	Write Socket and Copy Register
1	0	0	0	1	xx8hx	Read I/O Event Indication Status(*)
0	1	0	0	1	xx8hx	Write I/O Event Indication Status(*)

***** The I/O Event Indication Status Register is only available on BA revisions of the ZX6017. (See device top mark for revision level.)

Table 63. ZiLOG EEPROM Programming Extensions[1]

$\overline{WE}$	$\overline{OE}$	$\overline{REG}$	$\overline{CE1}$	$\overline{CE2}$	Address	Action
0	1	0	0	1	7F0h	Write EEPROM Address
1	0	0	0	1	7F0h	Read EEPROM Status
0	1	0	0	1	7F2h	Write EEPROM Data
1	0	0	0	1	7F2h	Read EEPROM Data
0	1	0	0	1	7F4h	EEPROM Command
1	0	0	0	1	7F6h	Revision Register

***** The I/O Event Indication Status Register is only available on BA revisions of the ZX6017. (See device top mark for revision level.)

CONFIGURATION REGISTERS

EEPROM Register

Address: SELECT 0Ah
Name: PCMCIA Configuration Option Register CCR0
Type: Write/Read

Table 64. PCMCIA Configuration Option Register CCR0: Address 0Ah

Bit Placement	Bit Name	Description
Bits 5–0	Configuration Index	Card configuration chosen by the system.
Bit 6	Level Request	Level mode interrupts are selected when this bit is set to 1. Pulse mode interrupts are selected when this bit is set to 0.
Bit 7	SRESET	Setting this bit to 1 places the card in the reset state.

EEPROM Register
Address: SELECT 0Bh
Name: PCMCIA Card Status Register CCR1
Type: Write/Read

Table 65. PCMCIA Card Status Register CCR1: Address 0Bh

Bit Placement	Bit Name	Description
Bit 0	Reserved	Must be 0.
Bit 1	Interrupt	This bit represents the state of the Interrupt request signal.
Bit 2	Power Down	The card enters the power down state when this bit is set to 1. Also see Register 2Bh (.
Bit 3	Audio	Set this bit to 1 for audio information.
Bit 4	Reserved	Must be 0.
Bit 5	IOIS8	System can only provide I/O cycles with an 8-bit D7-D0 data path.
Bit 6	SIGCHG	This bit is set and reset by the host to allow a state change from the status register. Also see Register 1Fh (Table 68).
Bit 7	Changed	

EEPROM Register

Address: SELECT 0Ch
Name: PCMCIA Pin Replacement Register CCR2
Type: Write/Read

Table 66. PCMCIA Pin Replacement Register CCR2: Address 0Ch

Bit Placement	Bit Name	Description
Bit 0	RWPROT	Write Protect switch.
Bit 1	RRDY//BSY	When read, this bit represents the internal state of the RRDY/$\overline{\text{BSY}}$ signal. When written, this bit acts as a mark for writing the corresponding bit CRDY/$\overline{\text{BSY}}$.
Bit 2	RBVD2	When read, this bit represents the internal state of the Battery Voltage detection circuits on cards which contain a battery. This signal represents the values on PCMCIA pin BVD2. Also see Register 2Ch (Table 54).
Bit 3	RBVD1	When read, this bit represents the internal state of the Battery Voltage detection circuits on cards which contain a battery. This signal represents the values on PCMCIA pin BVD1. Also see Register 2Ch (Table 54).
Bit 4[1]	CWPROT	This bit is set to 1 when RWPROT changes state.
Bit 5[1]	CRDY//BSY	This bit is set to 1 when the bit RRDY//BSY changes state.
Bit 6[1]	CBVD2	This bit is set to 1 when the corresponding bit RBVD2 changes state.
Bit 7[1]	CBVD1	This bit is set to 1 when the corresponding bit RBVD1 changes state.

NOTES:
1. When this register is read, these four bits are reset.

EEPROM Register
Address: SELECT 0Dh
Name: PCMCIA Socket and Copy Register CCR3
Type: Write/Read

Table 67. PCMCIA socket and Copy Register CCR3: Address 0Dh

Bit Placement	Bit Name	Description
Bits 3–0	Socket Number	This field indicates to the card that it is located in the nth socket. The first socket is numbered 0. This permits cards designed to share a common set of I/O ports to do so while remaining uniquely identifiable.
Bits 5–4	Copy Number	Cards which indicate in their CIS that they support more than one copy of identically configured cards, should have a copy number (0 to MAX twin cards, MAX = n – 1) written back to the socket and copy register.
Bit 7	Reserved	

EEPROM Register

Address: SELECT 1Fh
Name: PCMCIA I/O Event Indication CCR4
Type: Read/Write

Table 68. PCMCIA I/O Event Indication CCR4: Address 1Fh

Bit Placement	Bit Name	Description
Bit 7	RSVDEVT3	Input pin EXTP_STSCHG/RES2 sets this bit. When this bit is set and the PIEnab bit is set to 1, the changed bit in the Card configuration and status register is also set to 1.
Bit 6	RSVDEVT2	Input pin ATA_DATA8/RES1 sets this bit. When this bit is set and the PIEnab bit is set to 1, the changed bit in the Card configuration and status register is also set to 1.
Bit 5	PIEvt	The card latches this bit to a 1on receipt of a validated incoming packet over an RF channel. The source of this signal is ATA_DATA9/PACK_IN. When this bit is set to 1 and the PIEnab bit is set to 1, the changed bit in the Card configuration and status register is also set to 1. And, if the SIGCHG bit in the card configuration status register has also been set by the host, the STSCHG pin (pin 63) goes Low. The host writing a 1 to this bit clears it to 0. Writing a 0 to this bit has no effect.
Bit 4	RIEvt	This bit is latched to a 1 by the card after the receipt of a 1 on the $\overline{\text{ATA}}$/$\overline{\text{PDIAG}}$/ATA_BHE/RING-IN signal. When this bit is set to 1 and the RIEnab bit is set to 1, the changed bit in the Card configuration and status register is also set to 1. And, if the SIGCHG bit in the card configuration status register has also been set by the host, then the STSCHG pin (pin 63) goes Low. The host writing a 1 to this bit clears it to 0. Writing a 0 to this bit has no effect.

Table 68. PCMCIA I/O Event Indication CCR4: Address 1Fh (Continued)

Bit Placement	Bit Name	Description
Bit 3	RSVDENAB3	Setting this bit enables the Changed bit in the card configuration and status register to be set when the RSVDEVT3 bit is set. When this bit is cleared, this feature is disabled.
Bit 2	RSVDENAB2	Setting this bit enables the Changed bit in the card configuration and status register to be set when the RSVDEVT2 bit is set. When this bit is cleared, this feature is disabled.
Bit 1	PIENAB	Setting this bit enables the changed bit in the Card configuration and status register to be set when the PIEvt bit is set. When this bit is cleared, this feature is disabled.
Bit 0	RIENAB	Setting this bit enables the changed bit in the Card configuration and status register to be set when the RIEvt bit is set. When this bit is cleared, this feature is disabled.

Appendix A: Multifunction Pins

OVERVIEW OF MULTIFUNCTION PINS

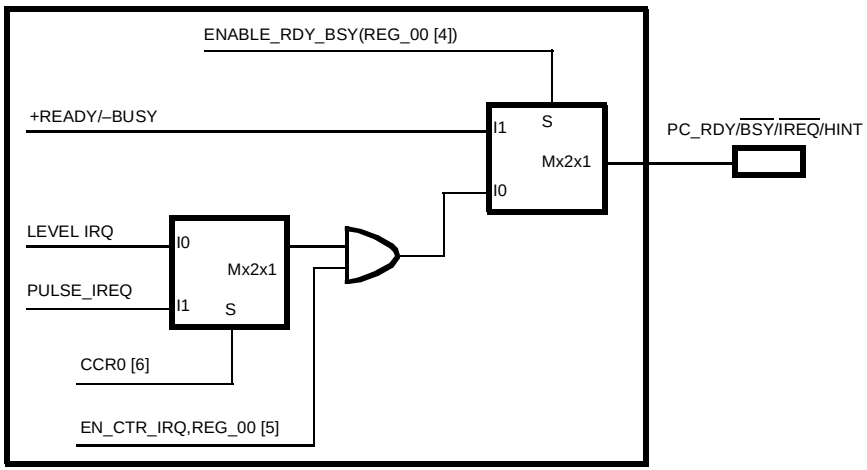


Figure 12. Z16017BA PC_RDY/$\overline{\text{BSY}}$/$\overline{\text{IREQ}}$/HINT Pin

Note: Width of the PULSE_IREQ is: T = 192 x Tpc_mclk_in

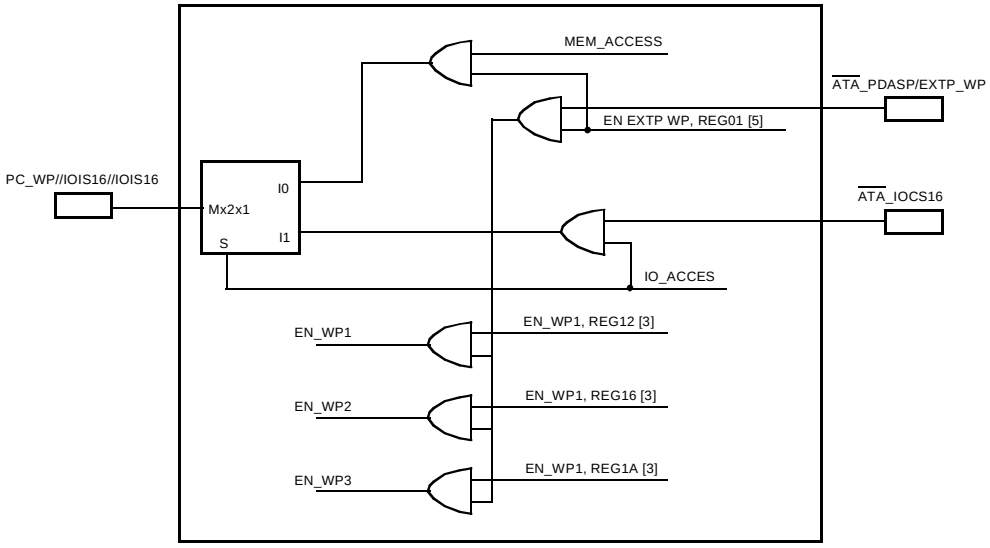


Figure 13. Z86017BA PC_WP//IOIS16//IOIS16 Pin

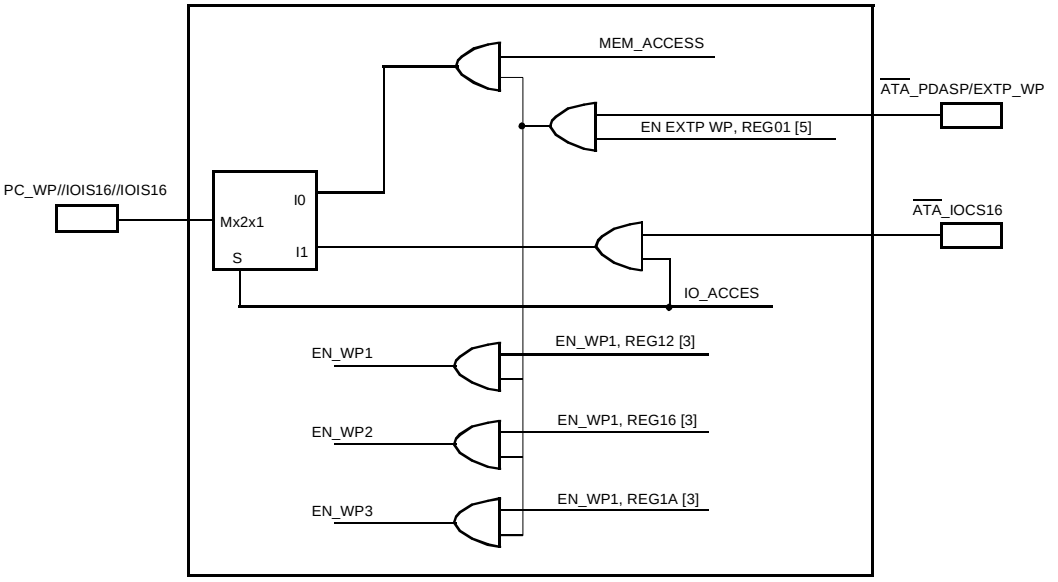


Figure 14. Z16017BA PC_WP//IOIS16//IOIS16 Pin

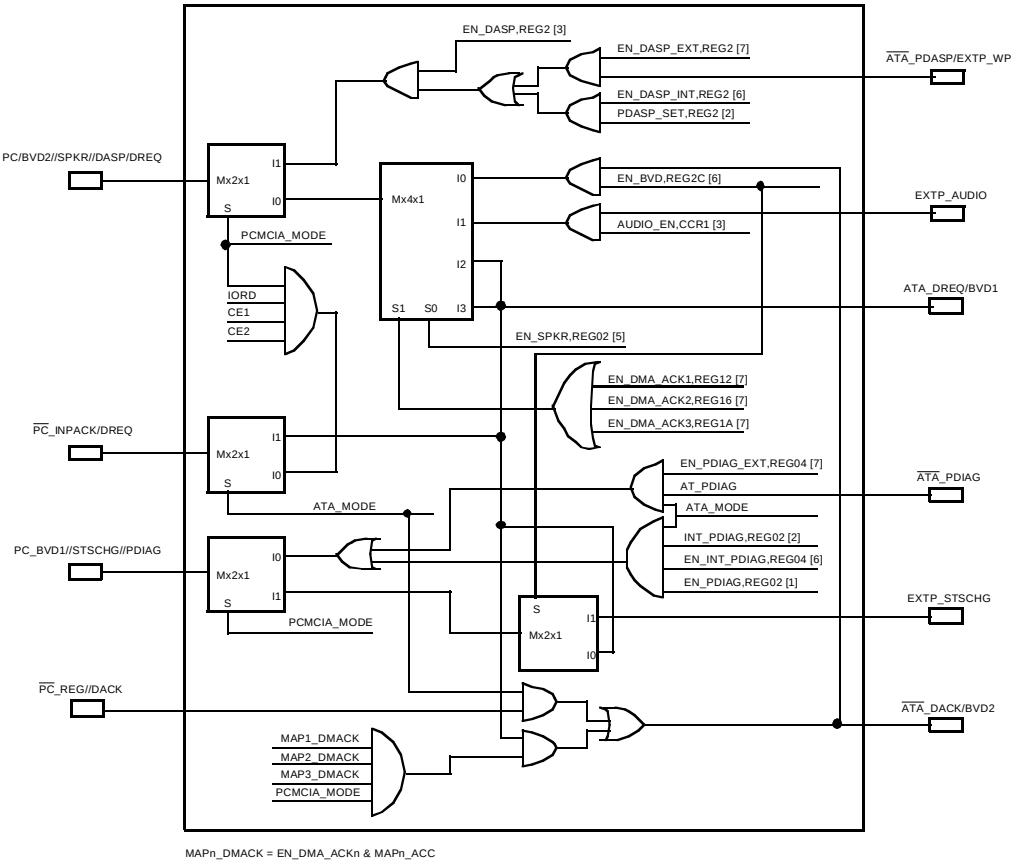


Figure 15. Z86017BA (Overview of Internal Structure)

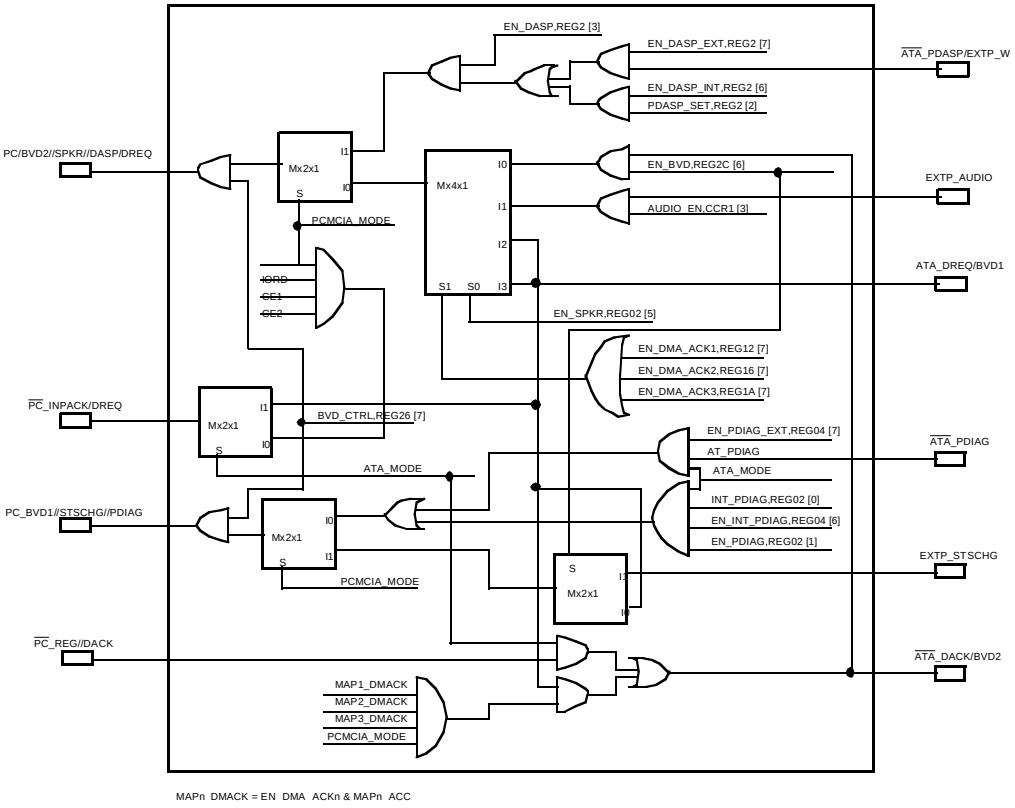


Figure 16. Z16017BA (Overview of Internal Structure)

Appendix B: Electrical Characteristics and Timing

Table 69. Absolute Maximum Ratings

Parameter	Symbol	Unit	Min. Value	Max. Value
Supply Voltage	V_{DD}	V	–0.5	7.0
Input Voltage	V_I	V	–0.5	V_{DD} + 0.5
Output Voltage	V_O	V	–0.5	+ 0.5 V_{DD}
Storage Temperature	T_{STG}	C	–40	+125
Temperature Under Bias	T_{BIAS}	C	–25	+85

Table 70. DC Electrical Characteristics

VCC = 3.3V ± 10%

		T_A = 0°C to +70°C				
Sym.	**Parameter**	**Minimum**	**Maximum**	**Typical at 25°C**	**Units**	**Conditions**
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC}		V	
V_{IL}	Input Low Voltage	–0.3	0.1 V_{CC}		V	
V_{OH}	Output High Voltage	1.8			V	I_{OH} = 4 mA
V_{OH}	Output High Voltage	V_{CC} – 100 mV			V	I_{OH} = 100 µA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = 4 mA
V_{RH}	Reset Input High Voltage	0.8 V_{CC}	V_{CC}		V	
V_{Rl}	Reset Input Low Voltage	–0.3	0.1 V_{CC}		V	
I_{IL}	Input Leakage	–2	2		µA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	–2	2		µA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		–80		µA	V_{RL} = 0V
I_{CC}	Supply Current[1]		4	3	mA	@ 20 MHz
I_{CC1}	Standby Current[2]		300	250	µA	
V_{IH}	Input High Voltage	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	–0.3	0.8		V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –6 mA
V_{OH}	Output High Voltage	V_{CC} –100 mV			V	I_{OH} = 100 µA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = 6 mA

Table 70. DC Electrical Characteristics (Continued)

VCC = 3.3V ± 10%

T_A = 0°C to +70°C						
Sym.	**Parameter**	**Minimum**	**Maximum**	**Typical at 25°C**	**Units**	**Conditions**
V_{RH}	Reset Input High Voltage	3.8	V_{CC}		V	
V_{Rl}	Reset Input Low Voltage	–0.3	0.8		V	
I_{IL}	Input Leakage	–2	2		µA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	–2	2		µA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		–80		µA	V_{RL} = 0V
I_{CC}	Supply Current[1]		5	4	mA	@ 20 MHz
I_{CC1}	Standby Current[2]		350	300	µA	

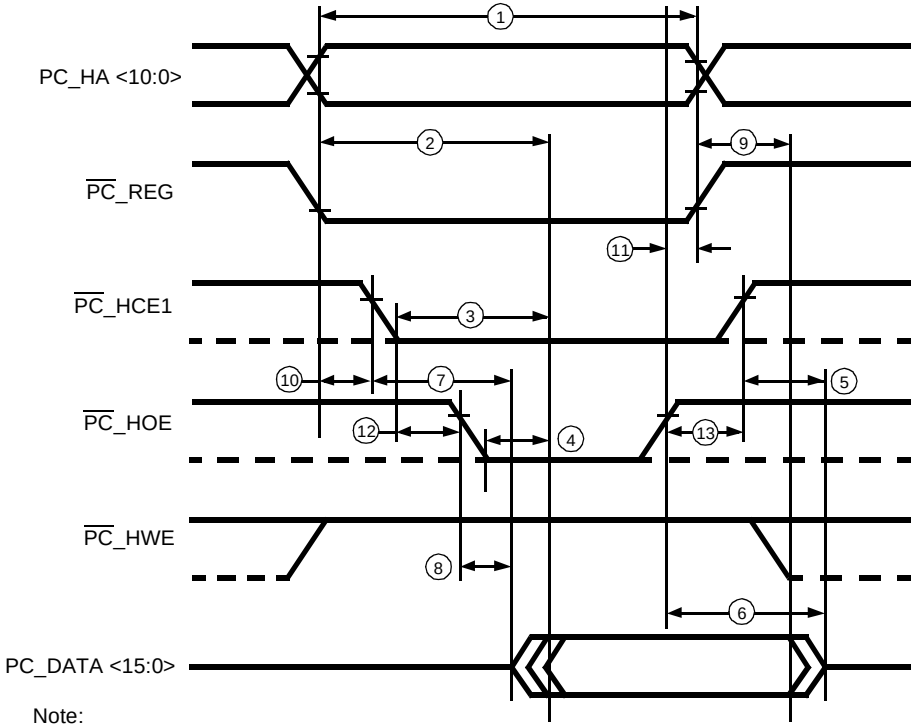
1. All inputs driven to 0V, VCC and outputs floating.
2. EN_Pads Bit Set, PC_MCLK=0, EE_SK=0

INTERNAL ATTRIBUTE MEMORY TIMING

Table 71. Internal Attribute Memory Timing

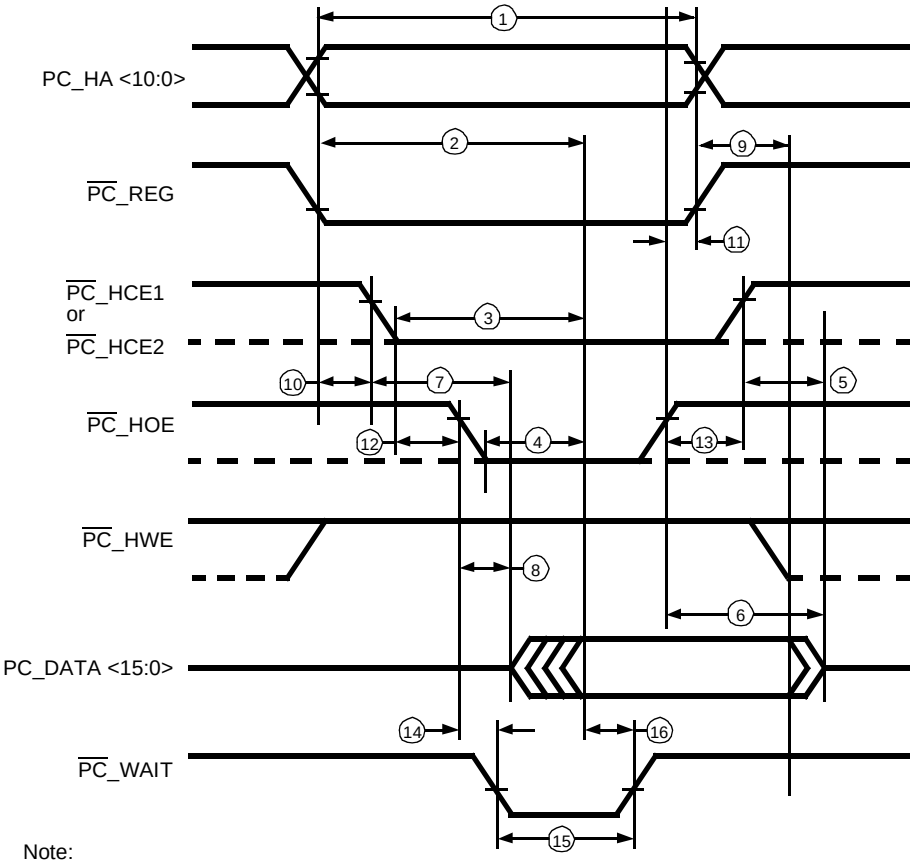
(Speed Version: 300 ns)

No.	Symbol	Parameter	Minimum	Maximum	Units
1	TcR	Read Cycle Time	300		ns
2	TaA	Address Access Time		300	ns
3	TaCE	Card Enable Time		300	ns
4	TaOE	Output Enable Access Time		150	ns
5	TdisCE	Output Disable Time from CE		100	ns
6	TdisOE	Output Disable Time from OE		100	ns
7	TenCE	Output Enable Time from CE	5		ns
8	TenOE	Output Enable Time from OE	5		ns
9	TvA	Data Valid from Address Change	0		ns
10	TsuA	Address Setup Time	30		ns
11	ThA	Address Hold Time	20		ns
12	TsuCE	Card Enable Setup Time	0		ns
13	ThCE	Card Enable Hold Time	20		ns
14	TvWToe	Wait Valid from OE		35	ns
15	TwWT	Wait Pulse Width		12	µs
16	TvWT	Data Setup for Wait Released	0		ns



Note:
PC_REG is active Low for Attribute Memory reads only.

Figure 17. PCMCIA Read Memory Timing, No Wait States



Note:
PC_REG is active Low for Attribute Memory reads only.

Figure 18. PCMCIA Read Memory Timing, Wait State Enabled

Table 72. PCMCIA Memory Write Timing

No.	Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
17	TcW	Write Cycle Time	200		150		100		ns
18	TwWE	Write Pulse Width	120		80		60		ns
19	TsuA	Address Setup Time	20		20		10		ns
20	TsuAwe	Address Setup Time for WE	140		100		70		ns
21	TsuCwe	Card Enable Setup Time for WE	140		100		70		ns
22	TsuDwe	Data Setup Time for WE	60		50		40		ns
23	ThD	Data Hold Time	30		20		15		ns
24	TrecWE	Write Recover Time	30		20		15		ns
25	TdisOwe	Output Disable Time from WE		90		75		50	ns
26	TdisOE	Output Disable Time from OE		90		75		50	ns
27	TenWE	Output Enable Time from WE	5		5		5		ns
28	TsuCwe	Output Enable Setup from WE	10		10		10		ns
29	ThCwe	Card Enable Hold from WE	10		10		10		ns
30	TsuCE	Card Enable Setup Time	0		0		0		ns
31	ThCE	Card Enable Hold Time	20		20		15		ns

Table 72. PCMCIA Memory Write Timing (Continued)

No.	Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
32	TvWTwe	Wait Valid from WE		35		35		35	ns
33	TwWT	Wait Pulse Width		12		12		12	µs
34	TvWT	WE High from Wait Released	0		0		0		ns

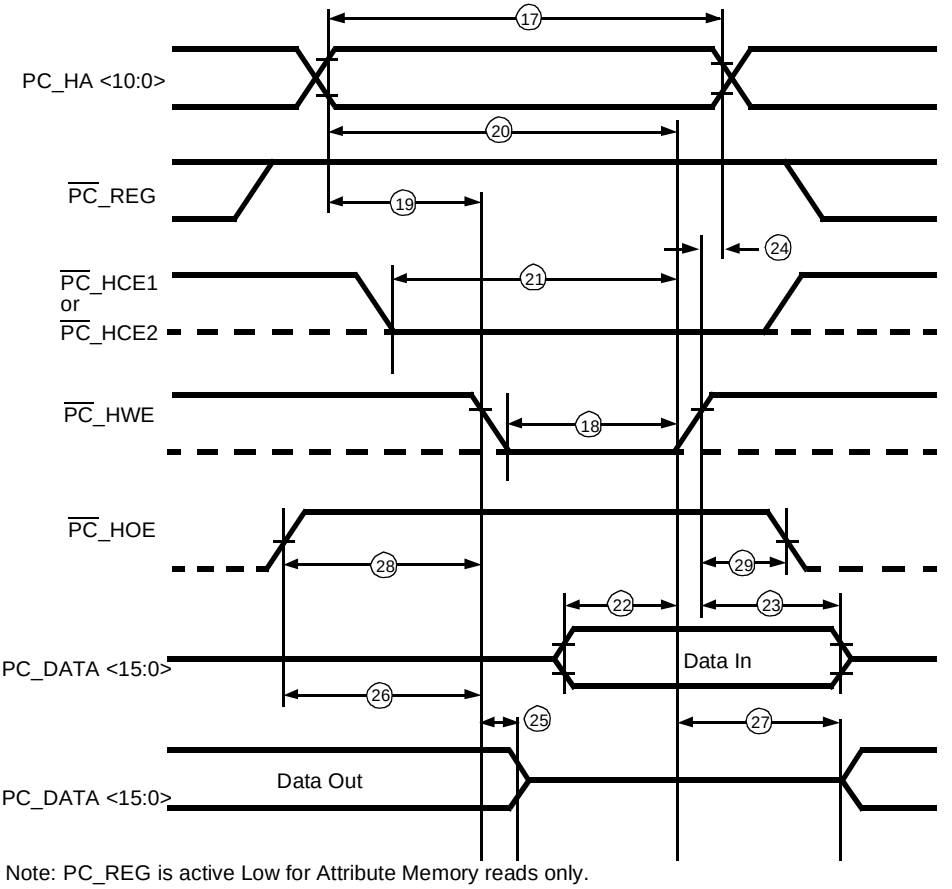


Figure 19. PCMCIA Write Memory Timing, No Wait States

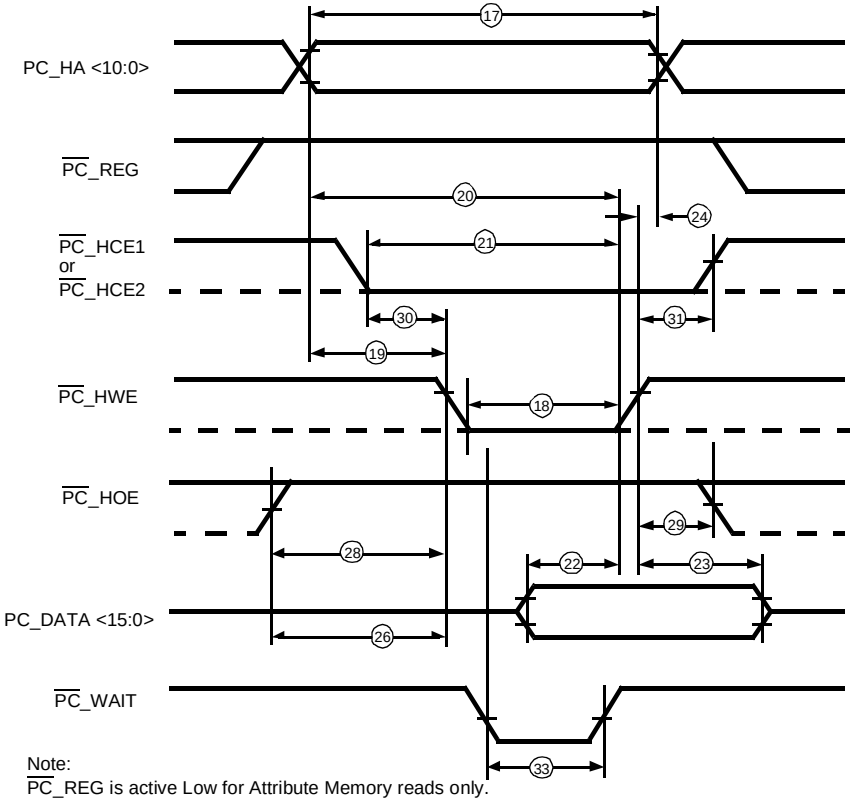


Figure 20. PCMCIA Write Memory Timing, Wait State Enabled

Table 73. I/O Read Timing Specification

No.	Symbol	Parameter	Minimum	Maximum	Units
35	TdIORD	Data Delay After IORD	100		ns
36	ThIORD	Data Hold Following IORD	0		ns
37	twIORD	IORD Width Time	165		ns
38	TsuAiord	Address Setup Before IORD	70		ns
39	ThAiord	Address Hold Following IORD	20		ns
40	TsuCEiord	CE Setup Before IORD	5		ns
41	ThCEiord	CE Hold Following IORD	20		ns
42	TsuRGiord	REG Setup Before IORD	5		ns
43	ThRGiord	REG Hold Following IORD	0		ns
44	TdIPKiord	INPACK Delay to IORD	0	45	ns
45	TdIPKiord	INPACK Delay from IORD		45	ns
46	TdIOISad	IOIS16 Delay from Address		35	ns
47	TdIOISadr	IOIS16 Delay Rise from Address		35	ns
48	TdWiord	Wait Delay from IORD		35	ns
49	TdWTr	Data Delay from Wait Rising		35	ns
50	TwWT	Wait Width Time		12	µs

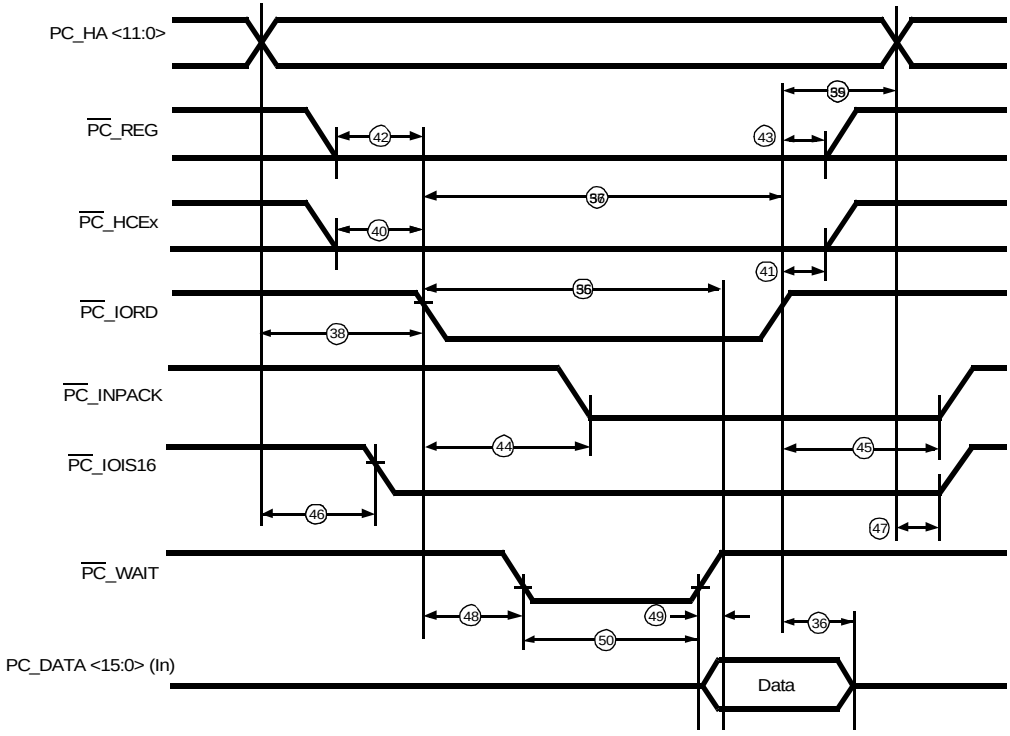


Figure 21. I/O Read Timing

Table 74. I/O Write Timing Specification

No.	Symbol	Parameter	Minimum	Maximum	Units
51	TsuIOWR	Data Setup before IOWR	60		ns
52	ThIOWR	Data Hold after IOWR	30		ns
53	TwIOWR	IOWR Width Time	165		ns
54	TsuAiowr	Address Setup to IOWR	70		ns
55	ThAiowr	Address Hold after IOWR	20		ns
56	TsuCEiowr	CE Setup before IOWR	5		ns
57	ThCEiowr	CE Hold after IOWR	20		ns
58	TsuRGiowr	REG Setup before IOWR	5		ns
59	ThRGiowr	REG Hold after IOWR	0		ns
60	TdIOISadr	IOIS16 Delay Falling from Address		35	ns
61	TIdIOISadr	IOIS16 delay Rising from Address		35	ns
62	TdWTiowr	Wait Delay Falling from IOWR		35	ns
63	TwWT	Wait Width Timing		12	µs

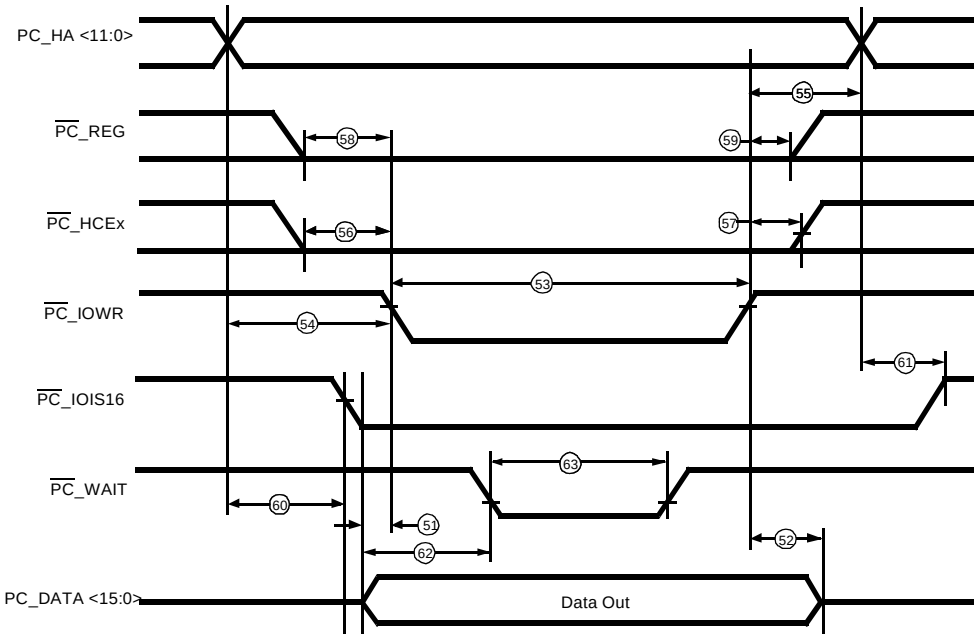


Figure 22. I/O Write Timing

Table 75. Skew Timing Between PCMCIA And ATA/IDE or Peripheral Bus

No.	Symbol	Parameter	Minimum	Maximum	Units
64	TskADR	Address Skew	0	25	ns
65	TskI/Of	I/O Fall Skew	0	25	ns
66	TskI/Or	I/O Rise Skew	0	25	ns
67	TskMEMf	Mem Fall Skew	0	25	ns
68	TskMEMr	Mem Rise Skew	0	25	ns

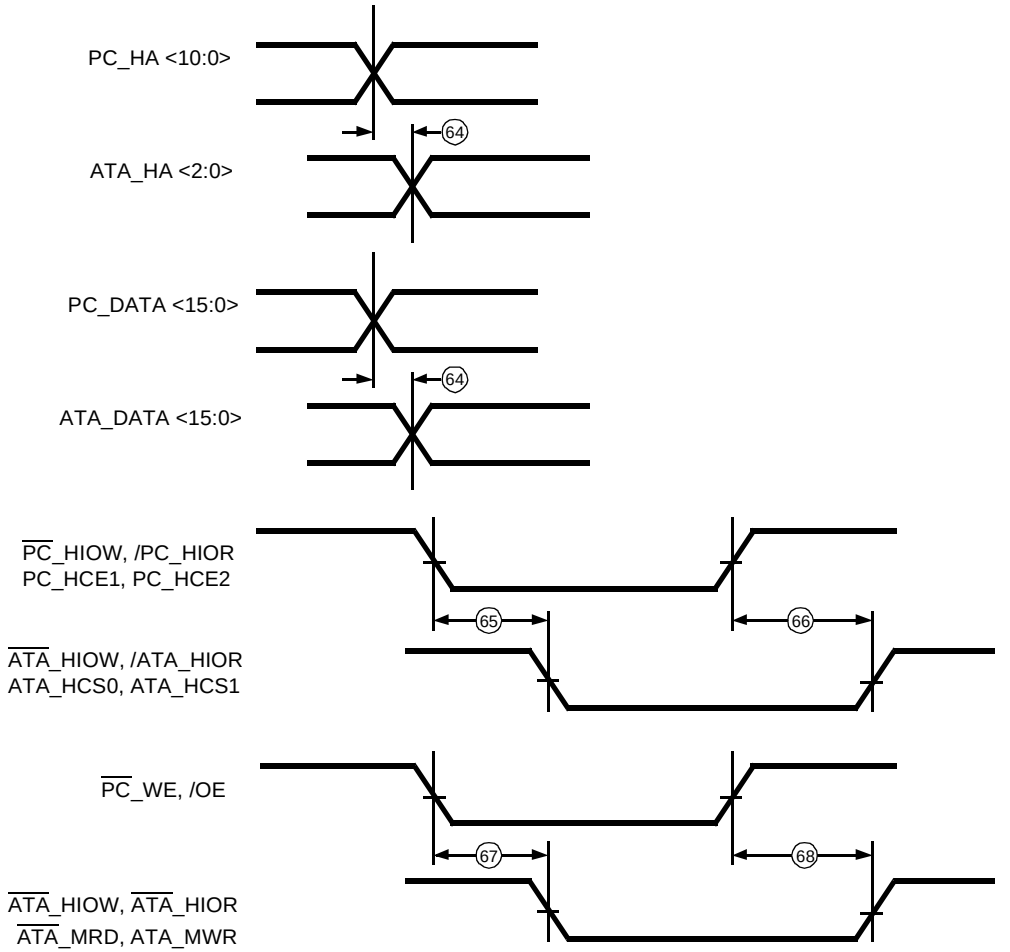


Figure 23. Skew Timing Between PCMCIA and ATA/IDE or Peripheral Bus

017 DEVICE SLEW DELAY

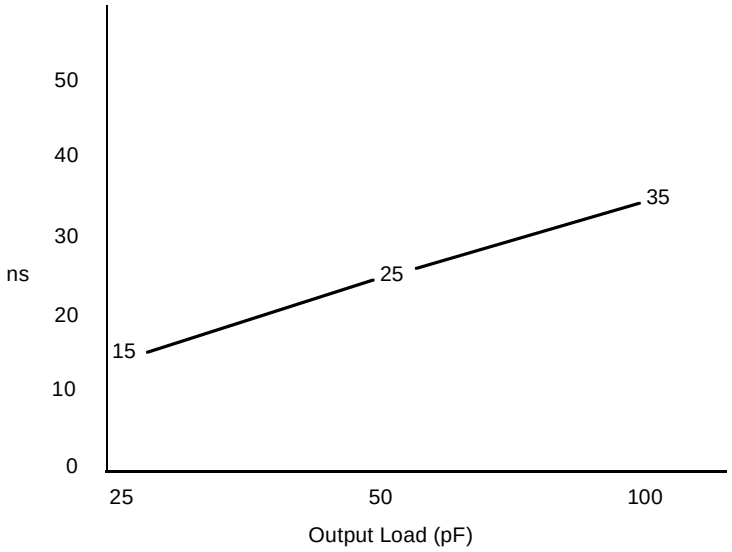


Figure 24. 017 Slew Delay Derating Curve (Typical)

Table 76. Serial Interface Timing

No.	Symbol	Parameter	Minimum	Maximum	Units
69	TpMCKin	Master Clock In Period	50		ns
70	TsuCS	CS Setup to CLK time	25		ns
71	ThCS	CS Hold after CLK	0		ns
72	ThDout	Data Hold Time	10		ns
73	TsuDout	Data Setup Time	25		ns
74	ThDin	Data Hold Time	0		ns
75	TsuDin	Data Setup Time	25		ns
76	TpCKw	Clock Period, Master	200		ns
77	TpCKs	Clock Period, Slave	200		ns

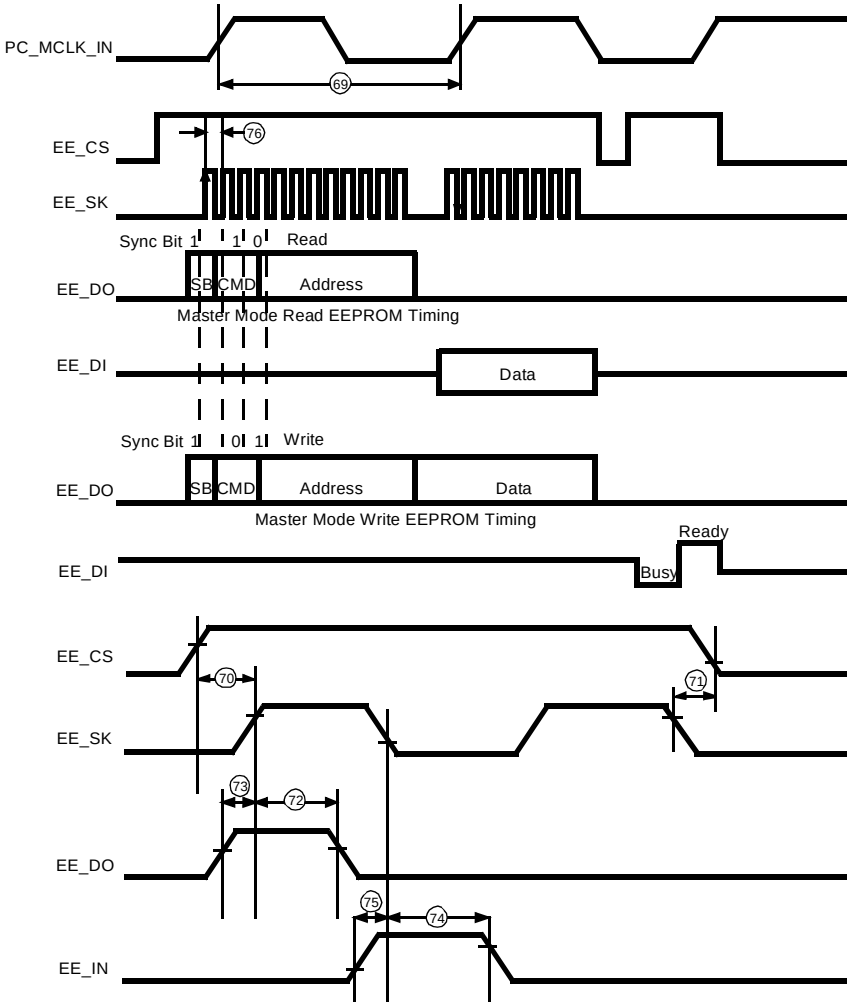


Figure 25. FMaster Mode Read EEPROM Timing

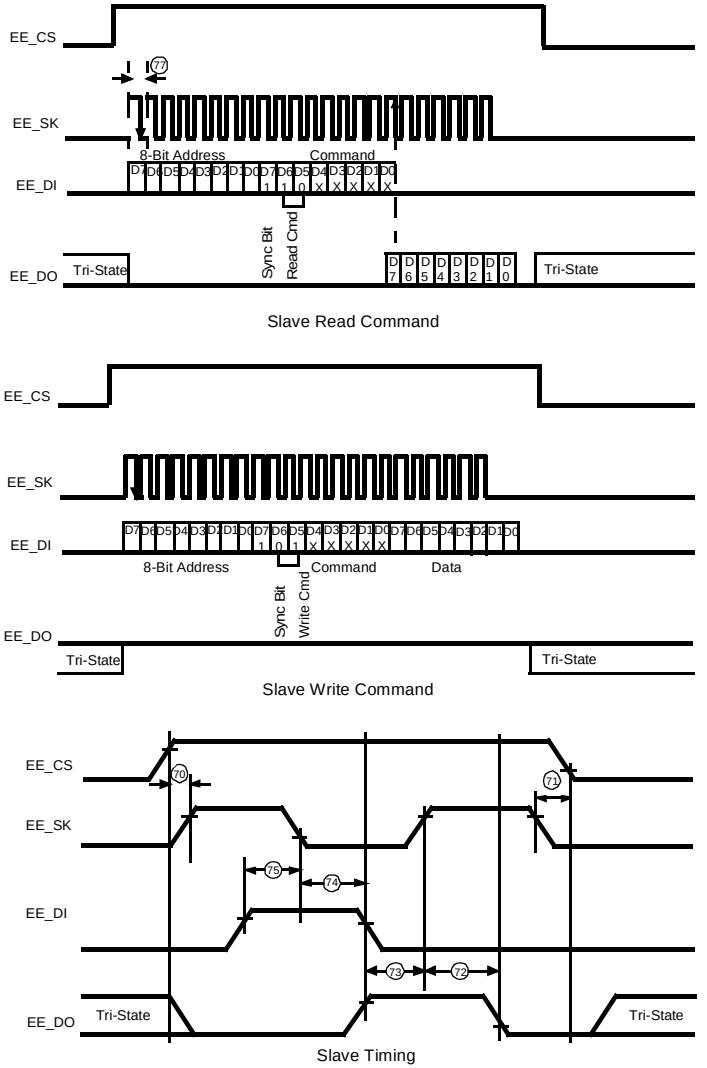


Figure 26. Slave Interface Timing (Read)

Appendix C: Timing Examples

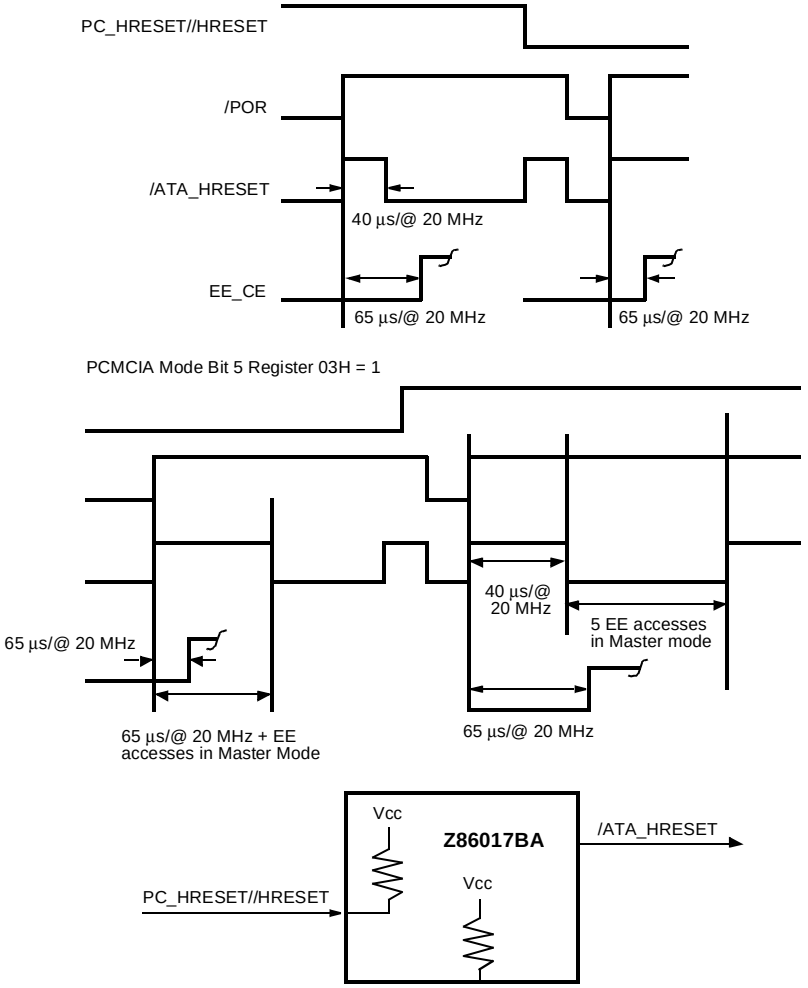


Figure 27. Z16017BA Reset Timing PCMCIA Mode

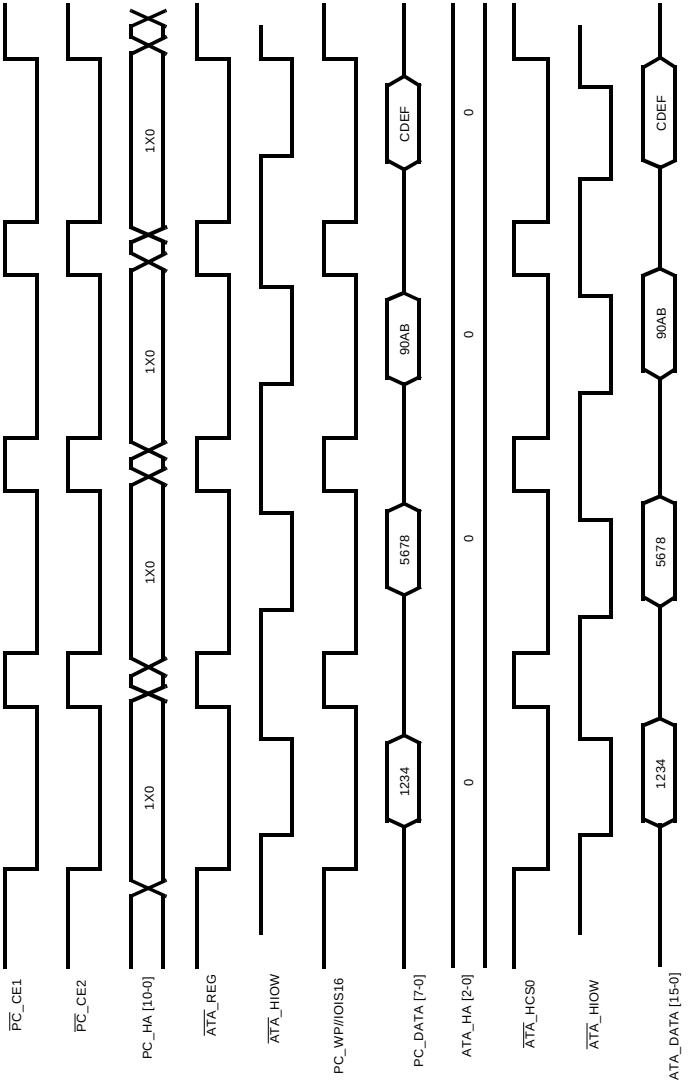


Figure 28. PCMCIA ATA/IDE 16-Bit I/O Write (Register 24 = 01, Internal IOIS 16 is selected)

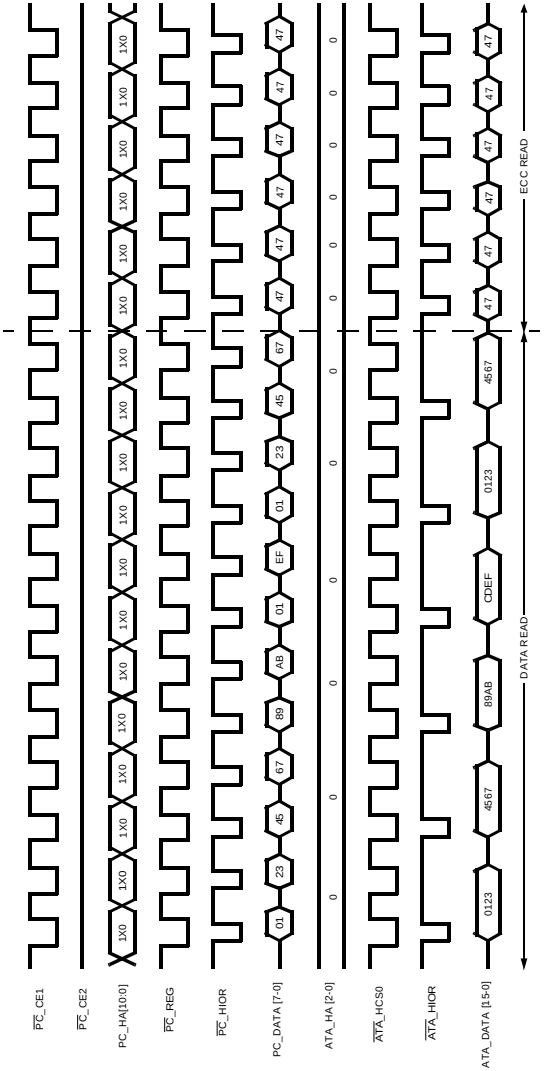


Figure 29. PCMCIA ATA / IDE 8-Bit Long Read (Reading 512-byte data plus 6-byte ECC)

Appendix D: Packaging and Ordering Information

20 MHZ PCMCIA ADAPTER CHIPS

Z86017	Z86M17	Z16017	Z16M17
100-Pin VQFP	100-pin VQFP	100-Pin VQFP	100-Pin VQFP
Z8601720ASC	Z86M1720ASC	Z1601720ASC	Z16M1720ASC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Package

A = VQFP

Temperature

S = 0° to +70° C

Speed

20 = 20 MHz

Environmental

C = Plastic Standard

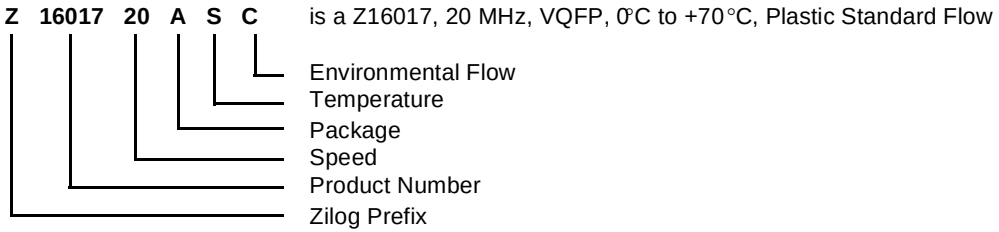
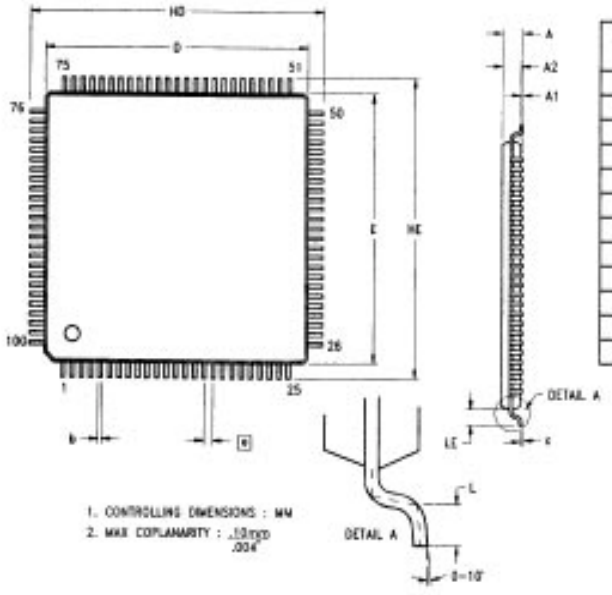


Figure 30. Example Package Name

Package Dimensions



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.35	1.60	.053	.063
A1	0.05	0.20	.002	.008
A2	1.30	1.50	.051	.059
b	0.15	0.26	.006	.010
c	0.10	0.20	.004	.008
HD	15.85	16.15	.624	.636
D	13.90	14.10	.547	.555
HE	15.85	16.15	.624	.636
E	13.90	14.10	.547	.555
e	0.50 TYP		.0197 TYP	
L	0.35	0.65	.014	.026
LE	0.90	1.10	.035	.043

Figure 31. 100-Lead VQFP Package Diagram

Appendix E: PCMCIA Interface Development Kit

GENERAL DESCRIPTION

The Z8601700ZCO Development Kit allows easy evaluation of the functions and capabilities of the Z86017 PCMCIA Interface Adapter. The board provides a ZIF socket for easy insertion and removal of the Z86017, as well as a full pin-out header for access to all signals. The board also provides breadboard space to assist in development.

Power to the Z86017 can either be supplied through a common point for current measurements applied through the interface, or supplied through a separate power connector. Programming the Z86017 is accomplished through the SPI port of a microcontroller or through the on-board EEPROM. The main clock source is supplied through the interface or through the on-board clock.

Z86017 SPECIFICATIONS

Power Requirements:

3.0V < VCC < +5.5V

Dimensions

Length: 7.6 in. (19.3 cm)

Width: 4.5 in. (11.4 cm)

KIT CONTENTS

Evaluation Board

- Z86017 PCMCIA Interface Adapter Device
- 100-Pin VQFP ZIF Socket
- 256 X 8-Byte EEPROM
- 20 MHz Oscillator
- Headers for full Z86017 pin-out
- Headers for access for PCMCIA signals
- Headers for connection to AT-Bus (on both Host and ATA side)
- Headers for connection to PCMCIA Extender Card
- Header for intelligent peripheral programming of EEPROM
- Power Connector

ZPCMCIA0ZDP PCMCIA Extender Card

Cables

- Two 6-inch, 34-pin IDC to 34-pin IDC Cables
- Power Cable with 1.0A Fuse
- Power Cable with Banana Plugs

Software

- Example Initialization Code

Documentation

- Z8601700ZCO Evaluation Kit User's Manual
- Z86017/Z16017 Reference Manual
- Product Registration Card

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru