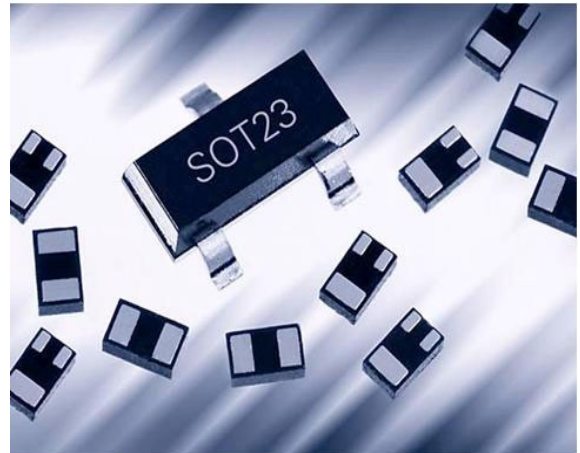
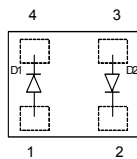
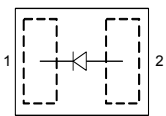


Silicon Deep Trench PIN Diodes

- Optimized for low bias current antenna switches in hand held applications
- Very low capacitance at zero volt reverse bias at frequencies above 1GHz (typ. 0.19 pF)
- Low forward resistance (typ. 1.3Ω @ $I_F = 3 \text{ mA}$)
- Improved ON / OFF mode harmonic distortion balance
- Pb-free (RoHS compliant) package


BAR90-02EL
BAR90-02ELS
BAR90-098LRH


Type	Package	Configuration	L_S (nH)	Marking
BAR90-02ELS	TSSLP-2-3	single, leadless	0.2	J*
BAR90-02EL	TSLP-2-19	single, leadless	0.4	X
BAR90-098LRH	TSLP-4-7	anti-parallel pair, leadless	0.4	T9

* Marking of TSSLP-2-3 with underline

Maximum Ratings at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	80	V
Forward current	I_F	100	mA
Total power dissipation	P_{tot}		mW
$T_S \leq 137^\circ\text{C}$, BAR90-02ELS		150	
$T_S \leq 133^\circ\text{C}$, all others		250	
Junction temperature	T_j	150	$^\circ\text{C}$
Operating temperature range	T_{op}	-55 ... 125	
Storage temperature	T_{stg}	-55 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾	R_{thJS}		K/W
BAR90-02ELS		≤ 90	
All others		≤ 65	

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

DC Characteristics

Breakdown voltage $I_{(BR)} = 5 \mu\text{A}$	$V_{(BR)}$	80	-	-	V
Reverse current $V_R = 60 \text{ V}$	I_R	-	-	50	nA
Forward voltage $I_F = 3 \text{ mA}$ $I_F = 100 \text{ mA}$	V_F	0.75 -	0.81 0.9	0.87 1	V

¹⁾For calculation of R_{thJA} please refer to Application Note AN077 (Thermal Resistance Calculation)

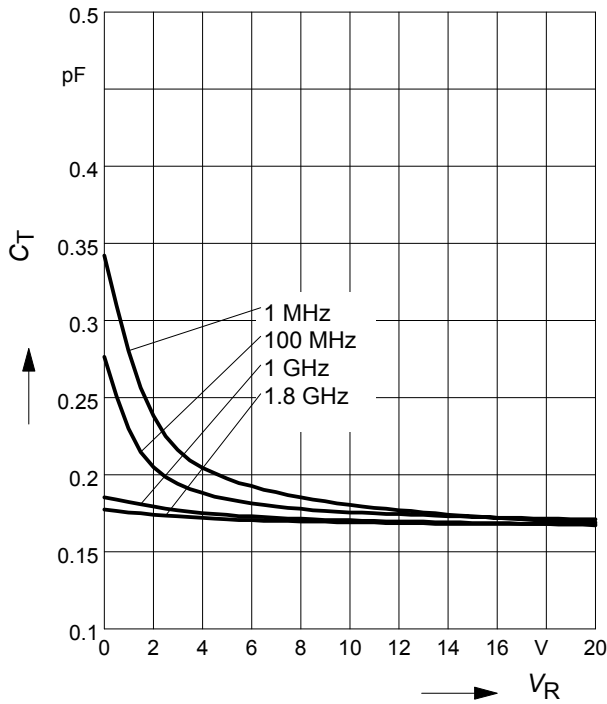
Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics					
Diode capacitance $V_R = 1\text{ V}, f = 1\text{ MHz}$ $V_R = 0\text{ V}, f = 100\text{ MHz}$ $V_R = 0\text{ V}, f = 1\text{ GHz}$ $V_R = 0\text{ V}, f = 1.8\text{ GHz}$	C_T	-	0.25 0.3 0.19 0.18	0.35 - - -	pF
Reverse parallel resistance $V_R = 0\text{ V}, f = 100\text{ MHz}$ $V_R = 0\text{ V}, f = 1\text{ GHz}$ $V_R = 0\text{ V}, f = 1.8\text{ GHz}$	R_P	-	35 5 4	- - -	k Ω
Forward resistance $I_F = 1\text{ mA}, f = 100\text{ MHz}$ $I_F = 3\text{ mA}, f = 100\text{ MHz}$ $I_F = 10\text{ mA}, f = 100\text{ MHz}$	r_f	-	2 1.3 0.8	- 2.3 -	Ω
Charge carrier life time $I_F = 10\text{ mA}, I_R = 6\text{ mA}$, measured at $I_R = 3\text{ mA}$, $R_L = 100\ \Omega$	τ_{rr}	-	750	-	ns
I-region width	W_I	-	20	-	μm
Insertion loss ¹⁾ $I_F = 1\text{ mA}, f = 1.8\text{ GHz}$ $I_F = 3\text{ mA}, f = 1.8\text{ GHz}$ $I_F = 10\text{ mA}, f = 1.8\text{ GHz}$	I_L	-	0.16 0.11 0.08	- - -	dB
Isolation ¹⁾ $V_R = 0\text{ V}, f = 0.9\text{ GHz}$ $V_R = 0\text{ V}, f = 1.8\text{ GHz}$ $V_R = 0\text{ V}, f = 2.45\text{ GHz}$	I_{SO}	-	18.5 13.5 11.5	- - -	

¹⁾BAR90-02EL in series configuration, $Z = 50\ \Omega$

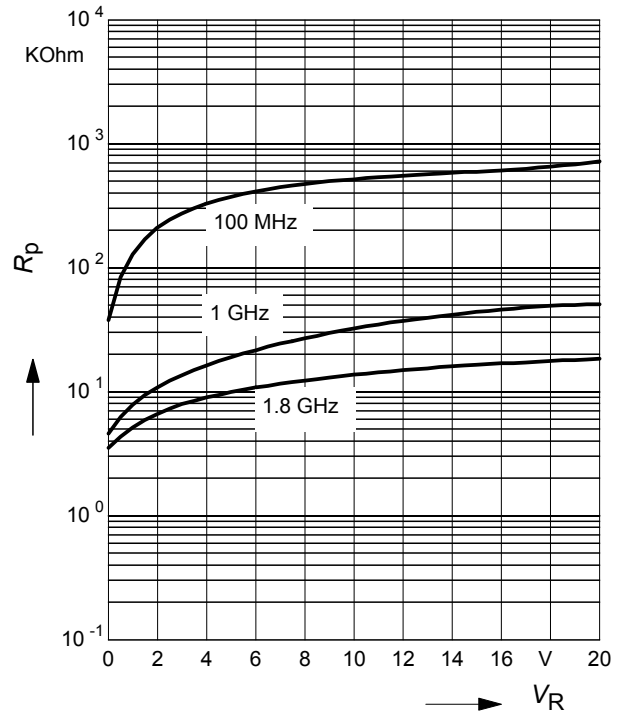
Diode capacitance $C_T = f(V_R)$

$f =$ Parameter



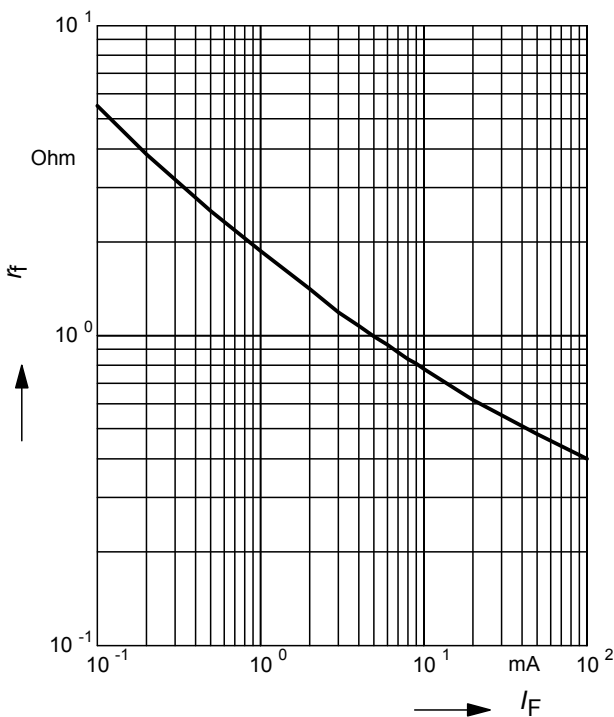
Reverse parallel resistance $R_p = f(V_R)$

$f =$ Parameter



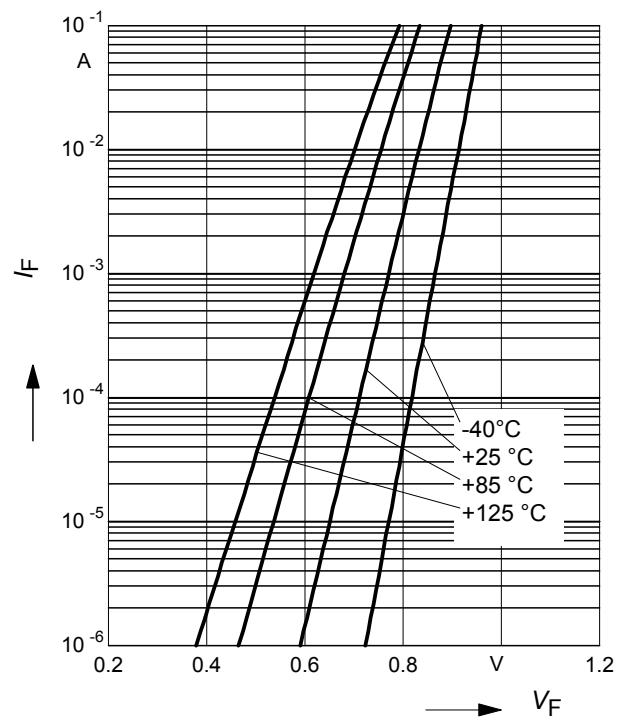
Forward resistance $r_f = f(I_F)$

$f = 100$ MHz



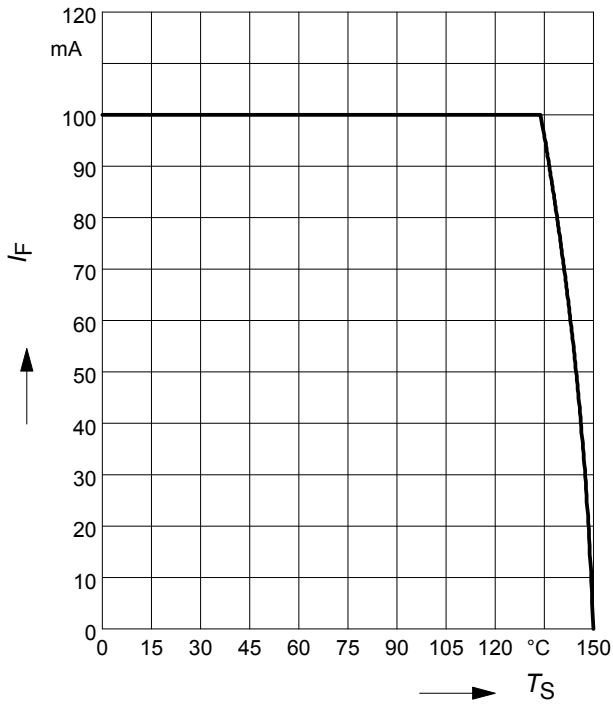
Forward current $I_F = f(V_F)$

$T_A =$ Parameter



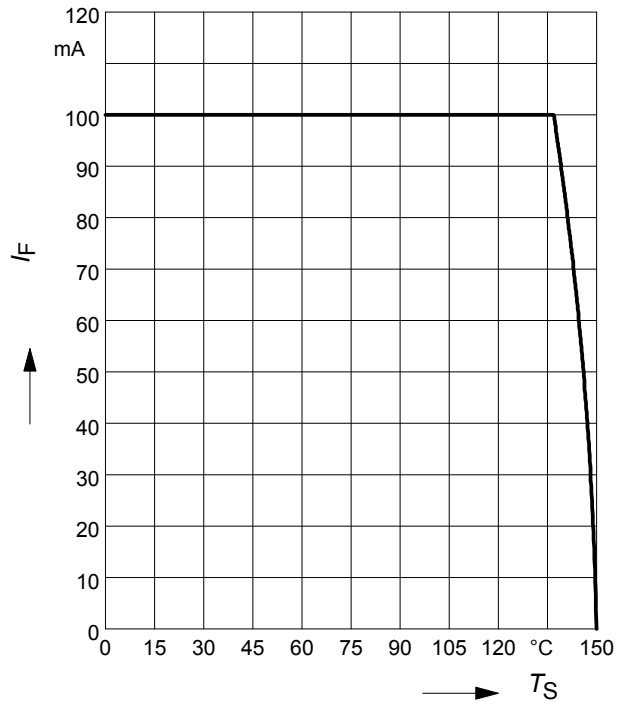
Forward current $I_F = f(T_S)$

BAR90-02EL / -098LRH



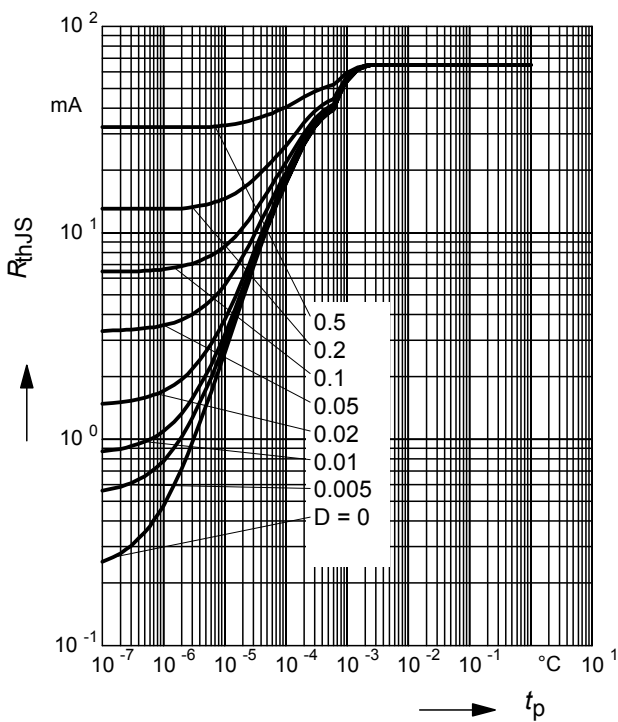
Forward current $I_F = f(T_S)$

BAR90-02ELS



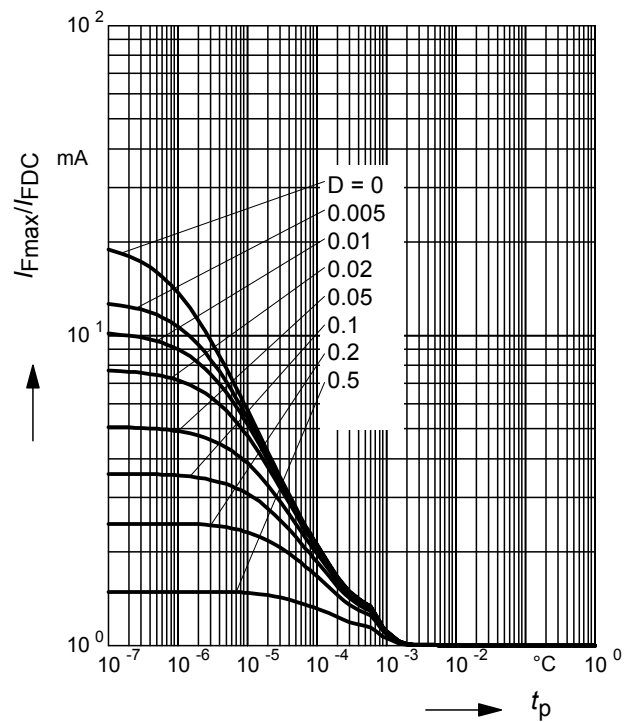
Permissible Puls Load $R_{thJS} = f(t_p)$

BAR90-02EL / -098LRH



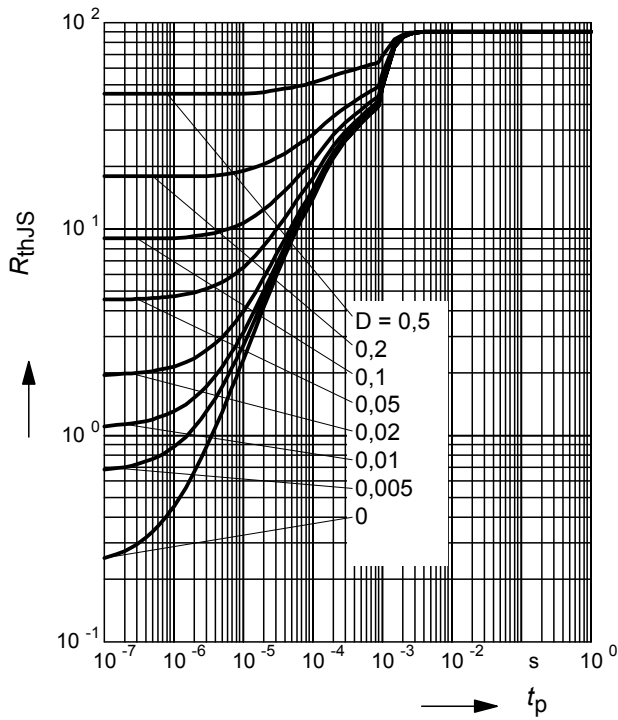
Permissible Pulse Load

$I_{Fmax} / I_{FDC} = f(t_p)$ BAR90-02EL / -098LRH



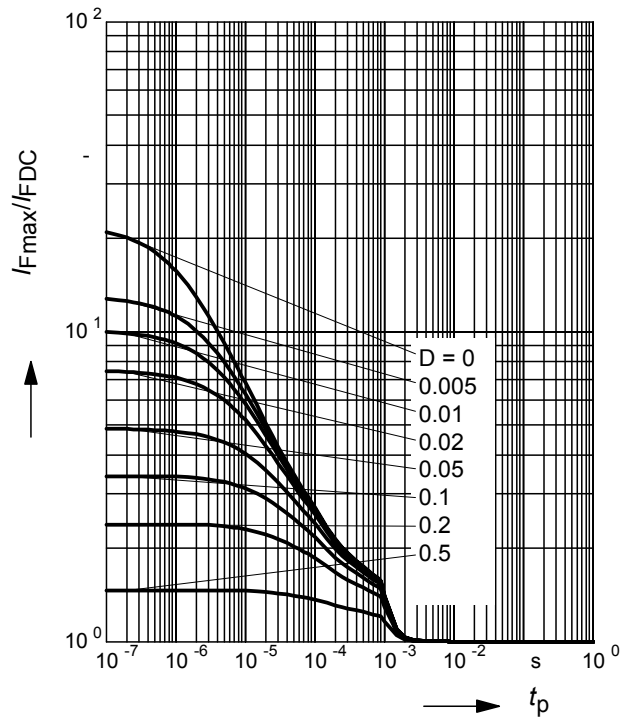
Permissible Puls Load $R_{thJS} = f(t_p)$

BAR90-02ELS



Permissible Pulse Load $I_{Fmax}/I_{FDC} = f(t_p)$

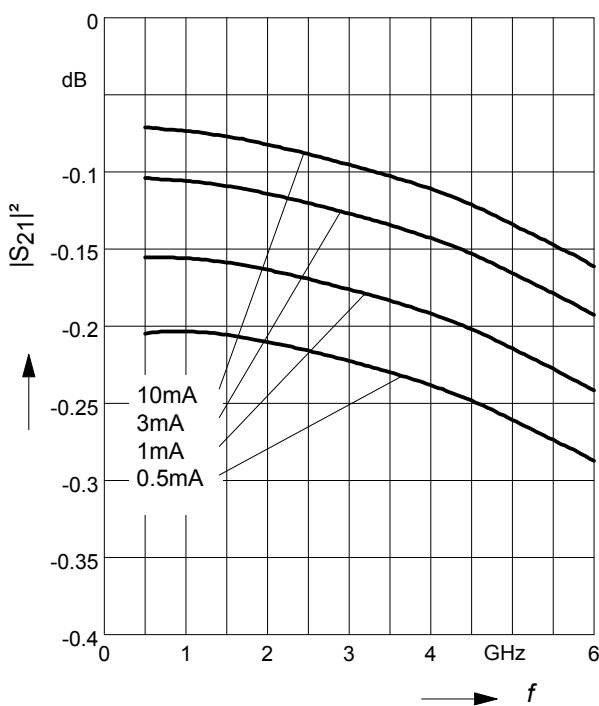
BAR90-02ELS



Insertion loss $I_L = -|S_{21}|^2 = f(f)$

I_F = Parameter

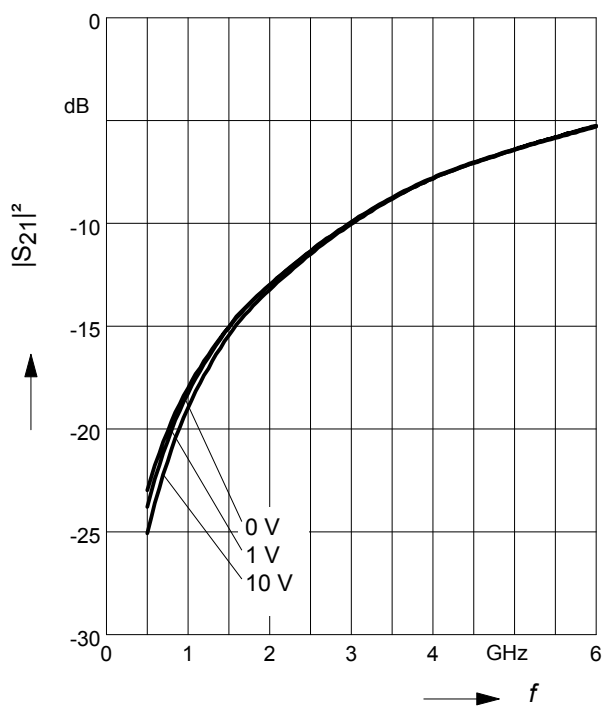
BAR90-02EL in series configuration, $Z = 50\Omega$



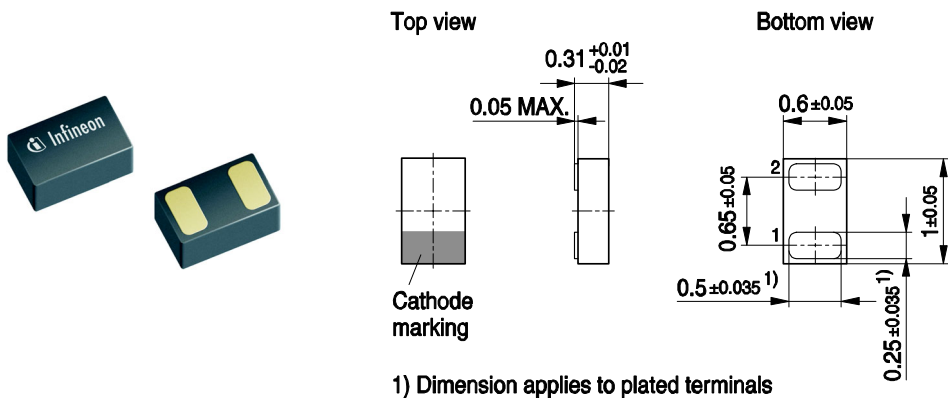
Isolation $I_{SO} = -|S_{21}|^2 = f(f)$

V_R = Parameter

BAR90-02EL in series configuration, $Z = 50\Omega$



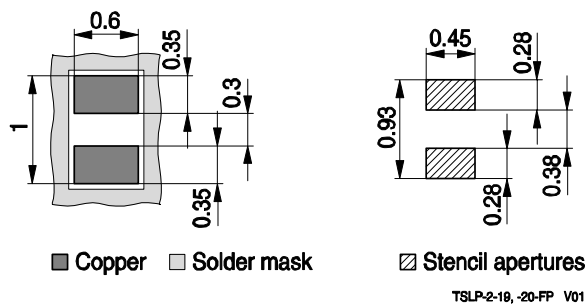
Package Outline



TSLP-2-19, -20-PO V01

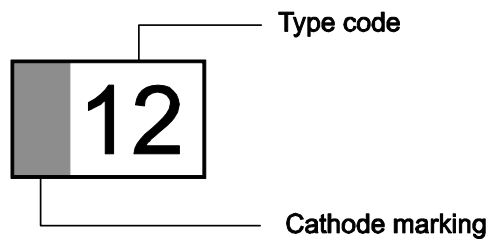
Foot Print

For board assembly information please refer to Infineon website „Packages“



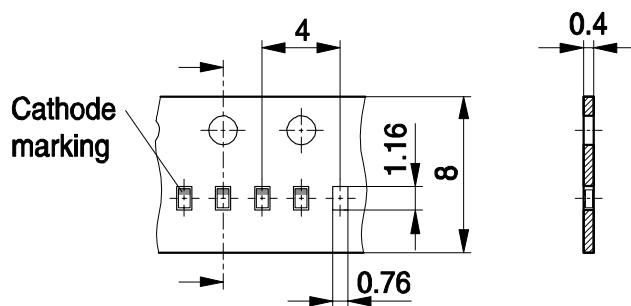
TSLP-2-19, -20-FP V01

Marking layout (Example)



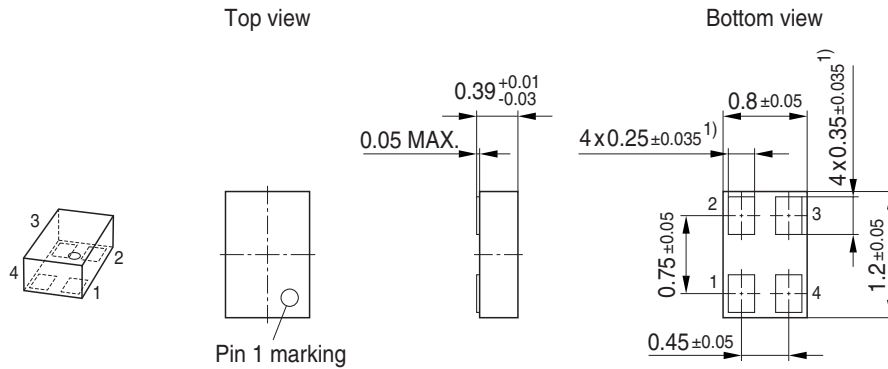
Standard Packing

Reel Ø 180 mm: 15.000 Pieces / Reel
 Reel Ø 330 mm: 6.000 Pieces / Reel
 Reel Ø 330 mm: 50.000 Pieces / Reel



TSLP-2-19, -20-TP V02

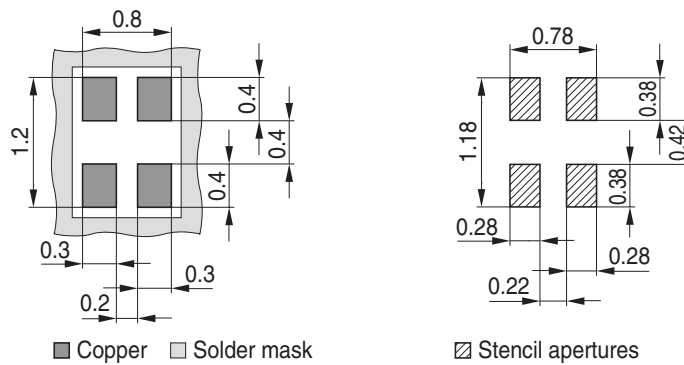
Package Outline



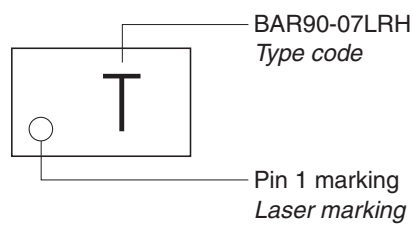
1) Dimension applies to plated terminal

Foot Print

For board assembly information please refer to Infineon website "Packages"

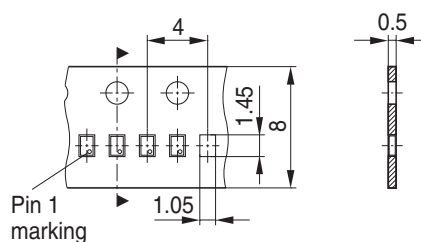


Marking Layout (Example)

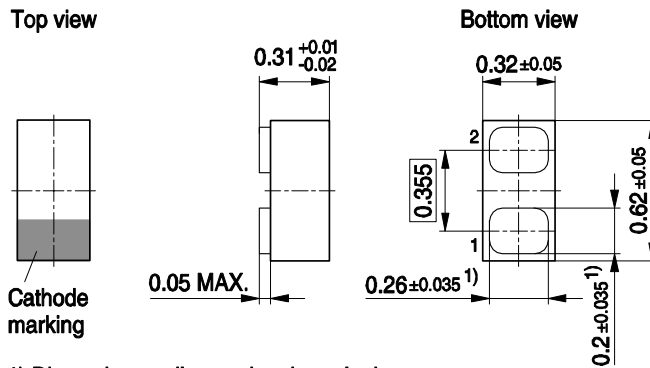


Standard Packing

Reel \varnothing 180 mm = 15.000 Pieces/Reel



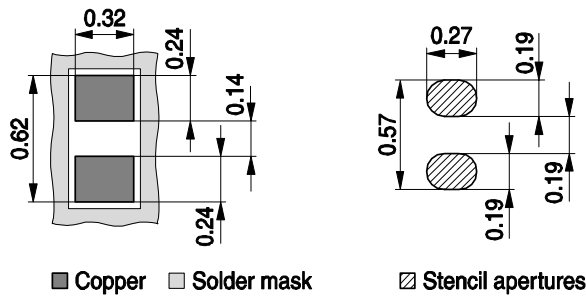
Package Outline



1) Dimension applies to plated terminals

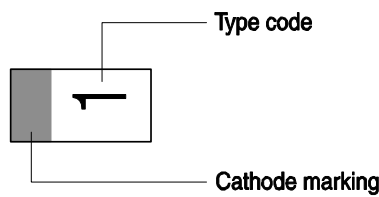
Foot Print

For board assembly information please refer to Infineon website "Packages"



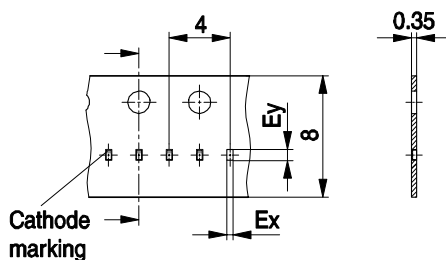
■ Copper □ Solder mask ▨ Stencil apertures

Marking Layout



Standard Packing

Reel ø330 mm = 15.000 Pieces/Reel



Tape type	Ex	Ey
Punched Tape	0.43	0.73
Embossed Tape	0.37	0.67

Deliveries can be both tape types (no selection possible). Specification allows identical processing (pick & place) by users.

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- Техническую поддержку проекта.
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