

## General Description

The SY88993AL limiting post amplifier, with its wide bandwidth, is ideal for use as a post amplifier in fiber-optic receivers with data rates up to 3.2Gbps. Signals as small as 4mV<sub>PP</sub> can be amplified to drive devices with CML inputs or AC-coupled PECL inputs. The SY88993AL generates a chatter-free Loss-of-Signal (LOS) open collector TTL output using an external resistor, as shown Figure 1.

The SY88993AL incorporates a programmable level detect function to identify when the input signal has been lost. This information can be fed back to the /EN input of the device to maintain stability under loss of signal conditions. Using LOS<sub>LVL</sub> pin the sensitivity of the level detect can be adjusted. The LOS<sub>LVL</sub> voltage can be set by connecting a resistor divider between V<sub>CC</sub> and V<sub>REF</sub>, Figure 5.

Datasheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

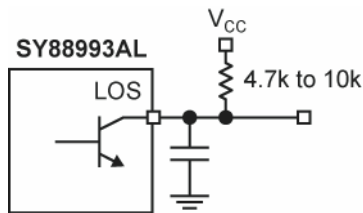


Figure 1. LOS<sub>LVL</sub> resistor configuration

## Features

- Up to 3.2Gbps operation
- Low noise CML data outputs
- Chatter-Free LOS generation
- Open Collector TTL LOS output
- TTL /EN Input
- Differential PECL inputs for data
- Single 3.3V power supply
- Available in a tiny 10-pin (3mm x 3mm) MSOP

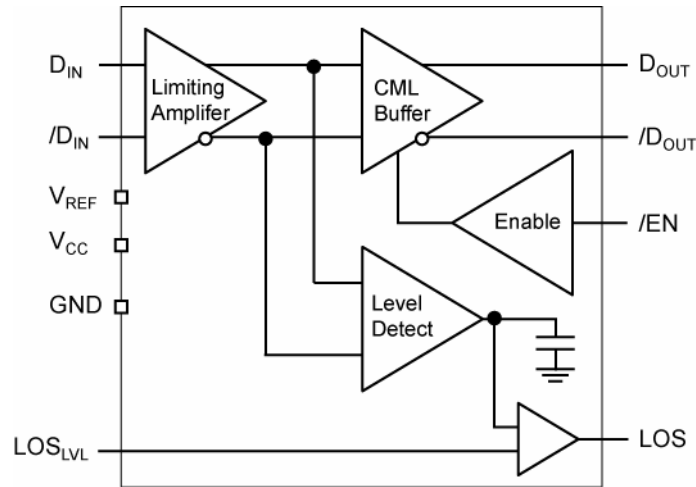
## Applications

- PON
- SFP/SFF/GBIC optical transceivers
- Gigabit Ethernet
- 1X and 2X Fibre Channel
- SONET/SDH: OC 3/12/24/48 – STM 1/4/8/16
- Line driver and line receiver

## Markets

- FTTX
- Datacom/Telecom

## Block Diagram



## Detailed Description

The SY88993AL is a high-sensitivity limiting post amplifier that operates from a single +3.3V power supply, over temperatures from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Signals with data rates up to 3.2Gbps and as small as  $4\text{mV}_{PP}$  can be amplified. Figure 2 shows the allowed input voltage swing. The SY88993AL generates a LOS output.  $LOS_{LVL}$  sets the sensitivity of the input amplitude detection.

### Input Amplifier/Buffer

Figure 3 shows a simplified schematic of the SY88993AL's input stage. The high-sensitivity of the input amplifier allows signals as small as  $4\text{mV}_{PP}$  to be detected and amplified. The input amplifier also allows input signals as large as  $1800\text{mV}_{PP}$ . Input signals below  $6\text{mV}_{PP}$  are linearly amplified with a typical 38dB differential voltage gain. Since it is a limiting amplifier, the SY88993AL outputs typically  $800\text{mV}_{PP}$  voltage-limited waveforms for input signals that are greater than  $10\text{mV}_{PP}$ . Applications requiring the SY88993AL to operate with high-gain should have the upstream TIA placed as close as possible to the SY88993AL's input pins to ensure the best performance of the device.

### Output Buffer

The SY88993AL's CML output buffer is designed to drive  $50\Omega$  lines. The output buffer requires appropriate termination for proper operation. An external  $50\Omega$  resistor to  $V_{CC}$  for each output pin provides this. Figure 4 shows a simplified schematic of the output stage.

### Loss-of-Signal

The SY88993AL generates a chatter-free LOS open-collector TTL output which requires an external pull-up

resistor, as shown in Figure 1. LOS is used to determine that the input amplitude is large enough to be considered a valid input. LOS asserts high if the input amplitude falls below the threshold sets by  $LOS_{LVL}$  and de-asserts low otherwise. LOS can be fed back to the enable bar ( $/EN$ ) input to maintain output stability under a loss of signal condition.  $/EN$  de-asserts the true output signal without removing the input signals. Typically, 5.6dB LOS hysteresis is provided to prevent chattering.

### Loss-of-Signal Level Set

The SY88993AL incorporates a programmable level detect function to identify when the input signal has been lost. This information can be fed back to the  $/EN$  input of the device to maintain stability under loss of signal conditions. Using  $LOS_{LVL}$  pin the sensitivity of the level detect can be adjusted. The  $LOS_{LVL}$  voltage can be set by connection a resistor divider between  $V_{CC}$  and  $V_{REF}$ , Figure 5.

### Hysteresis

The SY88993AL typically provides 5.6dB LOS electrical hysteresis. By definition, a power ratio measured in dB is  $10\log(\text{power ratio})$ . Power is calculated as  $V_{IN}^2/R$  for an electrical signal. Hence, the same ratio can be stated as  $20\log(\text{voltage ratio})$ . While in linear mode, the electrical voltage input changes linearly with the optical power and therefore, the ratios change linearly. Thus, the optical hysteresis in dB is half the electrical hysteresis in dB given in the data sheet. Since the SY88993AL is an electrical device, this data sheet refers to hysteresis in electrical terms. With 5.6dB LOS hysteresis, a voltage factor of about 2 is required to assert or de-assert LOS.

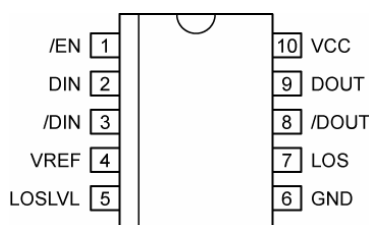
## Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88993ALKG	K10-1	Industrial	993L with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY88993ALKGTR <sup>(1)</sup>	K10-1	Industrial	993L with Pb-Free bar-line indicator	Pb-Free NiPdAu

**Note:**

1. Tape and reel.

## Pin Configuration



**10-Pin MSOP (K10-1)**

## Pin Description

Pin Number	Pin Name	Pin Function
1	/EN	TTL (Input): Output enable (Active Low).
2	DIN	Data (Input): Data input.
3	/DIN	Data (Input): Complementary data input.
4	VREF	Output: Reference voltage output for LOS Level Set (See Figure 3).
5	LOSLVL	Input: Loss-of-Signal Level Set
6	GND	Ground.
7	LOS	TTL Output (Open Collector): Loss-of-Signal indicator (Active High).
8	/DOUT	CML (Output): Inverting data output.
9	DOUT	CML (Output): Data output.
10	VCC	Power Supply: Positive power supply.

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage ( $V_{CC}$ )	0V to +4.0V
Input Voltage (DIN, /DIN)	0V to $V_{CC}$
Lead Temperature (soldering, #sec.)	260°C
Storage Temperature ( $T_s$ )	-55°C to +85°C

**Operating Ratings<sup>(2)</sup>**

Supply Voltage ( $V_{IN}$ )	+3.0V to +3.6V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Junction Thermal Resistance	
MSOP ( $\theta_{JA}$ )	113°C/W
MSOP ( $\psi_{JB}$ )	96°C/W

**DC Electrical Characteristics**

$V_{CC} = +3.3V \pm 10\%$ ;  $R_{LOAD} = 50\Omega$  to  $V_{CC}$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless noted. Typical values at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{CC}$	Power Supply Current	No output load.		40	55	mA
$I_{OH}$	LOS Output Leakage	$V_{CC} = 3.6V$			100	$\mu A$
$LOS_{LVL}$	LOSLVL Level		$V_{REF}$		$V_{CC}$	V
$V_{OH}$	Output HIGH Voltage		$V_{CC}-20$	$V_{CC}-5$	$V_{CC}$	mV
$V_{OL}$	Output LOW Voltage	Note 9	$V_{CC}-350$	$V_{CC}-400$	$V_{CC}-475$	mV
$Z_O$	Single-Ended Output Impedance	Note 10	40	50	60	$\Omega$
$V_{REF}$	Reference Voltage		$V_{CC}-1.38$	$V_{CC}-1.32$	$V_{CC}-1.26$	V
$V_{OFFSEST}$	Differential Output Offset				$\pm 80$	mV
$V_{CMR}$	Common Mode Range		$GND \pm 2$		$V_{CC}-0.2$	V

**TTL DC Electrical Characteristics**

$V_{CC} = +3.3V \pm 10\%$ ;  $R_{LOAD} = 50\Omega$  to  $V_{CC}$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	/EN Input HIGH Voltage		2.0			
$V_{IL}$	/EN Input LOW Voltage				0.8	V
$I_{IH}$	/EN Input HIGH Current	$V_{IN} = 2.7V$ $V_{IN} = V_{CC}$			20 100	$\mu A$ $\mu A$
$I_{IL}$	/EN Input LOW Current	$V_{IN} = 0.5V$	-300			$\mu A$

**Notes:**

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

## AC Electrical Characteristics

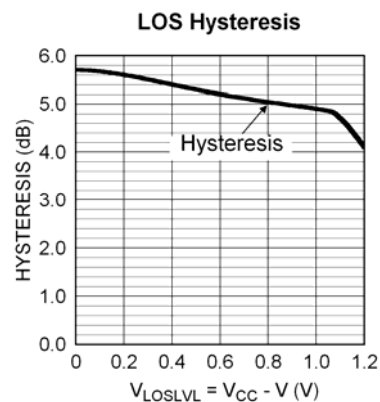
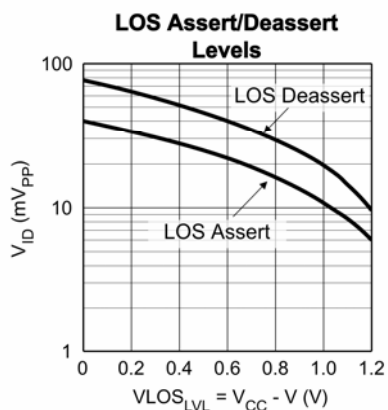
$V_{CC} = +3.3V \pm 10\%$ ;  $R_{LOAD} = 50\Omega$  to  $V_{CC}$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
LOS <sub>AH</sub>	High LOS Assert Level	$V_{LOSLVL} = V_{CC}$	30	43		mV <sub>PP</sub>
LOS <sub>DH</sub>	High LOS De-assert Level	$V_{LOSLVL} = V_{CC}$		83	95	mV <sub>PP</sub>
HYS <sub>H</sub>	High LOS Hysteresis		2	5.6	8	dB
LOS <sub>AM</sub>	Medium LOS Assert Level	$V_{LOSLVL} = V_{CC} - 400mV$	20	31		mV <sub>PP</sub>
LOS <sub>DM</sub>	Medium LOS De-assert Level	$V_{LOSLVL} = V_{CC} - 400mV$		55	65	mV <sub>PP</sub>
HYS <sub>M</sub>	Medium LOS Hysteresis		2	5.6	8	dB
LOS <sub>AL</sub>	Low LOS Assert Level	$V_{LOSLVL} = V_{CC} - 800mV$	10	19		mV <sub>PP</sub>
LOS <sub>DL</sub>	Low LOS De-assert Level	$V_{LOSLVL} = V_{CC} - 800mV$		31	45	mV <sub>PP</sub>
HYS <sub>L</sub>	Low LOS Hysteresis		2	5.6	8	dB
PSRR	Power Supply Rejection Ratio	Note 4		35		dB
t <sub>OFFL</sub>	LOS Release Time Minimum Input	Note 5		0.1	0.5	$\mu s$
t <sub>OFFH</sub>	LOS Release Time Maximum Input	Note 5		0.1	0.5	$\mu s$
t <sub>ONL</sub>	LOS Assert Time	Note 5		0.2	0.5	$\mu s$
t <sub>r</sub> , t <sub>f</sub>	Differential Output Rise/Fall Time (20% to 80%)	Note 6		60	120	Ps
V <sub>ID</sub>	Input Voltage Range		4		1800	mV <sub>PP</sub>
V <sub>OD</sub>	Differential Output Voltage Swing	Note 7, 8, 9, 10	700	800	950	mV <sub>PP</sub>
V <sub>SR</sub>	LOS Sensitivity Range		4		50	mV <sub>PP</sub>
A <sub>V(Diff)</sub>	Differential Voltage Gain			38		DB
B <sub>-3dB</sub>	3dB Bandwidth			2.5		GHz
S <sub>21</sub>	Single-Ended Small Signal-Gain		26	32		dB

### Notes:

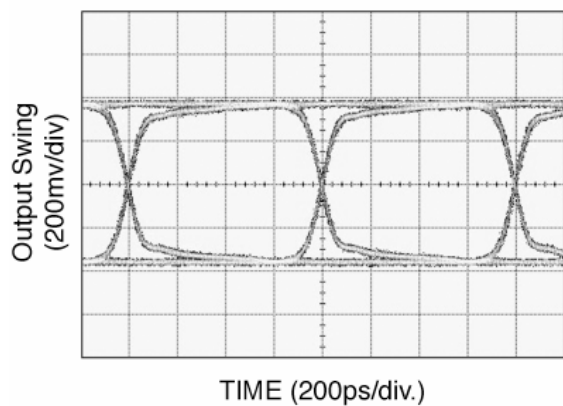
4. Input referred noise = RMS output noise/low frequency gain. Input referred, 55MHz.
5. Input is a 200MHz square wave, tr < 300ps.
6. With input signal V<sub>ID</sub> > 50mV<sub>PP</sub> with 50 $\Omega$  load.
7. Input is a 200MHz square wave, tr < 300ps, 50 $\Omega$  load.
8. V<sub>ID</sub> > 10mV<sub>PP</sub>.
9. Output levels are based on 50 $\Omega$  impedance. If the load impedance is different, the output level will be changed.
10. See output structure.

## Typical Characteristics

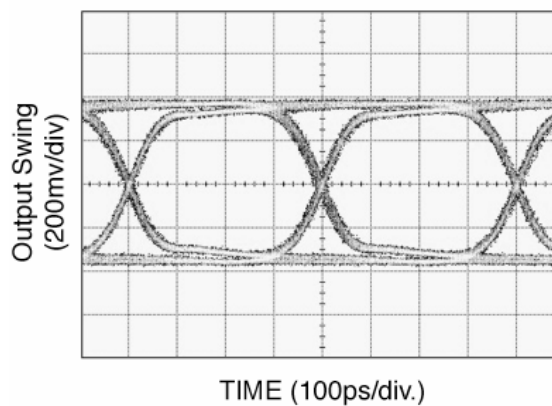


## Functional Characteristics

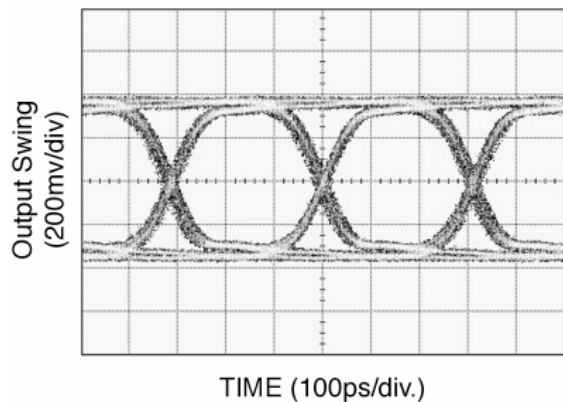
20mV<sub>PP</sub> Input at 1.25Gbps, PRBS 2<sup>23</sup>-1



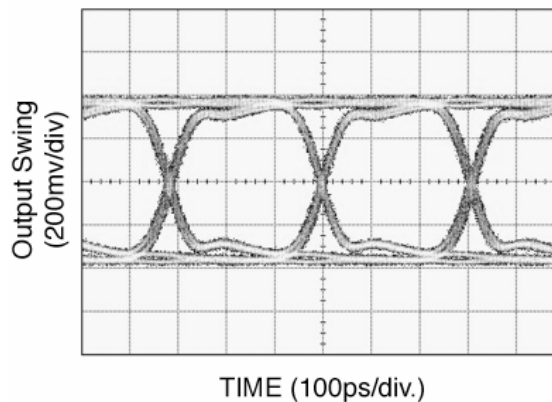
20mV<sub>PP</sub> Input at 2.5Gbps, PRBS 2<sup>23</sup>-1



20mV<sub>PP</sub> Input at 3.2Gbps, PRBS 2<sup>23</sup>-1



500mV<sub>PP</sub> Input at 3.2Gbps, PRBS 2<sup>23</sup>-1



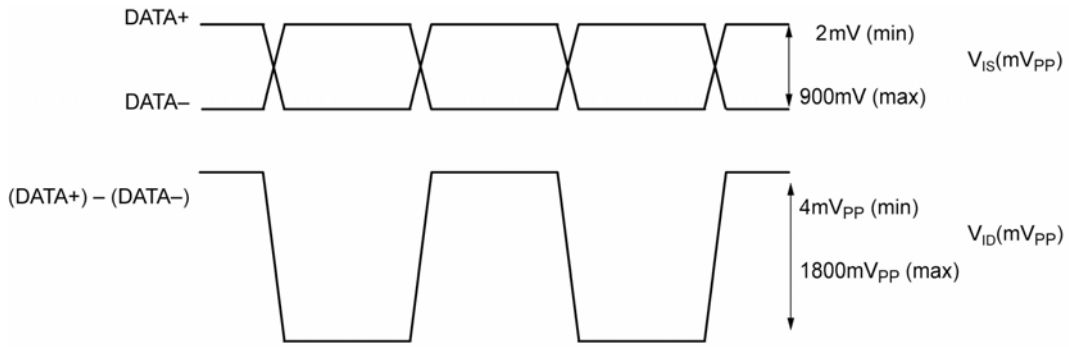


Figure 2.  $V_{IS}$  and  $V_{ID}$

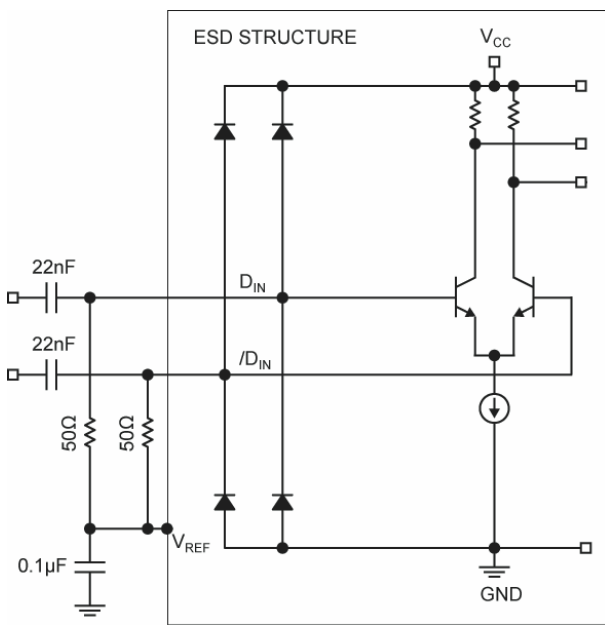


Figure 3. Differential Input Configuration

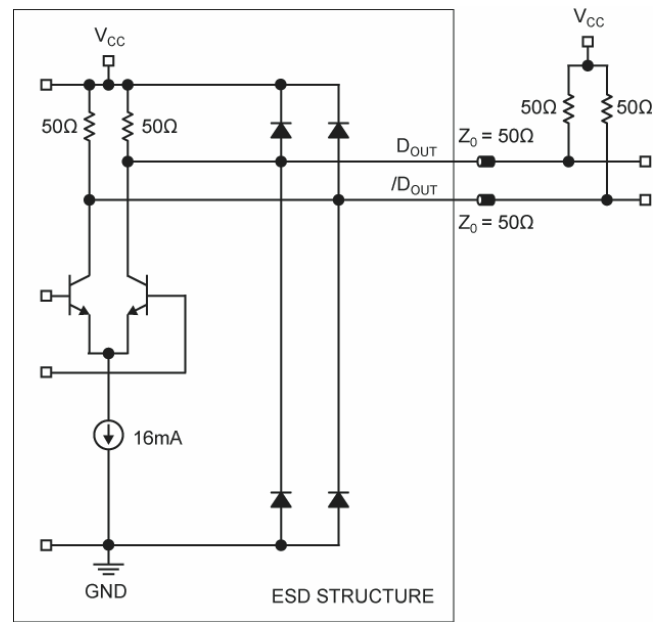


Figure 4. Differential Output Configuration

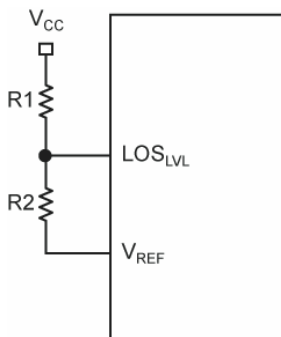
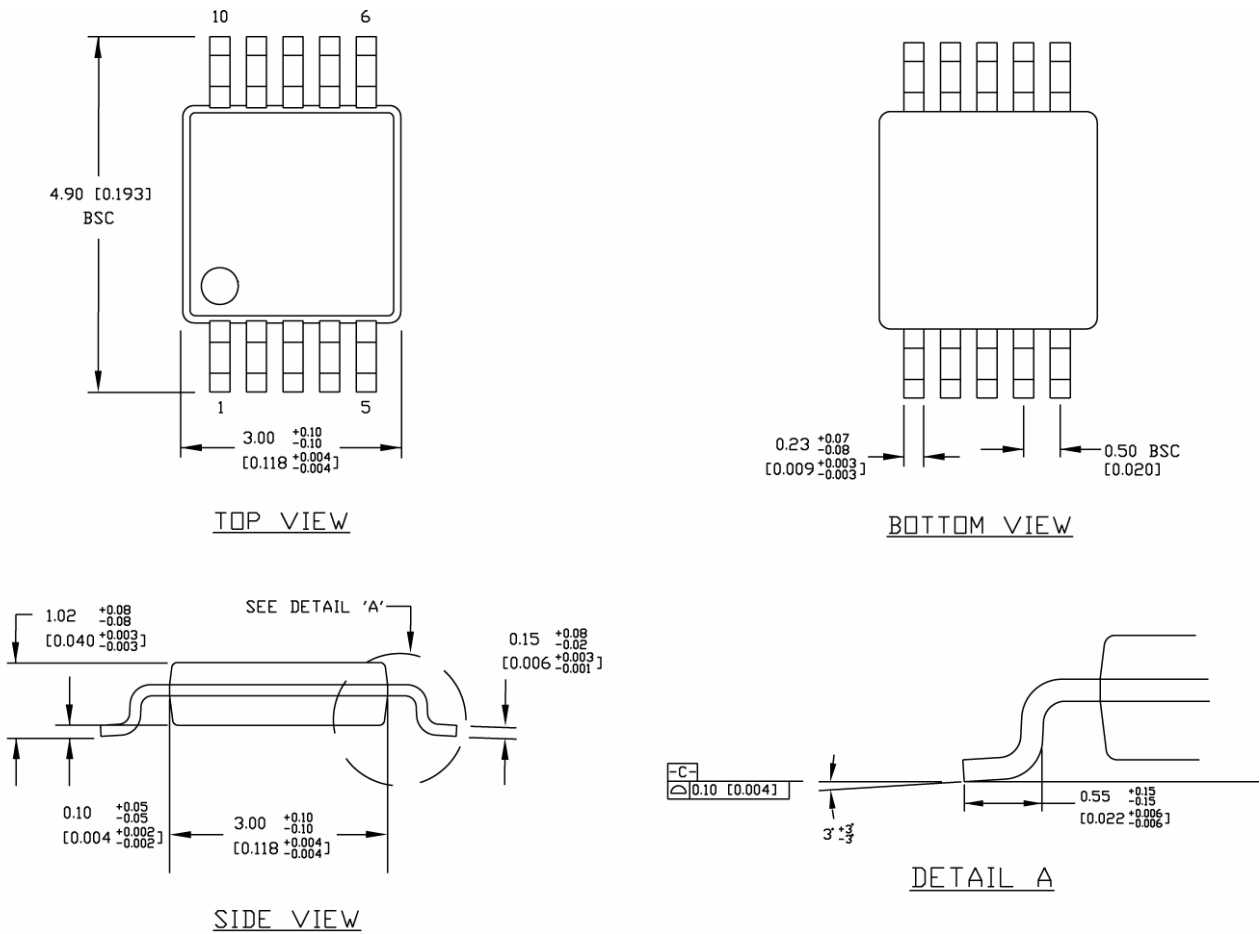


Figure 5. LOSLVL Circuit

**Notes:**

1. Resistor Divider =  $R2 / (R1 + R2)$
2.  $R1 + R2 \geq 5k\Omega$

**Package Information**



**NOTES:**

1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

**10-Pin MSOP (K10-1)**

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