Triple Half-bridge DMOS Output Driver with Serial Input Control ATA6826

ATA6826
Driver IC

Application Note

1. Introduction

ATA6826 is a fully protected universal driver interface designed in SMARTIS™1 technology. It is used to control up to 3 different loads by a microcontroller in automotive and industrial applications. The ATA6826 is housed in a SO14 package.

Each of the 3 high-side and 3 low-side drivers is capable of driving currents up to 1A. The drivers are internally connected to form 3 half bridges, and can be controlled separately from a standard serial peripheral interface. Therefore, different types of loads such as bulbs, resistors, capacitors and inductors can be combined. The IC design particularly supports applications of H-bridges to drive DC motors.

Protection against short-circuit conditions, overtemperature and undervoltage is implemented. Various diagnostic functions and a very low quiescent current in standby mode enable a wide range of applications. Automotive qualification with respect to conducted interferences, EMC and 2-kV ESD protection gives added value and enhanced quality for demanding up-market applications.

2. Design Kit

The design kit includes the following components:

- ATA6826 design software
- Basic application board ATA6826-DK
- Link cable to PC, 25-lead 1:1
- Application note
- Datasheet “ATA6826: Triple Half-bridge DMOS Output Driver with Serial Input Control”

2.1 Description

The heart of the ATA6826 design kit is a PC-controlled basic application board. By means of the ATA6826 design kit, a user can adapt the loads (refer to Figure 2-2 on page 3) easily via row connector pins. The design software interface controls the design kit.

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2.2 Features

- Screwless row connector pins for external loads switched by low-side or high-side drivers
- Easy adaptation of loads directly on the ATA6826 design kit
- Direct switch of loads to V_S or GND
- Forward/reverse rotation of DC motors by full-bridge application
- Paralleling of outputs for powerful applications
- PC adaptation via standard “SUB-DE” connectors (plug 4 in Figure 2-2 on page 3)
- Input for 5V VCC power supply alternatively on board or external by row connector 2
- Indicate rotation direction of DC motors by LEDs, best function at V_{Batt} = 12V
- PC-controlled functions via software user interface
- All pins are easily accessible via test points
- Inhibit switch on board or by external input

Figure 2-1. Block Diagram

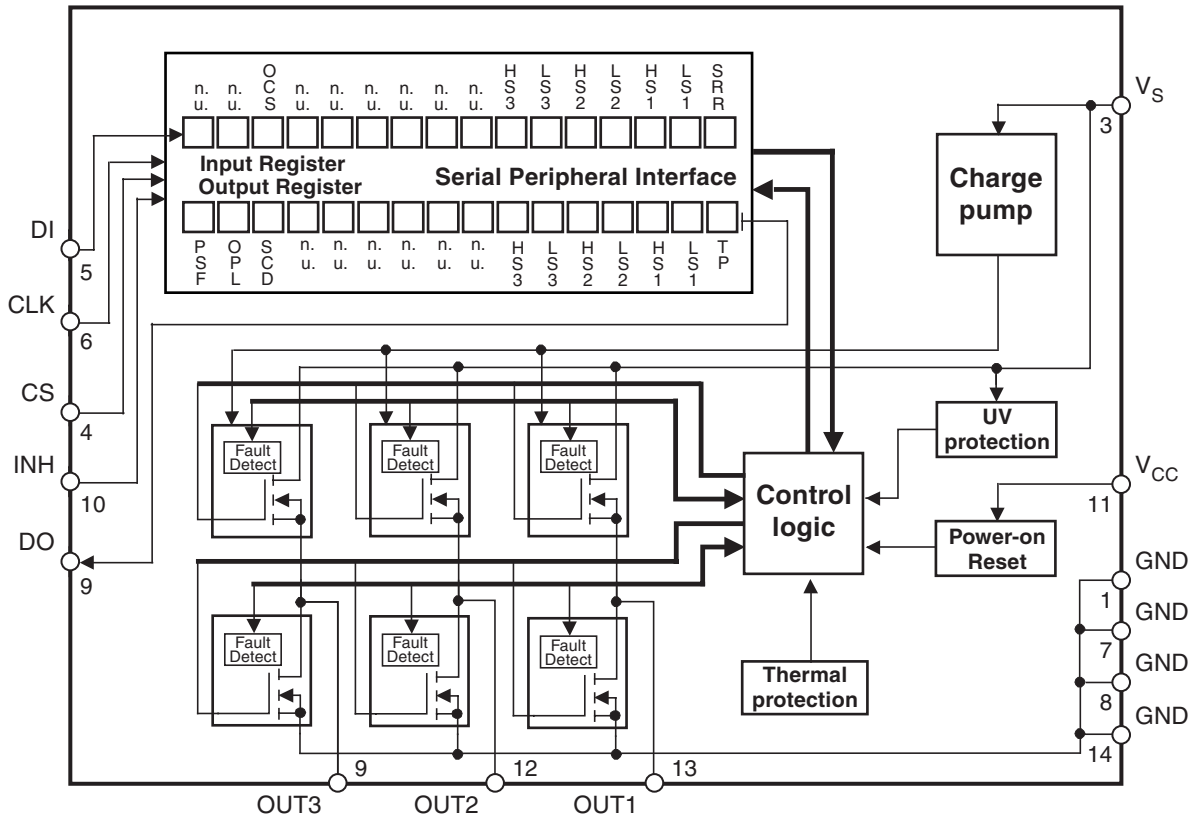


Figure 2-2. ATA6826-DK Basic Application Board Schematic

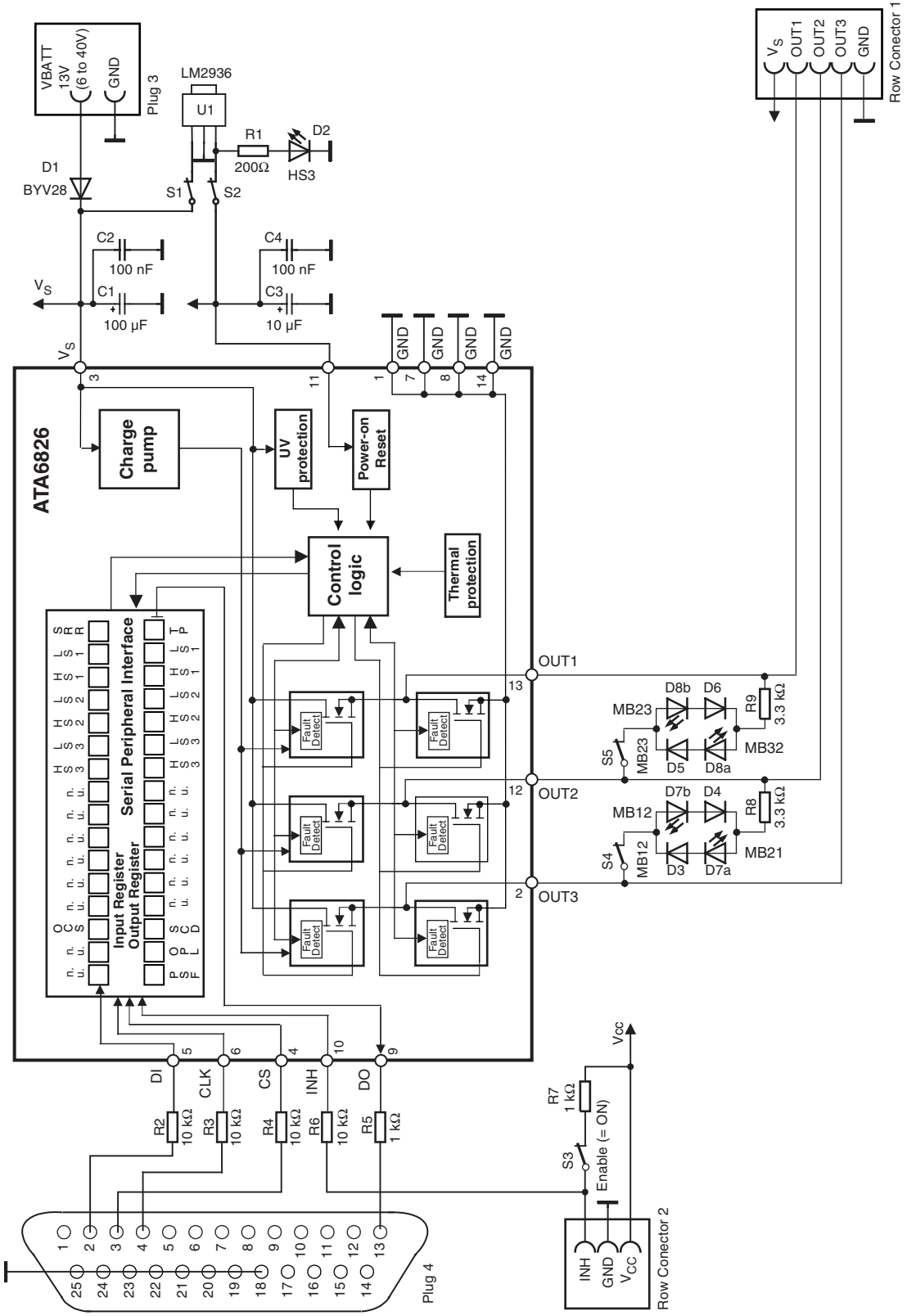


Figure 2-3. ATA6826-DK Design Kit, Basic Application Board Component Placement; Top Side, Top View

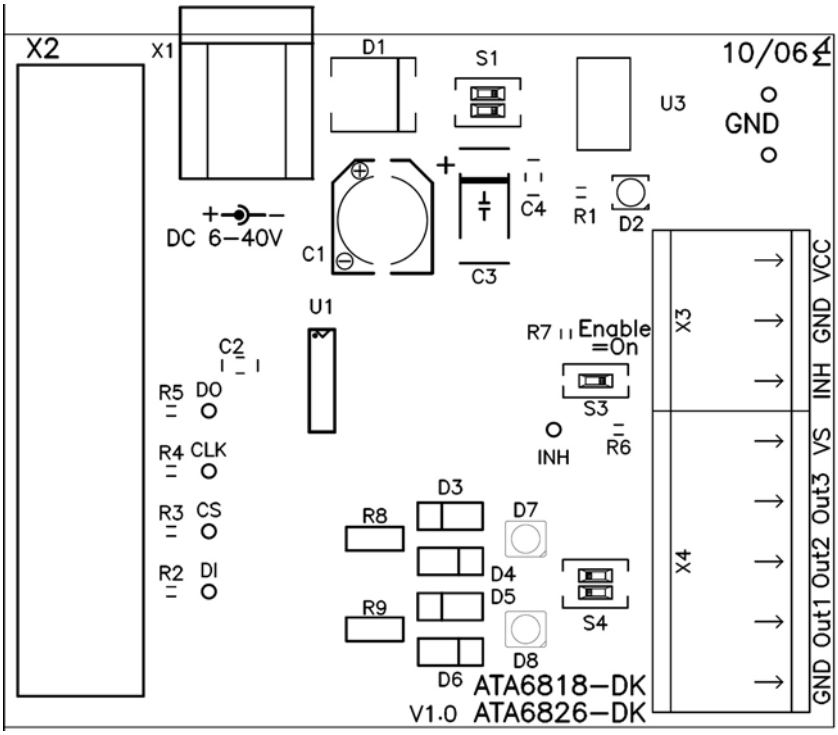


Figure 2-4. ATA6826-DK Design Kit, Basic Application Board Top Side, Top View

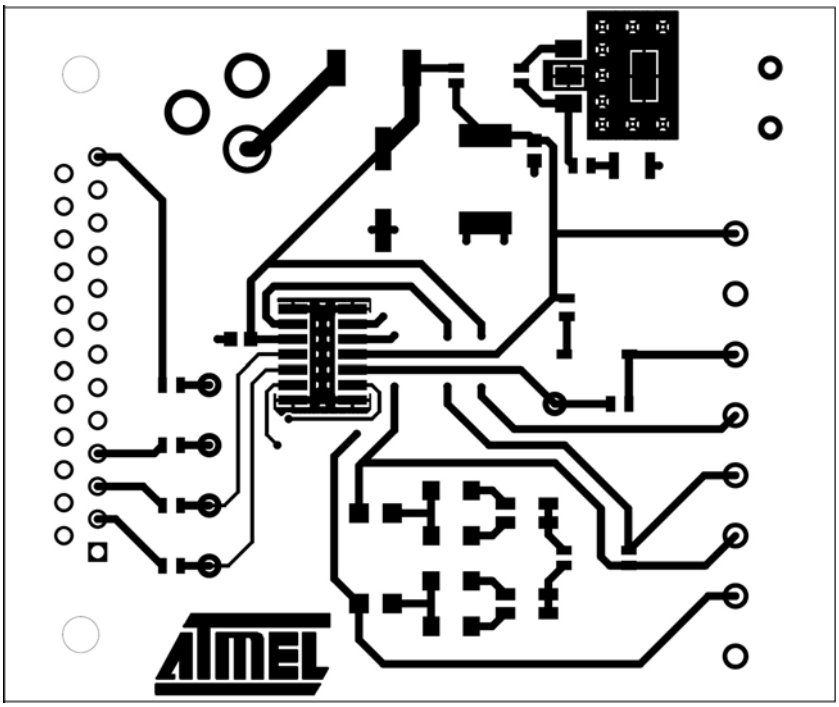
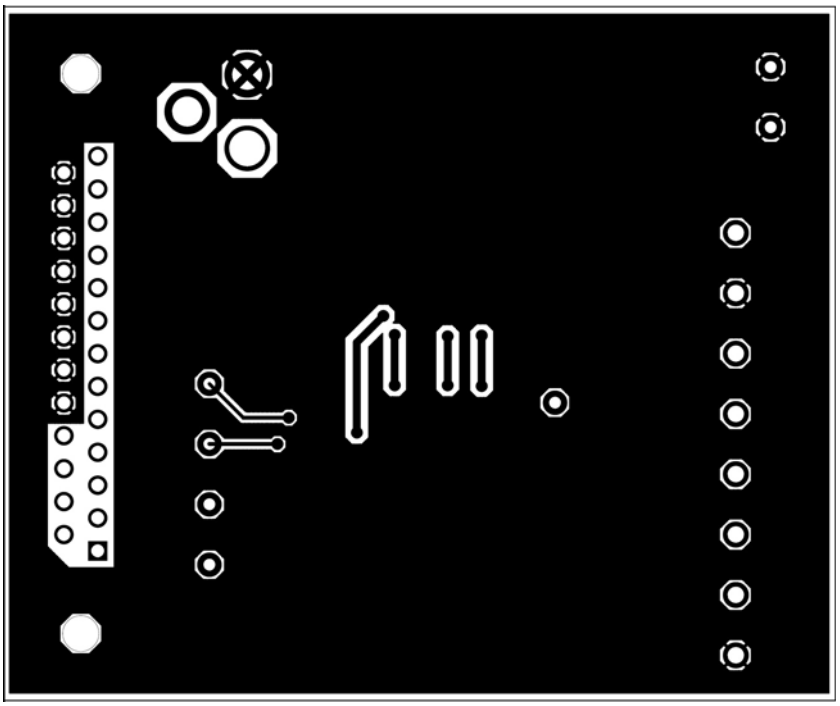


Figure 2-5. ATA6826-DK Design Kit, Basic Application Board; Bottom Side, Top View (as if PCB were Transparent)



3. Design Software

3.1 Installation

The ATA6826 design kit includes the ATA6826 software. The user can also download the latest revision of the software from the company's website, www.atmel.com. Start the installation process by executing the *.exe* file from the CD-ROM or website. The installation saves the ATA6826.exe file to a user-defined directory (for example, D:\Programs\ATA6826) and the system files to the appropriate system directories. Use the enclosed parallel cable to connect the PC's parallel port to the basic application board. Double-clicking on the ATA6826 icon (Figure 3-1) starts the software user interface.

Figure 3-1. Software Icon

3.2 Description

The ATA6826 design kit and the software user interface show the principal functions of the ATA6826, and enables the designer to directly create a design according to current needs. The software user interface includes all functions of the ATA6826 and provides convenient control of the ATA6826 via the basic application board. Use the adjust register (representing the microcontroller) on the left side of the software user interface to pre-adjust the required input data (refer to Figure 3-2 on page 7). Clicking the **Send Data** button shifts the pre-adjusted data (16 bits) into the input register of the serial peripheral interface. The output drivers are activated in accordance with the 16-bit input information. For more detailed information regarding the serial peripheral interface, please refer to the datasheet for ATA6826.

The **Send Data Loop** button causes an uninterrupted data transfer. Each output can be directly adjusted by switching the accessory bit.

The **Reset** button resets all bits to the default state. To quit the program, click the **End** button.

If available, up to three parallel interface ports (LPT1 to LPT3) can be selected to establish the proper connection. The software will detect the connected port.

By default, the input register OCS is set high, activating the overcurrent shutdown.

After power-on, all IC outputs are disabled. Before any data can be loaded into the IC, the enable switch on the board must be set to the ON position, or a high level has to be applied to the INH pin of the raw connector (IC-internal pull-down). As soon as the 1st dataword is sent, the IC reports the current condition in the output register.

3.3 Ordering Information

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Figure 3-2. Software User Interface

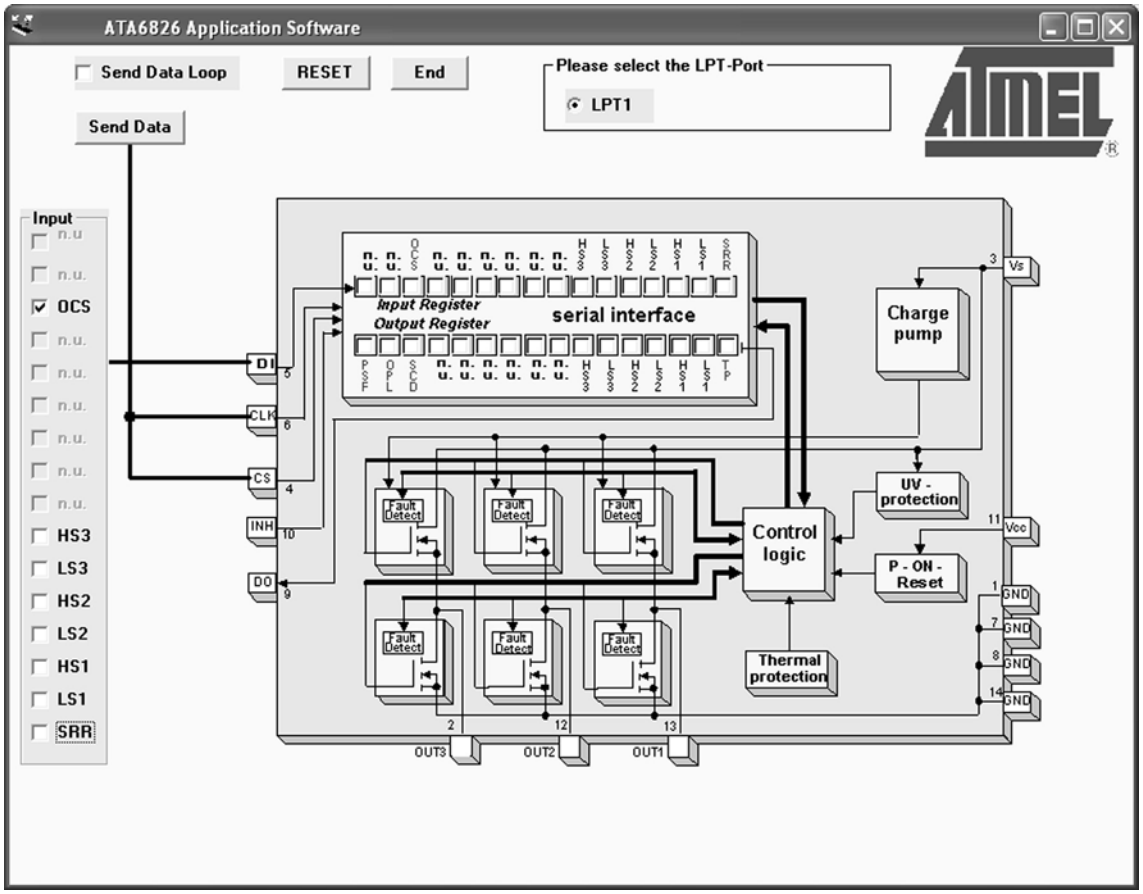


Table 3-1. Functions of the Serial Interface Register Bits

Bit	Input Register	Function
0	SRR	Status register reset (high = reset; the bits PSF, OPL and SCD in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	n.u.	Not used
8	n.u.	Not used
9	n.u.	Not used
10	n.u.	Not used
11	n.u.	Not used
12	n.u.	Not used
13	OCS	Overcurrent shutdown (high = overcurrent shutdown is active)
14	n.u.	Not used
15	n.u.	Not used

4. Applications

4.1 Demonstration Application

A typical demonstration application consists of a dual full-bridge arrangement with microcontroller and watchdog to control two DC motors. Such a dual H-bridge arrangement with common mid-rail allows for independent control of the motors for both directions of rotation. Enter the appropriate dataword according to Table 4-1 on page 9 to set the desired function.

When operating in a safety-critical environment, the use of a separate watchdog IC is recommended (for example, U5021M).

Unlike other circuits of the Atmel driver family, the open-load detection of ATA6826 is active for all output stages that are currently switched on. If the current through any high-side or low-side switch does not reach the open-load-detection threshold, an open-load is detected: in the output register the OPL bit is set to high. The OPL bit is buffered until reset by activation of the SRR bit.

The standby mode is activated by setting the hardware inhibit pin INH to 0V. In this case all outputs are switched to tri-state, and any data in the input and output registers is deleted. Switching pin 10 back to 5V initiates an internal power-on reset.

Short-circuit detection can easily be demonstrated by intentional false activation of the half-bridge components, for example, HS1 and LS1. This will cause the SCD bit in the output register to be set. Depending on the OCS bit, the affected outputs are switched off either by reaching overtemperature or by reaching overcurrent. The corresponding status bits in the output register are set to low. The SCD bit can be reset and the disabled outputs can be re-enabled by activating the SRR bit. Please note that such activation of SRR just initiates a reset pulse, not a permanent reset state.

The overtemperature pre-warning is visible at bit TP. While pin CS is set to low, the pre-warning information is visible in real time at pin DO, because TP is the first bit of the output register. Consequently, the TP bit is not buffered.

As all high-side drivers are internally connected to their low-side counterparts in order to form a half bridge, switching from HS active to LS active or vice versa with a single programming sequence could potentially imply some shoot-through current peak across both drivers during the switching operation. The intelligent internal timing of ATA6826 guarantees that such cross-over currents are avoided.

Undervoltage detection can be demonstrated with a variable power supply. As soon as the supply voltage V_{VS} falls below threshold, all activated loads are switched off and the PSF bit in the output register is set. If the voltage returns to the normal level, the outputs switch on again to their previous setting. The PSF bit latches the undervoltage occurance and needs to be reset by SRR activation in the input register.

If the IC is not used in the typical H-bridge arrangement, parallel operation of outputs is possible for more powerful applications. Two output stages at a time can be paralleled to achieve currents up to 2A.

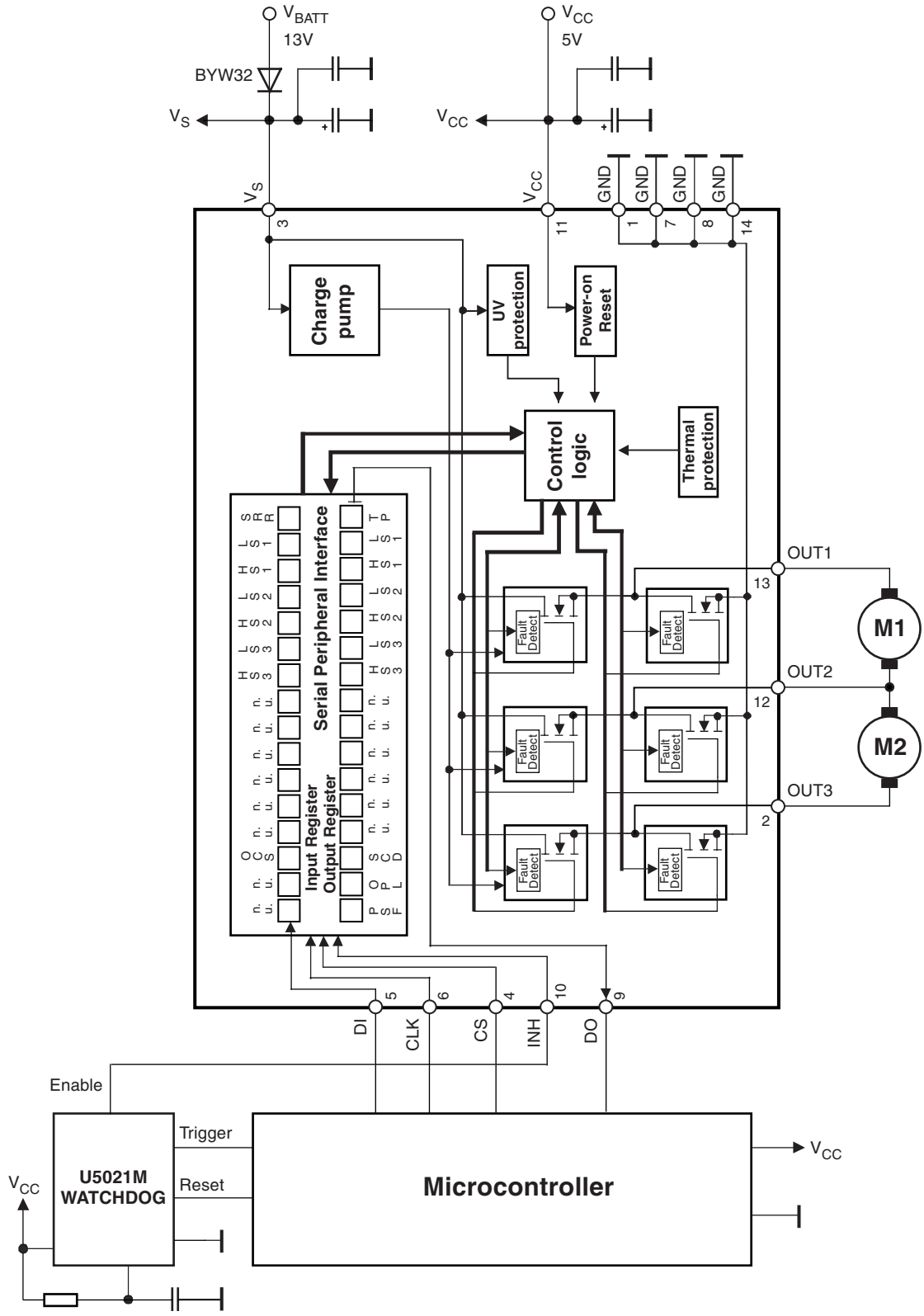
In any case, the IC's maximum power dissipation has to be considered. Excellent thermal contact to an on-board cooling area is obligatory for powerful applications.

Table 4-1. Configuration Table of the Required Datawords to Set Certain Functions of the Application Circuit (See Figure 4-1 on page 10)

	Bit 13 (OCS)	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
M1 Forward	x			H			H	
M1 Reverse	x				H	H		
M2 Forward	x	H			H			
M2 Reverse	x		H	H				

Note: x = do not care for this demonstration; if set to high: overcurrent shutdown is active

Figure 4-1. Application With Microcontroller and Watchdog



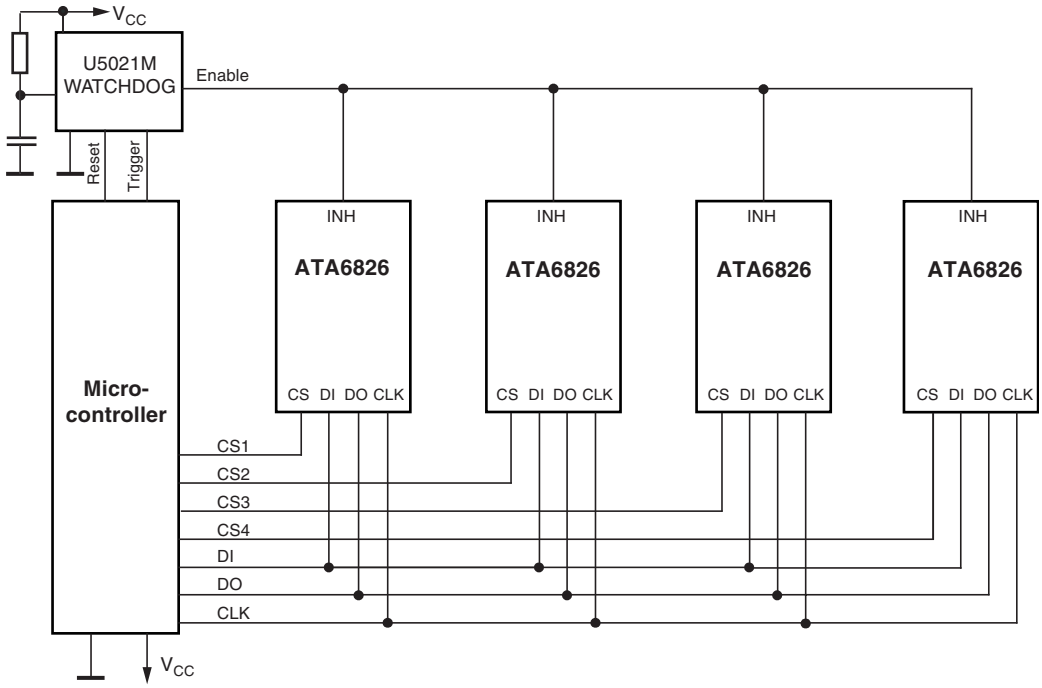
4.2 Parallel Operation of Several ATA6826s

In applications with a high number of loads, parallel operation of the ATA6826 via the microcontroller is possible.

Separate control of the ATA6826's serial peripheral interface is provided by chip select pins CS1 to CS4 (for the function of the serial peripheral interface, please refer to the datasheet).

For simultaneous operation of the serial peripheral interfaces (that is, CS1 through CS4 are active at the same time), each of the data outputs (DO) needs to communicate with a dedicated microcontroller input pin.

Figure 4-2. Parallel Operation With Microcontroller and Watchdog



4.3 Daisy Chaining of Several ATA6826s

In applications with a larger number of loads, there's a second option for connecting several ATA6826s to the microcontroller. The daisy-chain arrangement requires only one CS line; the data signal is handed over step-by-step from one ATA6826 to the next as long as the CS signal stays low. It should be evident that this advantage is traded for slower reaction times, as several programming cycles are needed to load the desired setting into each ATA6826.

The DI pin of the first IC acts as input for all ICs while the DO of the last IC represents the output for the whole chain. The data word intended for the last IC has to be put in first, followed by the word for the previous IC, and so on. Only *n* shifts total will be needed for a number *n* of ICs, as any DI information is transferred immediately to the output register.

Table 4-2 clarifies the above method: the n = 3 data words A, B, C are shifted into the driver ICs numbers 1, 2 and 3, while the initial contents of the registers are termed as X to Z. It can be seen that the desired status of the input registers DI is reached after n = 3 shift operations.

Figure 4-3. Daisy Chain Operation With Microcontroller and Watchdog

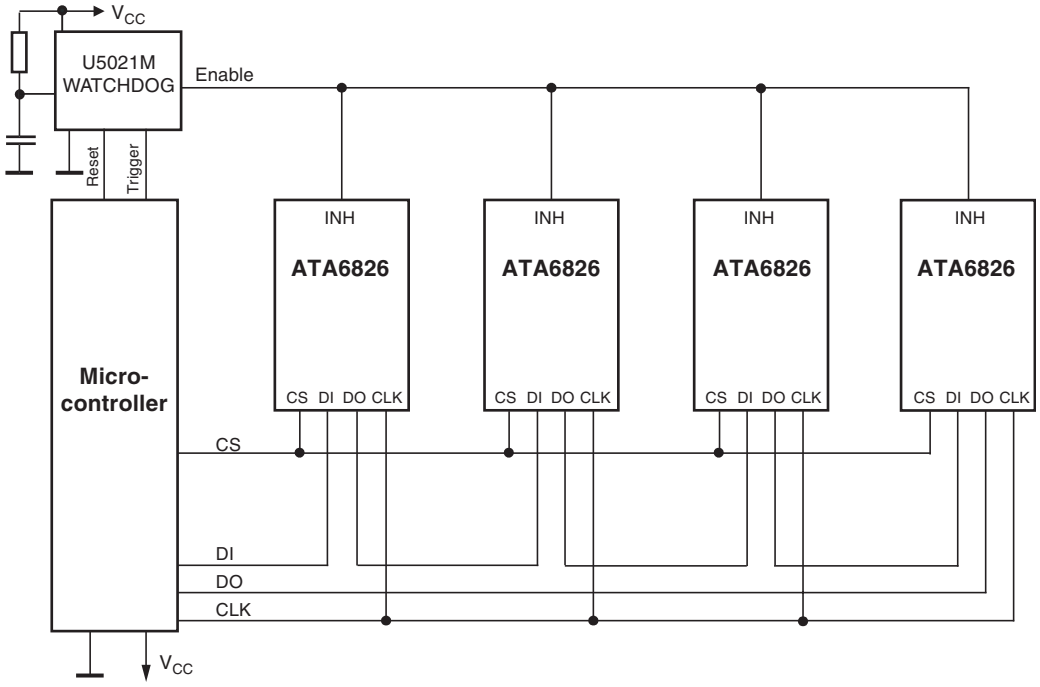


Table 4-2. Principal Method of Shifting Data Words Through Daisy-chained ICs

I/O Cycle	0			1			2		
IC number	1	2	3	1	2	3	1	2	3
DI	A			B	A		C	B	A
DO	Z	Y	X	A	Z	Y	B	A	Z

5. Thermal Considerations

5.1 Cooling Area Design

The IC should be connected to a cooling area onboard. All thermal pins (4 GND pins) are directly connected to the cooling area. Figure 5-1 shows the cooling arrangement with the SO14 housing of the ATA6826. The cooling area extension should be increased or decreased according to the required power dissipation (see Figure 5-2). The cooling area extension is calculated as follows: $2 \times L^2$ = cooling area extension [mm^2].

The effect of the cooling area on the PCB can be further improved if the bottom side of the PCB is ground-plated and thermal vias are placed along the cooling area. A via diameter of 0.3 mm to 0.4 mm and a spacing of 1 mm to 1.5 mm has proven to be most suitable. Some care should be taken of the copper area's planarity; it should especially be avoided that any solder bumps arise at the thermal vias.

Figure 5-1. Recommended Cooling Area Extension

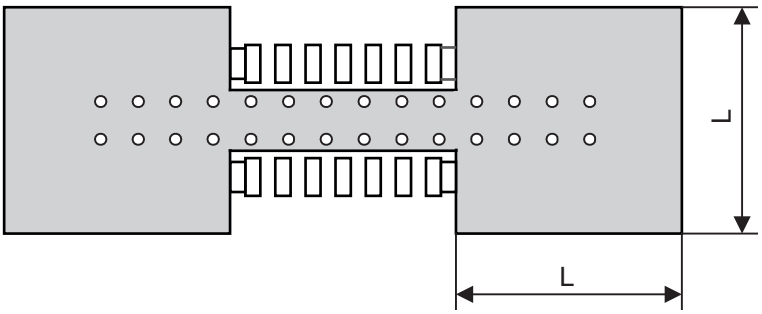
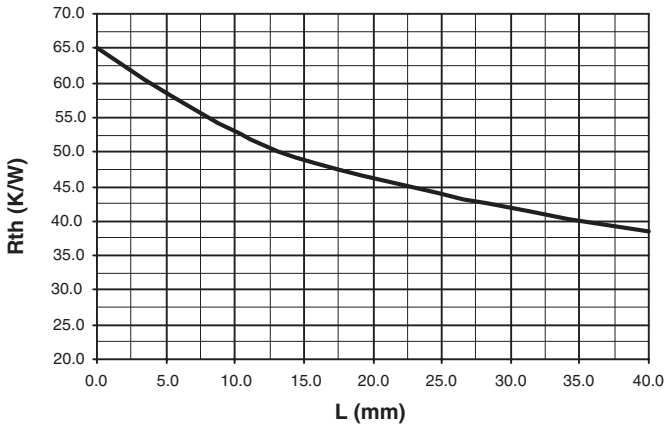


Figure 5-2. Thermal Resistance Versus Adapted Cooling-area Size on Board



6. Overload Considerations

6.1 Driver Output Shorted to V_S

During normal operation, ATA6826 is protected against short circuits by an overcurrent limitation. However, some attention has to be paid to certain abnormal operating conditions that might occur in practice. In particular, we have to consider the case of an output shorted to V_{out} while the IC is not connected to supply voltage V_S. Under these conditions, an unwanted backward current flows from the shorted output via the voltage supply pin to the capacitor C1. Figure 6-1 illustrates the situation.

The backward current I_b flows from OUTx via the HSx output stage to the V_S pin until the capacitor C1 is charged to V_{out} (minus the drop across the diode). Its value is strongly influenced by the capacitance of C1, but the quality of C1 (ESR) and any parasitic resistance will also have an impact. The recommended range for C1 is 22 µF to 100 µF. As stated in the datasheet, the maximum reverse current is 17A for a duration of 150 µs. The graph illustrated in Figure 6-2 shows the typical voltage and reverse current gradients for a capacitor value of 100 µF.

Figure 6-1. Current Flow in the Case of HSx Shorted to V_{out}

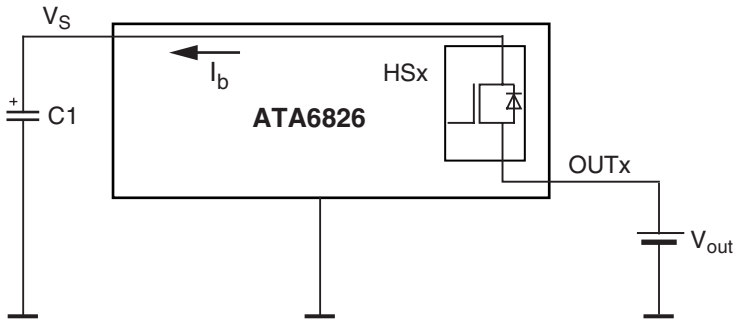
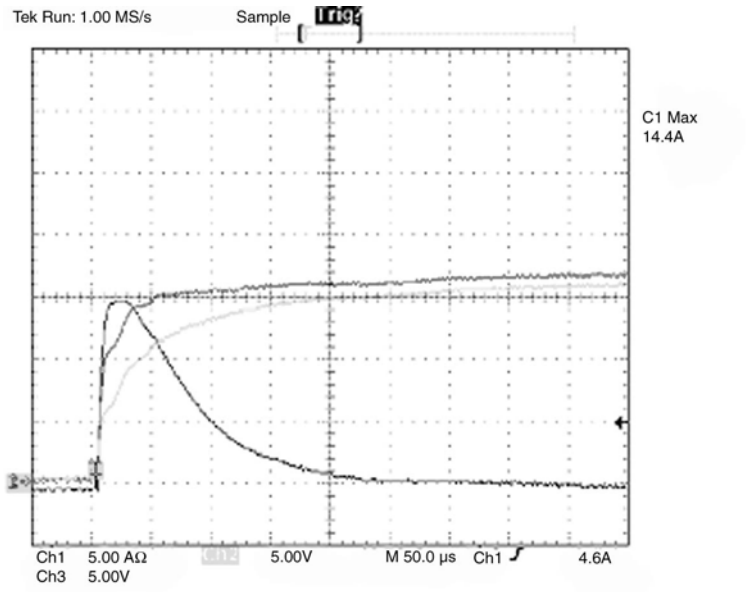


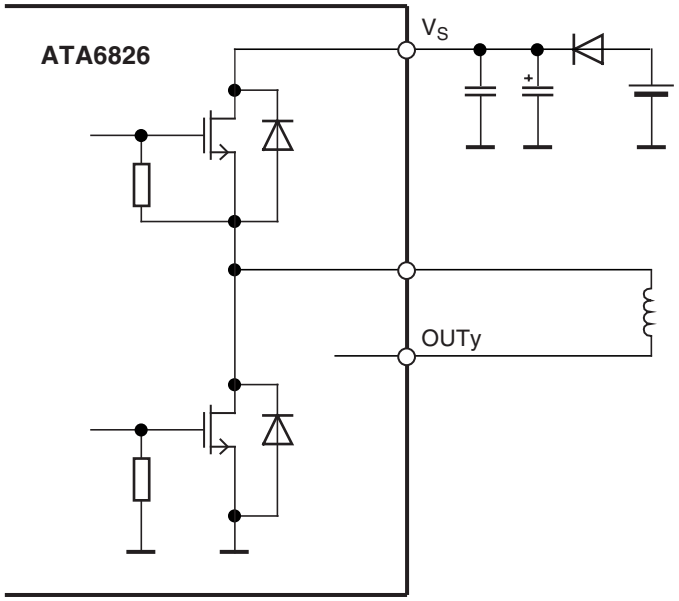
Figure 6-2. Current and Voltage Gradients
for V_{out} = 16V, C1 = 100 µF; Channel 1 = I_b, Channel 2 = V_{Vs}, Channel 3 = V_{out}



6.2 Inductive Shutdown

Any driver IC faces a challenge when an inductive load is connected to its outputs, as the energy stored in the inductance leads to a voltage peak when the load is switched off. An inductive load connected to the low-side driver outputs causes a voltage peak with positive polarity, while for the high-side outputs such peak is negative. In order to prevent any damage to the IC's output stages, some protective means have to be implemented. Figure 6-3 illustrates the principal protection circuit of the outputs.

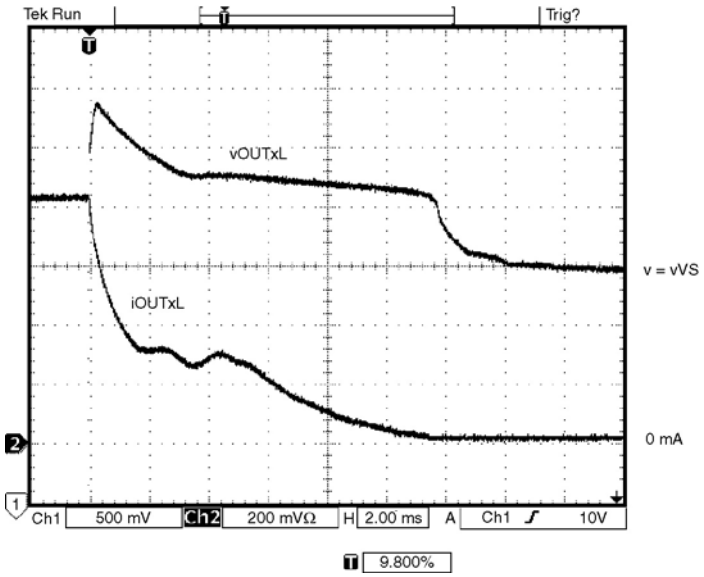
Figure 6-3. Principal Clamping Structure at a Driver Stage



The clamping structures at the output stages limit the voltage peak and provide a path for the current after switching off. The maximum inductive shutdown energy for ATA6826 is specified as 15 mJ. This value applies for both low-side and high-side outputs. The energy W_L stored in the inductor L during the switched-on state can be calculated using the following formula:

$$w_L = \frac{L \times I_L^2}{2}$$

Figure 6-4. Inductive Pulse at Low-side Output;
Channel 1: Gradient of V_{out} (10V offset), Channel 4: Gradient of I_{out} (200 mA/Div.), Pulse Energy: W_L = 5 mJ



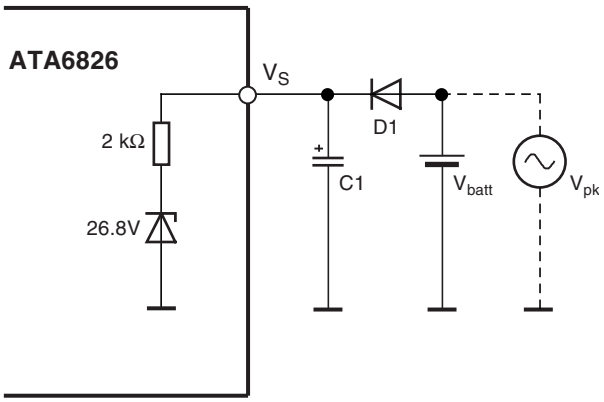
6.3 Discharger Circuit

Many typical applications use an inverse-polarity protection diode, such as D1 in Figure 6-5, in the power-supply feed to prevent any damage if V_S is applied with the wrong polarity. Despite the popularity of this method, it involves a certain danger.

During inhibit mode, the IC consumes only an extremely low current I_{VS}, such as 20 µA at maximum. Any peaks on the supply voltage (V_{pk} in Figure 6-5) will gradually charge the blocking capacitor (C9 in Figure 6-5). D1 prevents the capacitor from discharging via the power supply; due to the extremely small quiescent current, discharging via the IC can also be neglected.

This means that during long periods in inhibit mode, the IC's supply voltage could increase continuously until the maximum supply voltage limit of 40V is exceeded, damaging the IC. ATA6826 therefore features a discharger circuit that prevents such unwanted effects. If V_S exceeds a threshold value of approximately 27V, the blocking capacitor is discharged via an integrated resistor until V_S again falls below the threshold.

Figure 6-5. Functional Principle of the Discharger Circuit



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