QLx4270-DP

DisplayPort Lane Extender

FN6972
Rev 2.00
March 3, 2010

The QLx4270-DP is a settable quad receive-side equalizer with extended functionality for DisplayPort applications. The QLx4270-DP compensates for the frequency dependent attenuation of copper cables, allowing operation on ultra-thin 40AWG cable.

The small form factor, highly-integrated quad design is ideal for high-density data transmission applications including active copper cable assemblies.

Operating on a single 1.2V power supply, the QLx4270-DP enables per channel throughputs of up to 2.7Gb/s. The QLx4270-DP uses current mode logic (CML) inputs/outputs and is packaged in a 4mmx7mm 46 lead QFN.

Features

- Supports data rates up to 2.7Gb/s per lane
- Low power (78mW per channel)
- Low latency (<500ps)
- Four equalizers in a 4mmx7mm QFN package for straight route-through architecture and simplified routing
- Each equalizer boost is independently pin selectable and programmable
- 1.2V supply voltage

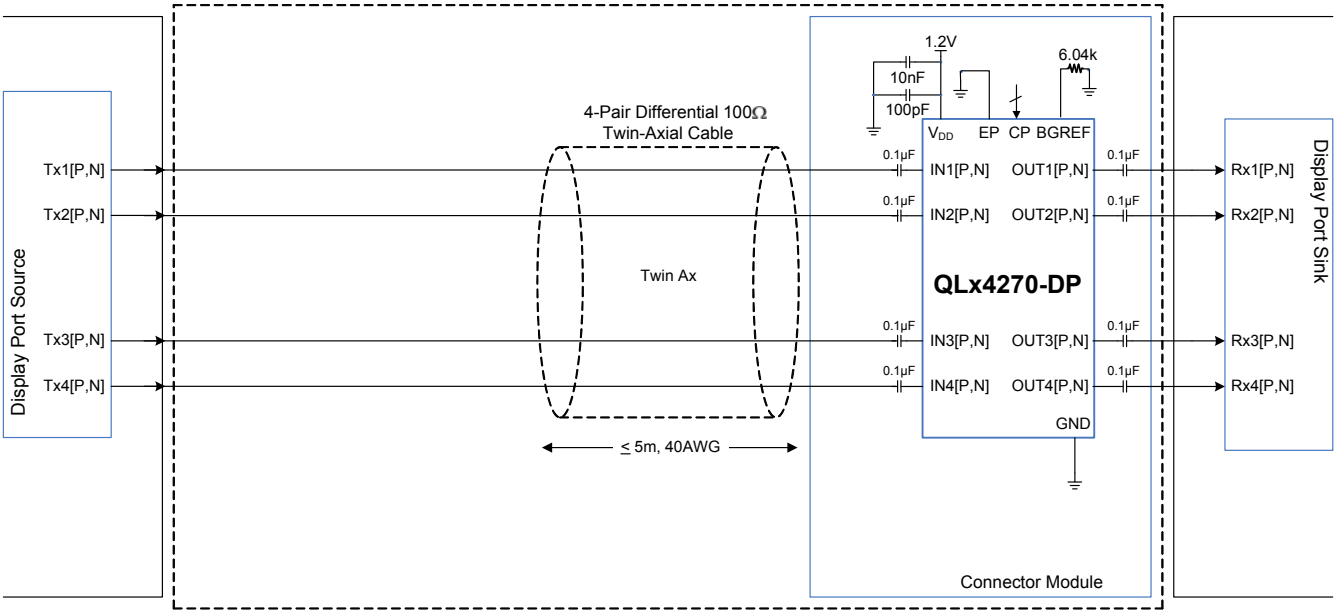
Applications

- DisplayPort (VESA DisplayPort Standard v1.1a)
- DisplayPort adaptors and repeaters

Benefits

- Thinner gauge cable
- Extends cable reach greater than 5x
- Improved BER

Typical Application Circuit



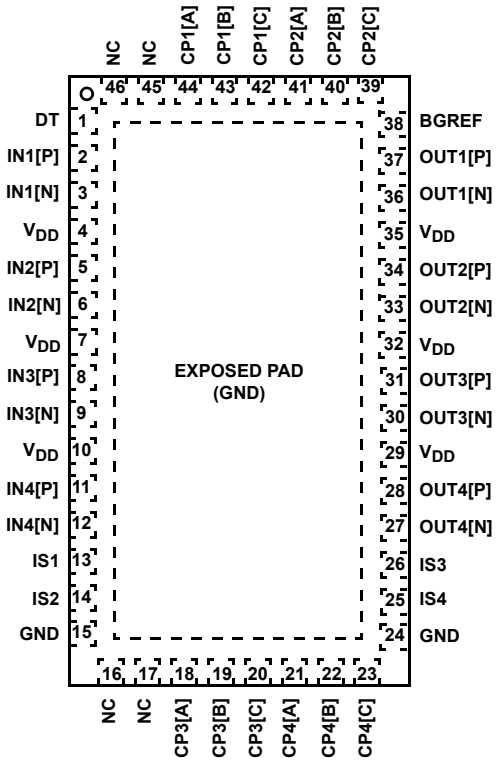
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
QLX4270RIQT7	QLX4270RIQ	0 to +70	46 Ld QFN 7” Prod. Tape & Reel; Qty 1,000	L46.4x7
QLX4270RIQSR	QLX4270RIQ	0 to +70	46 Ld QFN 7” Sample Reel; Qty 100	L46.4x7

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration

QLx4270-DP
(46 LD QFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
DT	1	Detection Threshold. Reference DC CURRENT threshold for input signal power detection. Data output Out[k] is muted when the power of the equalized version of In[k] falls below the threshold. Tie to ground to disable electrical idle preservation and always enable the limiting amplifier.
IN1[P,N]	2, 3	Equalizer 1 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
V_{DD}	4, 7, 10, 29, 32, 35	Power supply. 1.2V supply voltage. The use of parallel 100pF and 10nF decoupling capacitors to ground is recommended for each of these pins for broad high-frequency noise suppression.
IN2[P,N]	5, 6	Equalizer 2 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
IN3[P,N]	8, 9	Equalizer 3 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
IN4[P,N]	11, 12	Equalizer 4 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
IS1	13	Impedance Select 1. CMOS logic input. When the voltage on this pin is LOW, the single-ended input impedance of In1P and In1N each go above 200kΩ and powers down the channel. This can be used to disable some of the channels in case the DisplayPort application has less than four links, in order to save power consumption. Otherwise, connect to VDD to hold the input impedance at 50Ω.
IS2	14	Impedance Select 2. CMOS logic input. When the voltage on this pin is LOW, the single-ended input impedance of In1P and In1N each go above 200kΩ and powers down the channel. This can be used to disable some of the channels in case the DisplayPort application has less than four links, in order to save power consumption. Otherwise, connect to VDD to hold the input impedance at 50Ω.
GND	15, 24	Ground
NC	16, 17, 45, 46	No-Connect
CP3[A,B,C]	18, 19, 20	Control pins for setting equalizer 3. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
CP4[A,B,C]	21, 22, 23	Control pins for setting equalizer 4. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
IS4	25	Impedance Select 4. CMOS logic input. When the voltage on this pin is LOW, the single-ended input impedance of In1P and In1N each go above 200kΩ and powers down the channel. This can be used to disable some of the channels in case the DisplayPort application has less than four links, in order to save power consumption. Otherwise, connect to VDD to hold the input impedance at 50Ω.
IS3	26	Impedance Select 3. CMOS logic input. When the voltage on this pin is LOW, the single-ended input impedance of In1P and In1N each go above 200kΩ and powers down the channel. This can be used to disable some of the channels in case the DisplayPort application has less than four links, in order to save power consumption. Otherwise, connect to VDD to hold the input impedance at 50Ω.
OUT4[N,P]	27, 28	Equalizer 4 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
OUT3[N,P]	30, 31	Equalizer 3 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
OUT2[N,P]	33, 34	Equalizer 2 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
OUT1[N,P]	36, 37	Equalizer 1 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
BGREF	38	External bandgap reference resistor. Recommended value of 6.04kΩ ±1%.
CP2[C,B,A]	39, 40, 41	Control pins for setting equalizer 2. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
CP1[C,B,A]	42, 43, 44	Control pins for setting equalizer 1. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
Exposed Pad	-	Exposed ground pad. For proper electrical and thermal performance, this pad should be connected to the PCB ground plane.

Absolute Maximum Ratings

Supply Voltage (V_{DD} to GND) . . . . . -0.3V to 1.3V
Voltage at All Input Pins . . . . . -0.3V to V_{DD} + 0.3V
ESD Rating at all pins . . . . . 2kV (HBM)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
46 Ld QFN (Notes 1, 2)	32	2.3

Operating Ambient Temperature Range . . . . . 0°C to +70°C
Storage Ambient Temperature Range . . . . -55°C to +150°C
Maximum Junction Temperature . . . . . +125°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Operating Conditions

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		1.1	1.2	1.3	V
Operating Ambient Temperature	T_A		0	25	70	°C
Bit Rate		NRZ data applied to any channel	1.5		2.7	Gb/s

Control Pin Characteristics

V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 800mV$_{P-P}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
'LOW' Resistance State		CP[k]	0		1	kΩ	3
'MID' Resistance State		CP[k]	22.5	25	27.5	kΩ	3
'HIGH' Resistance State		CP[k]	500		∞	kΩ	3
Input Current		Current draw on digital pin, i.e., CP[k]		30	100	µA	

NOTE:

3. If four CP pins are tied together, the resistance values in this table should be divided by four.

Electrical Characteristics

V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 800mV$_{P-P}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}			260		mA	
IC Input Amplitude Range	V_{IN}	Measured differentially at data source before encountering channel loss	340		1380	mV$_{P-P}$	4
DC Differential Input Resistance		Measured on input channel IN[k]	80	100	120	Ω	
DC Single-Ended Input Resistance		Measured on input channel IN[k]P or IN[k]N	40	50	60	Ω	
Input Return Loss (Differential)	$S_{DD}11$	50MHz to 1.35GHz	9			dB	5
Output Amplitude Range	V_{OUT}	Measured differentially at OUT[k]P and OUT[k]N with 50Ω load on both output pins	150	550	650	mV$_{P-P}$	
Differential Output Impedance		Measured on OUT[k]	80	105	120	Ω	
Output Return Loss (Differential)	$S_{DD}22$	50MHz to 1.35GHz	10			dB	5
Output Return Loss (Common Mode)	$S_{CC}22$	50MHz to 1.35GHz	5			dB	5

Electrical Characteristics V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 800mV_{P-P}, unless otherwise noted. **(Continued)**

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Output Return Loss (Com. to Diff. Conversion)	$S_{DC}22$	50MHz to 1.35GHz	20			dB	5
Output Residual Jitter		2.7Gb/s; Up to 2m 38AWG standard twin-axial cable (11.5dB loss)		0.15	0.2	UI	4, 6, 7
Output Transition Time	t_r, t_f	20% to 80%	30	60	100	ps	8
Lane-to-Lane Skew					50	ps	
Propagation Delay		From IN[k] to OUT[k]			500	ps	

NOTES:

4. After channel loss, differential amplitudes at QLx4270-DP inputs must meet the input voltage range specified in "Absolute Maximum Ratings" on page 4.
5. Temperature = +25°C, V_{DD} = 1.2V.
6. Output residual jitter is the difference between the total jitter at the lane extender output and the total jitter of the transmitted signal (as measured at the input to the channel). Total jitter (TJ) is DJ_{pp} + 14.1 x RJ_{RMS}.
7. Measured using a PRBS 2^7-1 pattern. Deterministic jitter at the input to the lane extender is due to frequency-dependent, media-induced loss only.
8. Rise and fall times measured using a 1GHz clock with a 20ps edge rate.

Control Pin Boost Setting

The voltages at the CP pins are used to determine the boost level of each channel of QLx4270-DP. For each of the four channels, k, the [A], [B], and [C] control pins (CP[k]) are associated with a 3-bit non binary word. While [A] can take one of two values, 'LOW' or 'HIGH', [B] and [C] can take one of three different values: 'LOW', 'MIDDLE', or 'HIGH'. This is achieved by changing the value of a resistor connected between VDD and the CP pin, which is internally pulled low with a 25kΩ resistor. Thus, a 'HIGH' state is achieved by using a 0Ω resistor, 'MIDDLE' is achieved with a 25kΩ resistor, and 'LOW' is achieved with an open resistance. Table 1 defines the mapping from the 3-bit CP word to the 18 out of 32 possible levels available via the serial interface on the Evaluation Board kit.

TABLE 1. MAPPING BETWEEN CP-SETTING RESISTOR AND QLx4270-DP BOOST LEVELS

RESISTANCE BETWEEN CP PIN AND V_{DD}			SERIAL BOOST LEVEL
CP[A]	CP[B]	CP[C]	
Open	Open	Open	0
Open	Open	25kΩ	2
Open	Open	0Ω	4
Open	25kΩ	Open	6
Open	25kΩ	25kΩ	8
Open	25kΩ	0Ω	10
Open	0Ω	Open	12
Open	0Ω	25kΩ	14
Open	0Ω	0Ω	15
0Ω	Open	Open	16

TABLE 1. MAPPING BETWEEN CP-SETTING RESISTOR AND QLx4270-DP BOOST LEVELS (Continued)

RESISTANCE BETWEEN CP PIN AND V_{DD}			SERIAL BOOST LEVEL
CP[A]	CP[B]	CP[C]	
0Ω	Open	25kΩ	17
0Ω	Open	0Ω	19
0Ω	25kΩ	Open	21
0Ω	25kΩ	25kΩ	23
0Ω	25kΩ	0Ω	24
0Ω	0Ω	Open	26
0Ω	0Ω	25kΩ	28
0Ω	0Ω	0Ω	31

If all four channels are to use the same boost level, then a minimum number of board resistors can be realized by tying together like CP[k][A,B,C] pins across all channels k. For instance, all four CP[k][A] pins can be tied to the same resistor running to VDD. Consequently, only three resistors are needed to control the boost of all four channels. If the CP Pins are tied together and the 25kΩ is used, the value changes to a 3.125kΩ resistor because the 25kΩ is divided by 4.

Channel Power-Down

The IS[k] pin powers down the equalizer channel when pulled low. This feature allows individually to power down unused channels and to minimize power consumption. Example: for DisplayPort applications with 1 or 2 links, the unused channels may be powered down to save power. The current draw for a channel is reduced from 50mA to 3.8mA when powered down.

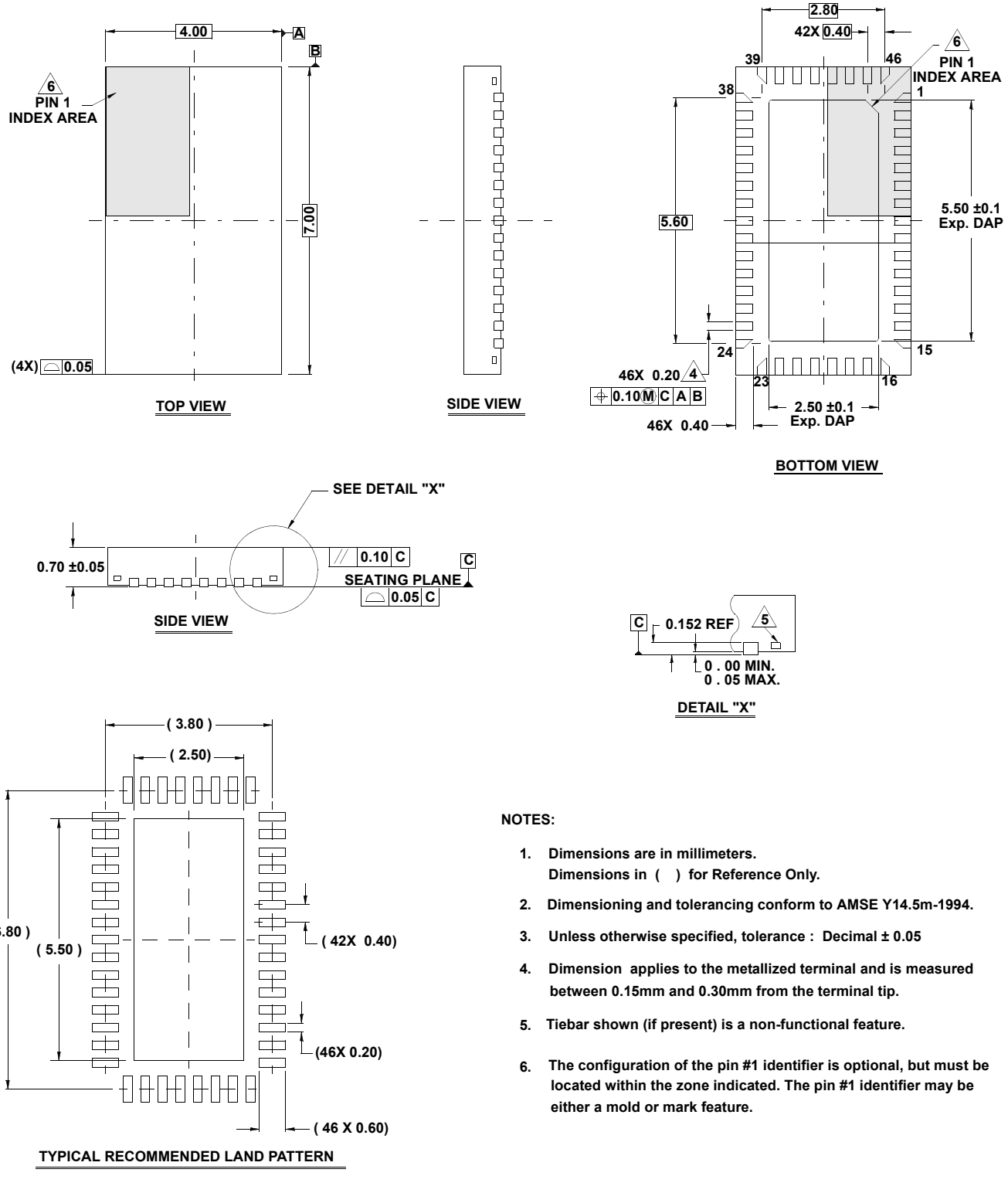
About Q:Active®

Historically, cable manufacturers have relied on thick wire gauge cables to deliver Deep Color images to the monitors and projectors. However, these cables are bulky, unwieldy and esthetically unappealing. To address this, Intersil has developed its groundbreaking Q:ACTIVE® product line. By integrating its analog ICs inside DisplayPort cables, Intersil is able to achieve unsurpassed improvements in cable gauges, reach and transmitted image quality.

Package Outline Drawing

L46.4x7

46 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE (TQFN)
Rev 0, 9/09



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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