36 Outputs VFD Controller/Driver

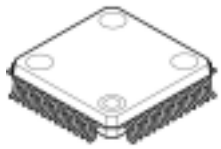
■ GENERAL DESCRIPTION

The **NJU3427** is a 36-output VFD (Vacuum Fluorescent Display) controller/driver.

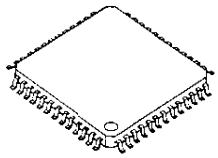
The **NJU3427** consists of high-voltage driving circuit, Timing/ Segment driver select circuit, display data RAM (DDRAM), address counter, instruction register, reset circuit serial interface and oscillator.

The direct control from the MPU and high voltage drivers make the **NJU3427** well suited for various VFD displays

■ Package



NJU3427FA2

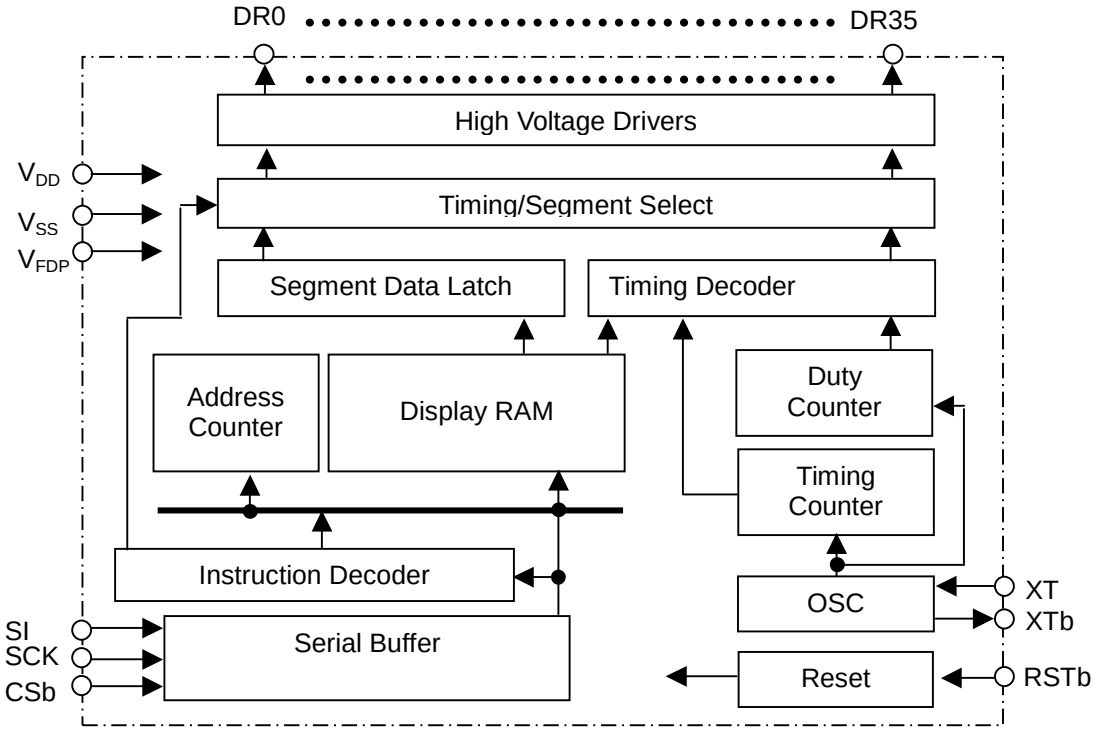


NJU3427FH2

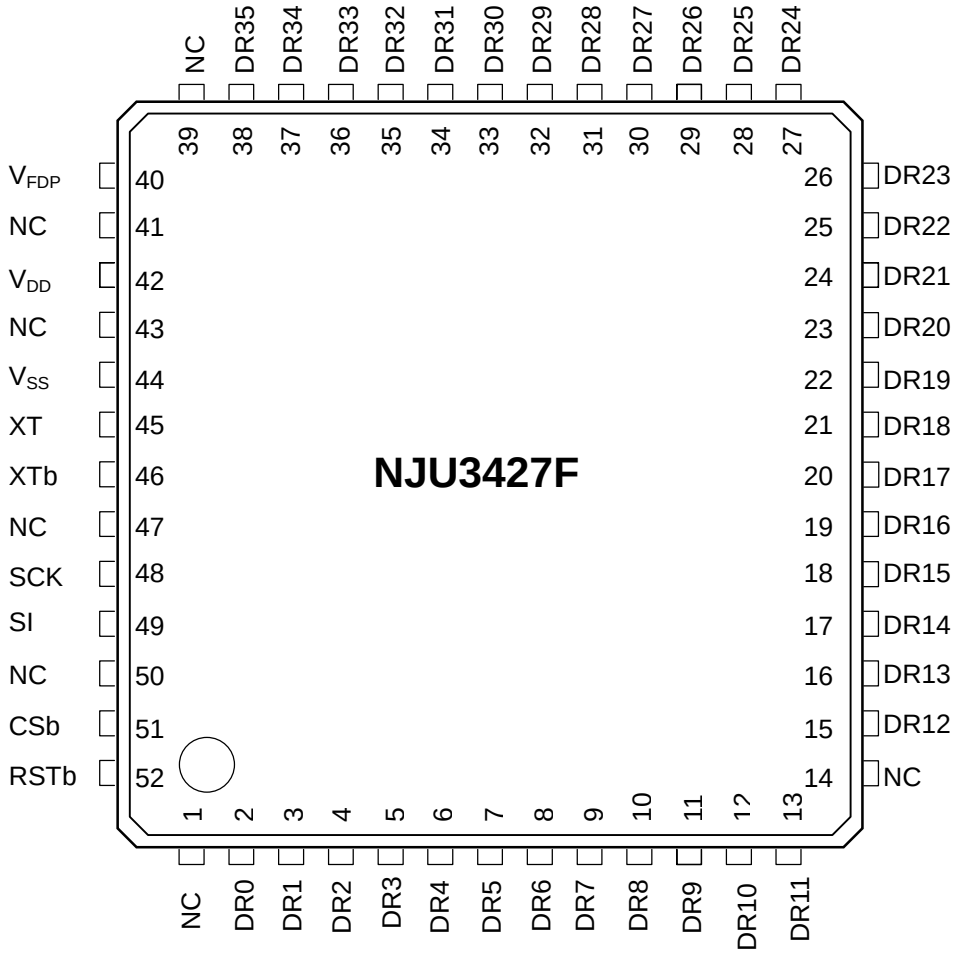
■ FEATURES

- Display Capability — From 20-Seg x16-Timing to 28-Seg x 4-Timing
  - DR0 Pin (I_{SO1}) — 20mA(V_{DD}=5V)
  - DR1~DR35 Pins (I_{SO2}) — 10mA(V_{DD}=5V)
- Segment and Timing Driver Configure — 4 patterns
- High VFD Driving Voltage — $|V_{DD}-V_{FDP}|\leq 40V$
- Programmable Display Duty Ratio — 1/4, 1/8, 1/12 or 1/16
- Programmable Timing Signal Duty Ratio — 2/16, 4/16, 6/16, 8/16, 10/16, 12/16, 14/16, 15/16
- Display ON/OFF
- Display Data RAM — 47x8 bits
- CR Oscillator — External CR and capable of clock input from outside
- Serial Data Transfer — Clock frequency: 2MHz Max.
- Logic Power Supply — 3.0V / 5.0V
- C-MOS
- Package — QFP52-A2, QFP52-H2

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

No.	Symbol	Function
42	V_{DD}	Logic power supply 3.0V / 5.0V
44	V_{SS}	GND V_{SS}=0V
40	V_{FDP}	Power supply for VFD driving
2 ~ 13, 15 ~ 38	DR0~ DR35	Driving signal output The configure of the Segment and Timing drivers is determined by the instruction, refer to (2) Instruction Register.
52	RSTb	Reset If RSTb="L", reset occurs, but data on DDRAM not changing.
51	CSb	Chip select If CSb="L", data transmission is enabled.
48	SCK	Serial clock
49	SI	Serial data input (8-bit/one word)
45, 46	XT, XTb	Connecting external capacitor and resistor, or input clock via this pin If using external clock, input clock signal via XT and keep XTb open.
1, 14, 39, 41, 43, 47, 50	NC	No connect Usually open.

■ FUNCTION DESCRIPTION

(1) Address Counter

The address counter specifies the RAM address, and the display data from CPU is written to the specified address.

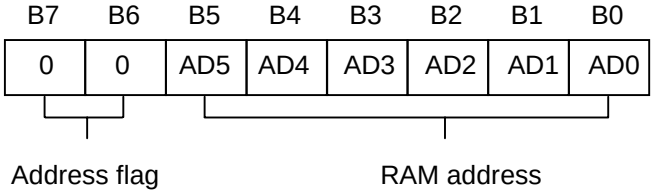
If the upper 2 bits (B7, B6) of the 1st word are “0,0”, the rest 6 bits (B5~B0) will be interpreted as RAM address. The 2nd word will be interpreted as display data and saved on the RAM which address is specified by the B5~B0 of the 1st data.

Once the RAM address is determined by the 1st data, the address counter will automatically increase (+1) for every following word. So there is no need to specify the address for every word for a consecutive data transfer.

During display data writing, even there is unused or not-existing RAM area, be sure to input 8-bit serial data. The data allocated to the above mentioned area is invalid.

The RAM address range varies with programmable duty ratios. For 1/4 duty, the address range is from”00H~0FH”. For 1/8 duty, the range is from “00H~1FH”. For 1/12 duty, the range is from “00H~23H”. For 1/16 duty, the range is from “00H~2FH”. When automatically increased address excess the address range and display data is still transferred from CPU, the address counter will return to “00H” and count up again.

Address Data



DDRAM MAP1

● 1/16 duty (T=16, S=20)

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
T0	00_H							
T1	03_H							
T2	06_H							
T3	09_H							
T4	$0C_H$							
T5	$0F_H$							
T6	12_H							
T7	15_H							
T8	18_H							
T9	$1B_H$							
T10	$1E_H$							
T11	21_H							
T12	24_H							
T13	27_H							
T14	$2A_H$							
T15	$2D_H$							
	S0	S1	S2	S3	S4	S5	S6	S7

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
01_H								
04_H								
07_H								
$0A_H$								
$0D_H$								
10_H								
13_H								
16_H								
19_H								
$1C_H$								
$1F_H$								
22_H								
25_H								
28_H								
$2B_H$								
$2E_H$								
	S8	S9	S10	S11	S12	S13	S14	S15

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
02_H								
05_H								
08_H								
$0B_H$								
$0E_H$								
11_H								
14_H								
17_H								
$1A_H$								
$1D_H$								
20_H								
23_H								
26_H								
29_H								
$2C_H$								
$2F_H$								
	S16	S17	S18	S19	S20	S21	S22	S23

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
	S24	S25	S26	S27				

● 1/12 duty (T=12, S=24)

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
T0	00_H							
T1	03_H							
T2	06_H							
T3	09_H							
T4	$0C_H$							
T5	$0F_H$							
T6	12_H							
T7	15_H							
T8	18_H							
T9	$1B_H$							
T10	$1E_H$							
T11	21_H							
T12	–							
T13	–							
T14	–							
T15	–							
	S0	S1	S2	S3	S4	S5	S6	S7

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
01_H								
04_H								
07_H								
$0A_H$								
$0D_H$								
10_H								
13_H								
16_H								
19_H								
$1C_H$								
$1F_H$								
22_H								
–								
–								
–								
–								
	S8	S9	S10	S11	S12	S13	S14	S15

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
02_H								
05_H								
08_H								
$0B_H$								
$0E_H$								
11_H								
14_H								
17_H								
$1A_H$								
$1D_H$								
20_H								
23_H								
–								
–								
–								
–								
	S16	S17	S18	S19	S20	S21	S22	S23

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
–								
	S24	S25	S26	S27				

Not-using RAM area

Not-existing RAM area

RAM MAP 2

- 1/8 duty (T=8, S=28)

	RAM address	D0	D1	D2	D3	D4	D5	D6	D7
T0	00_H								
T1	04_H								
T2	08_H								
T3	$0C_H$								
T4	10_H								
T5	14_H								
T6	18_H								
T7	$1C_H$								
T8	–								
T9	–								
T10	–								
T11	–								
T12	–								
T13	–								
T14	–								
T15	–								
		S0	S1	S2	S3	S4	S5	S6	S7

	RAM address	D0	D1	D2	D3	D4	D5	D6	D7
T0	01_H								
T1	05_H								
T2	09_H								
T3	$0D_H$								
T4	11_H								
T5	15_H								
T6	19_H								
T7	$1D_H$								
T8	–								
T9	–								
T10	–								
T11	–								
T12	–								
T13	–								
T14	–								
T15	–								
		S8	S9	S10	S11	S12	S13	S14	S15

	RAM address	D0	D1	D2	D3	D4	D5	D6	D7
T0	02_H								
T1	06_H								
T2	$0A_H$								
T3	$0E_H$								
T4	12_H								
T5	16_H								
T6	$1A_H$								
T7	$1E_H$								
T8	–								
T9	–								
T10	–								
T11	–								
T12	–								
T13	–								
T14	–								
T15	–								
		S16	S17	S18	S19	S20	S21	S22	S23

	RAM address	D0	D1	D2	D3	D4	D5	D6	D7
T0	03_H								
T1	07_H								
T2	$0B_H$								
T3	$0F_H$								
T4	13_H								
T5	17_H								
T6	$1B_H$								
T7	$1F_H$								
T8	–								
T9	–								
T10	–								
T11	–								
T12	–								
T13	–								
T14	–								
T15	–								
		S24	S25	S26	S27				

- 1/4 duty (T=4, S=28)

	RAM address	D0	D1	D2	D3	D4	D5	D6	D7
T0	00_H								
T1	04_H								
T2	08_H								
T3	$0C_H$								
T4	–								
T5	–								
T6	–								
T7	–								
T8	–								
T9	–								
T10	–								
T11	–								
T12	–								
T13	–								
T14	–								
T15	–								
		S0	S1	S2	S3	S4	S5	S6	S7

	RAM address	D0	D1	D2	D3	D4	D5	D6	D7
T0	01_H								
T1	05_H								
T2	09_H								
T3	$0D_H$								
T4	–								
T5	–								
T6	–								
T7	–								
T8	–								
T9	–								
T10	–								
T11	–								
T12	–								
T13	–								
T14	–								
T15	–								
		S8	S9	S10	S11	S12	S13	S14	S15

	RAM address	D0	D1	D2	D3	D4	D5	D6	D7
T0	02_H								
T1	06_H								
T2	$0A_H$								
T3	$0E_H$								
T4	–								
T5	–								
T6	–								
T7	–								
T8	–								
T9	–								
T10	–								
T11	–								
T12	–								
T13	–								
T14	–								
T15	–								
		S16	S17	S18	S19	S20	S21	S22	S23

	RAM address	D0	D1	D2	D3	D4	D5	D6	D7
T0	03_H								
T1	07_H								
T2	$0B_H$								
T3	$0F_H$								
T4	–								
T5	–								
T6	–								
T7	–								
T8	–								
T9	–								
T10	–								
T11	–								
T12	–								
T13	–								
T14	–								
T15	–								
		S24	S25	S26	S27				

Not-using RAM area

Not-existing RAM area

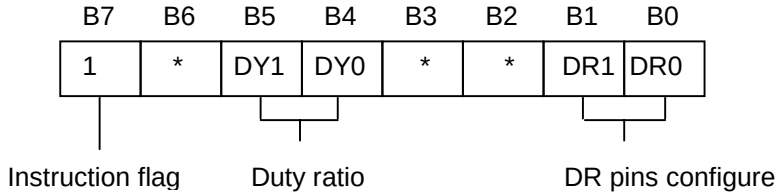
(2) Instruction Register 1

The Instruction Register 1 is used for setting duty ratio and driver (DR) pins configure. If B7 of the 1st word is "1", the rest 4 bits (B5, B4, B1, B0) is interpreted as instruction 1.

The value on register is initialized to the default by reset signal. But, during power on, the value of register 1 is unspecified, it is necessary to set value in register 1.

The contents of the "Instruction register 1" is initially set up by reset signal, as shown below. Because the NJU3427 is unstable during power on, reset shall be executed.

Instruction Register 1 Default
Duty ratio 1/16
DR pins pattern 1



DY1	DY0	Duty Ratio
0	0	1/16
0	1	1/12
1	0	1/8
1	1	1/4

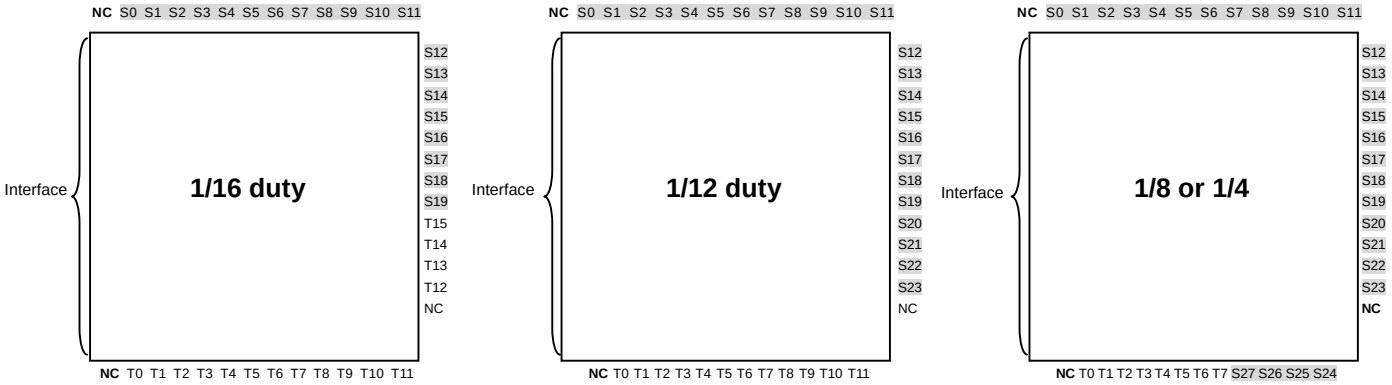
Note): For Segment and Timing pins configure, please refer to "The Relationship Between Duty Ratio and Segment/Timing Pins". When select 1/4 and 1/8 duty, configures of segment and timing pins are the same.

DR1	DR0	DR configure
0	0	Pattern 1
0	1	Pattern 2
1	0	Pattern 3
1	1	Pattern 4

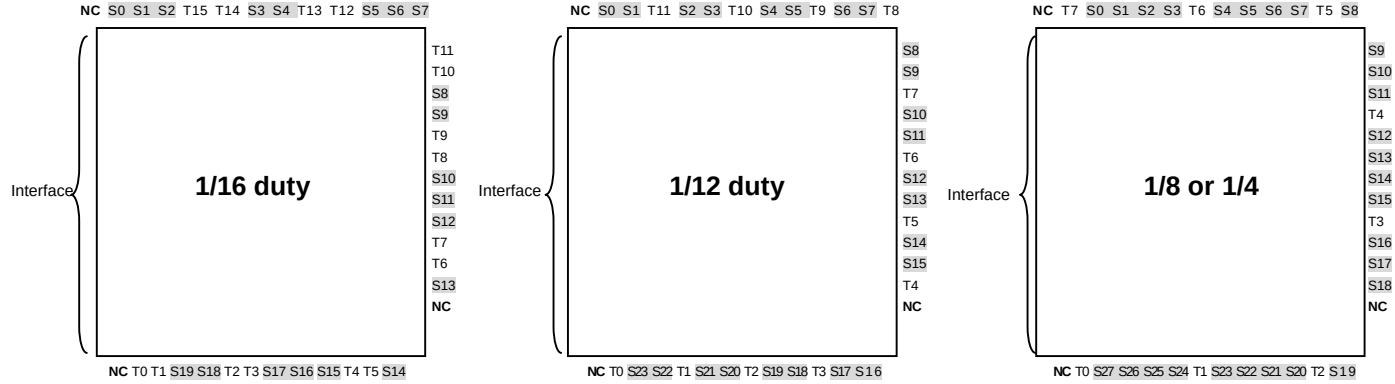
Note): For Segment and Timing pins configure, please refer to "The relationship Between Duty Ratio and Segment/Timing Pins".

The Relationship Between Duty Ratio and Segment (S)/Timing (T) Pins Configure

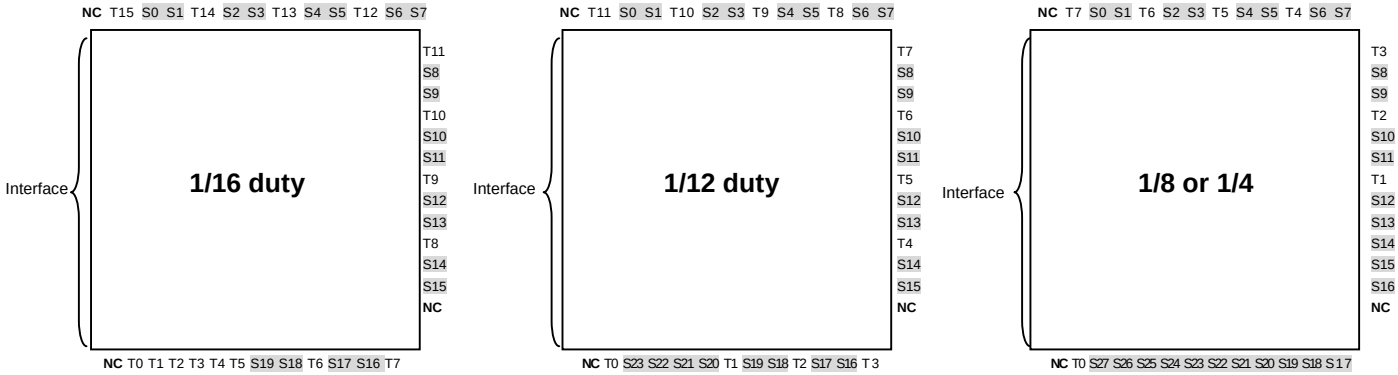
- Pattern 1



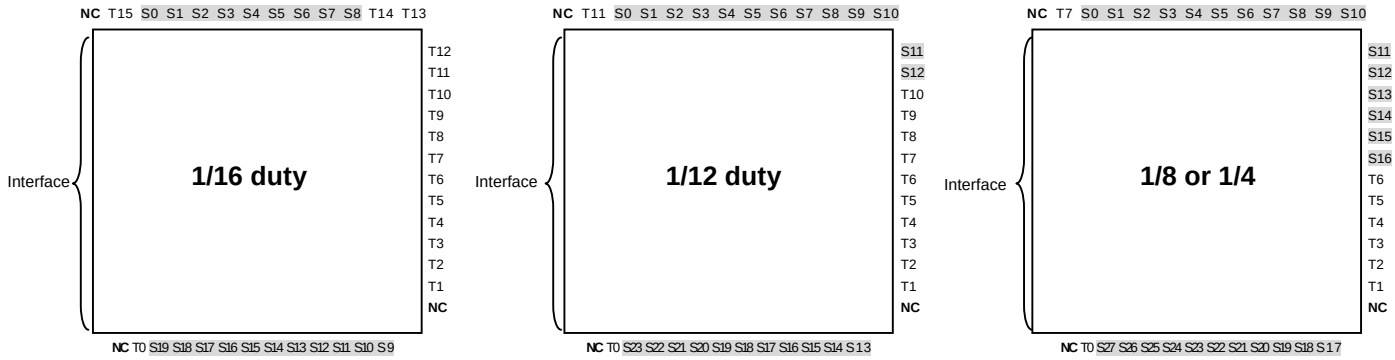
- Pattern 2



- Pattern 3



- Pattern 4



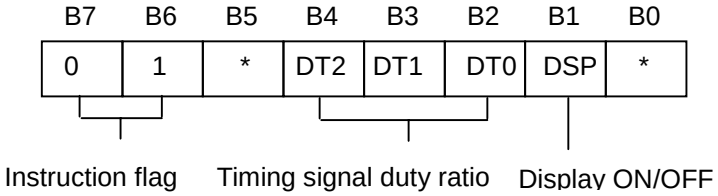
(3) Instruction Register 2

The Instruction Register 2 is used for setting Timing signal duty ratio and controlling display ON/OFF. If B7 and B6 of the 1st word are "0, 1", the rest 4 bits (B4~B1) is interpreted as instruction 2.

When power on or reset signal input, the Register 2 is initialized as below: Because the NJU3427 is unstable during power on, reset shall be executed.

Instruction Register 2 Default

Timing duty ratio	2/16
Display ON/OFF	OFF



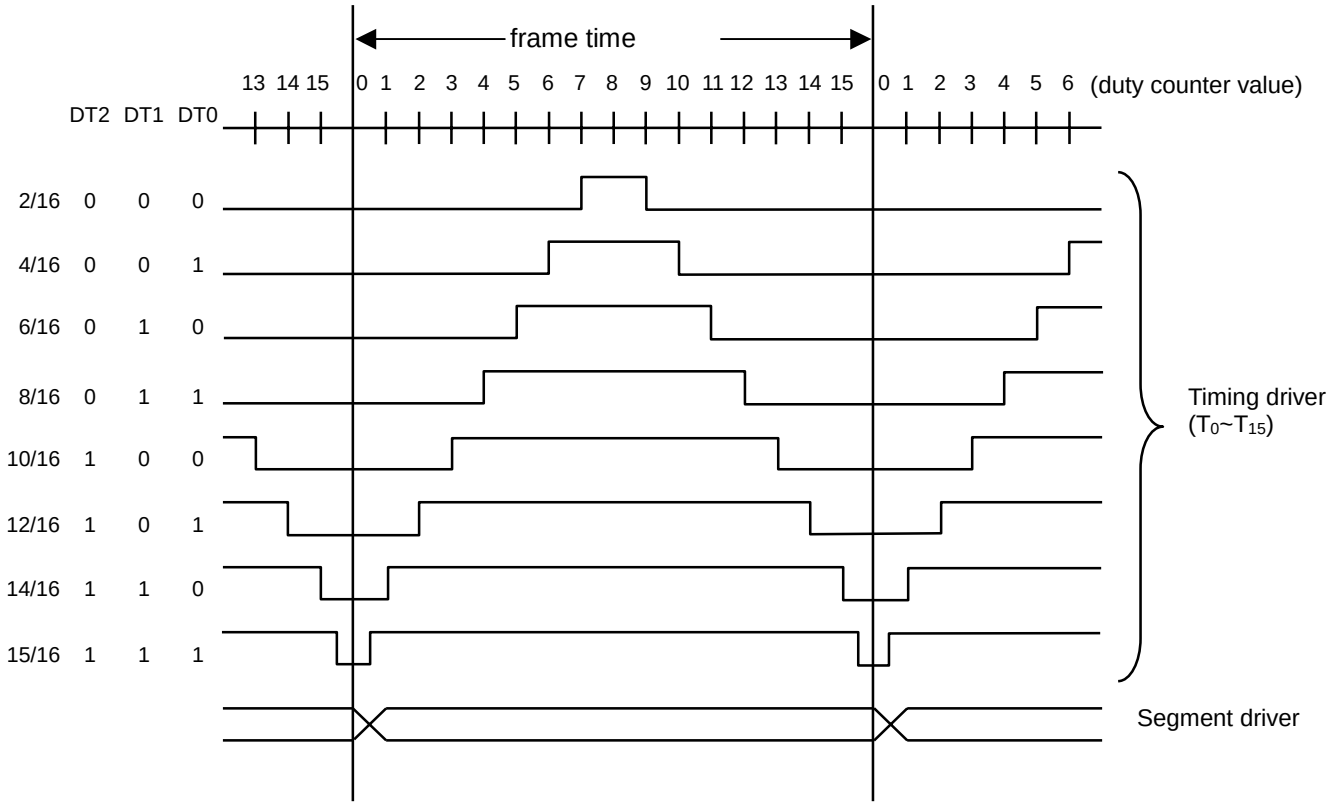
DT2	DT1	DT0	Timing duty ratio
0	0	0	2/16
0	0	1	4/16
0	1	0	6/16
0	1	1	8/16
1	0	0	10/16
1	0	1	12/16
1	1	0	14/16
1	1	1	15/16

Note): For the output waveform, refer to "**Timing Signal Duty Ratio**".

DSP	Display control
0	OFF
1	ON

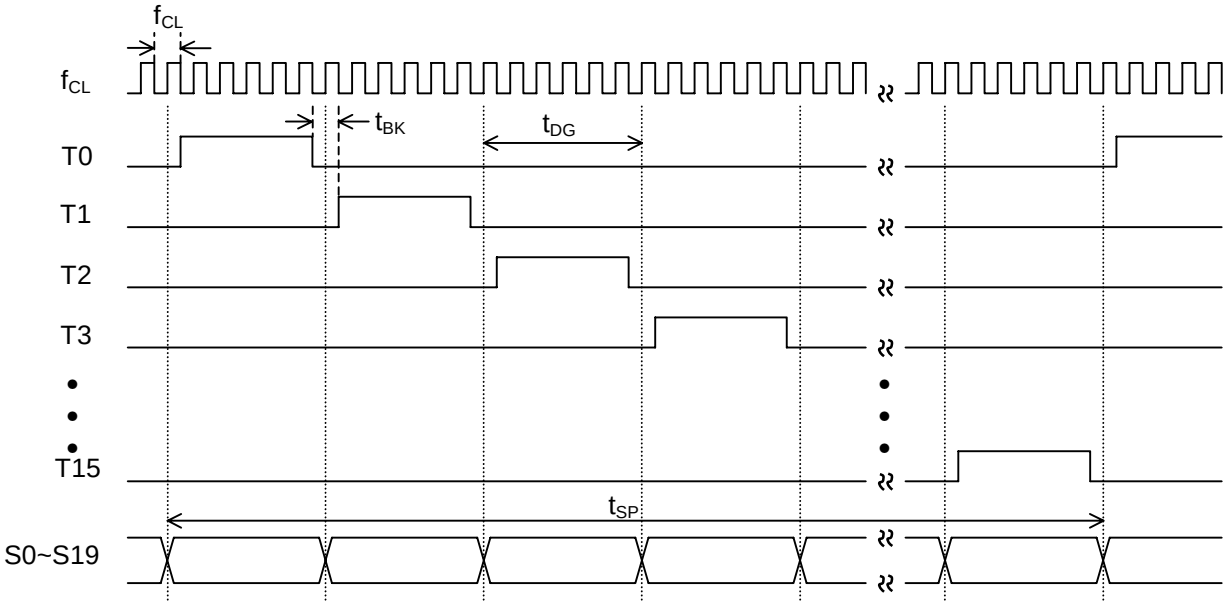
Note): During display off, there is no signal from Timing pins and Segment pins.

● Timing Signal and Duty Ratio



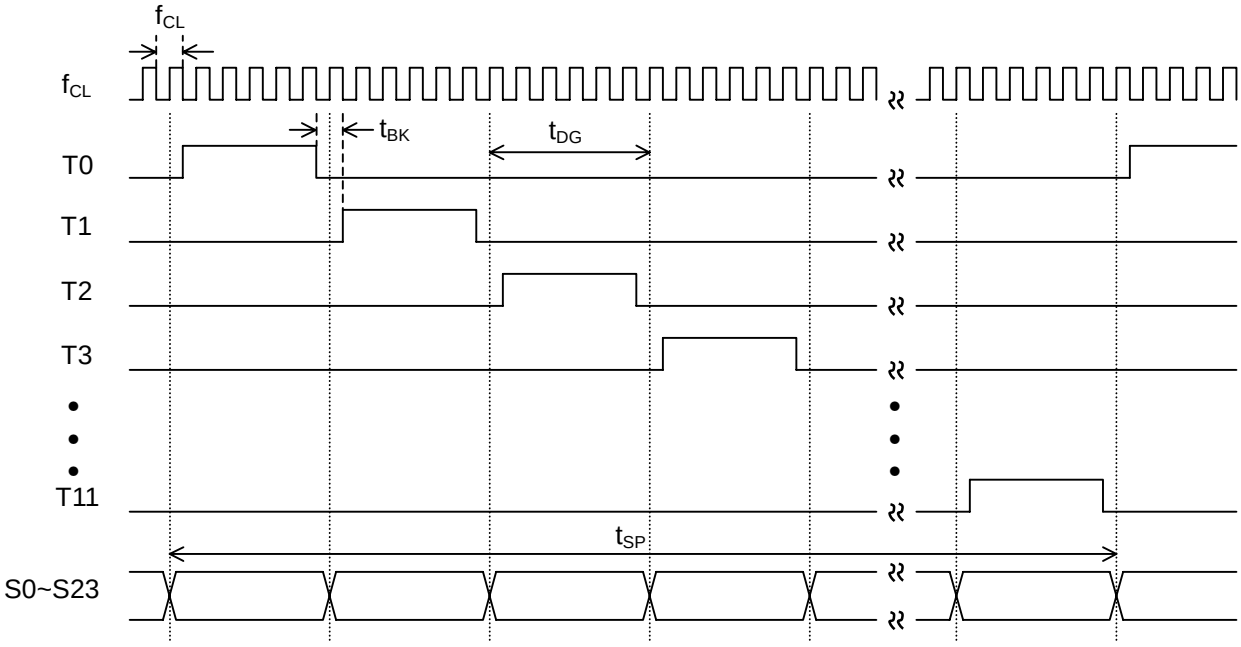
- Display Timing Charter

  - Duty ratio 1/16



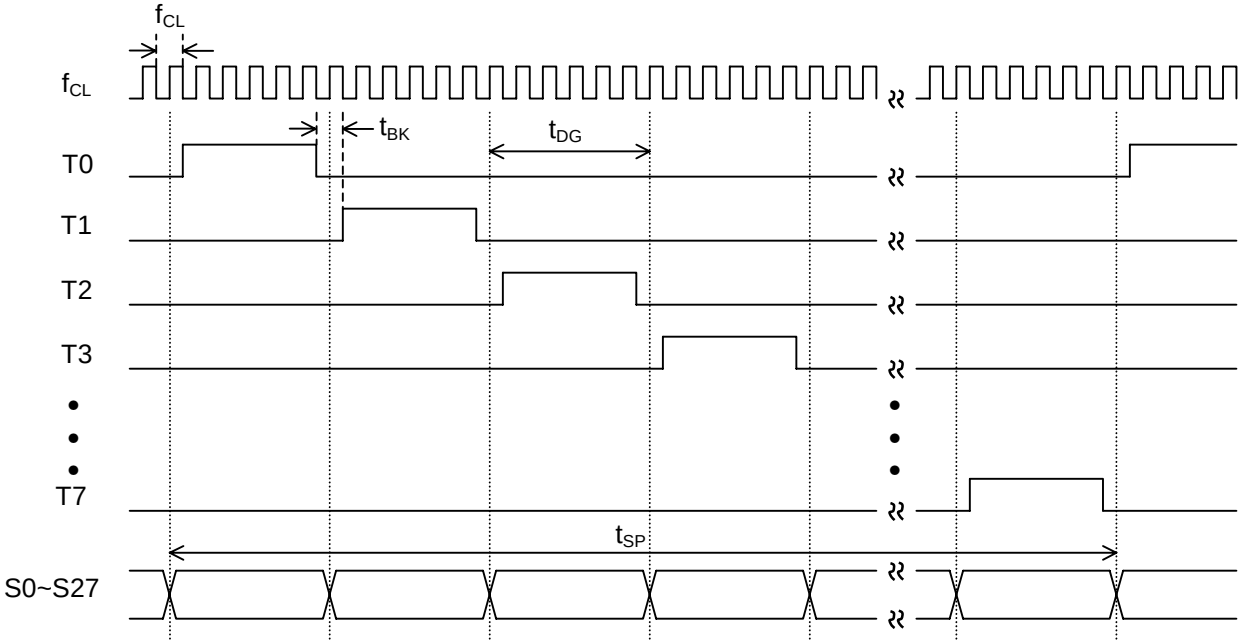
External Clock Frequency	800kHz~2.5MHz	f_{CL}
Minimum Blinking Time	40µs~12.8µs	$t_{BK}=(1/f_{CL})$ x 16 x 2
(Timing Signal Duty Ratio = 15/16)		
1-character display time	640µs ~204.8µs	$t_{DG}=t_{BK}$ x 16
Frame time	10.24ms~3.2768ms	$t_{SP}=t_{DG}$ x 16

  - Duty ratio 1/12



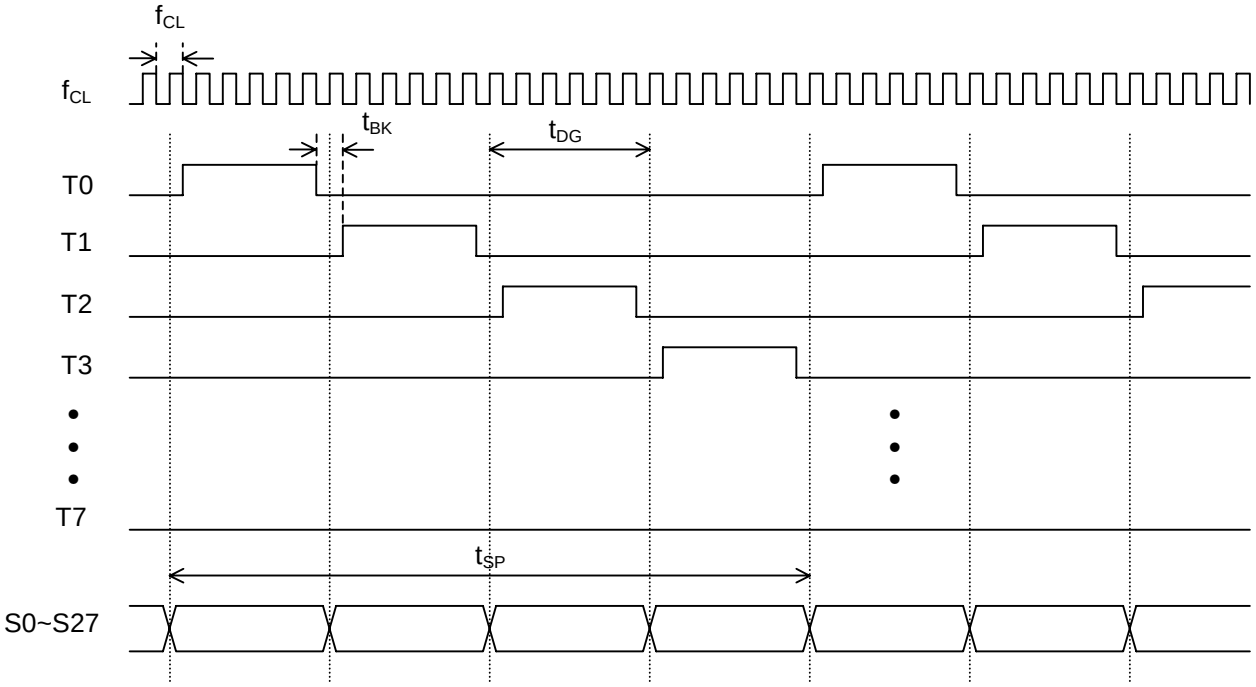
External Clock Frequency	800kHz~2.5MHz	f_{CL}
Minimum Blinking Time	55µs~17.6µs	$t_{BK}=(1/f_{CL})$ x 22 x 2
(Timing Signal Duty Ratio = 15/16)		
1-character display time	880µs ~281.6µs	$t_{DG}=t_{BK}$ x 16
Frame time	10.56ms~3.3792ms	$t_{SP}=t_{DG}$ x 12

- Duty Ratio 1/8



External Clock Frequency	800kHz~2.5MHz	(f_{CL})
Minimum Blinking Time	80µs~25.6µs	$t_{BK}=(1/f_{CL})$ x 32 x 2
(Timing Signal Duty Ratio = 15/16)		
1-character display time	1.28ms~409.6µs	$t_{DG}=t_{BK}$ x 10
Frame time	10.24ms~3.2768ms	$t_{SP}=t_{DG}$ x 8

- Duty ratio 1/4 (T4~T7 output pins)

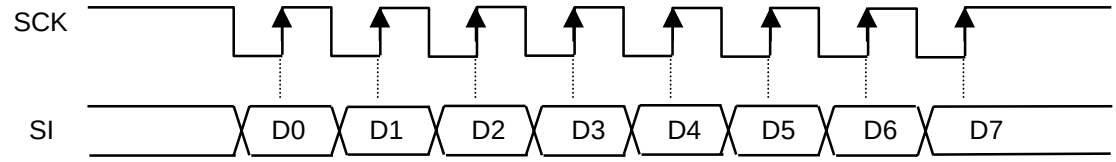


External Clock Frequency	800kHz~2.5MHz	(f_{CL})
Minimum Blanking Time	160µs~51.2µs	$t_{BK}=(1/f_{CL})$ x 64 x 2
(Timing Signal Duty Ratio = 15/16)		
1-character display time	2.56ms~819.2µs	$t_{DG}=t_{BK}$ x 16
Frame time	10.24ms~3.2768ms	$t_{SP}=t_{DG}$ x 4

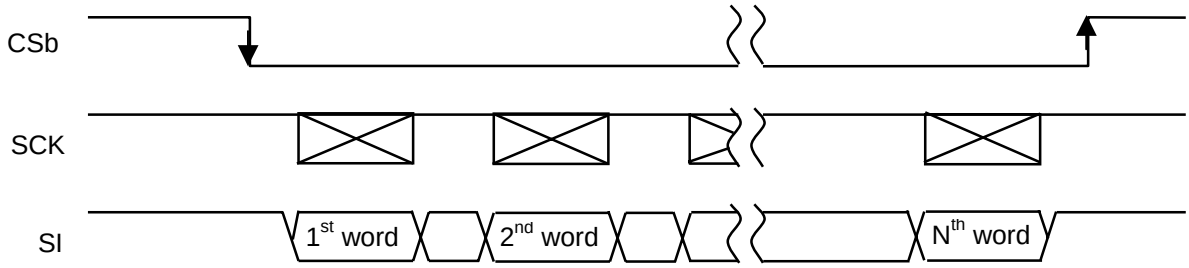
(4) Serial Interface

8-bit per word serial data is transferred from CPU to NJU3427 with synchronous clock signal (SCK). At the every rising edge of the SCK, data is taken in, and at the rising edge of CSb, the data of words are latched.

If the 1st data is address data when CSb becoming "L", without changing CSb, the following data will be interpreted as display data. If the 1st data is instruction, without changing CSb signal, all the following data is invalid.



Serial data transmission



Serial data transmission format

- Serial Data

1st word

Address data

B7	B6	B5	B4	B3	B2	B1	B0
0	0	AD5	AD4	AD3	AD2	AD1	AD0

Instruction 1

B7	B6	B5	B4	B3	B2	B1	B0
1	*	DY1	DY0	*	*	DR1	DR0

*:don't care

Instruction 2

B7	B6	B5	B4	B3	B2	B1	B0
0	1	*	DT2	DT1	DT0	DSP	*

*:don't care

From the 2nd word

If the 1st word is address data display data

If the 1st word is instruction data invalid data

(5) Reset Circuit

If RSTb="L", reset circuit functions, and the following default is set up. Because the NJU3427 is unstable during power on, reset shall be executed.

Address Data
(AD0, AD1, AD2, AD3, AD4, AD5): (0, 0, 0, 0, 0, 0)

Instruction Register 1

Duty ratio	1/16
DR pins configure	Pattern 1

Instruction Register 2

Timing signal duty ratio	2/16
Display ON/OFF	OFF

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Conditions
Power Supply	V_{DD}	-0.3~+7.0	V	
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V	
VFD Driving Voltage	V_{FDP}	V_{DD}-45~V_{DD}+0.3	V	V_{DD} as reference voltage
H Level Output Current 1	I_{OH1}	-35	mA	DR_0 output, signal pin
H Level Output Current 2	I_{OH2}	-15	mA	DR_1 ~ DR_{35} output, signal pin
L Level Output Current	I_{OL}	20	mA	
Operating Temperature	Topr	-40 ~ 85	°C	
Storage Temperature	Tstg	-55 ~ 125	°C	
Power Dissipation	PD	900(QFP52-A2) 1200(QFP52-H2)	mW	Glass epoxy board (76.2 x114.3x1.6mm)

Note 1): The IC must be used within the Absolute Maximum Ratings, otherwise, an electrical or physical stress may cause a permanent damage to it.

Note 2): De-coupling capacitors should be placed between V_{DD}-V_{SS} and V_{FDP}-V_{SS}.

Note 3): The condition of V_{DD}> V_{SS}≥ V_{FDP} and V_{SS}=0 must be maintained.

■ ELECTRICAL CHARACTERISTICS

DC Characteristics 1

(V_{DD}=5.0V, V_{SS}=0V, Ta=-40 ~ 85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Power Supply (1)	V_{DD}	V_{DD} pin	4.5	-	5.5	V
Power Supply (2)	V_{FDP}	V_{FDP} pin and V_{DD} as reference	-40	-	V_{SS}	V
H Level Input Voltage	V_{IH}	XT, RSTb, CSb, SCK, SI pins	0.8V_{DD}	-	-	V
L Level Input Voltage	V_{IL}		-	-	0.2V_{DD}	
Input off-leak current	I_{IZ}	CSb, SCK, SI pins V_{DD}=5.5V, V_I=0 or 5.5V	-	-	±1	μA
Display Current	I_{OH}	DR_0 pin; V_{DD}=4.5V,V_{FDP}=V_{DD}-40	-11.5	-20	-	mA
		DR_1 ~ DR_{35} pin; V, V_{OH}=V_{DD}-2.25V	-5.5	-10	-	mA
Pull-up Resistance	R_{UR}	RSTb pin, Ta=25°C, V_I=V_{SS}	100	-	300	kΩ
Pull-down Resistance	R_{DST}	DR_0 ~ DR_{35} pins, Ta=25°C V_I=V_{DD}, V_{FDP}=V_{DD}-40V	75	-	195	kΩ
Logic Circuit Power Supply	I_{SS}	V_{SS} pin CR oscillation (R=6.8kΩ, C=100pF), All Segment/Timing pins open, RSTb open All Segment/Timing pins output display OFF signal.	-	0.6	0.8	mA
Operation Current	I_{FDP}	V_{FDP} pin, V_{FDP}=V_{DD}-40V, CR oscillation (R=6.8kΩ, C=100pF), All driving pins output display ON signal	-	12	16.5	mA
CR Oscillation Frequency	f_{CR}	Ta=25°C R=6.8kΩ, C=100pF	1.05	1.13	1.21	MHz

• AC Characteristics 1

(V_{DD}=5.0V, V_{SS}=0V, Ta=-40 ~ 85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
External Clock Frequency	f_{CL}	Fig 1	0.8	-	2.5	MH_Z
Width of External Clock Pulse	t_{CLH}, t_{CLL}	Fig 1	200			ns
Data Setup Time	t_{SIS}	Fig2	35			ns
Data Hold Time	t_{SIH}	Fig2	35			ns
Clock Frequency	f_{SCK}	Fig3			2.0	MH_Z
Clock Pulse Width	t_{SCKH}, t_{SCKL}	Fig3	200			ns
External Clock Rising Time, Falling Time	t_{CLH}, t_{CLL}	Fig2			250	ns
Clock Interval Time	t_{SCI}	Fig3	10			μs
Reset Pulse Width	t_{RSTb}	Fig4	10			μs

• DC Characteristics 2

(V_{DD}=3.0V, V_{SS}=0V, Ta=-40 ~ 85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Power Supply (1)	V_{DD}	V_{DD} pin	2.7	-	3.6	V
Power Supply (2)	V_{FDP}	V_{FDP} pin and V_{DD} as reference	-40	-	V_{SS}	V
H Level Input Voltage	V_{IH}	XT, RSTb, CSb, SCK, SI pins	0.8V_{DD}	-	-	V
L Level Input Voltage	V_{IL}		-	-	0.2V_{DD}	
Input off-leak current	I_{IZ}	CSb, SCK, SI pins V_{DD}=3.6V, V_I=0 or 3.6V	-	-	±1	μA
Display Current	I_{OH}	DR_0 pin; V_{DD}=2.7V,V_{FDP}=V_{DD}-40 V, V_{OH}=V_{DD}-1.35V	-5.0	-9.0	-	mA
		DR_1 ~ DR_{35} pin; V_{DD}=2.7V,V_{FDP}=V_{DD}-40 V, V_{OH}=V_{DD}-1.35V	-2.5	-4.0	-	mA
Pull-up Resistance	R_{UR}	RSTb pin, Ta=25°C, V_I=V_{SS}	100	-	300	kΩ
Pull-down Resistance	R_{DST}	DR_0 ~ DR_{35} pins, Ta=25°C V_I=V_{DD}, V_{FDP}=V_{DD}-40V	75	-	195	kΩ
Logic Circuit Power Supply	I_{SS}	V_{SS} pin CR oscillation (R=4.7kΩ, C=100pF), All Segment/Timing pins open, RSTb open All Segment/Timing pins output display OFF signal.	-	0.25	0.35	mA
Operation Current	I_{FDP}	V_{FDP} pin, V_{FDP}=V_{DD}-40V, CR oscillation (R=4.7kΩ, C=100pF), All driving pins output display ON signal	-	12	16.5	mA
CR Oscillation Frequency	f_{CR}	Ta=25°C R=4.7kΩ, C=100pF	1.05	1.13	1.21	MHz

• AC Characteristics 2

(V_{DD}=3.0V, V_{SS}=0V, Ta=-40 ~ 85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
External Clock Frequency	f_{CL}	Fig 1	0.8	-	2.5	MH_Z
Width of External Clock Pulse	t_{CLH}, t_{CLL}	Fig 1	200			ns
Data Setup Time	t_{SIS}	Fig2	35			ns
Data Hold Time	t_{SIH}	Fig2	35			ns
Clock Frequency	f_{SCK}	Fig3			2.0	MH_Z
Clock Pulse Width	t_{SCKH}, t_{SCKL}	Fig3	200			ns
External Clock Rising Time, Falling Time	t_{CLH}, t_{CLL}	Fig2			250	ns
Clock Interval Time	t_{SCI}	Fig3	10			μs
Reset Pulse Width	t_{RSTb}	Fig4	10			μs

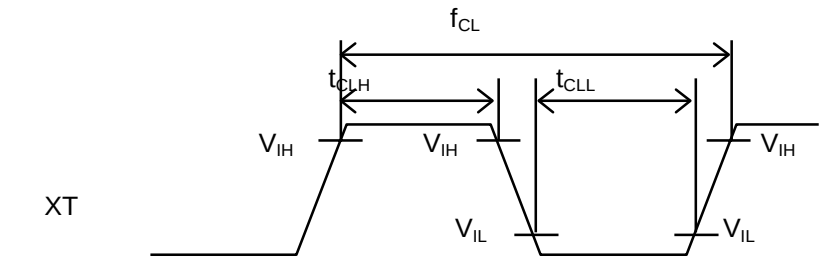


Fig1

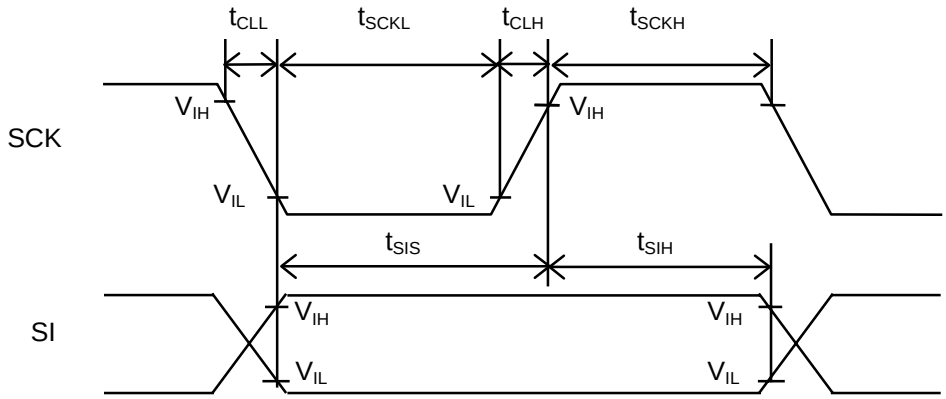


Fig2

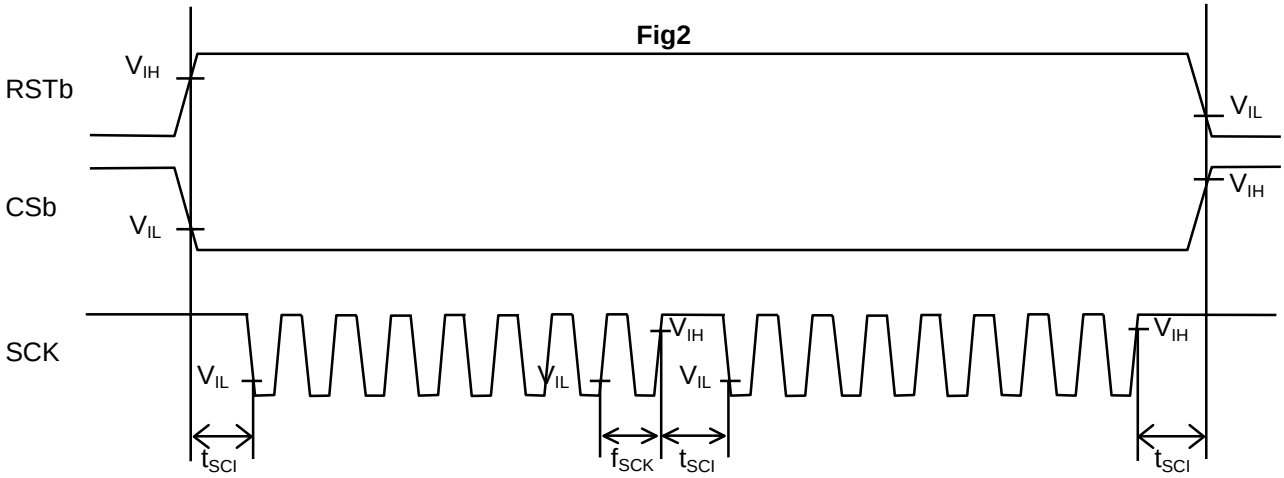


Fig3

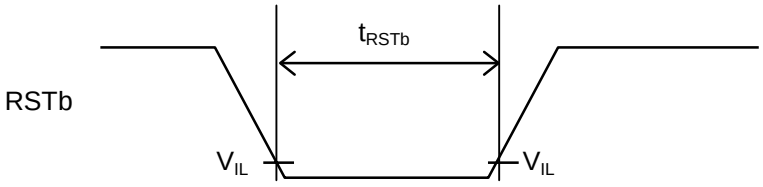
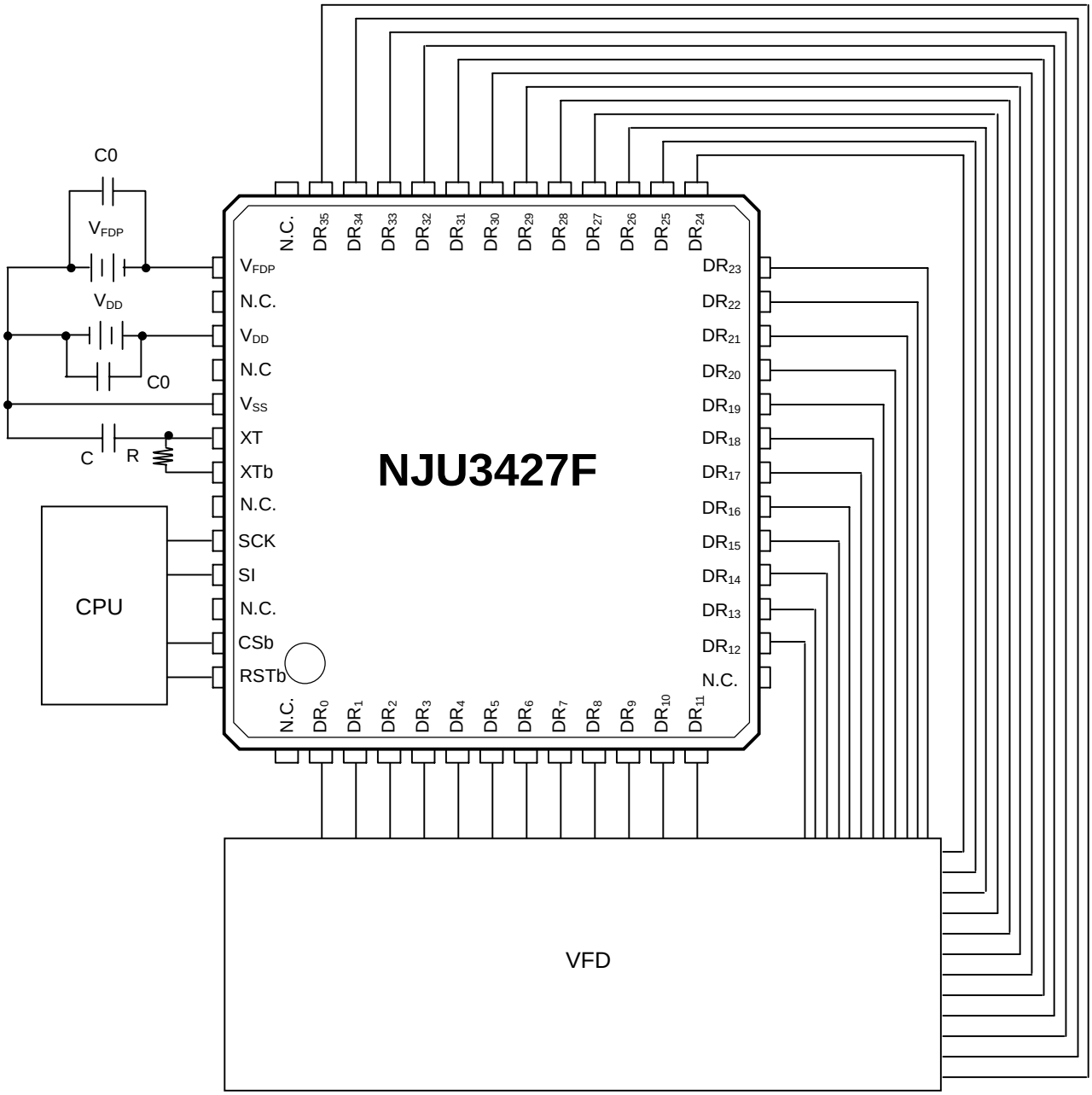


Fig4

■ APPLICATION CIRCUIT (CR OSCILLATION)



* Pay careful attention to reduce the noise from power supply and interface pins.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NJR:

NJU3427FA2

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru