

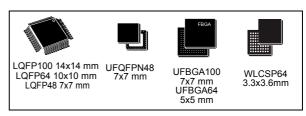
STM32F091xB STM32F091xC

ARM®-based 32-bit MCU, up to 256 KB Flash, CAN, 12 timers, ADC, DAC, and comm. interfaces, 2.0 - 3.6V

Datasheet - production data

Features

- Core: ARM[®] 32-bit Cortex[®]-M0 CPU, frequency up to 48 MHz
- Memories
 - 128 to 256 Kbytes of Flash memory
 - 32 Kbytes of SRAM with HW parity
- CRC calculation unit
- Reset and power management
 - Digital & I/Os supply: V_{DD} = 2.0 V to 3.6 V
 - Analog supply: V_{DDA} = V_{DD} to 3.6 V
 - Power-on/Power down reset (POR/PDR)
 - Programmable voltage detector (PVD)
 - Low power modes: Sleep, Stop, Standby
 - V_{BAT} supply for RTC and backup registers
- Clock management
 - 4 to 32 MHz crystal oscillator
 - 32 kHz oscillator for RTC with calibration
 - Internal 8 MHz RC with x6 PLL option
 - Internal 40 kHz RC oscillator
 - Internal 48 MHz oscillator with automatic trimming based on ext. synchronization
- Up to 88 fast I/Os
 - All mappable on external interrupt vectors
 - Up to 69 I/Os with 5V-tolerant capability and 19 with independent supply V_{DDIO2}
- 12-channel DMA controller
- One 12-bit, 1.0 µs ADC (up to 16 channels)
 - Conversion range: 0 to 3.6 V
 - Separate analog supply: 2.4 V to 3.6 V
- One 12-bit D/A converter (with 2 channels)
- Two fast low-power analog comparators with programmable input and output
- Up to 24 capacitive sensing channels for touchkey, linear and rotary touch sensors
- Calendar RTC with alarm and periodic wakeup from Stop/Standby



12 timers

- One 16-bit advanced-control timer for 6 channel PWM output
- One 32-bit and seven 16-bit timers, with up to 4 IC/OC, OCN, usable for IR control decoding or DAC control
- Independent and system watchdog timers
- SysTick timer
- · Communication interfaces
 - Two I²C interfaces supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink, one supporting SMBus/PMBus and wakeup
 - Up to eight USARTs supporting master synchronous SPI and modem control, three with ISO7816 interface, LIN, IrDA, auto baud rate detection and wakeup feature
 - Two SPIs (18 Mbit/s) with 4 to 16 programmable bit frames, and with I²S interface multiplexed
 - CAN interface
- HDMI CEC wakeup on header reception
- Serial wire debug (SWD)
- 96-bit unique ID
- All packages ECOPACK[®]2

Table 1. Device summary

=	
Reference Part number	
STM32F091xB	STM32F091CB, STM32F091RB, STM32F091VB
STM32F091xC	STM32F091CC, STM32F091RC, STM32F091VC

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F091xB/xC microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the ARM[®] Cortex[®]-M0 core, please refer to the Cortex[®]-M0 Technical Reference Manual, available from the www.arm.com website.





2 Description

The STM32F091xB/xC microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 256 Kbytes of Flash memory and 32 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. The device offers standard communication interfaces (two I²Cs, two SPIs/one I²S, one HDMI CEC and up to eight USARTs), one CAN, one 12-bit ADC, one 12-bit DAC with two channels, seven 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F091xB/xC microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F091xB/xC microcontrollers include devices in seven different packages ranging from 48 pins to 100 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F091xB/xC microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

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Table 2. STM32F091xB/xC family device features and peripheral counts

Peripheral		STM32	F091Cx	STM32	F091Rx	STM32	2F091Vx	
Flash memory (Kbyte)		128	256	128	256	128	256	
SRAM	(Kbyte)			1	32	1	1	
Advanced control		1 (16-bit)						
Timers	General purpose		5 (16-bit) 1 (32-bit)					
	Basic			2	(16-bit)			
	SPI [I ² S] ⁽¹⁾				2 [2]			
	I ² C				2			
Comm. interfaces	USART	(3			8		
mionacco	CAN	1						
	CEC		1					
	12-bit ADC (number of channels)		1 (10 ext. + 3 int.) (16 ext. + 3 int.)					
	t DAC f channels)	1 (2)						
Analog co	omparator	2						
GP	lOs	3	8		52	3	38	
Capacitive sensing channels		17 18 2		24				
Max. CPU	frequency	48 MHz						
Operating voltage		2.0 to 3.6 V						
Operating temperature		A	Ambient operating temperature: -40°C to 85°C / -40°C to 105°C Junction temperature: -40°C to 105°C / -40°C to 125°C			5°C		
Packages		LQF UFQF	P48 PN48	UFB	FP64 GA64 CSP64		FP100 GA100	

^{1.} The SPI interface can be used either in SPI mode or in I²S audio mode.

SWCLK SWDIO as AF POWER Serial Wire Debug VOLT.REG $V_{DD} = 2 \text{ to } 3.6 \text{ V}$ 3.3 V to 1.8 V Obl Flash Or memory interface Flash GPL up to 256 KB 32-bit CORTEX-M0 CPU OKIN ← SUPPLY SUPERVISION $f_{MAX} = 48 \text{ MHz}$ V_{DDIO2} OKIN ◀ NRST SRAM 32 KB SRAM controller matri Reset ◀ V_{DDA} POR/PDR Int ◀ V_{SSA} NVIC @ V_{DDA} V_{DD} Bus HSI14 RC 14 MHz PVD HSI RC 8 MHz @ V_{DDA} PLLCLK @ V_{DD} LSI GP DMA RC 40 kHz XTAL OSC OSC_IN 12 channels HSI48 4-32 MHz RC 48MHz Ind. Window WDG PA[15:0] GPIO port A RESET & CLOCK ₹. CONTROL V_{BAT} = 1.65 to 3.6 V PB[15:0] GPIO port B OSC32_IN OSC32_OUT PC[15:0] GPIO port C System and peripheral XTAL32 kHz clocks PD[15:0] GPIO port D 3 TAMPER-RTC RTC AHB reg (ALARM OUT) PE[15:0] GPIO port E RTC interface PF[10:9], PF6 PF[3:0] Щ GPIO port F CRS SYNC 4 channels 3 compl. channels BRK, ETR input as AF PWM TIMER 1 CRC PAD 8 groups of 4 channels 4 ch., ETR as AF TIMER 2 32-bit Sensing Controller switches AHB TIMER 3 4 ch., ETR as AF SYNC APR TIMER 14 1 channel as AF EXT. IT WKUP 88 AF [2 channels 1 compl, BRK as AF TIMER 15 SRAM 1 channel 1 compl, BRK as AF 256 B TIMER 16 į į 1 channel 1 compl, BRK as AF IR_OUT as AF TIMER 17 TX, RX as AF **BxCAN** Window WDG RX, TX,CTS, RTS, CK as AF USART1 MOSI/SD SPI1/I2S1 MISO/MCK SCK/CK NSS/WS as AF RX, TX,CTS, RTS, CK as AF USART2 DBGMCU RX, TX,CTS, RTS, CK as AF USART3 MOSI/SD SPI2/I2S2 RX, TX,CTS, RTS, CK as AF USART4 SCK/CK NSS/WS as AF SYSCFG IF USART5 RX, TX, RTS, CK as AF USART6 RX, TX, RTS, CK as AF INPUT + GP comparator 1 USART7 RX, TX, RTS, CK as AF OUTPUT GP comparator 2 USART8 RX, TX, RTS, CK as AF as AF @ V_{DDA} SCL, SDA, SMBA (20 mA FM+) as AF I2C1 Temp. SCL, SDA (20 mA FM+) as AF I2C2 16x AD input IF 12-bit ADC CEC as AF HDMI-CEC TIMER 6 12-bit DAC ►DAC OUT1 V_{DDA} V_{SSA} TIMER 7 @ V_{DDA} 12-bit DAC ► DAC_OUT2 @ V_{DDA} Power domain of analog blocks: V_{BAT} V_{DD} V_{DDA} MSv34957V2

Figure 1. Block diagram



3 Functional overview

Figure 1 shows the general block diagram of the STM32F091xB/xC devices.

3.1 ARM®-Cortex®-M0 core

The ARM[®] Cortex[®]-M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM[®] Cortex[®]-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The STM32F091xB/xC devices embed ARM core and are compatible with all ARM tools and software.

3.2 Memories

The device has the following features:

- 32 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
 - up to 256 Kbytes of embedded Flash memory for programs and data
 - Option bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex[®]-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bits are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot pin is shared with the standard GPIO and can be disabled through the boot selector option bits. The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10 or I²C on pins PB6/PB7.



3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- V_{DD} = V_{DDIO1} = 2.0 to 3.6 V: external power supply for I/Os (V_{DDIO1}) and the internal regulator. It is provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC are used). It is provided externally through VDDA pin. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be established first.
- V_{DDIO2} = 1.65 to 3.6 V: external power supply for marked I/Os. V_{DDIO2} is provided externally through the VDDIO2 pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA}, but it must not be provided without a valid supply on V_{DD}. The V_{DDIO2} supply is monitored and compared with the internal reference voltage (V_{REFINT}). When the V_{DDIO2} is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt. Refer to the pinout diagrams or tables for concerned I/Os list.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to Figure 13: Power supply scheme.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD}



threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F091xB/xC microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1, USART1, USART2, USART3, COMPx, V_{DDIO2} supply comparator or the CEC.

The CEC, USART1, USART2, USART3 and I2C1 peripherals can be configured to enable the HSI RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches



Note:

back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

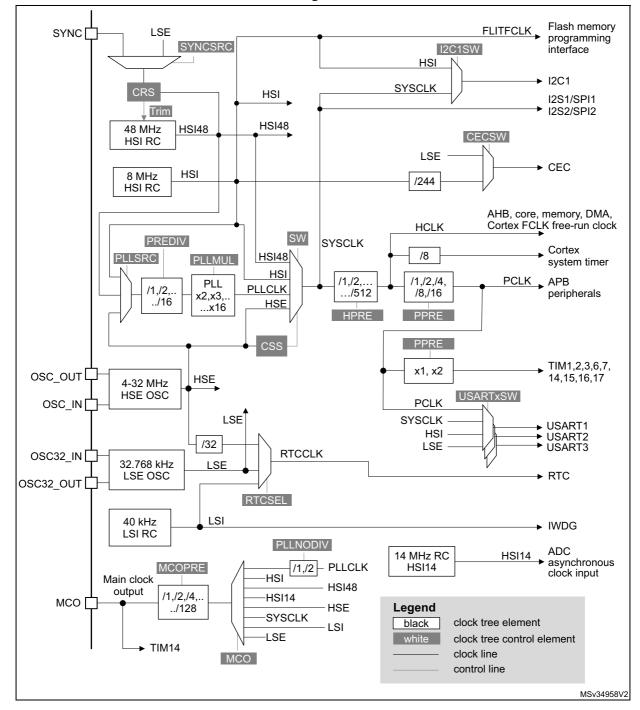


Figure 2. Clock tree

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.



Additionally, also the internal RC 48 MHz oscillator can be selected for system clock or PLL input source. This oscillator can be automatically fine-trimmed by the means of the CRS peripheral using the external synchronization.

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 12-channel general-purpose DMAs (seven channels for DMA1 and five channels for DMA2) manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMAs support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14), DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex[®]-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 32 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 88 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 16 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), V _{DDA} = 3.3 V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), V _{DDA} = 3.3 V (± 10 mV)	0x1FFF F7C2 - 0x1FFF F7C3

Table 3. Temperature sensor calibration values

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The



precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
	Raw data acquired at a temperature of 30 °C (± 5 °C), V _{DDA} = 3.3 V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA} , and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

Six DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to Table 28: Embedded internal reference voltage for the value and precision of the internal reference voltage.

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.13 Touch sensing controller (TSC)

The STM32F091xB/xC devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists in charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate. For operation, one capacitive sensing GPIO in each group is connected to an external capacitor and cannot be used as effective touch sensing channel.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 5. Capacitive sensing GPIOs available on STM32F091xB/xC devices

Group	Capacitive sensing signal name	Pin name
	TSC_G1_IO1	PA0
1	TSC_G1_IO2	PA1
ı	TSC_G1_IO3	PA2
	TSC_G1_IO4	PA3
	TSC_G2_IO1	PA4
2	TSC_G2_IO2	PA5
2	TSC_G2_IO3	PA6
	TSC_G2_IO4	PA7
	TSC_G3_IO1	PC5
3	TSC_G3_IO2	PB0
3	TSC_G3_IO3	PB1
	TSC_G3_IO4	PB2
	TSC_G4_IO1	PA9
4	TSC_G4_IO2	PA10
4	TSC_G4_IO3	PA11
	TSC_G4_IO4	PA12

Group	Capacitive sensing signal name	Pin name
	TSC_G5_IO1	PB3
5	TSC_G5_IO2	PB4
	TSC_G5_IO3	PB6
	TSC_G5_IO4	PB7
	TSC_G6_IO1	PB11
6	TSC_G6_IO2	PB12
	TSC_G6_IO3	PB13
	TSC_G6_IO4	PB14
	TSC_G7_IO1	PE2
7	TSC_G7_IO2	PE3
'	TSC_G7_IO3	PE4
	TSC_G7_IO4	PE5
	TSC_G8_IO1	PD12
8	TSC_G8_IO2	PD13
	TSC_G8_IO3	PD14
	TSC_G8_IO4	PD15



Table 6. Number of capacitive sensing channels available on STM32F091xB/xC devices

Analog I/O group	Number of capacitive sensing channels						
Analog I/O group	STM32F091Vx	STM32F091Cx					
G1	3	3	3				
G2	3	3	3				
G3	3	3	2				
G4	3	3	3				
G5	3	3	3				
G6	3	3	3				
G7	3	0	0				
G8	3	0	0				
Number of capacitive sensing channels	24	18	17				

3.14 Timers and watchdogs

The STM32F091xB/xC devices include up to six general-purpose timers, two basic timers and an advanced control timer.

Table 7 compares the features of the different timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	3
	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
General purpose	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM14	16-bit	Up	integer from 1 to 65536	No	1	-
	TIM15	16-bit	Up	integer from 1 to 65536	Yes	2	1
	TIM16 TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	1
Basic	TIM6 TIM7	16-bit	Up	integer from 1 to 65536	Yes	-	-

3.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- · output compare
- PWM generation (edge or center-aligned modes)
- one-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.14.2 General-purpose timers (TIM2, 3, 14, 15, 16, 17)

There are six synchronizable general-purpose timers embedded in the STM32F091xB/xC devices (see *Table 7* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F091xB/xC devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.



TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.14.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- Periodic wakeup unit with programmable resolution and period.
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.16 Inter-integrated circuit interface (I²C)

Up to two I²C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive on most of the associated I/Os.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Table 8. Comparison of I²C analog and digital filters

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	–Extra filtering capability vs.standard requirements–Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts



verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C peripherals can be served by the DMA controller.

Refer to Table 9 for the differences between I2C1 and I2C2.

Table 9. STM32F091xB/xC I²C implementation

I ² C features ⁽¹⁾	I2C1	I2C2
7-bit addressing mode	Х	Х
10-bit addressing mode	X	Х
Standard mode (up to 100 kbit/s)	X	Х
Fast mode (up to 400 kbit/s)	Х	Х
Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive I/Os	Х	Х
Independent clock	X	-
SMBus	Х	-
Wakeup from STOP	Х	-

^{1.} X = supported.

3.17 Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds up to eight universal synchronous/asynchronous receivers/transmitters (USART1, USART2, USART3, USART4, USART5, USART6, USART7, USART8) which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1, USART2 and USART3 support also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and have a clock domain independent of the CPU clock, allowing to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller.

Table 10. STM32F091xB/xC USART implementation

USART modes/features ⁽¹⁾	USART1 USART2 USART3	USART4	USART5 USART6 USART7 USART8
Hardware flow control for modem	Х	Х	-
Continuous communication using DMA	Х	Х	Х
Multiprocessor communication	Х	Х	Х
Synchronous mode	Х	Х	Х
Smartcard mode	Х	-	-

USART modes/features ⁽¹⁾	USART1 USART2 USART3	USART4	USART5 USART6 USART7 USART8
Single-wire half-duplex communication	Х	Х	Х
IrDA SIR ENDEC block	Х	-	-
LIN mode	Х	-	-
Dual clock domain and wakeup from Stop mode	Х	-	-
Receiver timeout interrupt	Х	-	-
Modbus communication	Х	-	-
Auto baud rate detection	Х	-	-
Driver Enable	Х	Х	Х

Table 10. STM32F091xB/xC USART implementation (continued)

3.18 Serial peripheral interface (SPI) / Inter-integrated sound interface (I²S)

Two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I²S interfaces (multiplexed with SPI1 and SPI2 respectively) supporting four different audio standards can operate as master or slave at half-duplex communication mode. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, they can output a clock for an external audio component at 256 times the sampling frequency.

Table 11. STM32F091xB/xC SPI/I2S implementa	tion
(1)	

SPI features ⁽¹⁾	SPI1 and SPI2
Hardware CRC calculation	X
Rx/Tx FIFO	X
NSS pulse mode	X
I ² S mode	X
TI mode	Х

^{1.} X = supported.

^{1.} X = supported.

3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.20 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.21 Clock recovery system (CRS)

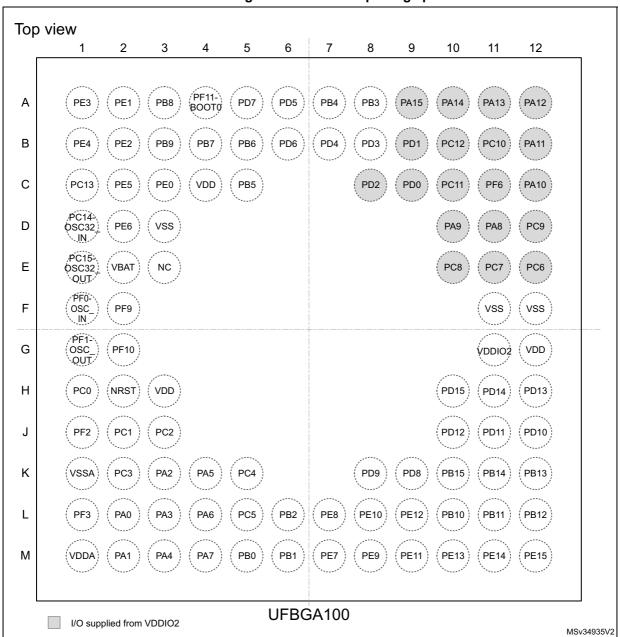
The STM32F091xB/xC embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.22 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts and pin descriptions

Figure 3. UFBGA100 package pinout



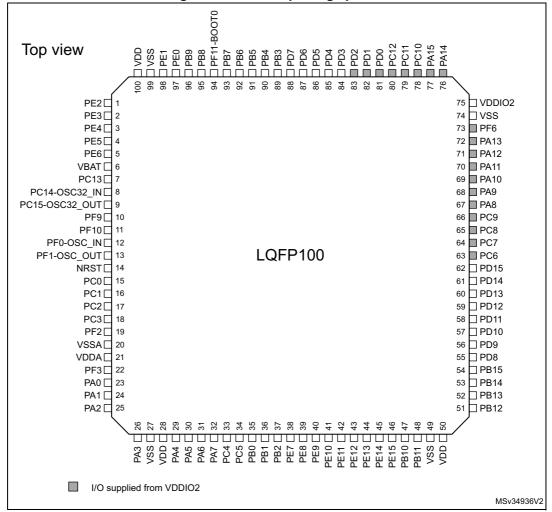


Figure 4. LQFP100 package pinout



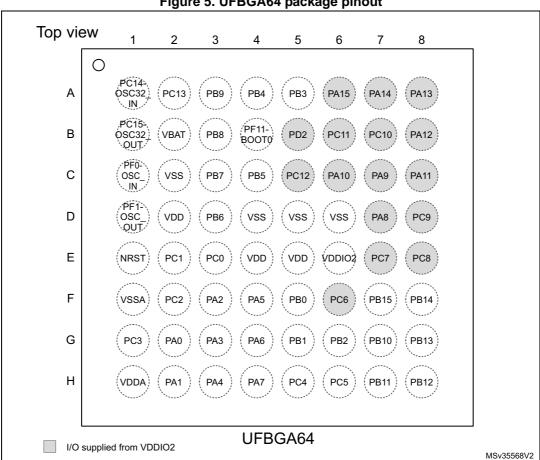


Figure 5. UFBGA64 package pinout

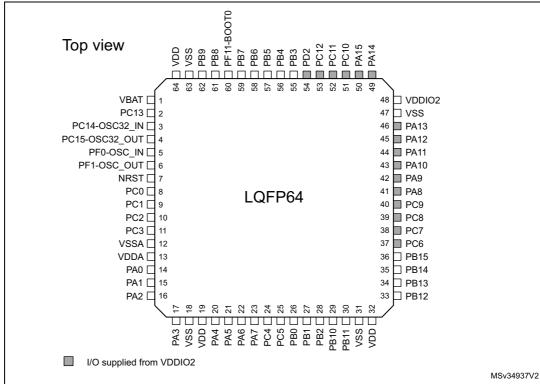


Figure 6. LQFP64 package pinout



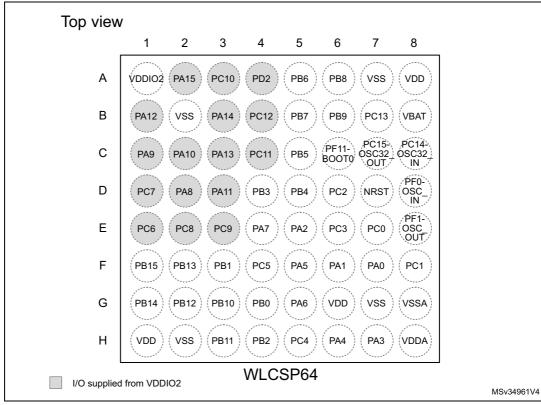


Figure 7. WLCSP64 package pinout

The above figure shows the package in top view, changing from bottom view in the previous document versions.

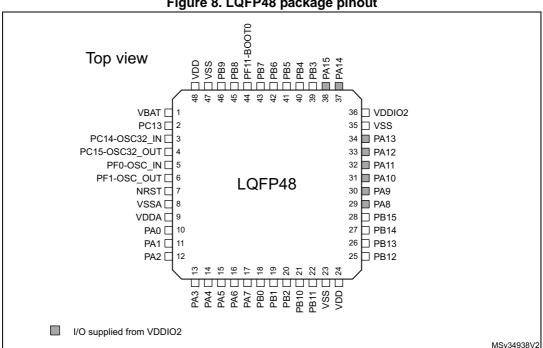


Figure 8. LQFP48 package pinout

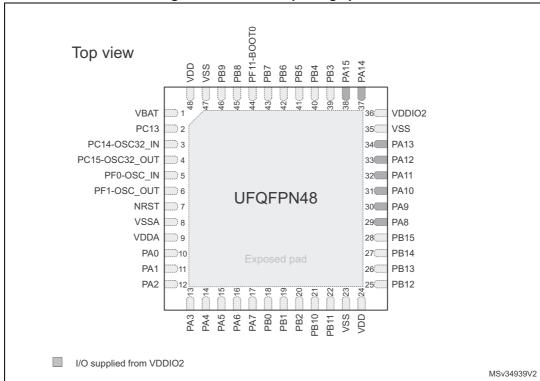


Figure 9. UFQFPN48 package pinout

Table 12. Legend/abbreviations used in the pinout table

Na	me	Abbreviation	Definition				
Pin r	name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name					
		S	Supply pin				
Pin	type	I/O	Input / output pin				
		FT	5 V-tolerant I/O				
		FTf 5 V-tolerant I/O, FM+ capable					
I/O str	ucture	TTa 3.3 V-tolerant I/O directly connected to ADC					
		TC Standard 3.3 V I/O					
		RST Bidirectional reset pin with embedded weak pull-up resistor					
No	tes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and reset.					
Pin	Alternate functions	Functions selected through GPIOx_AFR registers					
functions	Additional functions	Functions directly	selected/enabled through peripheral registers				

Table 13. STM32F091xB/xC pin definitions

	Pi	n nui	mber	s		1able 13. STM32	551	,,,,,	۲	Pin function	ıs
-	• •			- 						1 III Tallottol	
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48	Pin name (function upon reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
B2	1	-	-	-	-	PE2	I/O	FT		TSC_G7_IO1, TIM3_ETR	-
A1	2	-	-	-	-	PE3	I/O	FT		TSC_G7_IO2, TIM3_CH1	-
B1	3	-	-	-	-	PE4	I/O	FT		TSC_G7_IO3, TIM3_CH2	-
C2	4	-	-	-	-	PE5	I/O	FT		TSC_G7_IO4, TIM3_CH3	-
D2	5	-	-	-	-	PE6	I/O	FT		TIM3_CH4	WKUP3, RTC_TAMP3
E2	6	B2	1	B8	1	VBAT	S		-	Backup power s	upply
C1	7	A2	2	В7	2	PC13	I/O	TC	(1) (2)	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
D1	8	A1	3	C8	3	PC14- OSC32_IN (PC14)	I/O	TC	(1) (2)	-	OSC32_IN
E1	9	B1	4	C7	4	PC15- OSC32_OUT (PC15)	I/O	TC	(1) (2)	-	OSC32_OUT
F2	10	-	-	-	-	PF9	I/O	FT		TIM15_CH1, USART6_TX	-
G2	11	-	-	-	-	PF10	I/O	FT		TIM15_CH2, USART6_RX	-
F1	12	C1	5	D8	5	PF0-OSC_IN (PF0)	I/O	FTf		CRS_SYNC, I2C1_SDA	OSC_IN
G1	13	D1	6	E8	6	PF1-OSC_OUT (PF1)	1/0	FTf		I2C1_SCL	OSC_OUT
H2	14	E1	7	D7	7	NRST	1/0	RST		Device reset input / interr (active low)	•
H1	15	E3	8	E7	-	PC0	I/O	ТТа		EVENTOUT, USART6_TX, USART7_TX	ADC_IN10
J2	16	E2	9	F8	-	PC1	I/O	ТТа		EVENTOUT, USART6_RX, USART7_RX	ADC_IN11
J3	17	F2	10	D6	1	PC2	I/O	TTa		SPI2_MISO, I2S2_MCK, EVENTOUT, USART8_TX	ADC_IN12
K2	18	G1	11	E6	-	PC3	I/O	ТТа		SPI2_MOSI, I2S2_SD, EVENTOUT, USART8_RX	ADC_IN13

Table 13. STM32F091xB/xC pin definitions (continued)

	Pi	n nui	mber	s						Pin function	ns
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48	Pin name (function upon reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
J1	19	-	-	-	-	PF2	I/O	FT		EVENTOUT, USART7_TX, USART7_CK_RTS	WKUP8
K1	20	F1	12	G8	8	VSSA	S	-		Analog grou	nd
M1	21	H1	13	Н8	9	VDDA	S	ı		Analog power s	upply
L1	22	-	-	-	-	PF3	I/O	FT		EVENTOUT, USART7_RX, USART6_CK_RTS	
L2	23	G2	14	F7	10	PA0	I/O	ТТа		USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1, USART4_TX COMP1_OUT	RTC_TAMP2, WKUP1, ADC_IN0, COMP1_INM6
M2	24	H2	15	F6	11	PA1	I/O	ТТа		USART2_RTS, TIM2_CH2, TIM15_CH1N, TSC_G1_IO2, USART4_RX, EVENTOUT	ADC_IN1, COMP1_INP
K3	25	F3	16	E5	12	PA2	I/O	ТТа		USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3 COMP2_OUT	ADC_IN2, WKUP4, COMP2_INM6
L3	26	G3	17	H7	13	PA3	I/O	TTa		USART2_RX,TIM2_CH4, TIM15_CH2, TSC_G1_IO4	ADC_IN3, COMP2_INP
D3	27	C2	18	G7	-	VSS	S	-		Ground	
Н3	28	D2	19	G6	-	VDD	S	-		Digital power s	upply
М3	29	Н3	20	H6	14	PA4	I/O	ТТа		SPI1_NSS, I2S1_WS, TIM14_CH1, TSC_G2_IO1, USART2_CK, USART6_TX	COMP1_INM4, COMP2_INM4, ADC_IN4, DAC_OUT1
K4	30	F4	21	F5	15	PA5	I/O	ТТа		SPI1_SCK, I2S1_CK, CEC, TIM2_CH1_ETR, TSC_G2_IO2, USART6_RX	COMP1_INM5, COMP2_INM5, ADC_IN5, DAC_OUT2



Table 13. STM32F091xB/xC pin definitions (continued)

	Pi	n nui	mber	s						Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48	Pin name (function upon reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
L4	31	G4	22	G5	16	PA6	I/O	ТТа		SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS	ADC_IN6
M4	32	H4	23	E4	17	PA7	I/O	ТТа		SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7
K5	33	H5	24	H5	-	PC4	I/O	TTa		EVENTOUT, USART3_TX	ADC_IN14
L5	34	H6	25	F4	-	PC5	I/O	TTa		TSC_G3_IO1, USART3_RX	ADC_IN15, WKUP5
M5	35	F5	26	G4	18	PB0	I/O	ТТа		TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK	ADC_IN8
M6	36	G5	27	F3	19	PB1	I/O	ТТа		TIM3_CH4, USART3_RTS, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
L6	37	G6	28	H4	20	PB2	I/O	FT		TSC_G3_IO4	-
M7	38	ı	-	-	-	PE7	I/O	FT		TIM1_ETR, USART5_CK_RTS	-
L7	39	-	-	-	-	PE8	I/O	FT		TIM1_CH1N, USART4_TX	-
M8	40	-	-	-	-	PE9	I/O	FT		TIM1_CH1, USART4_RX	
L8	41	-	-	-	-	PE10	I/O	FT		TIM1_CH2N, USART5_TX	-
M9	42	-	-	-	-	PE11	I/O	FT		TIM1_CH2, USART5_RX	-
L9	43	-	-	-	-	PE12	I/O	FT		SPI1_NSS, I2S1_WS, TIM1_CH3N	-
M10	44	-	-	-	-	PE13	I/O	FT		SPI1_SCK, I2S1_CK, TIM1_CH3	-

Table 13. STM32F091xB/xC pin definitions (continued)

	Pi	n nui	nber	s						Pin function	ıs
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48	Pin name (function upon reset)	Pin type	Pin type I/O structure		Alternate functions	Additional functions
M11	45	ı	ı	-	-	PE14	I/O	FT		SPI1_MISO, I2S1_MCK, TIM1_CH4	-
M12	46	1	-	-	-	PE15	I/O	FT		SPI1_MOSI, I2S1_SD, TIM1_BKIN	-
L10	47	G7	29	G3	21	PB10	I/O	FTf		SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_TX, CEC, TSC_SYNC, TIM2_CH3	-
L11	48	H7	30	НЗ	22	PB11	I/O	FTf		USART3_RX, TIM2_CH4, EVENTOUT, TSC_G6_IO1, I2C2_SDA	-
F12	49	D5	31	H2	23	VSS	S	-		Ground	
G12	50	E5	32	H1	24	VDD	S	-		Digital power supply	
L12	51	H8	33	G2	25	PB12	I/O	FT		TIM1_BKIN, TIM15_BKIN, SPI2_NSS, I2S2_WS, USART3_CK, TSC_G6_IO2, EVENTOUT	-
K12	52	G8	34	F2	26	PB13	I/O	FTf		SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_CTS, TIM1_CH1N, TSC_G6_IO3	-
K11	53	F8	35	G1	27	PB14	I/O	FTf		SPI2_MISO, I2S2_MCK, I2C2_SDA, USART3_RTS, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	-
K10	54	F7	36	F1	28	PB15	I/O	FT		SPI2_MOSI, I2S2_SD, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	WKUP7, RTC_REFIN
K9	55	-	-	-	-	PD8	I/O	FT		USART3_TX	-
K8	56	-	-	-	-	PD9	I/O	FT		USART3_RX	-
J12	57	-	-	-	-	PD10	I/O	FT		USART3_CK	-
J11	58	-	-	-	-	PD11	I/O	FT		USART3_CTS	-



Table 13. STM32F091xB/xC pin definitions (continued)

	Pi	n nui	mber							Pin function	ıs
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48	Pin name (function upon reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
J10	59	ı	ı	-	ı	PD12	I/O	FT		USART3_RTS, TSC_G8_IO1, USART8_CK_RTS	-
H12	60	ı	ı	-	-	PD13	I/O	FT		TSC_G8_IO2, USART8_TX	-
H11	61	-	-	-	-	PD14	I/O	FT		TSC_G8_IO3, USART8_RX	-
H10	62	-	-	-	-	PD15	I/O	FT		TSC_G8_IO4, CRS_SYNC, USART7_CK_RTS	-
E12	63	F6	37	E1	-	PC6	I/O	FT	(3)	TIM3_CH1, USART7_TX	-
E11	64	E7	38	D1	-	PC7	I/O	FT	(3)	TIM3_CH2, USART7_RX	-
E10	65	E8	39	E2	-	PC8	I/O	FT	(3)	TIM3_CH3, USART8_TX	-
D12	66	D8	40	E3	-	PC9	I/O	FT	(3)	TIM3_CH4, USART8_RX	-
D11	67	D7	41	D2	29	PA8	I/O	FT	(3)	USART1_CK, TIM1_CH1, EVENTOUT, MCO, CRS_SYNC	-
D10	68	C7	42	C1	30	PA9	I/O	FT	(3)	USART1_TX, TIM1_CH2, TIM15_BKIN, MCO, TSC_G4_IO1, I2C1_SCL	-
C12	69	C6	43	C2	31	PA10	I/O	FT	(3)	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2, I2C1_SDA	-
B12	70	C8	44	D3	32	PA11	I/O	FT	(3)	CAN_RX, USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT, I2C2_SCL	-
A12	71	B8	45	B1	33	PA12	I/O	FT	(3)	CAN_TX, USART1_RTS, TIM1_ETR, COMP2_OUT, TSC_G4_IO4, EVENTOUT, I2C2_SDA	-
A11	72	A8	46	С3	34	PA13	I/O	FT	(3) (4)	IR_OUT, SWDIO	-
C11	73	-	-	-	-	PF6	I/O	FT	(3)	-	-
F11	74	D6	47	B2	35	VSS	S	-		Ground	
G11	75	E6	48	A1	36	VDDIO2	S	ı		Digital power su	ıpply

Table 13. STM32F091xB/xC pin definitions (continued)

	Pi	n nui	mber	s						Pin function	ıs
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48	Pin name (function upon reset)	Pin type	O/I		Alternate functions	Additional functions
A10	76	A7	49	В3	37	PA14	I/O	FT	(3) (4)	USART2_TX, SWCLK	-
A9	77	A6	50	A2	38	PA15	I/O	FT	(3)	SPI1_NSS, I2S1_WS, USART2_RX, USART4_RTS, TIM2_CH1_ETR, EVENTOUT	-
B11	78	В7	51	А3	-	PC10	I/O	FT	(3)	USART3_TX, USART4_TX	-
C10	79	В6	52	C4	-	PC11	I/O	FT	(3)	USART3_RX, USART4_RX	-
B10	80	C5	53	B4	-	PC12	I/O	FT	(3)	USART3_CK, USART4_CK, USART5_TX	-
C9	81	-	-	-	-	PD0	I/O	FT	(3)	SPI2_NSS, I2S2_WS, CAN_RX	-
В9	82	-	-	-	-	PD1	I/O	FT	(3)	SPI2_SCK, I2S2_CK CAN_TX	-
C8	83	B5	54	A4	-	PD2	I/O	FT	(3)	USART3_RTS, TIM3_ETR, USART5_RX	-
В8	84	-	-	-	-	PD3	I/O	FT		SPI2_MISO, I2S2_MCK, USART2_CTS	-
В7	85	-	-	-	-	PD4	I/O	FT		SPI2_MOSI, I2S2_SD, USART2_RTS	-
A6	86	-	-	-	-	PD5	I/O	FT		USART2_TX	-
В6	87	-	-	-	-	PD6	I/O	FT		USART2_RX	-
A5	88	-	-	-	-	PD7	I/O	FT		USART2_CK	-
A8	89	A5	55	D4	39	PB3	I/O	FT		SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT, USART5_TX	-
A7	90	A4	56	D5	40	PB4	I/O	FT		SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT, USART5_RX	-



Table 13. STM32F091xB/xC pin definitions (continued)

	Pi	n nui	mber	s						Pin function	ıs
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48	Pin name (function upon reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
C5	91	C4	57	C5	41	PB5	I/O	FT		SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2, USART5_CK_RTS	WKUP6
B5	92	D3	58	A5	42	PB6	I/O	FTf		I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03	-
B4	93	C3	59	B5	43	PB7	I/O	FTf		I2C1_SDA, USART1_RX, USART4_CTS, TIM17_CH1N, TSC_G5_IO4	-
A4	94	B4	60	C6	44	PF11-BOOT0	I/O	FT		-	Boot memory selection
A3	95	В3	61	A6	45	PB8	I/O	FTf		I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	-
В3	96	A3	62	В6	46	PB9	I/O	FTf		SPI2_NSS, I2S2_WS, I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT, CAN_TX	-
СЗ	97	ı	-	-	ı	PE0	I/O	FT		EVENTOUT, TIM16_CH1	-
A2	98	-	-	-	-	PE1	I/O	FT		EVENTOUT, TIM17_CH1	-
D3	99	D4	63	A7	47	VSS	S	-		Ground	
C4	100	E4	64	A8	48	VDD	S	-		Digital power su	ıpply

PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:

- The speed should not exceed 2 MHz with a maximum load of 30 pF.

- These GPIOs must not be used as current sources (e.g. to drive an LED).

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^{2.} After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.

^{3.} PC6, PC7, PC8, PC9, PA8, PA9, PA10, PA11, PA12, PA13, PF6, PA14, PA15, PC10, PC11, PC12, PD0, PD1 and PD2 I/Os are supplied by VDDIO2

^{4.} After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.



Table 14. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART2_CTS	TIM2_CH1_ETR	TSC_G1_IO1	USART4_TX	-	-	COMP1_OUT
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	TSC_G1_IO2	USART4_RX	TIM15_CH1N	-	-
PA2	TIM15_CH1	USART2_TX	TIM2_CH3	TSC_G1_IO3	-	-	-	COMP2_OUT
PA3	TIM15_CH2	USART2_RX	TIM2_CH4	TSC_G1_IO4	-	-	-	-
PA4	SPI1_NSS, I2S1_WS	USART2_CK	-	TSC_G2_IO1	TIM14_CH1	USART6_TX	-	-
PA5	SPI1_SCK, I2S1_CK	CEC	TIM2_CH1_ETR	TSC_G2_IO2	-	USART6_RX	-	-
PA6	SPI1_MISO, I2S1_MCK	TIM3_CH1	TIM1_BKIN	TSC_G2_IO3	USART3_CTS	TIM16_CH1	EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM1_CH1N	TSC_G2_IO4	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	CRS_SYNC	-	-	-
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2	TSC_G4_IO1	I2C1_SCL	MCO	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	TSC_G4_IO2	I2C1_SDA	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	TSC_G4_IO3	CAN_RX	I2C2_SCL	-	COMP1_OUT
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	TSC_G4_IO4	CAN_TX	I2C2_SDA	-	COMP2_OUT
PA13	SWDIO	IR_OUT	-	-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-	-
PA15	SPI1_NSS, I2S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT	USART4_RTS	-	-	-

	Table 15. Alternate functions selected through GPIOB_AFR registers for port B								
Pin name	AF0	AF1	AF2	AF3	AF4	AF5			
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2	USART3_CK	-			
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3	USART3_RTS	-			
PB2	-	-	-	TSC_G3_IO4	-	-			
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1	USART5_TX	-			
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2	USART5_RX	TIM17_BKIN			
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	USART5_CK_RTS	-			
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3	-	-			
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4	USART4_CTS	-			
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC	CAN_RX	-			
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	CAN_TX	SPI2_NSS, I2S2_WS			
PB10	CEC	I2C2_SCL	TIM2_CH3	TSC_SYNC	USART3_TX	SPI2_SCK, I2S2_CK			
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	TSC_G6_IO1	USART3_RX	-			
PB12	SPI2_NSS, I2S2_WS	EVENTOUT	TIM1_BKIN	TSC_G6_IO2	USART3_CK	TIM15_BKIN			
PB13	SPI2_SCK, I2S2_CK	-	TIM1_CH1N	TSC_G6_IO3	USART3_CTS	I2C2_SCL			
PB14	SPI2_MISO, I2S2_MCK	TIM15_CH1	TIM1_CH2N	TSC_G6_IO4	USART3_RTS	I2C2_SDA			
PB15	SPI2_MOSI, I2S2_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-			



Table 16. Alternate functions selected through GPIOC_AFR registers for port C

Pin name	AF0	AF1	AF2
PC0	EVENTOUT	USART7_TX	USART6_TX
PC1	EVENTOUT	USART7_RX	USART6_RX
PC2	EVENTOUT	SPI2_MISO, I2S2_MCK	USART8_TX
PC3	EVENTOUT	SPI2_MOSI, I2S2_SD	USART8_RX
PC4	EVENTOUT	USART3_TX	-
PC5	TSC_G3_IO1	USART3_RX	-
PC6	TIM3_CH1	USART7_TX	-
PC7	TIM3_CH2	USART7_RX	-
PC8	TIM3_CH3	USART8_TX	-
PC9	TIM3_CH4	USART8_RX	-
PC10	USART4_TX	USART3_TX	-
PC11	USART4_RX	USART3_RX	-
PC12	USART4_CK	USART3_CK	USART5_TX
PC13	-	-	-
PC14	-	-	-
PC15	-	-	-

Table 17. Alternate functions selected through GPIOD_AFR registers for port D

Pin name	AF0	AF1	AF2
PD0	CAN_RX	SPI2_NSS, I2S2_WS	-
PD1	CAN_TX	SPI2_SCK, I2S2_CK	-
PD2	TIM3_ETR	USART3_RTS	USART5_RX
PD3	USART2_CTS	SPI2_MISO, I2S2_MCK	-
PD4	USART2_RTS	SPI2_MOSI, I2S2_SD	-
PD5	USART2_TX	-	-
PD6	USART2_RX	-	-
PD7	USART2_CK	-	-
PD8	USART3_TX	-	-
PD9	USART3_RX	-	-
PD10	USART3_CK	-	-
PD11	USART3_CTS	-	-
PD12	USART3_RTS	TSC_G8_IO1	USART8_CK_RTS
PD13	USART8_TX	TSC_G8_IO2	-
PD14	USART8_RX	TSC_G8_IO3	-
PD15	CRS_SYNC	TSC_G8_IO4	USART7_CK_RTS

Table 18. Alternate functions selected through GPIOE_AFR registers for port E

Pin name	AF0	AF1
PE0	TIM16_CH1	EVENTOUT
PE1	TIM17_CH1	EVENTOUT
PE2	TIM3_ETR	TSC_G7_IO1
PE3	TIM3_CH1	TSC_G7_IO2
PE4	TIM3_CH2	TSC_G7_IO3
PE5	TIM3_CH3	TSC_G7_IO4
PE6	TIM3_CH4	-
PE7	TIM1_ETR	USART5_CK_RTS
PE8	TIM1_CH1N	USART4_TX
PE9	TIM1_CH1	USART4_RX
PE10	TIM1_CH2N	USART5_TX
PE11	TIM1_CH2	USART5_RX
PE12	TIM1_CH3N	SPI1_NSS, I2S1_WS
PE13	TIM1_CH3	SPI1_SCK, I2S1_CK
PE14	TIM1_CH4	SPI1_MISO, I2S1_MCK
PE15	TIM1_BKIN	SPI1_MOSI, I2S1_SD

Table 19. Alternate functions selected through GPIOF_AFR registers for port F

Pin name	AF0	AF1	AF2
PF0	CRS_SYNC	I2C1_SDA	-
PF1	-	I2C1_SCL	-
PF2	EVENTOUT	USART7_TX	USART7_CK_RTS
PF3	EVENTOUT	USART7_RX	USART6_CK_RTS
PF6	-	-	-
PF9	TIM15_CH1	USART6_TX	-
PF10	TIM15_CH2	USART6_RX	-



5 **Memory mapping**

To the difference of STM32F091xC memory map in Figure 10, the two bottom code memory spaces of STM32F091xB end at 0x0001 FFFF and 0x0801 FFFF, respectively.

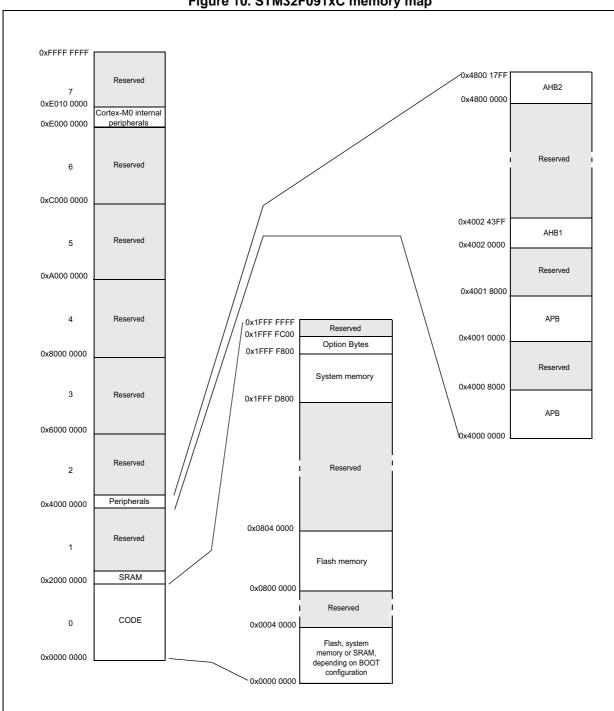


Figure 10. STM32F091xC memory map

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Table 20. STM32F091xB/xC peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
AHB2	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
ALIDZ	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
AHB1	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved

Table 20. STM32F091xB/xC peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
APB	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 2000 - 0x4001 23FF	1 KB	Reserved
	0x4001 1C00 – 0x4001 1FFF	1 KB	USART8
	0x4001 1800 – 0x4001 1BFF	1 KB	USART7
	0x4001 1400 – 0x4001 17FF	1 KB	USART6
	0x4001 0800 - 0x4001 13FF	3 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

Table 20. STM32F091xB/xC peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
	0x4000 7C00 - 0x4000 7FFF	1 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 6800 - 0x4000 6BFF	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	BxCAN
	0x4000 6100 - 0x4000 63FF	768 B	Reserved
	0x4000 6000 - 0x4000 60FF	256 B	CAN RAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	Reserved
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	USART5
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
APB	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1800 - 0x4000 1FFF	2 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25$ °C and $T_A = T_A$ max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

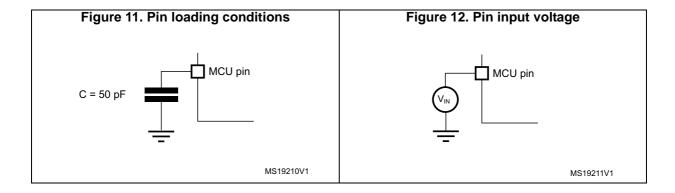
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 12.



6.1.6 Power supply scheme

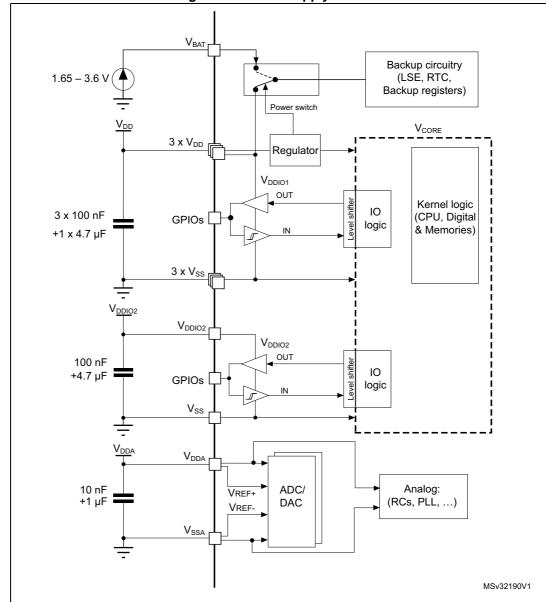


Figure 13. Power supply scheme

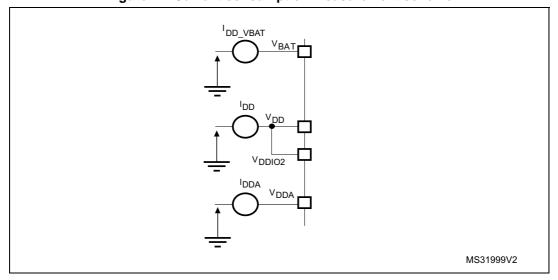
Caution:

Each power supply pair (V_{DD}/V_{SS} , V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

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6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 21: Voltage characteristics*, *Table 22: Current characteristics* and *Table 23: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 21. Voltage characteristics⁽¹⁾

Symbol	Ratings	Min	Max	Unit
V_{DD} – V_{SS}	External main supply voltage	- 0.3	4.0	V
V _{DDIO2} -V _{SS}	External I/O supply voltage	- 0.3	4.0	V
V _{DDA} -V _{SS}	External analog supply voltage	- 0.3	4.0	V
V _{DD} –V _{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	٧
V _{BAT} -V _{SS}	External backup supply voltage	- 0.3	4.0	V
	Input voltage on FT and FTf pins	V _{SS} - 0.3	V _{DDIOx} + 4.0 ⁽³⁾	٧
V _{IN} ⁽²⁾	Input voltage on TTa pins	V _{SS} - 0.3	4.0	V
	External main supply voltage -0.3 4.0 External I/O supply voltage -0.3 4.0 External analog supply voltage -0.3 4.0 Allowed voltage difference for $V_{DD} > V_{DDA}$ $ 0.4$ External backup supply voltage -0.3 4.0 Input voltage on FT and FTf pins $V_{SS} - 0.3$ $V_{DDIOx} + 4.0$	V		
$ \Delta V_{DDx} $	Variations between different V _{DD} power pins	-	50	mV
V _{SSx} - V _{SS}	•	-	50	mV
V _{ESD(HBM)}		<u> </u>		

All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

^{2.} V_{IN} maximum must always be respected. Refer to for the maximum allowed injected current values.

^{3.} Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

Table 22. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI _{VDD}	Total current into sum of all VDD power lines (source) ⁽¹⁾	120	
ΣI _{VSS}	Total current out of sum of all VSS ground lines (sink) ⁽¹⁾	-120	
I _{VDD(PIN)}	Maximum current into each VDD power pin (source) ⁽¹⁾	100	
I _{VSS(PIN)}	Maximum current out of each VSS ground pin (sink) ⁽¹⁾	-100	
,	Output current sunk by any I/O and control pin	25	
I _{IO(PIN)}	Output current source by any I/O and control pin	-25	
	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	80	
ΣΙ _{ΙΟ(PIN)}	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	-80	mA
	Total output current sourced by sum of all I/Os supplied by VDDIO2	-40	
	Injected current on FT and FTf pins	-5/+0 ⁽⁴⁾	
I _{INJ(PIN)} ⁽³⁾	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins ⁽⁵⁾	± 5	
ΣΙ _{ΙΝJ(PIN)}	Total injected current (sum of all I/O and control pins) ⁽⁶⁾	± 25	

- 1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
- 2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
- 3. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 21: Voltage characteristics* for the maximum allowed input voltage values.
- 4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
- On these I/Os, a positive injection is induced by V_{IN} > V_{DDA}. Negative injection disturbs the analog performance of the device. See note ⁽²⁾ below *Table 59: ADC accuracy*.
- When several inputs are submitted to a current injection, the maximum ΣI_{INJ(PIN)} is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 23. Thermal characteristics

Symbol	Ratings	Value	Unit
T _{STG}	Storage temperature range	-65 to +150	°C
T _J	Maximum junction temperature	150	°C



6.3 Operating conditions

6.3.1 General operating conditions

Table 24. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit	
f _{HCLK}	Internal AHB clock frequency	-	0	48	MHz	
f _{PCLK}	Internal APB clock frequency	-	0	48	IVII IZ	
V_{DD}	Standard operating voltage	-	2.0	3.6	V	
V _{DDIO2}	I/O supply voltage	Must not be supplied if V _{DD} is not present	1.65	3.6	V	
V	Analog operating voltage (ADC and DAC not used)	Must have a potential equal	V _{DD}	3.6	V	
V_{DDA}	Analog operating voltage (ADC and DAC used)	to or higher than V _{DD}	2.4	3.6	V	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V	
		TC and RST I/O	-0.3	V _{DDIOx} +0.3		
V_{IN}	I/O input voltage	TTa I/O	-0.3	V _{DDA} +0.3 ⁽¹⁾	V	
		FT and FTf I/O	-0.3	5.5 ⁽¹⁾		
		UFBGA100	-	364		
		LQFP100 -		476	ı	
	Power dissipation at T _A = 85 °C	LQFP64	-	455	mW	
P_{D}	for suffix 6 or T _A = 105 °C for suffix 7 ⁽²⁾	WLCSP64	-	377		
	suffix 7 ⁽²⁾	UFBGA64	-	308		
		LQFP48	-	370		
		UFQFPN48	-	625		
	Ambient temperature for the	Maximum power dissipation	-40	85	°C	
т.	suffix 6 version	Low power dissipation ⁽³⁾	-40	105	C	
TA	Ambient temperature for the	Maximum power dissipation	-40	105	°C	
	suffix 7 version	Low power dissipation ⁽³⁾	– 40 125		C	
TJ	lunction temperature resea	Suffix 6 version	-40	105	°C	
IJ	Junction temperature range	Suffix 7 version	-40	125		

^{1.} For operation with a voltage higher than V_{DDIOx} + 0.3 V, the internal pull-up resistor must be disabled.

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 25* are derived from tests performed under the ambient temperature condition summarized in *Table 24*.



^{2.} If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} . See Section 7.8: Thermal characteristics

In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see Section 7.8: Thermal characteristics).

Table 25. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t _{VDD}	V _{DD} rise time rate		0	∞	
	V _{DD} fall time rate	-	20	∞	
+	V _{DDA} rise time rate		0	∞	µs/V
t _{VDDA}	V _{DDA} fall time rate	-	20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 26* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Table 26. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{POR/PDR} ⁽¹⁾		Falling edge ⁽²⁾	1.80	1.88	1.96 ⁽³⁾	٧
YPOR/PDR	reset threshold	Rising edge	1.84 ⁽³⁾	1.92	2.00	V
V _{PDRhyst}	PDR hysteresis	-	-	40	-	mV
t _{RSTTEMPO} ⁽⁴⁾	Reset temporization	-	1.50	2.50	4.50	ms

The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.

Table 27. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
V _{PVD0}	F VD tilleshold 0	Falling edge	2	2.08	2.26 V 2.16 V 2.37 V 2.27 V 2.48 V 2.38 V 2.58 V 2.69 V 2.79 V	V
V	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
V _{PVD1}	PVD threshold 1	Falling edge	2.09	2.18	2.27	V
V	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
V _{PVD2}		Falling edge	2.18	2.28	2.38	V
V	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
V _{PVD3}	F VD tilleshold 3	Falling edge	2.28	2.38	2.48	V
V	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
V _{PVD4}	FVD tilleshold 4	Falling edge	2.37	2.48	2.48 2.59 V	V
V	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
V _{PVD5}	F AD HIRESHOID 3	Falling edge	2.47	2.58	2.69	V



^{2.} The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

^{3.} Data based on characterization results, not tested in production.

^{4.} Guaranteed by design, not tested in production.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
V _{PVD6}	F VD tillesiloid o	Falling edge 2.56 2.68 2.8	2.8	V		
V	PVD threshold 7	Rising edge	2.76	2.88	3	V
V _{PVD7}	PVD tillesiloid /	Falling edge	2.66	2.78	3 V 2.9 V	V
V _{PVDhyst} ⁽¹⁾	PVD hysteresis	-	-	100	-	mV
I _{DD(PVD)}	PVD current consumption	-	-	0.15	0.26 ⁽¹⁾	μA

Table 27. Programmable voltage detector characteristics (continued)

6.3.4 Embedded reference voltage

The parameters given in *Table 28* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{REFINT}	Internal reference voltage	-40 °C < T _A < +105 °C	1.2	1.23	1.25	V
t _{START}	ADC_IN17 buffer startup time	-	-	-	10 ⁽¹⁾	μs
t _{S_vrefint}	ADC sampling time when reading the internal reference voltage	-	4 ⁽¹⁾	-	-	μs
ΔV _{REFINT}	Internal reference voltage spread over the temperature range	V _{DDA} = 3 V	-	ı	10 ⁽¹⁾	mV
T _{Coeff}	Temperature coefficient	-	- 100 ⁽¹⁾	-	100 ⁽¹⁾	ppm/°C

Table 28. Embedded internal reference voltage

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.



^{1.} Guaranteed by design, not tested in production.

^{1.} Guaranteed by design, not tested in production.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency:
 - 0 wait state and Prefetch OFF from 0 to 24 MHz
 - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled f_{PCLK} = f_{HCLK}

The parameters given in *Table 29* to *Table 32* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.



Table 29. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V

		9. Typicai ai			II periphe				periphe			
Symbol	Parameter	Conditions	f _{HCLK}		N	lax @ T _A	(1)		М	ax @ T _A	(1)	Unit
Sy	Para			Тур	25 °C	85 °C	105 °C	Тур	25 °C	85 °C	105 °C	
		HSI48	48 MHz	26.9	29.5	30.3	30.6	14.7	16.1	16.3	16.4	
	lory	HOEL	48 MHz	26.7	29.2	30.1	30.3	14.6	16.0	16.2	16.2	
	Supply current in Run mode code executing from Flash memory	HSE bypass, PLL on	32 MHz	18.0	20.4	20.8	21.0	10.1	10.8	10.9	11.0	
	un m ash i		24 MHz	14.0	15.7	16.1	16.2	8.5	9.0	9.2	9.4	
	i R	HSE bypass,	8 MHz	4.8	5.3	5.5	5.9	3.0	3.2	3.3	3.5	
	rent y fror	PLL off	1 MHz	1.3	1.5	1.6	1.9	1.0	1.1	1.2	1.4	
	curi	1101 11 11	48 MHz	26.8	29.4	30.2	30.5	14.7	16.1	16.3	16.3	
	pply	HSI clock, PLL on	32 MHz	18.1	20.5	20.9	21.2	10.2	10.9	11.0	11.1	
	Sn ode 6		24 MHz	14.1	15.9	16.2	16.4	8.6	9.1	9.2	9.5	
	8	HSI clock, PLL off	8 MHz	4.9	5.4	5.6	5.9	3.1	3.2	3.4	3.5	mA
		HSI48	48 MHz	26.3	28.7	29.5	29.7	14.0	15.3	15.5	15.7	ША
			48 MHz	26.0	28.4	29.2	29.4	13.9	15.2	15.4	15.6	
	ode,	HSE bypass, PLL on	32 MHz	17.4	19.5	19.9	20.1	9.6	10.3	10.4	10.5	
	E &		24 MHz	13.3	15.1	15.5	15.6	7.6	8.2	8.4	8.5	
	n Ru y froi	HSE bypass, PLL off	8 MHz	4.4	4.9	5.1	5.3	2.4	2.6	2.8	2.9	
I_{DD}	ent ii uting		1 MHz	0.9	0.9	1.0	1.2	0.5	0.6	0.7	0.8	
	Supply current in Run mode, code executing from RAM		48 MHz	26.1	28.5	29.3	29.5	13.9	15.3	15.5	15.6	
	oply	HSI clock, PLL on	32 MHz	17.5	19.6	20.0	20.3	9.7	10.4	10.5	10.6	
	Sul		24 MHz	13.3	15.3	15.7	15.8	7.7	8.2	8.5	8.6	
		HSI clock, PLL off	8 MHz	4.6	5.0	5.2	5.4	2.5	2.7	2.9	3.0	
		HSI48	48 MHz	17.0	18.7	19.1	19.4	3.2	3.5	3.6	3.7	
			48 MHz	16.9	18.5	19.0	19.3	3.1	3.5	3.5	3.6	
	Pode	HSE bypass, PLL on	32 MHz	11.3	12.6	12.8	13.1	2.2	2.4	2.5	2.6	
	eb n		24 MHz	8.6	9.8	10.0	10.1	1.7	1.9	2.0	2.0	
	Sle	HSE bypass,	8 MHz	2.9	3.2	3.4	3.7	0.8	0.9	0.9	1.0	
	int ir	PLL off	1 MHz	0.4	0.6	0.6	0.7	0.3	0.4	0.4	0.5	mA
	urre		48 MHz	17.0	18.6	19.0	19.4	3.1	3.5	3.6	3.7	
	Supply current in Sleep mode	HSI clock, PLL on	32 MHz	11.4	12.7	13.0	13.2	2.3	2.5	2.6	2.7	
	Sup	0	24 MHz	8.7	9.9	10.1	10.2	1.8	2.0	2.1	2.2	
		HSI clock, PLL off	8 MHz	3.0	3.3	3.5	3.8	0.8	0.9	1.0	1.1	



1. Data based on characterization results, not tested in production unless otherwise specified.

Table 30. Typical and maximum current consumption from the V_{DDA} supply

	er			V _{DDA} = 2.4 V					V _{DDA}	= 3.6 \	/		
Symbol	a-met	Para-meter (1)	f _{HCLK}		М	Max @ T _A ⁽²⁾			М	ax @ T	A ⁽²⁾	Unit	
	Para			Тур	25 °C	85 °C	105 °C	Тур	25 °C	85 °C	105 °C		
		HSI48	48 MHz	312	333	338	347	316	334	341	350		
	Supply current in Run or Sleep	Supply bypas	HSE	48 MHz	147	168	178	181	160	181	192	197	
			bypass,	32 MHz	101	119	125	127	109	127	135	138	
		Run or	24 MHz	80	96	98	100	87	101	106	109		
		mode, bypass,	8 MHz	2.8	3.5	3.7	3.9	3.7	4.3	4.6	4.7		
I _{DDA}	,		1 MHz	2.7	3.2	3.5	3.8	3.3	3.9	4.4	4.7	μA	
	from		48 MHz	214	243	254	259	235	262	275	281		
	Flash memory	HSI clock, PLL on	32 MHz	166	193	203	204	185	207	216	220		
	or RAM			24 MHz	144	171	177	178	161	180	187	190	
		HSI clock, PLL off	8 MHz	65	83	85	86	77	90	92	93		

Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent from the frequency.

^{2.} Data based on characterization results, not tested in production unless otherwise specified.

Table 31. Typical and maximum consumption in Stop and Standby modes

Sym-	Para-		•		Тур	@V _{DD} (V _{DD} = \	/ _{DDA})	-	Max ⁽¹⁾				
bol	meter	Conditions		2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	Unit	
	Supply current in	mod	gulator in run de, all illators OFF	14.6	14.8	14.9	15.1	15.4	15.8	18	51	97		
I _{DD} mod	Stop mode	pow	gulator in low- ver mode, all illators OFF	3.3	3.4	3.6	3.8	4.1	4.4	11	53	106		
	Supply current in	LSI ON	ON and IWDG	0.9	1.0	1.1	1.2	1.3	1.4	2.3	2.7	3.6		
	Standby mode	LSI OF	OFF and IWDG	0.6	0.7	0.8	0.9	1.0	1.1	1.9	2.3	3.0		
	Supply current in Stop mode	current in	z	Regulator in run mode, all oscillators OFF	1.9	2.0	2.2	2.3	2.4	2.6	3.8	4.2	4.6	
			V _{DDA} monitoring O	Regulator in low-power mode, all oscillators OFF	1.9	2.0	2.2	2.3	2.4	2.6	3.8	4.2	4.6	μА
	current in Standby mode	V _{DE}	LSI ON and IWDG ON	2.3	2.5	2.7	2.8	3.0	3.3	3.8	4.2	4.8		
I _{DDA}		mode		LSI OFF and IWDG OFF	1.8	1.9	2.0	2.2	2.3	2.5	3.6	3.9	4.2	
IDDA	Supply	OFF	Regulator in run mode, all oscillators OFF	1.2	1.2	1.3	1.3	1.4	1.4	-	-	-		
	current in Stop mode	Stop	V _{DDA} monitoring OF	Regulator in low-power mode, all oscillators OFF	1.2	1.2	1.3	1.3	1.4	1.4	-	-	-	
	Supply current in	V _{DD}	LSI ON and IWDG ON	1.6	1.7	1.8	1.9	2.0	2.1	-	-	-		
	Standby mode	Standby		LSI OFF and IWDG OFF	1.1	1.1	1.1	1.2	1.3	1.3	-	-	-	

^{1.} Data based on characterization results, not tested in production unless otherwise specified.

Max⁽¹⁾ Typ @ V_{BAT} **Symbol Conditions** Unit **Parameter** 1.8 V 3.3 V T_A = 85 °C T_A = 105 °C 1.65 $T_A =$ 3.6 25°C LSE & RTC ON; "Xtal mode": lower driving 0.5 0.5 0.6 0.7 0.9 1.0 1.0 1.3 1.8 capability; RTC LSEDRV[1:0] = '00' domain μΑ I_{DD_VBAT} supply LSE & RTC ON; "Xtal current mode" higher driving 8.0 8.0 0.9 1.0 1.2 1.3 1.4 1.7 2.2 capability; LSEDRV[1:0] = '11'

Table 32. Typical and maximum current consumption from the V_{BAT} supply

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = V_{DDA} = 3.3 V
- All I/O pins are in analog input configuration
- The Flash memory access time is adjusted to f_{HCLK} frequency:
 - 0 wait state and Prefetch OFF from 0 to 24 MHz
 - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, f_{PCLK} = f_{HCLK}
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

^{1.} Data based on characterization results, not tested in production.

Table 33. Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal

Symbol	Parameter	£		sumption in mode	Typical con Sleep	Unit	
Symbol	, aramoto	f _{HCLK}	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Ollit
		48 MHz	26.7	15.1	16.4	3.8	
		36 MHz	20.4	11.8	12.7	3.3	
		32 MHz	18.5	11.0	11.4	3.0	
	Current	24 MHz	14.6	8.7	9.0	2.3	
	consumption	16 MHz	10.2	6.1	6.4	1.8	mA
I _{DD}	from V _{DD} supply	8 MHz	5.1	3.3	3.2	1.2	IIIA
	supply	4 MHz	3.3	2.2	2.3	1.1	
		2 MHz	2.2	1.7	1.7	1.1	
		1 MHz	1.6	1.4	1.4	1.1	
		500 kHz	1.4	1.2	1.2	1.0	
		48 MHz		17	72		
		36 MHz		13	31		
		32 MHz		1	19		
	Current	24 MHz		9	3		
1	consumption	16 MHz		6	57		μA
I _{DDA}	from V _{DDA}	8 MHz		2	.7		μΑ
	supply	4 MHz	2.7				
		2 MHz		2	.7		
		1 MHz		2	.7		
		500 kHz		2	.7		

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 53: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt



trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution:

Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 35: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

 I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_{S}$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.



Table 34. Switching output I/O current consumption

Symbol	Parameter	Conditions ⁽¹⁾	I/O toggling frequency (f _{SW})	Тур	Unit
			4 MHz	0.07	
		V _{DDIOx} = 3.3 V	8 MHz	0.15	
		$C = C_{INT}$	16 MHz	0.31	
			24 MHz	0.53	
			48 MHz	0.92	
			4 MHz	0.18	
		V _{DDIOx} = 3.3 V	8 MHz	0.37	
		$C_{EXT} = 0 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_{S}$	16 MHz	0.76	
			24 MHz	1.39	
	I/O current		48 MHz	2.188	
			4 MHz	0.32	
		$V_{DDIOx} = 3.3 \text{ V}$ $C_{EXT} = 10 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_{S}$	8 MHz	0.64	. mA
			16 MHz	1.25	
			24 MHz	2.23	
I _{SW}			48 MHz	4.442	
'500	consumption		4 MHz	0.49	
		$V_{DDIOx} = 3.3 V$ $C_{EXT} = 22 pF$ $C = C_{INT} + C_{EXT} + C_{S}$	8 MHz	0.94	
			16 MHz	2.38	
		INT EXT 0	24 MHz	3.99	
			4 MHz	0.64	
		$V_{DDIOx} = 3.3 \text{ V}$ $C_{EXT} = 33 \text{ pF}$	8 MHz	1.25	
		$C = C_{INT} + C_{EXT} + C_{S}$	16 MHz	3.24	
		INT EXT 0	24 MHz	5.02	
		V _{DDIOx} = 3.3 V	4 MHz	0.81	
		$C_{EXT} = 47 \text{ pF}$	8 MHz	1.7	
		$C = C_{INT} + C_{EXT} + C_{S}$ $C = C_{int}$	16 MHz	3.67	l
		V _{DDIOx} = 2.4 V	4 MHz	0.66	
		$C_{EXT} = 47 \text{ pF}$	8 MHz	1.43	
		$C = C_{INT} + C_{EXT} + C_{S}$	16 MHz	2.45	
		C = C _{int}	24 MHz	4.97	

^{1.} C_S = 7 pF (estimated value).



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 35*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 21: Voltage characteristics*

Table 35. Peripheral current consumption

	Peripheral	Typical consumption at 25 °C	Unit
	BusMatrix ⁽¹⁾	3.1	
	CRC	2.0	
	DMA1	5.5	
	DMA2	5.1	
	Flash memory interface	15.4	
	GPIOA	5.5	
AHB	GPIOB	5.4	μΑ/MHz
AIID	GPIOC	3.2	μΑνίνιι ιΖ
	GPIOD	3.1	
	GPIOE	4.0	
	GPIOF	2.5	
	SRAM	0.8	
	TSC	5.5	
	All AHB peripherals	61.0	

Table 35. Peripheral current consumption (continued)

	Peripheral	Typical consumption at 25 °C	Unit
	APB-Bridge ⁽²⁾	3.6	
	ADC ⁽³⁾	4.3	
	CAN	12.4	
	CEC	0.4	
	CRS	0.0	
	DAC ⁽³⁾	4.2	
	DBG (MCU Debug Support)	0.2	
	I2C1	2.9	
	I2C2	2.4	
	PWR	0.6	
	SPI1	8.8	
	SPI2	7.8	
	SYSCFG and COMP	1.9	
	TIM1	15.2	
	TIM14	2.6	
APB	TIM15	8.7	∧/\\
APB	TIM16	5.8	μA/MHz
	TIM17	7.0	
	TIM2	16.2	
	TIM3	11.9	
	TIM6	11.8	
	TIM7	2.5	
	USART1	17.6	
	USART2	16.3	
	USART3	16.2	
	USART4	4.7	
	USART5	4.4	
	USART6	5.5	
	USART7	5.2	
	USART8	5.1	
	WWDG	1.1	
	All APB peripherals	207.2	

^{1.} The BusMatrix is automatically active when at least one master is ON (CPU, DMA).



^{2.} The APB Bridge is automatically active when at least one peripheral is ON on the Bus.

The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, comparators, is not included. Refer to the tables of characteristics in the subsequent sections.

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 36* are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from Stop or Standby mode, SYSCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI line configured in event mode. The wakeup source from Standby mode is the WKUP1 pin (PA0).

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Symbol	Parameter	Conditions	Typ @Vdd = Vdda					Max	Unit
	rarameter	Conditions	= 2.0 V	= 2.4 V	= 2.7 V	= 3 V	= 3.3 V	IVIAX	Onic
	Wakeup from Stop mode	Regulator in run mode	3.2	3.1	2.9	2.9	2.8	5	
twustop		Regulator in low power mode	7.0	5.8	5.2	4.9	4.6	9	ue
t _{WUSTANDBY}	Wakeup from Standby mode	-	60.4	55.6	53.5	52	51	-	μs
t _{WUSLEEP}	Wakeup from Sleep mode	-		4 SY	SCLK cy	cles		-	

Table 36. Low-power mode wakeup timings

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 15: High-speed external clock source AC timing diagram*.

Table 37. High-speed external user clock characteristics

Symbol	Parameter ⁽¹⁾	Min	Тур	Max	Unit	
f _{HSE_ext}	User external clock source frequency	-	8	32	MHz	
V _{HSEH}	OSC_IN input pin high level voltage	0.7 V _{DDIOx}	ı	V_{DDIOx}	V	
V _{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	0.3 V _{DDIOx}	V	
$t_{w(HSEH)} \ t_{w(HSEL)}$	OSC_IN high or low time	15	-	-	ns	
$t_{r(HSE)}$ $t_{f(HSE)}$	r(HSE) OSC IN rise or fall time		-	20	115	



1. Guaranteed by design, not tested in production.

VHSEL

90%

10%

tr(HSE)

THSE

W(HSEH)

tw(HSEH)

tw(HSEL)

tw(HSEL)

MS19214V2

Figure 15. High-speed external clock source AC timing diagram

Low-speed external user clock generated from an external source

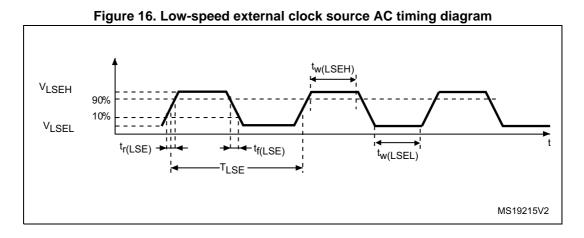
In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in Section 6.3.14. However, the recommended clock input waveform is shown in Figure 16.

Symbol	Parameter ⁽¹⁾	Min	Тур	Max	Unit
f _{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V _{LSEH}	OSC32_IN input pin high level voltage	0.7 V _{DDIOx}	-	V_{DDIOx}	V
V _{LSEL}	OSC32_IN input pin low level voltage	V _{SS}	-	0.3 V _{DDIOx}	٧
$\begin{matrix} t_{\text{w(LSEH)}} \\ t_{\text{w(LSEL)}} \end{matrix}$	OSC32_IN high or low time	450	1	1	ns
t _{r(LSE)}	OSC32_IN rise or fall time	-	-	50	115

Table 38. Low-speed external user clock characteristics

^{1.} Guaranteed by design, not tested in production.



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 39*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Conditions ⁽¹⁾	Min ⁽²⁾	Тур	Max ⁽²⁾	Unit
f _{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R _F	Feedback resistor	-	-	200	-	kΩ
		During startup ⁽³⁾	-	-	8.5	
		V_{DD} = 3.3 V, Rm = 30 Ω , CL = 10 pF@8 MHz	-	0.4	-	
	HSE current consumption	V_{DD} = 3.3 V, Rm = 45 Ω , CL = 10 pF@8 MHz	-	0.5	-	
I _{DD}		V_{DD} = 3.3 V, Rm = 30 Ω , CL = 5 pF@32 MHz	-	0.8	-	mA
		V_{DD} = 3.3 V, Rm = 30 Ω , CL = 10 pF@32 MHz	-	1	-	
		V _{DD} = 3.3 V, Rm = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
9 _m	Oscillator transconductance	Startup	10	-	-	mA/V
t _{SU(HSE)} ⁽⁴⁾	Startup time	V _{DD} is stabilized	-	2	-	ms

Table 39. HSE oscillator characteristics

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note:

For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.



^{1.} Resonator characteristics given by the crystal/ceramic resonator manufacturer.

^{2.} Guaranteed by design, not tested in production.

^{3.} This consumption level occurs during the first 2/3 of the $t_{\mbox{\scriptsize SU(HSE)}}$ startup time

^{4.} t_{SU(HSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

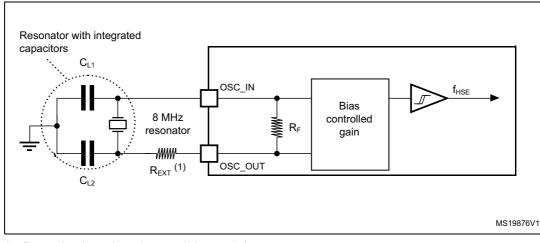


Figure 17. Typical application with an 8 MHz crystal

1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Conditions ⁽¹⁾	Min ⁽²⁾	Тур	Max ⁽²⁾	Unit
		low drive capability	-	0.5	0.9	
	I SE current consumption	medium-low drive capability	-	-	1	
I _{DD}	LSE current consumption	medium-high drive capability	-	-	1.3	μA
		high drive capability	-	-	1.6	
	Oscillator transconductance	low drive capability	5	-	-	
		medium-low drive capability	8	-	-	
9 _m		medium-high drive capability	15	-	-	μA/V
		high drive capability	25	-	-	
t _{SU(LSE)} ⁽³⁾	Startup time	V _{DDIOx} is stabilized	-	2	-	s

Table 40. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)



Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".

^{2.} Guaranteed by design, not tested in production.

^{3.} t_{SU(LSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note:

For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Resonator with integrated capacitors

OSC32_IN

Drive programmable amplifier

OSC32_OUT

OSC32_OUT

MS30253V2

Figure 18. Typical application with a 32.768 kHz crystal

Note:

An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 41* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*. The provided curves are characterization results, not tested in production.

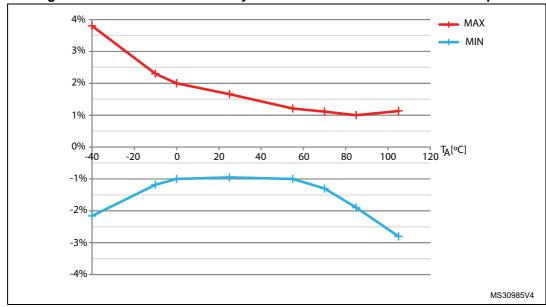
High-speed internal (HSI) RC oscillator

Table 41. HSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1 ⁽²⁾	%
DuCy _(HSI)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%
		$T_A = -40 \text{ to } 105^{\circ}\text{C}$	-2.8 ⁽³⁾	-	3.8 ⁽³⁾	
	Accuracy of the HSI oscillator	T _A = -10 to 85°C	-1.9 ⁽³⁾	-	2.3 ⁽³⁾	%
ACC		T _A = 0 to 85°C	-1.9 ⁽³⁾	-	2 ⁽³⁾	
ACC _{HSI}		T _A = 0 to 70°C	-1.3 ⁽³⁾	-	2 ⁽³⁾	70
		T _A = 0 to 55°C	-1 ⁽³⁾	-	2 ⁽³⁾	
		$T_A = 25^{\circ}C^{(4)}$	-1	-	1	
t _{su(HSI)}	HSI oscillator startup time	-	1 ⁽²⁾	-	2 ⁽²⁾	μs
I _{DDA(HSI)}	HSI oscillator power consumption	-	-	80	100 ⁽²⁾	μΑ

- 1. $V_{DDA} = 3.3 \text{ V}$, $T_A = -40 \text{ to } 105^{\circ}\text{C}$ unless otherwise specified.
- 2. Guaranteed by design, not tested in production.
- 3. Data based on characterization results, not tested in production.
- 4. Factory calibrated, parts not soldered.

Figure 19. HSI oscillator accuracy characterization results for soldered parts



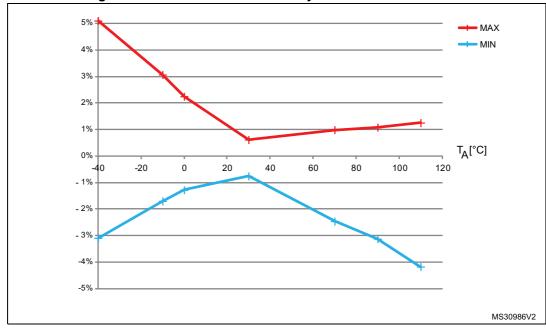
High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 42. HSI14 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{HSI14}	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1 ⁽²⁾	%
DuCy _(HSI14)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%
	Accuracy of the HSI14 oscillator (factory calibrated)	$T_A = -40 \text{ to } 105 ^{\circ}\text{C}$	-4.2 ⁽³⁾	-	5.1 ⁽³⁾	%
ACC		T _A = -10 to 85 °C	$-3.2^{(3)}$	-	3.1 ⁽³⁾	%
ACC _{HSI14}		T _A = 0 to 70 °C	-2.5 ⁽³⁾	-	2.3 ⁽³⁾	%
		T _A = 25 °C	-1	-	1	%
t _{su(HSI14)}	HSI14 oscillator startup time	-	1 ⁽²⁾	-	2 ⁽²⁾	μs
I _{DDA(HSI14)}	HSI14 oscillator power consumption	-	-	100	150 ⁽²⁾	μΑ

- 1. V_{DDA} = 3.3 V, T_{A} = -40 to 105 °C unless otherwise specified.
- 2. Guaranteed by design, not tested in production.
- 3. Data based on characterization results, not tested in production.

Figure 20. HSI14 oscillator accuracy characterization results



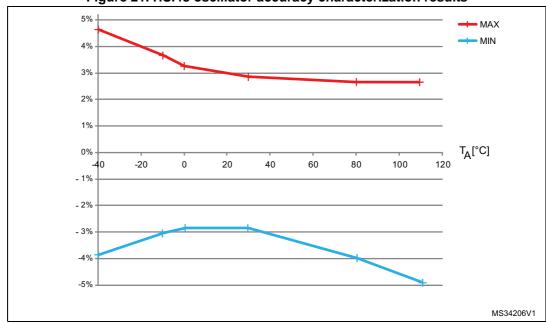
High-speed internal 48 MHz (HSI48) RC oscillator

Table 43. HSI48 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{HSI48}	Frequency	-	-	48	-	MHz
TRIM	HSI48 user-trimming step	-	0.09 ⁽²⁾	0.14	0.2 ⁽²⁾	%
DuCy _(HSI48)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%
	Accuracy of the HSI48	$T_A = -40 \text{ to } 105 ^{\circ}\text{C}$	-4.9 ⁽³⁾	-	4.7 ⁽³⁾	%
ACC		$T_A = -10 \text{ to } 85 ^{\circ}\text{C}$	-4.1 ⁽³⁾	-	3.7 ⁽³⁾	%
ACC _{HSI48}		T _A = 0 to 70 °C	-3.8 ⁽³⁾	-	3.4 ⁽³⁾	%
		T _A = 25 °C	-2.8	-	2.9	%
t _{su(HSI48)}	HSI48 oscillator startup time	-	-	-	6 ⁽²⁾	μs
I _{DDA(HSI48)}	HSI48 oscillator power consumption	-	-	312	350 ⁽²⁾	μА

- 1. V_{DDA} = 3.3 V, T_{A} = -40 to 105 °C unless otherwise specified.
- 2. Guaranteed by design, not tested in production.
- 3. Data based on characterization results, not tested in production.

Figure 21. HSI48 oscillator accuracy characterization results



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Low-speed internal (LSI) RC oscillator

Table 44. LSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Min	Тур	Max	Unit
f _{LSI}	Frequency	30	40	50	kHz
t _{su(LSI)} ⁽²⁾		-	-	85	μs
I _{DDA(LSI)} ⁽²⁾	LSI oscillator power consumption	-	0.75	1.2	μΑ

^{1.} V_{DDA} = 3.3 V, T_{A} = -40 to 105 °C unless otherwise specified.

6.3.9 PLL characteristics

The parameters given in *Table 45* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Table 45. PLL characteristics

Cumbal	Parameter	Value			Unit
Symbol	Farameter	Min	Тур	Max	Offic
r	PLL input clock ⁽¹⁾	1 ⁽²⁾	8.0	24 ⁽²⁾	MHz
f _{PLL_IN}	PLL input clock duty cycle	40 ⁽²⁾	-	60 ⁽²⁾	%
f _{PLL_OUT}	PLL multiplier output clock	16 ⁽²⁾	-	48	MHz
t _{LOCK}	PLL lock time	-	-	200 ⁽²⁾	μs
Jitter _{PLL}	Cycle-to-cycle jitter	-	-	300 ⁽²⁾	ps

Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL OUT}.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

Table 46. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Тур	Max ⁽¹⁾	Unit
t _{prog}	16-bit programming time	T _A = - 40 to +105 °C	40	53.5	60	μs
t _{ERASE}	Page (2 KB) erase time	T _A = - 40 to +105 °C	20	-	40	ms
t _{ME}	Mass erase time	T _A = - 40 to +105 °C	20	-	40	ms
	Supply current	Write mode	-	-	10	mA
IDD	Supply current	Erase mode	-	-	12	mA

^{1.} Guaranteed by design, not tested in production.



^{2.} Guaranteed by design, not tested in production.

^{2.} Guaranteed by design, not tested in production.

Symbol	Parameter	Conditions	Min ⁽¹⁾	Unit
N _{END}	Endurance	$T_A = -40 \text{ to } +105 ^{\circ}\text{C}$	10	kcycle
		1 kcycle ⁽²⁾ at T _A = 85 °C	30	
t _{RET}	Data retention	1 kcycle ⁽²⁾ at T _A = 105 °C	10	Year
		10 kcycle ⁽²⁾ at T _A = 55 °C	20	

Table 47. Flash memory endurance and data retention

- 1. Data based on characterization results, not tested in production.
- 2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 48*. They are based on the EMS levels and classes defined in application note AN1709.

Symbol	Parameter	Conditions	Level/ Class
V _{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 48 MHz, conforming to IEC 61000-4-2	2B
V _{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V _{DD} and V _{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25°C, f_{HCLK} = 48 MHz, conforming to IEC 61000-4-4	4B

Table 48. EMS characteristics

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

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Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Max vs. [fHSE/fHCLK] **Monitored** Conditions Unit Symbol Parameter frequency band 8/48 MHz 0.1 to 30 MHz 3 $V_{DD} = 3.6 \text{ V}, T_A = 25 ^{\circ}\text{C},$ 30 to 130 MHz 23 dBuV LQFP100 package Peak level S_{EMI} compliant with 130 MHz to 1 GHz 15 IEC 61967-2 **EMI Level** 4

Table 49. EMI characteristics

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Symbol	Ratings	Conditions	Packages	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C, conforming to JESD22-A114	All	2	2000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T _A = +25 °C, conforming to ANSI/ESD STM5.3.1	WLCSP64, LQFP100	C3	250	V
- (0)	(charge device moder)	IU ANSI/ESD STIVIS.S.T	All others	C4	500	

Table 50. ESD absolute maximum ratings

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 51. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T _A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{\rm SS}$ or above $V_{\rm DDIOx}$ (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 μ A/+0 μ A range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 52*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

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^{1.} Data based on characterization results, not tested in production.

Functional susceptibility **Symbol Description** Unit **Positive** Negative injection injection Injected current on BOOT0 -0 NA Injected current on PF1 pin (FTf pin) -0 NA Injected current on PC0 pin (TTA pin) -0 +5 mΑ $I_{IN,I}$ Injected current on PA4, PA5 pins with induced leakage NA -5 current on adjacent pins less than -20 µA Injected current on other FT and FTf pins -5 NA Injected current on all other TC, TTa and RST pins -5 +5

Table 52. I/O current injection susceptibility

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under the conditions summarized in *Table 24: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

Symbol **Parameter Conditions** Min Unit Тур Max TC and TTa I/O $0.3 V_{DDIOx} + 0.07^{(1)}$ Low level input FT and FTf I/O 0.475 V_{DDIOx}-0.2⁽¹⁾ V V_{IL} voltage All I/Os 0.3 V_{DDIOx} TC and TTa I/O 0.445 V_{DDIOx}+0.398⁽¹⁾ High level input $0.5 V_{DDIOx} + 0.2^{(1)}$ FT and FTf I/O V $V_{\text{IH}} \\$ voltage All I/Os 0.7 V_{DDIOx} 200(1) TC and TTa I/O Schmitt trigger V_{hys} mV hysteresis $100^{(1)}$ FT and FTf I/O TC, FT and FTf I/O TTa in digital mode ± 0.1 $V_{SS} \le V_{IN} \le V_{DDIOx}$ TTa in digital mode 1 Input leakage $V_{\text{DDIOx}} \le V_{\text{IN}} \le V_{\text{DDA}}$ μΑ I_{lkq} current⁽²⁾ TTa in analog mode ± 0.2 $V_{SS} \le V_{IN} \le V_{DDA}$ FT and FTf I/O 10 $V_{DDIOx} \le V_{IN} \le 5 V$

Table 53. I/O static characteristics

Table 53. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{PU}	Weak pull-up equivalent resistor (3)	V _{IN} = V _{SS}	25	40	55	kΩ
R _{PD}	Weak pull-down equivalent resistor ⁽³⁾	V _{IN} = - V _{DDIOx}	25	40	55	kΩ
C _{IO}	I/O pin capacitance	-	-	5	-	pF

- 1. Data based on design simulation only. Not tested in production.
- The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to Table 52: I/O current injection susceptibility.
- 3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* for standard I/Os, and in *Figure 23* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.



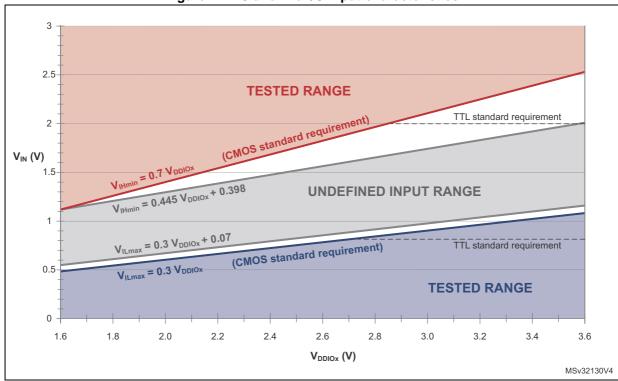
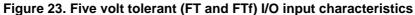
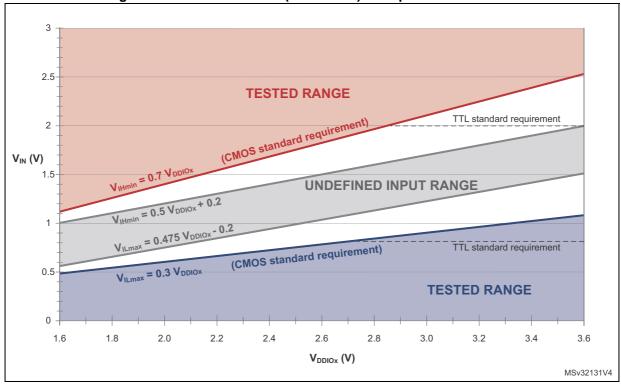


Figure 22. TC and TTa I/O input characteristics





Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOX}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 21: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see Table 21: Voltage characteristics).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 54. Output voltage characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OL}	Output low level voltage for an I/O pin	CMOS port ⁽²⁾	-	0.4	.,
V _{OH}	Output high level voltage for an I/O pin	$ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \ge 2.7 \text{ V}$	V _{DDIOx} -0.4	-	V
V _{OL}	Output low level voltage for an I/O pin	TTL port ⁽²⁾	-	0.4	.,
V _{OH}	Output high level voltage for an I/O pin	I _{IO} = 8 mA V _{DDIOx} ≥ 2.7 V	2.4	-	V
V _{OL} ⁽³⁾	Output low level voltage for an I/O pin	I _{IO} = 20 mA	-	1.3	V
V _{OH} ⁽³⁾	Output high level voltage for an I/O pin	V _{DDIOx} ≥ 2.7 V	V _{DDIOx} -1.3	-	V
V _{OL} ⁽³⁾	Output low level voltage for an I/O pin	I _{IO} = 6 mA	-	0.4	V
V _{OH} ⁽³⁾	Output high level voltage for an I/O pin	V _{DDIOx} ≥ 2 V	V _{DDIOx} -0.4	-	V
V _{OL} ⁽⁴⁾	Output low level voltage for an I/O pin	II I = 4 mA	-	0.4	V
V _{OH} ⁽⁴⁾	Output high level voltage for an I/O pin	I _{IO} = 4 mA	V _{DDIOx} -0.4	-	V
V _{OLFm+} ⁽³⁾	Output low level voltage for an FTf I/O pin in	I _{IO} = 20 mA V _{DDIOx} ≥ 2.7 V	-	0.4	V
	Fm+ mode	I _{IO} = 10 mA	-	0.4	V

The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 21:
 Voltage characteristics, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.

- 2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
- 3. Data based on characterization results. Not tested in production.
- 4. Data based on characterization results. Not tested in production.

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Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 24* and *Table 55*, respectively. Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Table 55. I/O AC characteristics⁽¹⁾⁽²⁾

OSPEEDRy [1:0] value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max	Unit
	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	2	MHz
	t _{f(IO)out}	Output fall time	C _L = 50 pF, V _{DDIOx} ≥ 2 V	-	125	ne
x0	t _{r(IO)out}	Output rise time		-	125	ns
XU	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	1	MHz
	t _{f(IO)out}	Output fall time	C _L = 50 pF, V _{DDIOx} < 2 V	-	125	ne
	t _{r(IO)out}	Output rise time		-	125	ns
	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	10	MHz
01	t _{f(IO)out}	Output fall time	C _L = 50 pF, V _{DDIOx} ≥ 2 V	-	25	ne
	t _{r(IO)out}	Output rise time		-	25	ns
	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	4	MHz
	t _{f(IO)out}	Output fall time	C _L = 50 pF, V _{DDIOx} < 2 V	-	62.5	ns
	t _{r(IO)out}	Output rise time		-	62.5	115
			C _L = 30 pF, V _{DDIOx} ≥ 2.7 V	-	50	
	f	Maximum frequency ⁽³⁾	C _L = 50 pF, V _{DDIOx} ≥ 2.7 V	-	30	MHz
	f _{max(IO)out}	Maximum nequency.	C _L = 50 pF, 2 V ≤ V _{DDIOx} < 2.7 V	-	20	IVII IZ
			C _L = 50 pF, V _{DDIOx} < 2 V	-	10	
			C _L = 30 pF, V _{DDIOx} ≥ 2.7 V	-	5	
11		Output fall time	C _L = 50 pF, V _{DDIOx} ≥ 2.7 V	-	8	
''	t _{f(IO)out}	Output fail time	C _L = 50 pF, 2 V ≤ V _{DDIOX} < 2.7 V	-	12	
			C _L = 50 pF, V _{DDIOx} < 2 V	-	25	ne
			C _L = 30 pF, V _{DDIOx} ≥ 2.7 V	-	5	ns
		Output rise time	C _L = 50 pF, V _{DDIOx} ≥ 2.7 V	-	8	
	t _{r(IO)} out	Output rise time	$C_L = 50 \text{ pF, } 2 \text{ V} \le \text{V}_{DDIOX} < 2.7 \text{ V}$	-	12	1
			C _L = 50 pF, V _{DDIOx} < 2 V	-	25	



OSPEEDRy [1:0] value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max	Unit
	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	2	MHz
Fm+ configuration (4)	t _{f(IO)out}	Output fall time	C _L = 50 pF, V _{DDIOx} ≥ 2 V	-	12	ne
	t _{r(IO)out}	Output rise time			34	ns
	f _{max(IO)out}	Maximum frequency ⁽³⁾			0.5	MHz
	t _{f(IO)out}	Output fall time	C _L = 50 pF, V _{DDIOx} < 2 V	-	16	ne
	t _{r(IO)out}	Output rise time			44	ns
-	t _{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

Table 55. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

- The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.
- 2. Guaranteed by design, not tested in production.
- 3. The maximum frequency is defined in Figure 24.
- When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

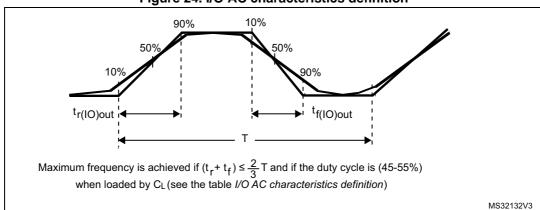


Figure 24. I/O AC characteristics definition

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} .

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

SymbolParameterConditionsMinTypMaxUnit $V_{\text{IL(NRST)}}$ NRST input low level voltage--- $0.3 \text{ V}_{\text{DD}} + 0.07^{(1)}$ $V_{\text{IH(NRST)}}$ NRST input high level voltage- $0.445 \text{ V}_{\text{DD}} + 0.398^{(1)}$ --

Table 56. NRST pin characteristics



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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{hys(NRST)}	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R _{PU}	Weak pull-up equivalent resistor ⁽²⁾	V _{IN} = V _{SS}	25	40	55	kΩ
V _{F(NRST)}	NRST input filtered pulse	-	-	-	100 ⁽¹⁾	ns
	NRST input not filtered pulse	2.7 < V _{DD} < 3.6	300 ⁽³⁾	-	-	ns
V _{NF(NRST)}	TVIXOT Input flot lilitered pulse	2.0 < V _{DD} < 3.6	500 ⁽³⁾	-	-	113

Table 56. NRST pin characteristics (continued)

- 1. Data based on design simulation only. Not tested in production.
- 2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).
- 3. Data based on design simulation only. Not tested in production.

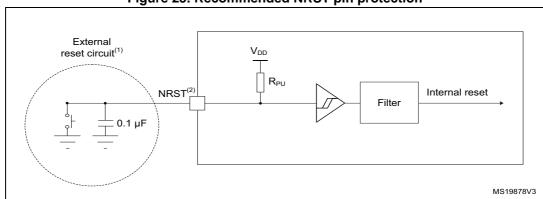


Figure 25. Recommended NRST pin protection

- 1. The external capacitor protects the device against parasitic resets.
- The user must ensure that the level on the NRST pin can go below the V_{IL(NRST)} max level specified in Table 56: NRST pin characteristics. Otherwise the reset will not be taken into account by the device.

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under the conditions summarized in *Table 24: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Symbol Conditions Unit **Parameter** Min Тур Max Analog supply voltage for 2.4 3.6 ٧ V_{DDA} ADC ON Current consumption of $V_{DDA} = 3.3 V$ 0.9 mA I_{DDA} (ADC) the ADC⁽¹⁾ ADC clock frequency 0.6 14 MHz f_{ADC} $f_S^{(2)}$ Sampling rate 12-bit resolution 0.043 1 MHz

Table 57. ADC characteristics

Table 57. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{TRIG} ⁽²⁾	External trigger frequency	f _{ADC} = 14 MHz, 12-bit resolution	-	-	823	kHz
11410		12-bit resolution	-	-	17	1/f _{ADC}
V _{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R _{AIN} ⁽²⁾	External input impedance	See Equation 1 and Table 58 for details	-	-	50	kΩ
R _{ADC} ⁽²⁾	Sampling switch resistance	1		kΩ		
C _{ADC} ⁽²⁾	Internal sample and hold capacitor	-	-	-	8	pF
t _{CAL} ⁽²⁾⁽³⁾	Calibration time	f _{ADC} = 14 MHz		5.9		μs
CAL, ,, ,	Calibration time	-		83		1/f _{ADC}
	ADO DD	ADC clock = HSI14	1.5 ADC cycles + 2 f _{PCLK} cycles	-	1.5 ADC cycles + 3 f _{PCLK} cycles	-
W _{LATENCY} (2)(4)	ADC_DR register ready latency	ADC clock = PCLK/2	-	4.5	-	f _{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f _{PCLK} cycle
		$f_{ADC} = f_{PCLK}/2 = 14 \text{ MHz}$		0.196		μs
		$f_{ADC} = f_{PCLK}/2$		5.5		1/f _{PCLK}
t _{latr} (2)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/4 = 12 \text{ MHz}$		0.219		μs
		$f_{ADC} = f_{PCLK}/4$		10.5		1/f _{PCLK}
		$f_{ADC} = f_{HSI14} = 14 \text{ MHz}$	0.179	-	0.250	μs
Jitter _{ADC}	ADC jitter on trigger conversion	f _{ADC} = f _{HSI14}	-	1	-	1/f _{HSI14}
t _S ⁽²⁾	Sampling time	f _{ADC} = 14 MHz	0.107	-	17.1	μs
ıs	Campling time	-	1.5	-	239.5	1/f _{ADC}
t _{STAB} ⁽²⁾	Stabilization time	-	14		1/f _{ADC}	
t _{CONV} ⁽²⁾	Total conversion time	f _{ADC} = 14 MHz, 12-bit resolution	1	-	18	μs
CONV 7	(including sampling time)	12-bit resolution	14 to 252 (t _S for successive ap			1/f _{ADC}

^{1.} During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 μA on I_{DD} and 60 μA on I_{DD} should be taken into account.

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^{2.} Guaranteed by design, not tested in production.

^{3.} Specified value includes only ADC timing. It does not include the latency of the register access.

^{4.} This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 58. R_{AIN} max for $f_{ADC} = 14$ MHz

T _s (cycles)	t _S (µs)	R _{AIN} max (kΩ) ⁽¹⁾
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

^{1.} Guaranteed by design, not tested in production.

Table 59. ADC accuracy⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Test conditions	Тур	Max ⁽⁴⁾	Unit
ET	Total unadjusted error		±1.3	±2	
EO	Offset error	f _{PCLK} = 48 MHz,	±1	±1.5	
EG	Gain error	f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 3 V to 3.6 V	±0.5	±1.5	LSB
ED	Differential linearity error	T _A = 25 °C	±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error		±3.3	±4	
EO	Offset error	f _{PCLK} = 48 MHz,	±1.9	±2.8	
EG	Gain error	f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 2.7 V to 3.6 V	±2.8	±3	LSB
ED	Differential linearity error	T _A = - 40 to 105 °C	±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error		±3.3	±4	
EO	Offset error	f _{PCLK} = 48 MHz,	±1.9	±2.8	
EG	Gain error	f_{ADC} = 14 MHz, R_{AIN} < 10 k Ω V_{DDA} = 2.4 V to 3.6 V T_A = 25 °C	±2.8	±3	LSB
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

^{1.} ADC DC accuracy values are measured after internal calibration.



- ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current
 - Any positive injection current within the limits specified for I_{INJ(PIN)} and ΣI_{INJ(PIN)} in Section 6.3.14 does not affect the ADC accuracy.
- Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
- Data based on characterization results, not tested in production.

Figure 26. ADC accuracy characteristics

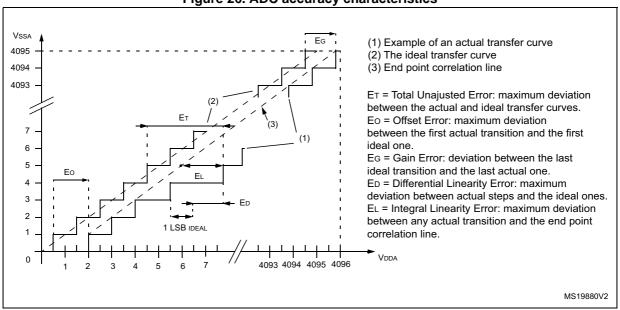
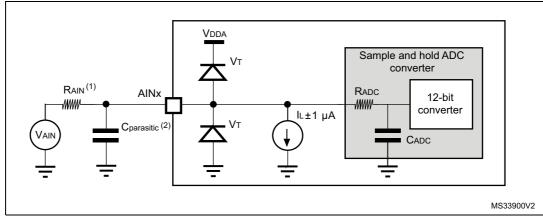


Figure 27. Typical connection diagram using the ADC



- Refer to Table 57: ADC characteristics for the values of R_{AIN} , R_{ADC} and C_{ADC} .
- $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in Figure 13: Power supply scheme. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

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6.3.17 DAC electrical specifications

Table 60. DAC characteristics

Symbol	Parameter	Min	Тур	Max	Unit	Comments
V _{DDA}	Analog supply voltage for DAC ON	2.4	-	3.6	٧	-
R _{LOAD} ⁽¹⁾	Resistive load with buffer	5	-	-	kΩ	Load connected to V _{SSA}
NLOAD.	ON	25	-	-	kΩ	Load connected to V _{DDA}
R _O ⁽¹⁾	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 $M\Omega$
C _{LOAD} ⁽¹⁾	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer ON	0.2	-	-	٧	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer ON	-	-	V _{DDA} – 0.2	V	$V_{\rm DDA}$ = 3.6 V and (0x155) and (0xEAB) at $V_{\rm DDA}$ = 2.4 V
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer OFF	-	_	V _{DDA} – 1LSB	٧	excursion of the DAC.
I _{DDA} ⁽¹⁾	DAC DC current consumption in quiescent	-	-	600	μA	With no load, middle code (0x800) on the input
·DDA	mode ⁽²⁾	-	-	700	μA	With no load, worst code (0xF1C) on the input
DNL ⁽³⁾	Differential non linearity Difference between two	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
	consecutive code-1LSB)	-	-	±2	LSB	Given for the DAC in 12-bit configuration
	Integral non linearity (difference between	-	-	±1	LSB	Given for the DAC in 10-bit configuration
INL ⁽³⁾	measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±4	LSB	Given for the DAC in 12-bit configuration
	Offset error	-	-	±10	mV	-
Offset ⁽³⁾	(difference between measured value at Code	-	-	±3	LSB	Given for the DAC in 10-bit at V _{DDA} = 3.6 V
	(0x800) and the ideal value = V _{DDA} /2)	-	-	±12	LSB	Given for the DAC in 12-bit at V _{DDA} = 3.6 V



Table 60. DAC characteristics (continued)

Symbol	Parameter	Min	Тур	Max	Unit	Comments	
Gain error ⁽³⁾	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration	
t _{SETTLING} (3)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	μs	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ	
Update rate ⁽³⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \le 50 \text{ pF, } R_{LOAD} \ge 5 \text{ k}\Omega$	
t _{WAKEUP} (3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	μs	$C_{LOAD} \le 50$ pF, $R_{LOAD} \ge 5$ k Ω input code between lowest and highest possible ones.	
PSRR+ (1)	Power supply rejection ratio (to V _{DDA}) (static DC measurement	-	-67	-40	dB	No R _{LOAD} , C _{LOAD} = 50 pF	

^{1.} Guaranteed by design, not tested in production.

^{2.} The DAC is in "quiescent mode" when it keeps the value steady on the output so no dynamic consumption is involved.

^{3.} Data based on characterization results, not tested in production.

6.3.18 Comparator characteristics

Table 61. Comparator characteristics

Symbol	Parameter	Conditi	ons	Min ⁽¹⁾	Тур	Max ⁽¹⁾	Unit
V_{DDA}	Analog supply voltage	-		V_{DD}	-	3.6	V
V _{IN}	Comparator input voltage range	-		0	-	V_{DDA}	1
V _{SC}	V _{REFINT} scaler offset voltage	-		-	±5	±10	mV
t _{S_SC}	V _{REFINT} scaler startup time from power down	-		-	-	0.2	ms
t _{START}	Comparator startup time	Startup time to reach prospecification	opagation delay	-	-	60	μs
		Ultra-low power mode		-	2	4.5	
	Propagation delay for	Low power mode		-	0.7	1.5	μs
	200 mV step with 100 mV overdrive	Medium power mode	-	0.3	0.6		
		High speed mode	V _{DDA} ≥ 2.7 V	-	50	100	- ns
		High speed mode	V _{DDA} < 2.7 V	-	100	240	
t _D		Ultra-low power mode		-	2	7	
	Propagation delay for	Low power mode		-	0.7	2.1	μs
	full range step with	Medium power mode		-	0.3	1.2	
	100 mV overdrive	High speed mode	V _{DDA} ≥ 2.7 V	-	90	180	ne
		Triigit speed mode	V _{DDA} < 2.7 V	-	110	300	ns
V _{offset}	Comparator offset error	-		-	±4	±10	mV
dV _{offset} /dT	Offset error temperature coefficient	-		-	18	-	μV/°C
		Ultra-low power mode		-	1.2	1.5	
 	COMP current	Low power mode		-	3	5	^
I _{DD(COMP)}	consumption	Medium power mode		-	10	15	μA
		High speed mode		-	75	100	

Table 61. Comparator characteristics (continued)

Symbol	Parameter	Conditions		Min ⁽¹⁾	Тур	Max ⁽¹⁾	Unit
		No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	
	Low hysteresis	High speed mode	3		13		
		(COMPxHYST[1:0]=01)		5	8	10	
V _{hys}	Comparator hysteresis	Medium hysteresis	High speed mode	7		26	mV
		(COMPxHYST[1:0]=10)	All other power modes	9	15	19	
		High hysteresis	High speed mode	18		49	
		(COMPxHYST[1:0]=11)	All other power modes	19	31	40	

^{1.} Data based on characterization results, not tested in production.



6.3.19 Temperature sensor characteristics

Table 62. TS characteristics

Symbol	Parameter	Min	Тур	Max	Unit
T _L ⁽¹⁾	V _{SENSE} linearity with temperature	-	± 1	± 2	°C
Avg_Slope ⁽¹⁾	Average slope	4.0	4.3	4.6	mV/°C
V ₃₀	Voltage at 30 °C (± 5 °C) ⁽²⁾	1.34	1.43	1.52	V
t _{START} ⁽¹⁾	ADC_IN16 buffer startup time	-	-	10	μs
t _{S_temp} ⁽¹⁾	ADC sampling time when reading the temperature	4	-	-	μs

^{1.} Guaranteed by design, not tested in production.

6.3.20 V_{BAT} monitoring characteristics

Table 63. V_{BAT} monitoring characteristics

Symbol	Parameter		Тур	Max	Unit
R	Resistor bridge for V _{BAT}	-	2 x 50	-	kΩ
Q	Ratio on V _{BAT} measurement	-	2	-	-
Er ⁽¹⁾	Error on Q	– 1	-	+1	%
t _{S_vbat} ⁽¹⁾	ADC sampling time when reading the V _{BAT}	4	-	-	μs

^{1.} Guaranteed by design, not tested in production.

6.3.21 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to Section 6.3.14: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 64. TIMx characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t(TIM)	Timer resolution time	-	-	1	-	t _{TIMxCLK}
^t res(TIM)	Time resolution time	f _{TIMxCLK} = 48 MHz	ı	20.8	ı	ns
	Timer external clock	-	ı	f _{TIMxCLK} /2	ı	MHz
f _{EXT}	frequency on CH1 to CH4	f _{TIMxCLK} = 48 MHz	-	24	-	MHz
	16-bit timer maximum	-	-	2 ¹⁶	-	t _{TIMxCLK}
tuan count	period	f _{TIMxCLK} = 48 MHz	ı	1365	ı	μs
^t MAX_COUNT	32-bit counter	-		2 ³²		t _{TIMxCLK}
	maximum period	f _{TIMxCLK} = 48 MHz	-	89.48	-	s



Measured at V_{DDA} = 3.3 V ± 10 mV. The V₃₀ ADC conversion result is stored in the TS_CAL1 byte. Refer to Table 3: Temperature sensor calibration values.

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	ms
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

Table 65. IWDG min/max timeout period at 40 kHz (LSI)⁽¹⁾

These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

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Prescaler WDGTB		Min timeout value	Max timeout value	Unit			
1	0	0.0853	5.4613				
2	1	0.1706	10.9226	me			
4	2	0.3413	21.8453	ms			
8	3	0.6826	43.6906				

Table 66. WWDG min/max timeout value at 48 MHz (PCLK)

6.3.22 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are guaranteed by design when the I2Cx peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{\rm DDIOX}$ is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to Section 6.3.14: I/O port characteristics for the I²C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

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Table 67. I²C analog filter characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t _{AF}	Maximum width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns

- 1. Guaranteed by design, not tested in production.
- 2. Spikes with widths below t_{AF(min)} are filtered.
- 3. Spikes with widths above $t_{\text{AF}(\text{max})}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 68* for SPI or in *Table 69* for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 24: General operating conditions*.

Refer to Section 6.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 68. SPI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f _{SCK}	SPI clock frequency	Master mode	-	18	MHz
1/t _{c(SCK)}	SPI Clock frequency	Slave mode	=	18	IVIIIZ
t _{r(SCK)}	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
t _{su(NSS)}	NSS setup time	Slave mode	4Tpclk	-	
t _{h(NSS)}	NSS hold time	Slave mode	2Tpclk + 10	-	
t _{w(SCKH)} t _{w(SCKL)}	SCK high and low time	Master mode, f _{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
t _{su(MI)}	Data input setup time	Master mode	4	-	
t _{su(SI)}	Data input setup time	Slave mode	5	-	
t _{h(MI)}	Data input hold time	Master mode	4	-	
t _{h(SI)}	Data input hold time	Slave mode	5	-	ns
t _{a(SO)} ⁽²⁾	Data output access time	Slave mode, f _{PCLK} = 20 MHz	0	3Tpclk	
t _{dis(SO)} (3)	Data output disable time	Slave mode	0	18	
t _{v(SO)}	Data output valid time	Slave mode (after enable edge)	-	22.5	
t _{v(MO)}	Data output valid time	Master mode (after enable edge)	-	6	
t _{h(SO)}	Data output hold time	Slave mode (after enable edge)	11.5	-	
t _{h(MO)}	Data output noid tille	Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

- 1. Data based on characterization results, not tested in production.
- 2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
- 3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z



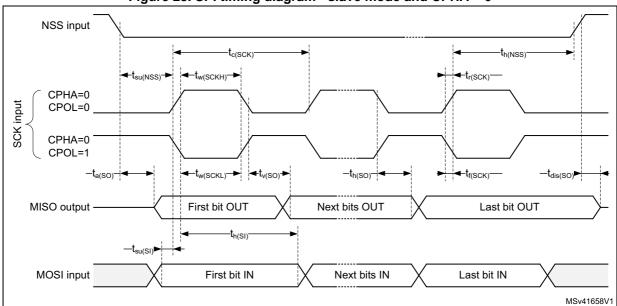
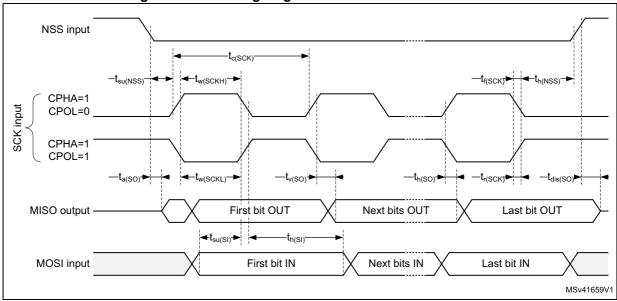


Figure 28. SPI timing diagram - slave mode and CPHA = 0





1. Measurement points are done at CMOS levels: 0.3 $V_{\rm DD}$ and 0.7 $V_{\rm DD}$.

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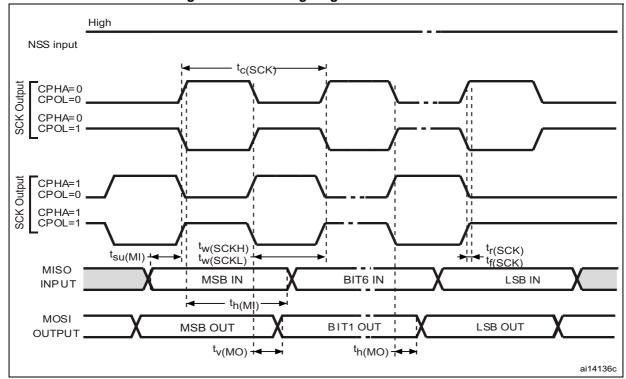


Figure 30. SPI timing diagram - master mode

1. Measurement points are done at CMOS levels: 0.3 $V_{\rm DD}$ and 0.7 $V_{\rm DD}$.

Table 69. I²S characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f _{CK}	I ² S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
1/t _{c(CK)}		Slave mode	0	6.5	
t _{r(CK)}	I ² S clock rise time	Canacitive land C = 15 pF	-	10	
t _{f(CK)}	I ² S clock fall time	Capacitive load C _L = 15 pF	-	12	
t _{w(CKH)}	I ² S clock high time	Master f _{PCLK} = 16 MHz, audio	306	-	
t _{w(CKL)}	I ² S clock low time	frequency = 48 kHz	312	-	
t _{v(WS)}	WS valid time	Master mode	2	-	ns
t _{h(WS)}	WS hold time	Master mode	2	-	
t _{su(WS)}	WS setup time	Slave mode	7	-	
t _{h(WS)}	WS hold time	Slave mode	0	-	
DuCy(SCK)	I ² S slave input clock duty cycle	Slave mode	25	75	%

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Symbol	Parameter	Conditions	Min	Max	Unit		
t _{su(SD_MR)}	Data input setup time	Master receiver	6	-			
t _{su(SD_SR)}	Data input setup time	Slave receiver	2	-			
t _{h(SD_MR)} ⁽²⁾	Data input hold time	Master receiver	4	-			
t _{h(SD_SR)} (2)	Data input hold time	Slave receiver	0.5	-	no		
t _{v(SD_MT)} ⁽²⁾	Data output valid time	Master transmitter	-	4	ns		
t _{v(SD_ST)} ⁽²⁾	Data output valid time	Slave transmitter	-	20			
t _{h(SD_MT)}	Data output hold time	Master transmitter	0	-			
t _{h(SD_ST)}	Data output hold time	Slave transmitter	13	-			

Table 69. I²S characteristics⁽¹⁾ (continued)

- 1. Data based on design simulation and/or characterization results, not tested in production.
- 2. Depends on f_{PCLK} . For example, if f_{PCLK} = 8 MHz, then T_{PCLK} = 1/ f_{PLCLK} = 125 ns.

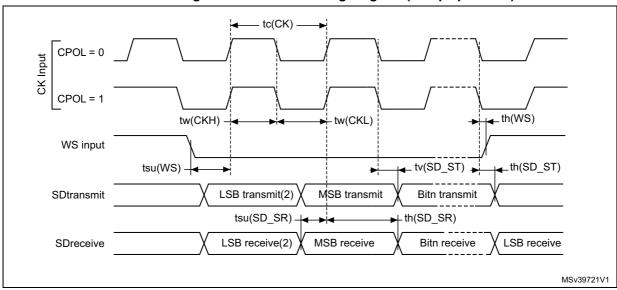


Figure 31. I²S slave timing diagram (Philips protocol)

- 1. Measurement points are done at CMOS levels: 0.3 × V_{DDIOx} and 0.7 × V_{DDIOx} .
- 2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

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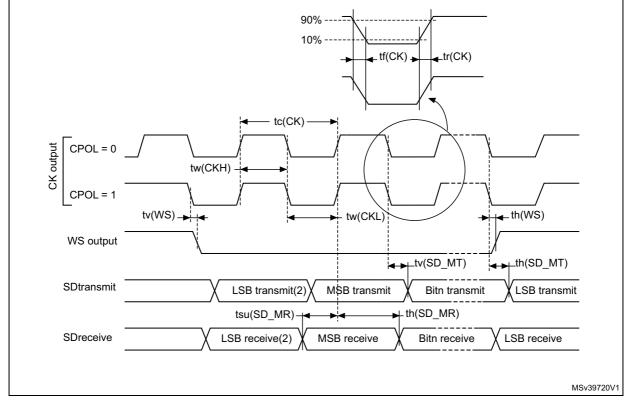


Figure 32. I²S master timing diagram (Philips protocol)

- 1. Data based on characterization results, not tested in production.
- 2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

CAN (controller area network) interface

Refer to Section 6.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

7.1 UFBGA100 package information

UFBGA100 is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra-fine-profile ball grid array package.

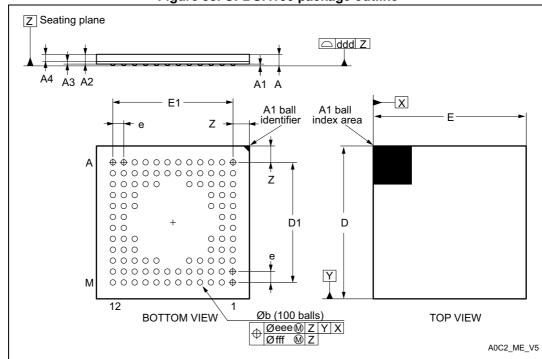


Figure 33. UFBGA100 package outline

1. Drawing is not to scale.

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Table 70. UFBGA100 package mechanical data

Compleal		millimeters		inches ⁽¹⁾		
Symbol N	Min.	Тур.	Max.	Min.	Тур.	Max.
Α	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-

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inches⁽¹⁾ millimeters Symbol Min. Тур. Max. Min. Тур. Max. 0.240 0.290 0.340 0.0094 0.0114 0.0134 b D 6.850 7.000 7.150 0.2697 0.2756 0.2815 5.500 0.2165 D1 Ε 0.2697 6.850 7.000 7.150 0.2756 0.2815 E1 5.500 0.2165 е 0.500 0.0197 Ζ 0.750 0.0295 ddd 0.080 0.0031 eee 0.150 0.0059 fff 0.050 0.0020

Table 70. UFBGA100 package mechanical data (continued)

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Figure 34. Recommended footprint for UFBGA100 package

Table 71. UFBGA100 recommended PCB design rules

Dimension	Recommended values		
Pitch	0.5		
Dpad	0.280 mm		
Dsm	0.370 mm typ. (depends on the solder mask registration tolerance)		
Stencil opening	0.280 mm		
Stencil thickness	Between 0.100 mm and 0.125 mm		

A0C2_FP_V1

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

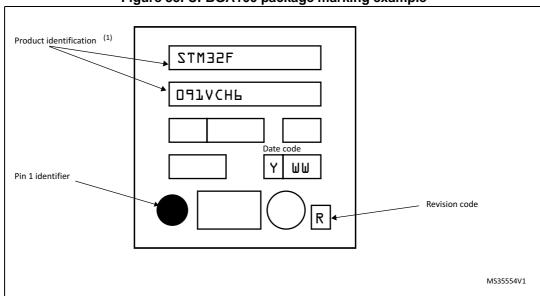


Figure 35. UFBGA100 package marking example

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



7.2 LQFP100 package information

LQFP100 is a100-pin, 14 x 14 mm low-profile quad flat package.

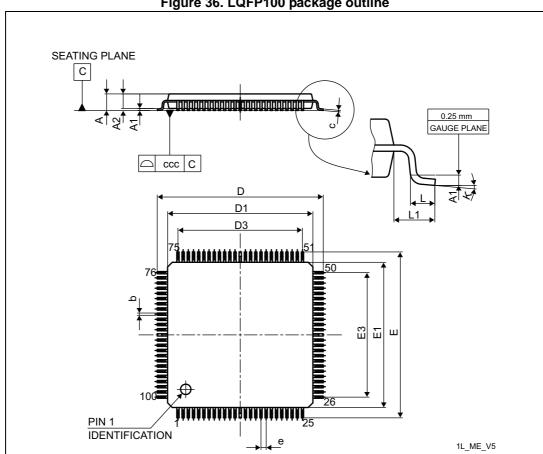


Figure 36. LQFP100 package outline

1. Drawing is not to scale.

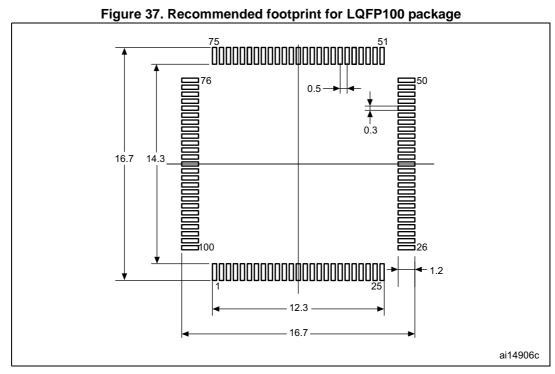
Table 72. LQPF100 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Max	Min	Тур	Max
Α	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
Е	15.800	16.000	16.200	0.6220	0.6299	0.6378

0	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Max	Min	Тур	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
е	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
CCC	-	-	0.080	-	-	0.0031

Table 72. LQPF100 package mechanical data (continued)

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

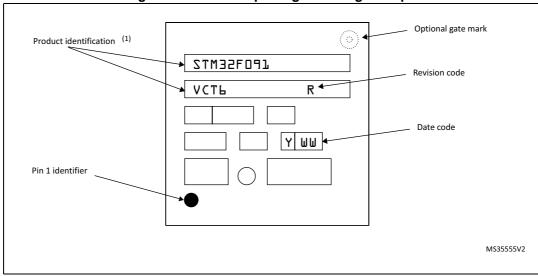


Figure 38. LQFP100 package marking example

Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet
qualified and therefore not yet ready to be used in production and any consequences deriving from such
usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering
samples in production. ST Quality has to be contacted prior to any decision to use these Engineering
Samples to run qualification activity.

7.3 UFBGA64 package information

UFBGA64 is a 64-ball, 5 x 5 mm, 0.5 mm pitch ultra-fine-profile ball grid array package.

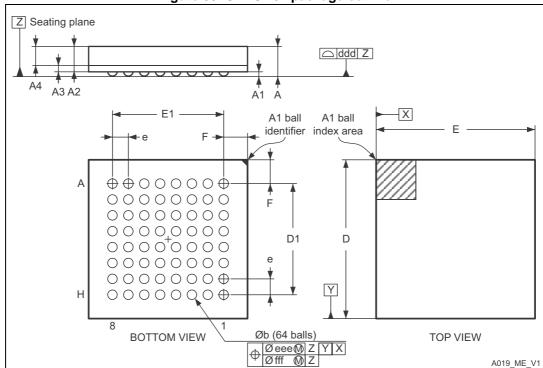


Figure 39. UFBGA64 package outline

1. Drawing is not to scale.

Table 73. UFBGA64 package mechanical data

Sumbal	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Max	Min	Тур	Max
Α	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
Е	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
е	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

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Table 73. UFBGA64 package mechanical data (continued)

Symbol		millimeters		inches ⁽¹⁾		
Symbol	Min	Тур	Max	Min	Тур	Max
Α	0.460	0.530	0.600	0.0181	0.0209	0.0236
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. Recommended footprint for UFBGA64 package

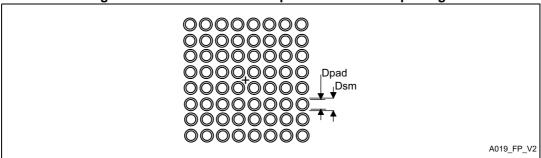


Table 74. UFBGA64 recommended PCB design rules

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

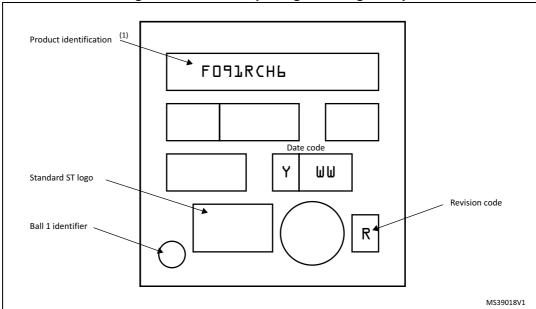


Figure 41. UFBGA64 package marking example

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



7.4 WLCSP64 package information

WLCSP64 is a 64-ball, 3.347 x 3.585 mm, 0.4 mm pitch wafer-level chip-scale package.

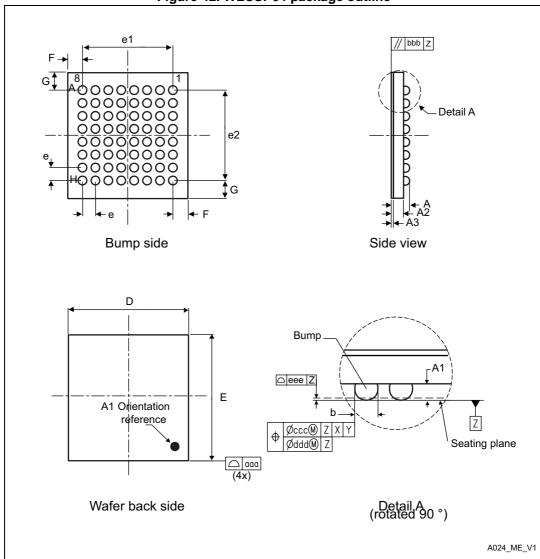


Figure 42. WLCSP64 package outline

1. Drawing is not to scale.

Table 75. WLCSP64 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Max	Min	Тур	Max
Α	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-

Symbol	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Max	Min	Тур	Max
b ⁽²⁾	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.312	3.347	3.382	0.1304	0.1318	0.1331
Е	3.550	3.585	3.620	0.1398	0.1411	0.1425
е	-	0.400	-	-	0.0157	-
e1	-	2.800	-	-	0.1102	-
e2	-	2.800	-	-	0.1102	-
F	-	0.2735	-	-	0.0108	-
G	-	0.3925	-	-	0.0155	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

Table 75. WLCSP64 package mechanical data (continued)

- 1. Values in inches are converted from mm and rounded to 4 decimal digits.
- 2. Dimension is measured at the maximum bump diameter parallel to primary datum ${\sf Z}$.

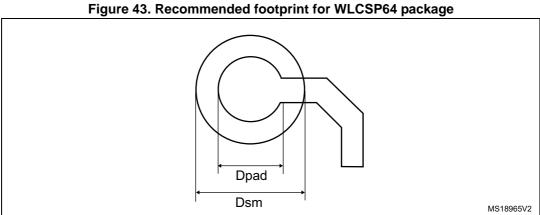


Table 76. WLCSP64 recommended PCB design rules

Dimension	Recommended values	
Pitch	0.4	
Dpad	260 µm max. (circular)	
рац	220 µm recommended	
Dsm	300 μm min. (for 260 μm diameter pad)	
PCB pad design	Non-solder mask defined via underbump allowed.	

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The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

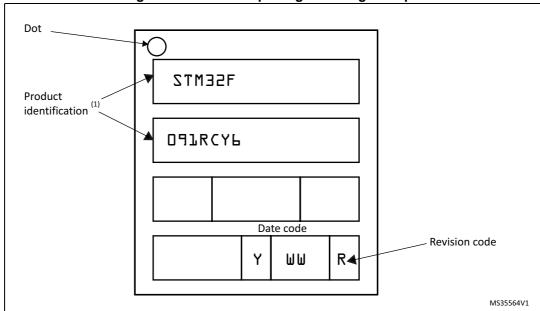


Figure 44. WLCSP64 package marking example

Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.5 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

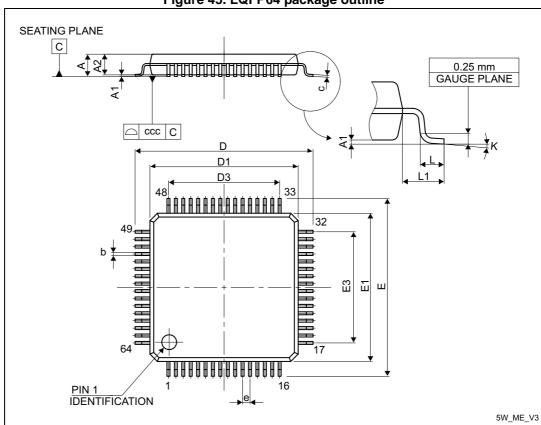


Figure 45. LQFP64 package outline

1. Drawing is not to scale.

Table 77. LQFP64 package mechanical data

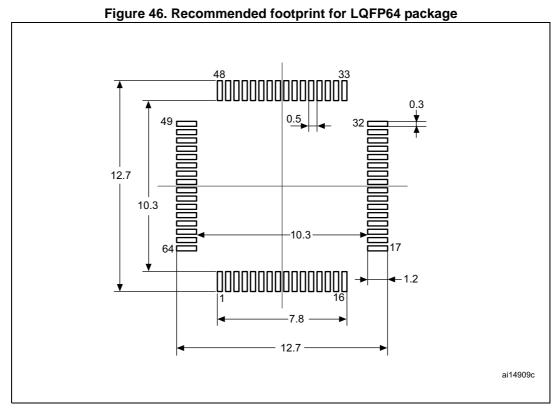
idolo III Edi I o i paolago moonamoar data						
Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Max	Min	Тур	Max
Α	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

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inches⁽¹⁾ millimeters **Symbol** Min Тур Max Min Тур Max 7.500 0.2953 E3 0.500 0.0197 е 0° 7° 0° 7° Κ 3.5° 3.5° L 0.450 0.600 0.750 0.0177 0.0236 0.0295 L1 1.000 0.0394 0.080 0.0031 CCC

Table 77. LQFP64 package mechanical data (continued)

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.



1. Dimensions are expressed in millimeters.

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

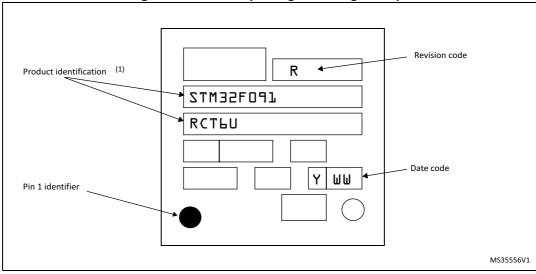


Figure 47. LQFP64 package marking example

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



7.6 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

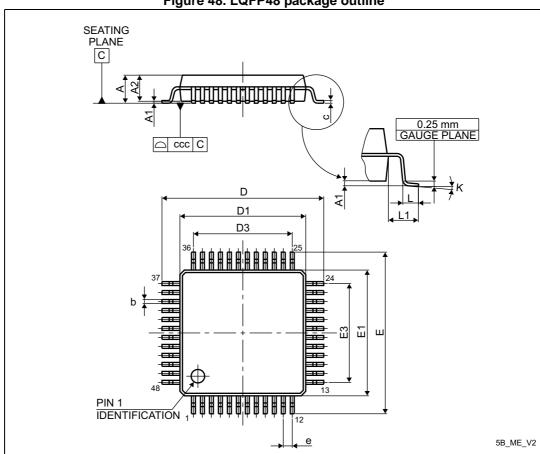


Figure 48. LQFP48 package outline

1. Drawing is not to scale.

Table 78. LQFP48 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Max	Min	Тур	Max
А	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
е	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080			0.0031

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

9.70 5.80 7.30 0.20 1.20 0.30 1.20 0

1. Dimensions are expressed in millimeters.

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The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

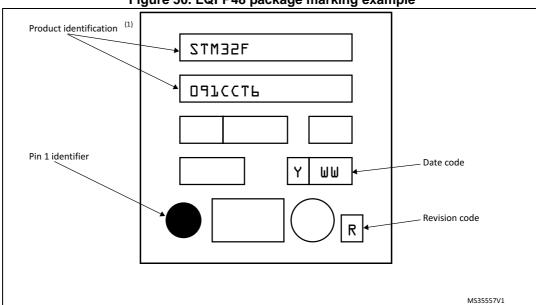


Figure 50. LQFP48 package marking example

^{1.} Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.7 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7x7 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

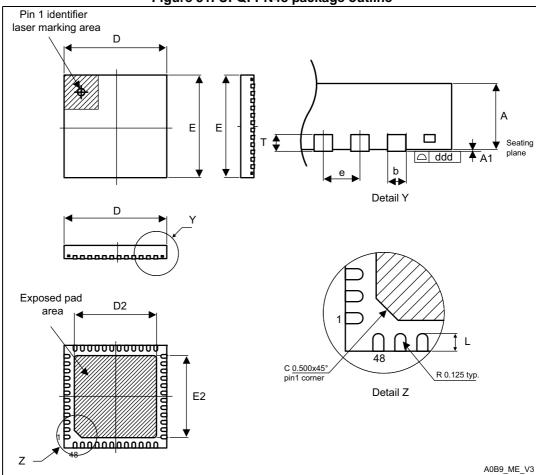


Figure 51. UFQFPN48 package outline

- 1. Drawing is not to scale.
- 2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
- There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

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Table 79. UFQFPN48 package mechanical data

Cumbal	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Max	Min	Тур	Max
А	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
Е	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
Т	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
е	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

5.60 7.30 5.80 **←** 0.50 0.55 A0B9_FP_V2

Figure 52. Recommended footprint for UFQFPN48 package

1. Dimensions are expressed in millimeters.

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

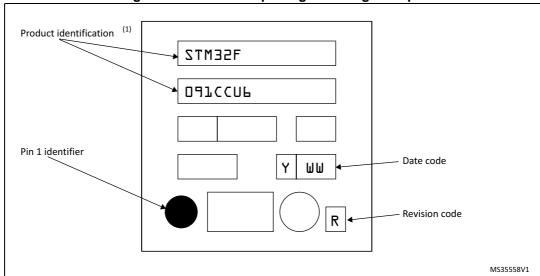


Figure 53. UFQFPN48 package marking example

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



7.8 Thermal characteristics

The maximum chip junction temperature (T_Jmax) must never exceed the values given in *Table 24: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \max = T_A \max + (P_D \max x \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

P_{I/O} max represents the maximum power dissipation on output pins where:

$$P_{I/O}$$
 max = $\Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH})$,

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient UFBGA100 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	42	
	Thermal resistance junction-ambient UFBGA64 - 5 × 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	44	°C/W
	Thermal resistance junction-ambient WLCSP64 - 0.4 mm pitch	53	
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	54	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	32	

Table 80. Package thermal characteristics

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.



Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F091xB/xC at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL} = 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL} = 1.3 V

 P_{INTmax} = 50 mA × 3.5 V= 175 mW

 $P_{IOmax} = 20 \times 8 \text{ mA} \times 0.4 \text{ V} + 8 \times 20 \text{ mA} \times 1.3 \text{ V} = 272 \text{ mW}$

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

 $P_{Dmax} = 175 + 272 = 447 \text{ mW}$

Using the values obtained in *Table 80* T_{Jmax} is calculated as follows:

For LQFP64, 45 °C/W

$$T_{\text{lmax}}$$
 = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts ($-40 < T_J < 105$ °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see Section 8: Ordering information).

Note:

With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6:
$$T_{Amax} = T_{Jmax}$$
 - $(45^{\circ}\text{C/W} \times 447 \text{ mW}) = 105\text{-}20.115 = 84.885 ^{\circ}\text{C}$
Suffix 7: $T_{Amax} = T_{Jmax}$ - $(45^{\circ}\text{C/W} \times 447 \text{ mW}) = 125\text{-}20.115 = 104.885 ^{\circ}\text{C}$

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL} = 0.4 V

 P_{INTmax} = 20 mA × 3.5 V= 70 mW

 P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: $P_{INTmax} = 70 \text{ mW}$ and $P_{IOmax} = 64 \text{ mW}$:

 $P_{Dmax} = 70 + 64 = 134 \text{ mW}$

Thus: P_{Dmax} = 134 mW

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Using the values obtained in $\textit{Table 80}\,\mathsf{T}_{\mathsf{Jmax}}$ is calculated as follows:

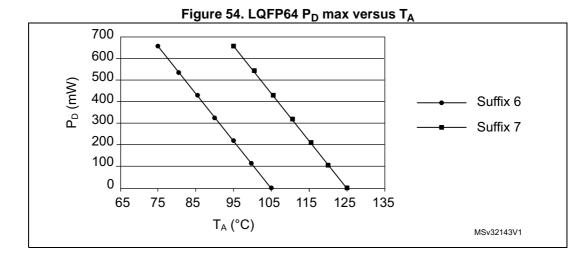
For LQFP64, 45 °C/W

$$T_{Jmax}$$
 = 100 °C + (45 °C/W × 134 mW) = 100 °C + 6.03 °C = 106.03 °C

This is above the range of the suffix 6 version parts ($-40 < T_J < 105$ °C).

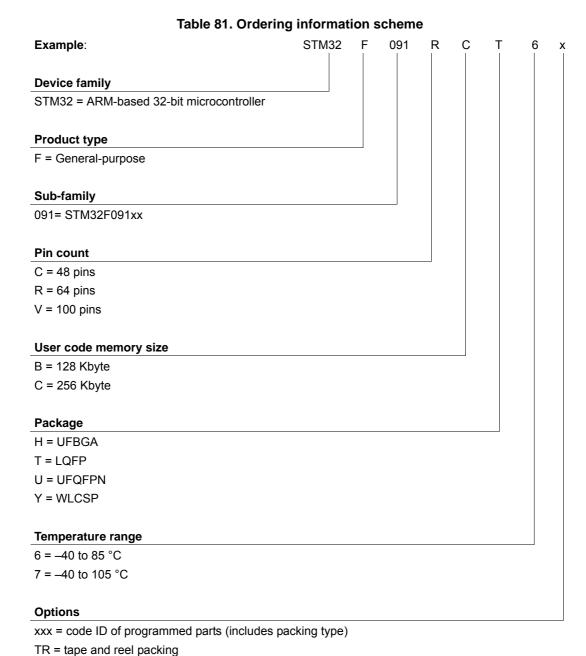
In this case, parts must be ordered at least with the temperature range suffix 7 (see Section 8: Ordering information) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to the figure below to select the required temperature range (suffix 6 or 7) according to your temperature or power requirements.



8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.



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blank = tray packing

9 Revision history

Table 82. Document revision history

Date	Revision	Changes
30-Oct-2014	1	Initial release.
09-Feb-2015	2	Updated: - Table: HSI oscillator characteristics, - Figure: HSI oscillator accuracy characterization results for soldered parts, - Figure: WLCSP64 wafer level chip size package mechanical drawing, - Table: WLCSP64 - 64-pin, 3.347 x 3.585 mm, 0.4 mm pitch wafer level chip scale package mechanical data,. Added: - Figure: WLCSP64 - 64-pin, 3.347 x 3.585 mm, 0.4 mm pitch wafer level chip scale recommended footprint.
17-Dec-2015	3	Section 2: Description: - Table 2: STM32F091xB/xC family device features and peripheral counts- I/O and capacitive channel numbers corrected Section 3: Functional overview: - updated Figure 1: Block diagram (number of AF) and Figure 2: Clock tree - Section 3.5.4: Low-power modes - added info. on comm. peripherals configurable to operate with HSI - Section 3.13: Touch sensing controller (TSC) - number of channels corrected - added number of complementary outputs for the general purpose and for the advance control timers in Table 7: Timer feature comparison - Table 9: STM32F091xB/xC f²C implementation - added 20mA value to Fast Mode Plus output drive Section 4: Pinouts and pin descriptions: - Package pinout figures updated (look and feel) - Figure 7: WLCSP64 package pinout - now presented in top view - Table 13: STM32F091xB/xC pin definitions - MCO moved from additional to alternate functions column - Table 19: Alternate functions selected through GPIOF_AFR registers for port F- lines PF4 and PF5 removed - Section 5: Memory mapping: - added information on STM32F091xB difference versus STM32F091xC map in Figure 10

Table 82. Document revision history (continued)

Date	Revision	Changes
		Section 6: Electrical characteristics: - footnote for V _{IN} max value in Table 21: Voltage
		characteristics - Table 28: Embedded internal reference voltage: added t _{START} parameter and removal of -40°-to-85° condition for V _{REFINT} and associated note - Figure 18: Typical application with a 32.768 kHz crystal - correction of OSC_IN and OSC_OUT to OSC32_IN and OSC32_OUT and f _{HSE} to f _{LSE}
		- Table 50: ESD absolute maximum ratings updated
		 V_{DDIOx} replaced V_{DD} in Figure 22: TC and TTa I/O input characteristics and Figure 23: Five volt tolerant (FT and FTf) I/O input characteristics
		- Table 53: I/O static characteristics- note removed
	3 (continued)	 Table 57: ADC characteristics - updated some parameter values, test conditions and added footnotes ⁽³⁾ and ⁽⁴⁾
		 I_{DDA} max value (DAC DC current consumption) in Table 60: DAC characteristics
		 Table 61: Comparator characteristics - min value added for V_{DDA}
		 Table 62: TS characteristics: removed the minimum value for t_{START} symbol and updated parameter name
17-Dec-2015		 R parameter typical. value in Table 63: V_{BAT} monitoring characteristics
		 Table 64: TIMx characteristics: removed Res_{TM} parameter line and all values put in new Typ column, t_{COUNTER} substituted with t_{MAX_COUNT}, values defined as powers of two
		 Table 69: f²S characteristics reorganized and max value added for t_{v(SD ST)}
		- Figure 32: L'S master timing diagram (Philips protocol) added definition of edge level references
		Section 7: Package information:
l		 Figure 33: UFBGA100 package outline and associated Table 70 updated
		- Figure 34 and associated Table 71 updated
		 Figure 35: UFBGA100 package marking example and associated text updated
		 Figure 38: LQFP100 package marking example and associated text updated
		 Table 74: UFBGA64 recommended PCB design rules added
		 Figure 41: UFBGA64 package marking example added
		Section 8: Part numbering:
		 added tray packing to options

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Table 82. Document revision history (continued)

Date	Revision	Changes
		Section 6: Electrical characteristics:
		 Table 40: LSE oscillator characteristics (f_{LSE} = 32.768 kHz) - information on configuring different drive capabilities removed. See the corresponding reference manual.
		 Table 28: Embedded internal reference voltage - V_{REFINT} values
10-Jan-2017	4	 Table 60: DAC characteristics - min. R_{LOAD} to V_{DDA} defined
		 Figure 28: SPI timing diagram - slave mode and CPHA = 0 and Figure 29: SPI timing diagram - slave mode and CPHA = 1 enhanced and corrected
		Section 8: Ordering information:
		 The name of the section changed from the previous "Part numbering"



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- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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