

Spread Aware™, Ten/Eleven Output Zero Delay Buffer

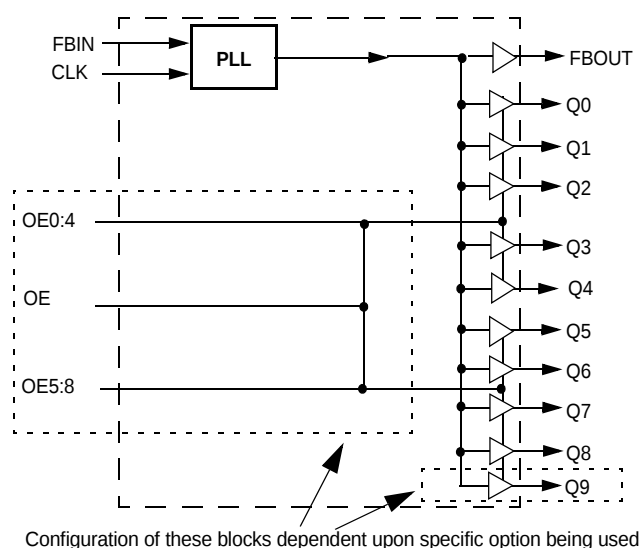
Features

- Spread Aware™ designed to work with spread spectrum frequency timing generator (SSFTG) reference signals
- Well suited to both 100- and 133-MHz designs
Ten (CY2509) or eleven (CY2510) low-voltage complementary metal oxide semiconductor (LVCMOS) / low-voltage transistor-transistor logic (LVTTTL) outputs.
- 50 ps typical peak cycle-to-cycle jitter
- Single output enable pin for CY2510 version, dual pins on CY2509 devices allow shutting down a portion of the outputs
- 3.3 V power supply
- On-chip 25 Ω damping resistors
- Available in 24-pin thin shrunk small outline package (TSSOP) package
- Improved tracking skew, but narrower frequency support limit when compared to W132-09B/10B

Key Specifications

Operating voltage:	3.3 V $\pm$ 10%
Operating range:	40 MHz < f_{OUT} < 140 MHz
Cycle-to-cycle jitter:	<100 ps
Output to output skew:	<100 ps
Phase error jitter:	<100 ps

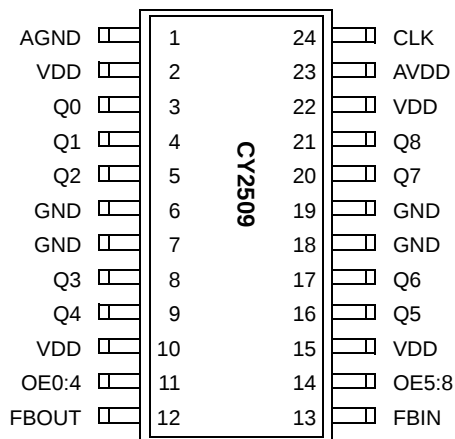
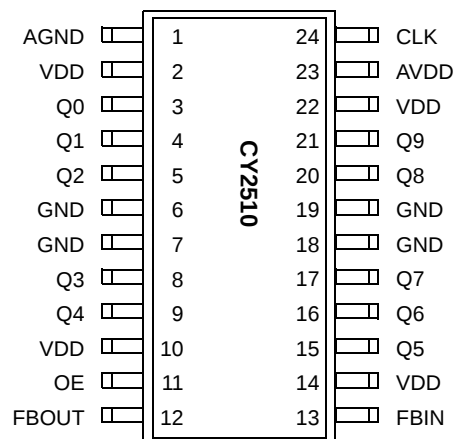
Block Diagram



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Pin Configurations



Pin Definitions

Pin Name	Pin No (2509)	Pin No (2510)	Pin Type	Pin Description
CLK	24	24	I	Reference input: Output signals Q0:9 will be synchronized to this signal.
FBIN	13	13	I	Feedback input: This input must be fed by one of the outputs (typically FBOUT) to ensure proper functionality. If the trace between FBIN and FBOUT is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations will be synchronized to the CLK signal input.
Q0:8	3, 4, 5, 8, 9, 16, 17, 20, 21	3, 4, 5, 8, 9, 15, 16, 17, 20	O	Integrated series resistor outputs: The frequency and phase of the signals provided by these pins will be equal to the reference signal if properly laid out. Each output has a 25 Ω series damping resistor integrated.
Q9	n/a	21	O	Integrated series resistor output: The frequency and phase of the signal provided by this pin will be equal to the reference signal if properly laid out. This output has a 25 Ω series damping resistor integrated.
FBOUT	12	12	O	Feedback output: This output has a 25 Ω series resistor integrated on chip. Typically it is connected directly to the FBIN input with a trace equal in length to the traces between outputs Q0:9 and the destination points of these output signals.
AVDD	23	23	P	Analog power connection: Connect to 3.3 V. Use ferrite beads to help reduce noise for optimal jitter performance.
AGND	1	1	G	Analog ground connection: Connect to common system ground plane.
VDD	2, 10, 15, 22	2, 10, 14, 22	P	Power connections: Connect to 3.3 V. Use ferrite beads to help reduce noise for optimal jitter performance.
GND	6, 7, 18, 19	6, 7, 18, 19	G	Ground connections: Connect to common system ground plane.
OE	n/a	11	I	Output enable input: Tie to V_{DD} (HIGH, 1) for normal operation. When brought to GND (LOW, 0) all outputs are disabled to a LOW state.
OE0:4	11	n/a	I	Output enable input: Tie to V_{DD} (HIGH, 1) for normal operation. When brought to GND (LOW, 0) outputs Q0:4 are disabled to a LOW state.
OE5:8	14	n/a	I	Output enable input: Tie to V_{DD} (HIGH, 1) for normal operation. When brought to GND (LOW, 0) outputs Q5:8 are disabled to a LOW state.

Overview

The CY2509/10 is a PLL-based clock driver designed for use in dual inline memory modules. The clock driver has output frequencies of up to 133 MHz and output to output skews of less than 250 ps. The CY2509/10 provides minimum cycle-to-cycle and long-term jitter, which is of significant importance to meet the tight input-to-input skew budget in DIMM applications.

The current generation of 256- and 512-megabyte memory modules needs to support 100-MHz clocking speeds. Especially for cards configured in 16x4 or 8x8 format, the clock signal provided from the motherboard is generally not strong enough to meet all the requirements of the memory and logic on the DIMM. The CY2509/10 takes in the signal from the motherboard and

buffers out clock signals with enough drive to support all the DIMM board clocking needs. The CY2509/10 is also designed to meet the needs of new PC133 SDRAM designs, operating to 133 MHz.

The CY2509/10 was specifically designed to accept SSFTG signals currently being used in motherboard designs to reduce EMI. Zero delay buffers which are not designed to pass this feature through may cause skewing failures.

Output enable pins allow for shutdown of output when they are not being used. This reduces EMI and power consumption.

Absolute Maximum Ratings ^[1]

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other

conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Min	Max	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	-0.5	+7.0	V
T_{STG}	Storage temperature	-65	+150	°C
T_A	Operating temperature	0	+70	°C
T_B	Ambient temperature under bias	-55	+125	°C
P_D	Power dissipation	0.5	—	W

DC Electrical Characteristics:

$T_A = 0\text{ °C to }70\text{ °C}$, $V_{DD} = 3.3\text{ V} \pm 10\%$

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply current	Unloaded, 100 MHz	—	—	200	mA
V_{IL}	Input low voltage		—	—	0.8	V
V_{IH}	Input high voltage		2.0	—	$V_{DD} + 0.3$	V
V_{OL}	Output low voltage	$I_{OL} = 12\text{ mA}$	—	—	0.8	V
V_{OH}	Output high voltage	$I_{OH} = -12\text{ mA}$	2.1	—	—	V
I_{IL}	Input low current	$V_{IN} = 0\text{ V}$	—	—	50	μA
I_{IH}	Input high current	$V_{IN} = V_{DD}$	—	—	50	μA

AC Electrical Characteristics:

$T_A = 0\text{ °C to }+70\text{ °C}$, $V_{DD} = 3.3\text{ V} \pm 10\%$

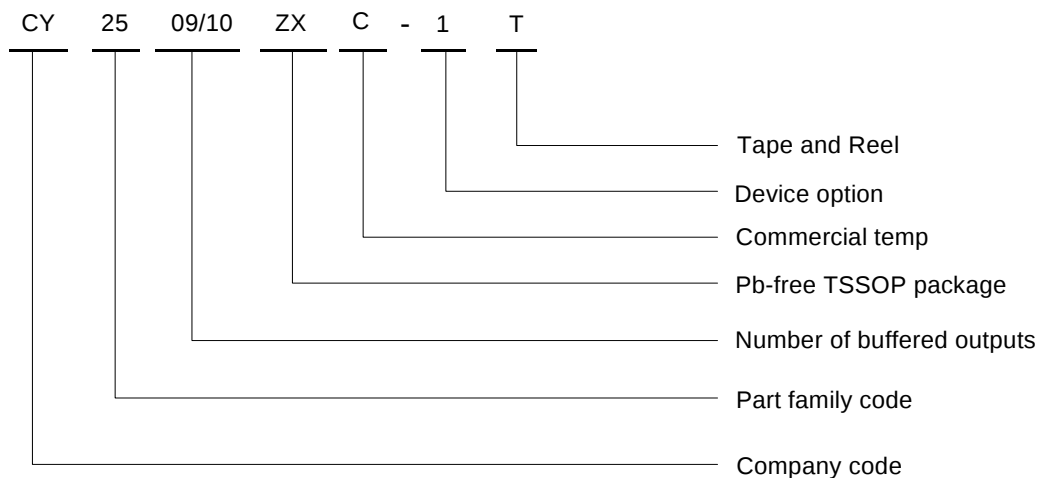
Parameter	Description	Test Condition	Min	Typ	Max	Unit
f_{OUT}	Output frequency	30-pF load ^[5]	40	—	140	MHz
t_R	Output rise time	0.8 V to 2.0 V, 30-pF load	—	—	2.1	ns
t_F	Output fall time	2.0 V to 0.8 V, 30-pF load	—	—	2.5	ns
t_{CLKR}	Input clock rise time ^[2]		—	—	4.5	ns
t_{CLKF}	Input clock fall time ^[2]		—	—	4.5	ns
t_{PEJ}	CLK to FBIN Skew Variation ^[3, 4]	Measured at $V_{DD}/2$	-350	0	350	ps
t_{SK}	Output to output skew	All outputs loaded equally	-100	0	100	ps
t_D	Duty cycle	30-pF load	43	50	58	%
t_{LOCK}	PLL lock time	Power supply stable	—	—	1.0	ms
t_{JC}	Jitter, Cycle-to-cycle		—	50	100	ps

Notes

- Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
- Longer input rise and fall time will degrade skew and jitter performance.
- Skew is measured at $V_{DD}/2$ on rising edges.
- Duty cycle is measured at $V_{DD}/2$.
- Production tests are run at 133 MHz.

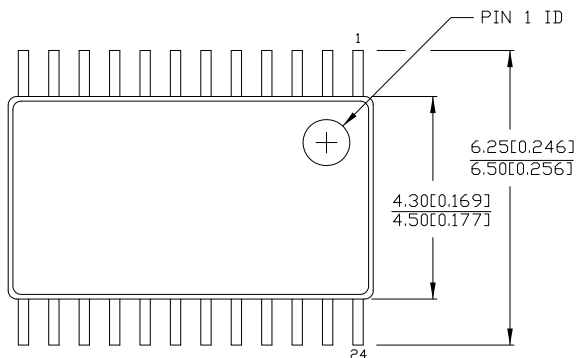
Ordering Information

Ordering Code	Package Type	Temperature Range
Pb-free		
CY2509ZXC-1	24-pin TSSOP	Commercial
CY2509ZXC-1T	24-pin TSSOP - Tape and Reel	Commercial
CY2510ZXC-1	24-pin TSSOP	Commercial
CY2510ZXC-1T	24-pin TSSOP - Tape and Reel	Commercial

Ordering Code Definitions


Package Drawing and Dimensions

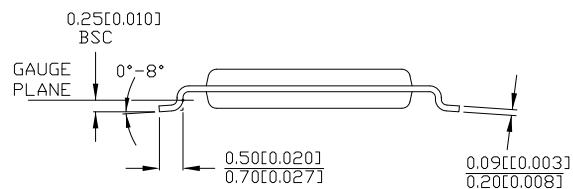
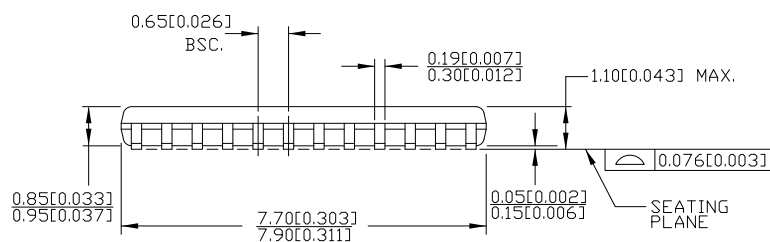
24-Lead Thin Shrunk Small Outline Package (4.40-mm Body) Z24



DIMENSIONS IN MM[INCHES] MIN. MAX.

REFERENCE JEDEC MO-153

PART #	
Z24.173	STANDARD PKG.
ZZ24.173	LEAD FREE PKG.



51-85119 * C

Acronyms

Acronym	Description
EMI	electromagnetic interference
LVC MOS	low-voltage complementary metal oxide semiconductor
LV TTL	low-voltage transistor-transistor logic
PLL	phase-locked loop
SSFTG	spread spectrum frequency timing generator
TSSOP	thin shrunk small outline package
ZDB	zero delay buffer

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
MHz	Megahertz
μA	microamperes
mA	milliamperes
ms	milliseconds
mV	millivolts
ns	nanoseconds
Ω	ohms
ppm	parts per million
%	percent
V	volts

Document History Page

Document Title: CY2509/10 Spread Aware™, Ten/Eleven Output Zero Delay Buffer Document Number: 38-07230				
Rev.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110495	01/07/02	SZV	Change from Spec number: 38-00914 to 38-07230
*A	122844	12/14/02	RBI	Power up requirements added to Operating Conditions Information
*B	352015	See ECN	RGL	Added Lead-free devices Added typical jitter and max. V_{IH} numbers
*C	385383	See ECN	RGL	Minor Change: Replaced the wrong package drawing
*D	2897373	03/22/10	CXQ	Updated ordering information table. Removed part numbers CY2509ZC-1, CY2510ZC-1, CY2509ZC-1T, CY2510ZC-1T Updated package diagram Updated copyright section
*E	3302008	07/05/11	CXQ	Updated to latest template Updated Figure 1 caption Updated Figure 2 caption Added Ordering Code Definitions Updated Package Drawing and Dimensions Added Acronyms and Units of Measure

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PSoC 1 | PSoC 3 | PSoC 5

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