DATA SHEET

UAA2082
Advanced pager receiver

Product specification
Supersedes data of 1995 Nov 27
File under Integrated Circuits, IC03

1996 Jan 15

Philips
Semiconductors

PHILIPS

Advanced pager receiver UAA2082

FEATURES

- Wide frequency range: VHF, UHF and 900 MHz bands
- High sensitivity
- High dynamic range
- Electronically adjustable filters on chip
- Suitable for data rates up to 2400 bits/s
- Wide frequency offset and deviation range
- Fully POCSAG compatible FSK receiver
- Power on/off mode selectable by the chip enable input
- Low supply voltage; low power consumption
- 1-cell battery-low detection circuit
- High integration level
- Interfaces directly to the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.

APPLICATIONS

- Wide area paging
- On-site paging
- Telemetry
- RF security systems
- Low bit-rate wireless data links.

GENERAL DESCRIPTION

The UAA2082 is a high-performance low-power radio receiver circuit primarily intended for VHF, UHF and 900 MHz pager receivers for wide area digital paging systems, employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK).

The receiver design is based on the direct conversion principle where the input signal is mixed directly down to the baseband by a local oscillator on the signal frequency. Two complete signal paths with signals of 90° phase difference are required to demodulate the signal.
All channel selectivity is provided by the built-in IF filters. The circuit makes extensive use of on-chip capacitors to minimize the number of external components.

The battery monitoring circuit has an external sense input and a 1.1 V detection threshold for easy operation in a single-cell supply concept.

The UAA2082 was designed to operate together with the PCA5000A, PCF5001 or PCD5003 POCSAG decoders, which contain a digital input filter for optimum call success rate.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2082H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
UAA2082U	28 pads	naked die; see Fig.8	

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current		2.3	2.7	3.2	mA
$I_{P(off)}$	stand-by current		–	–	3	µA
$P_{i(ref)}$	RF input sensitivity	BER ≤ $^3/_{100}$; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C				
		$f_{i(RF)}$ = 173 MHz	–	–126.5	–123.5	dBm
		$f_{i(RF)}$ = 470 MHz	–	–124.5	–121.5	dBm
		$f_{i(RF)}$ = 930 MHz	–	–120.0	–114.0	dBm
$P_{i(mix)}$	mixer input sensitivity	BER ≤ $^3/_{100}$; $f_{i(RF)}$ = 470 MHz; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C	–	–115.0	–110.0	dBm
V_{th}	detection threshold for battery LOW indicator	T_{amb} = 25 °C	1.05	1.10	1.15	V
		T_{amb} = –10 to +70 °C	1.03	1.10	1.17	V
T_{amb}	operating ambient temperature		–10	–	+70	°C

BLOCK DIAGRAMS (173 MHz)

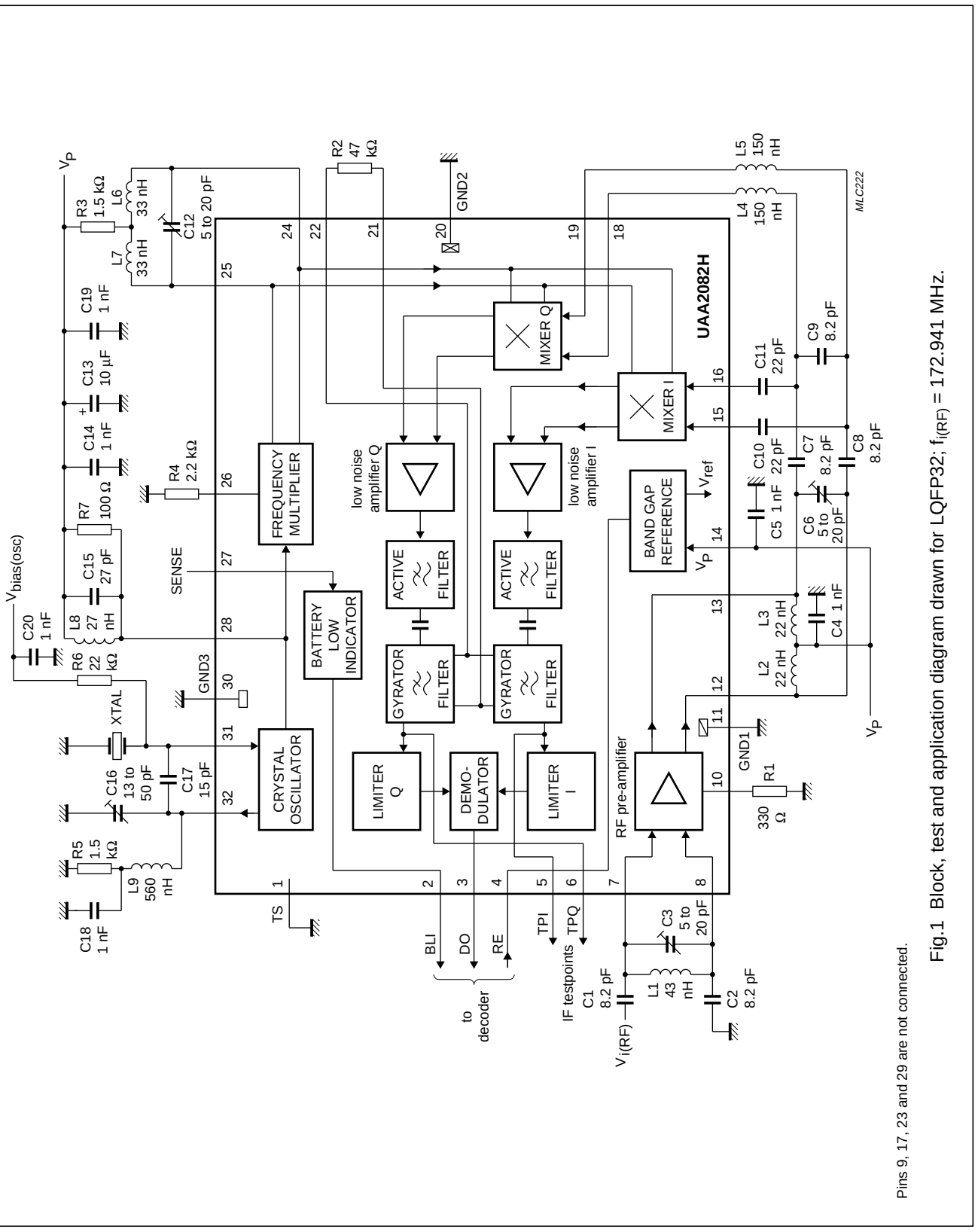


Fig.1 Block, test and application diagram drawn for LQFP32; $f_{i(RF)}$ = 172.941 MHz.

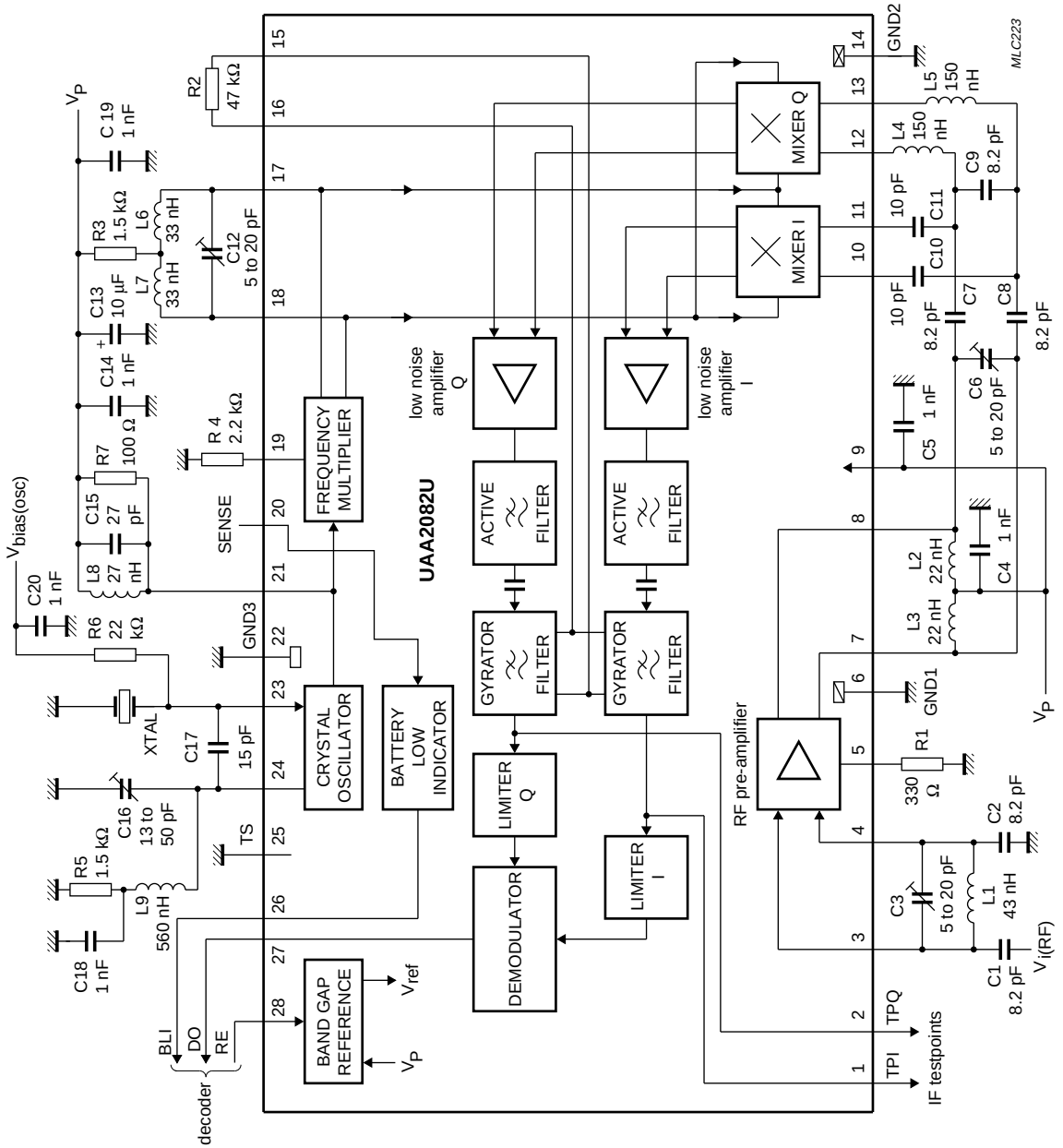


Fig.2 Block, test and application diagram drawn for naked die; $f_{i(RF)}$ = 172.941 MHz.

Table 1 Tolerances of components shown in Figs 1 and 2 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±5	Q_{min} = 100 at 173 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±20	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 30 at 57 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R7	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12	–	TC = (–750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18, C19, C20	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (–1700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 57.647 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF series capacitor at 25 °C), dynamic resistance R1 < 40 Ω, Δf = ±5 × 10^{-6} for T_{amb} = –10 to +55 °C with 25 °C reference, calibration plus aging tolerance: –5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAMS (470 MHz)

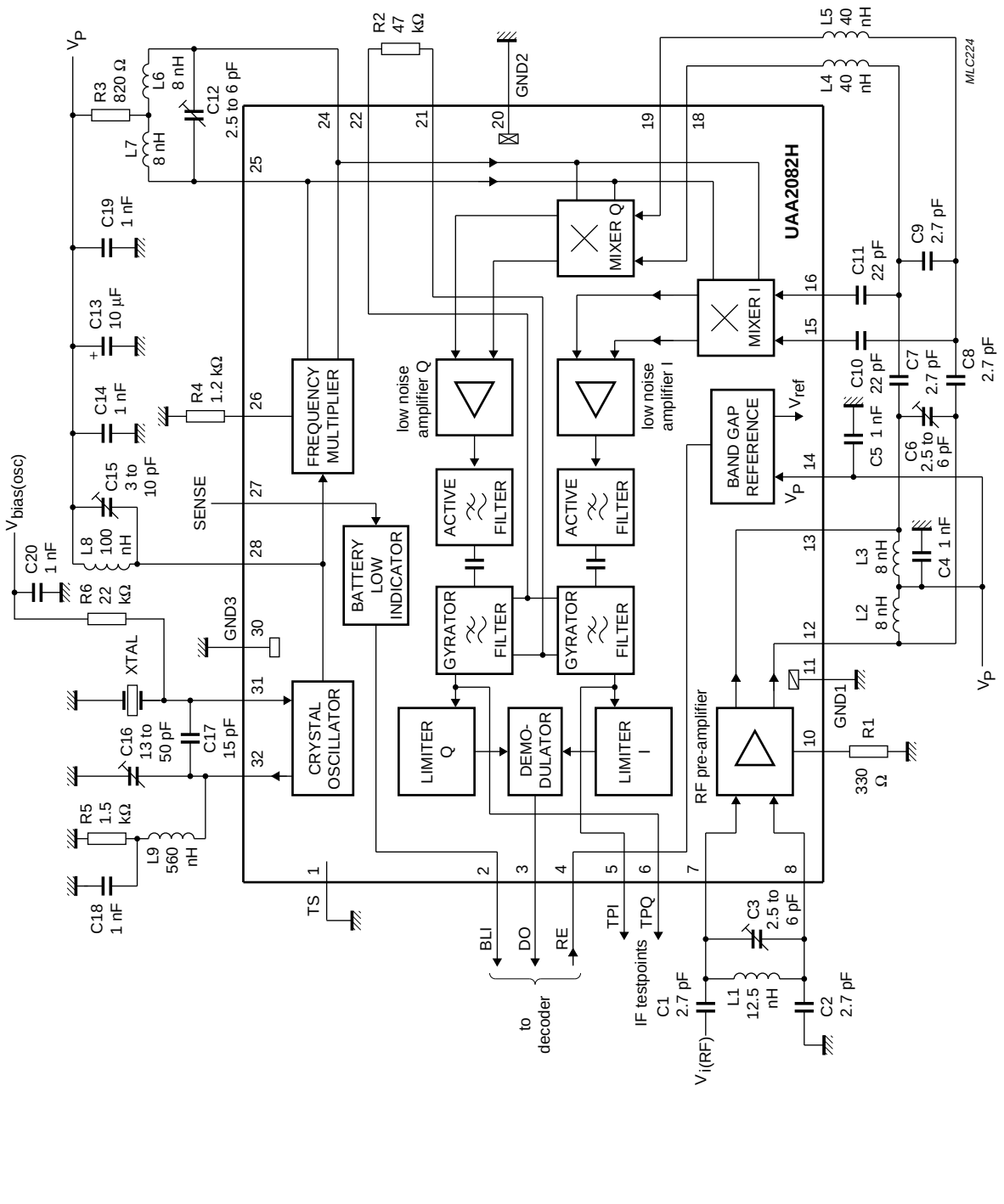


Fig.3 Block, test and application diagram drawn for LQFP32; $f_{i(RF)}$ = 469.95 MHz.

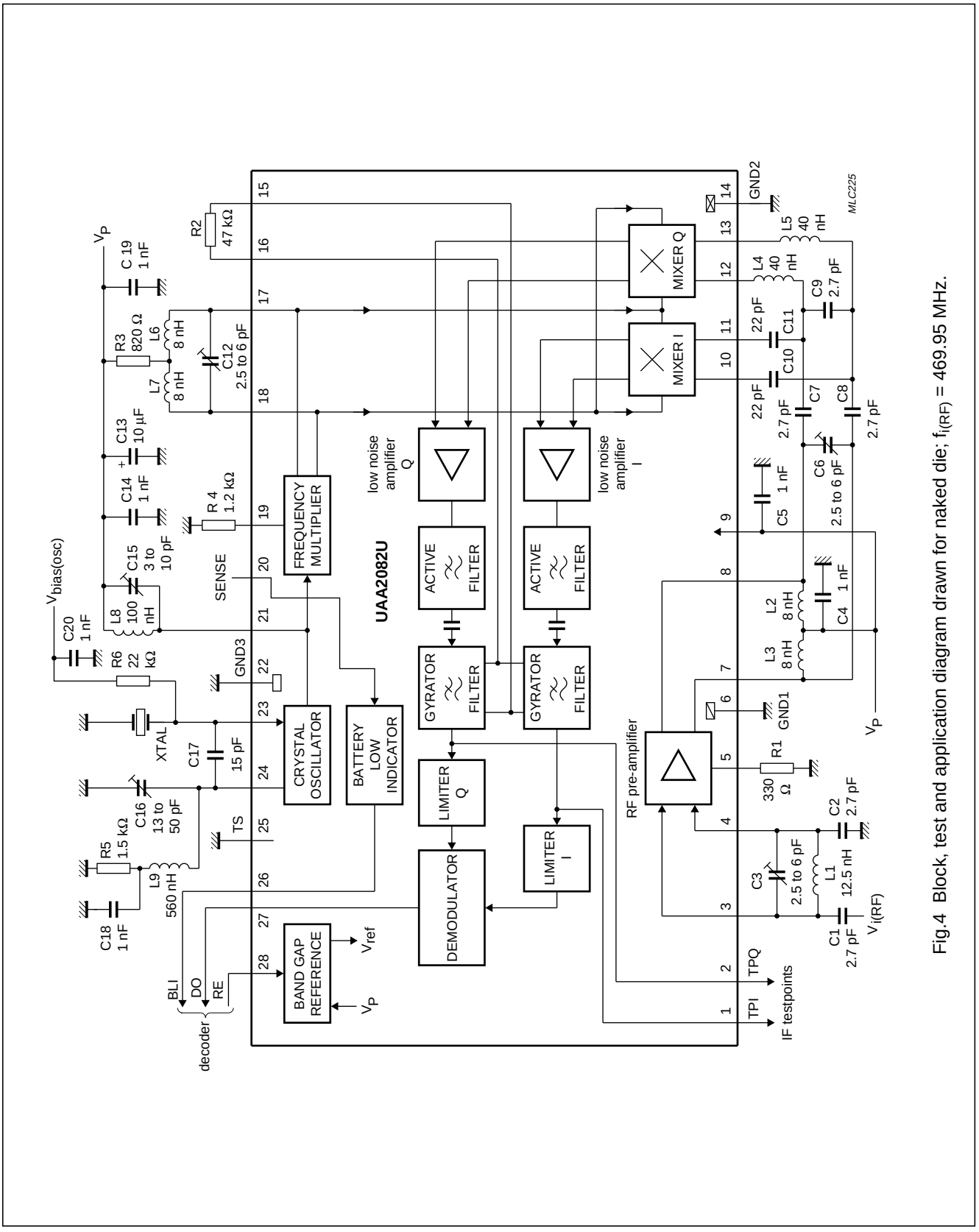


Fig.4 Block, test and application diagram drawn for naked die; $f_{i(RF)}$ = 469.95 MHz.

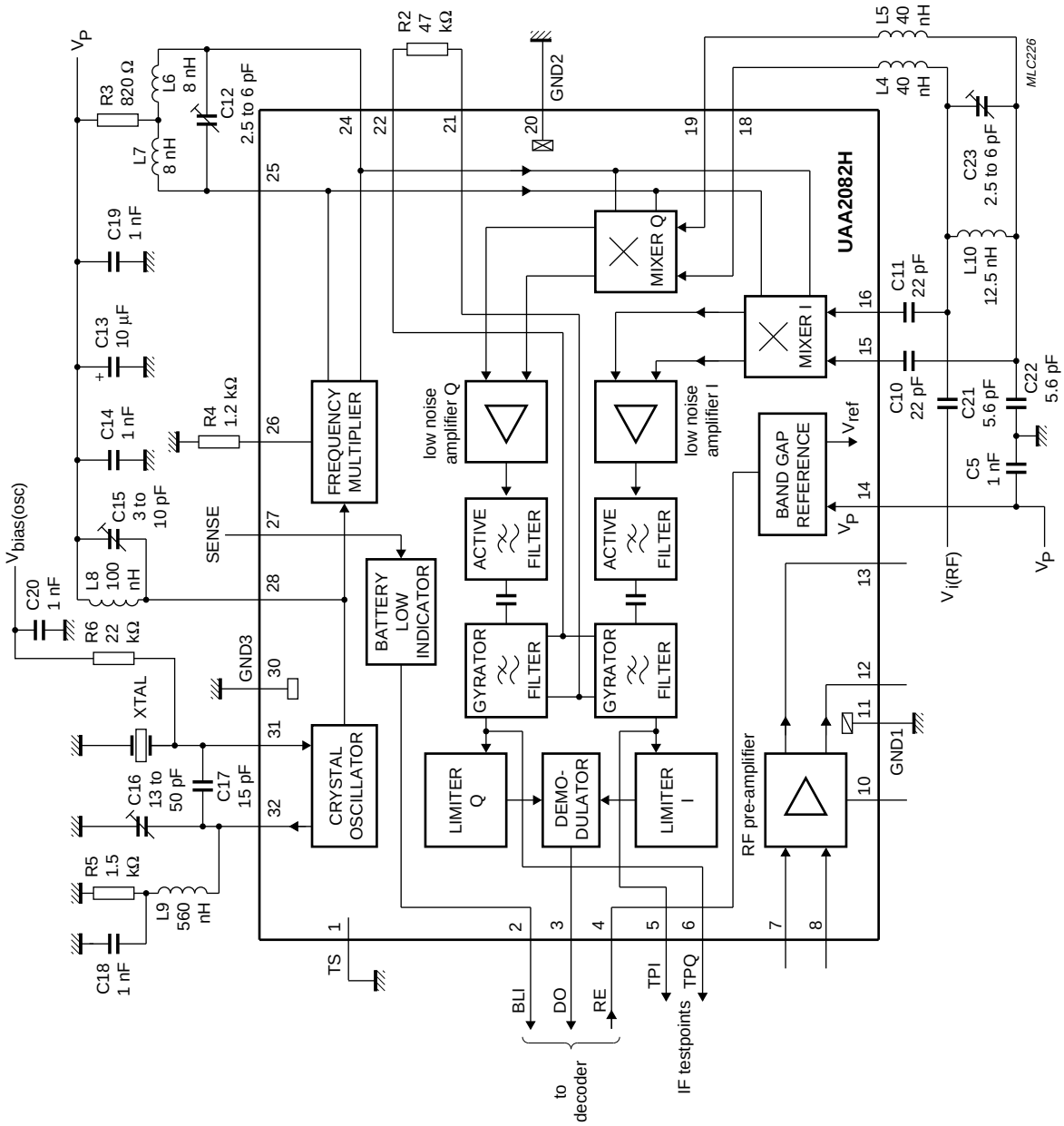


Fig.5 Mixer input sensitivity test circuit; $f_{i(RF)}$ = 469.95 MHz.

Table 2 Tolerances of components shown in Figs 3, 4 and 5 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1, L10	±5	Q_{min} = 145 at 470 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 40 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±10	Q_{min} = 30 at 156 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 40 at 78 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R6	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12, C23	–	TC = (–750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18 to C22	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (–1700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 78.325 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF capacitor at 25 °C), dynamic resistance R1 < 30 Ω, Δf = ±5 × 10^{-6} for T_{amb} = –10 to +55 °C with 25 °C reference, calibration plus aging tolerance: –5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAM (930 MHz)

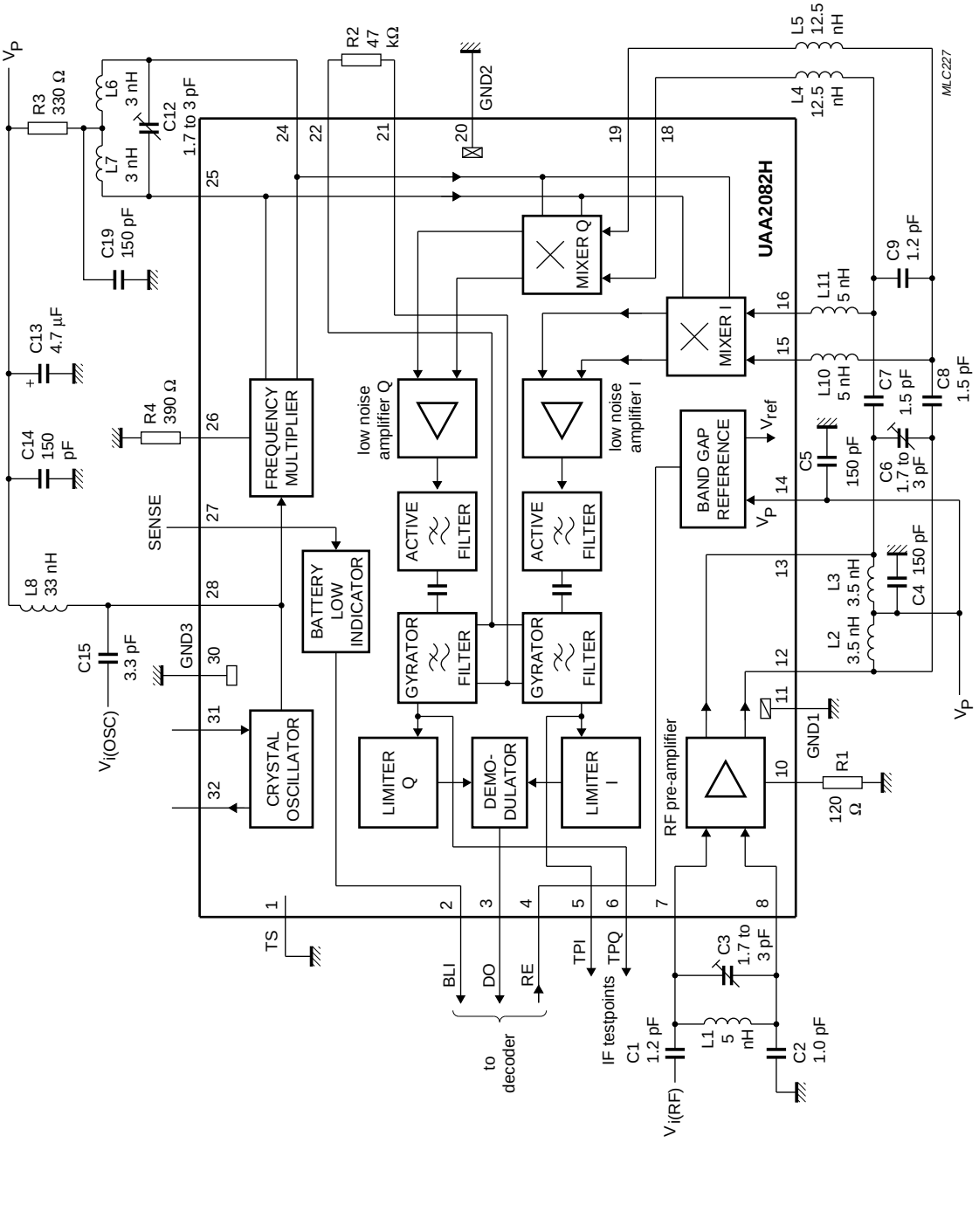


Fig.6 Test circuit; $f_{i(RF)}$ = 930.50 MHz.

Table 3 Tolerances of components shown in Fig.6 (note 1)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±10	Q_{typ} = 150 at 930 MHz
L2, L3, L6, L7	–	microstrip inductor
L4, L5	±5	Q_{typ} = 100 at 930 MHz
L8	±10	Q_{typ} = 65 at 310 MHz
L10, L11	±10	Q_{typ} = 150 at 930 MHz
Resistors		
R1 to R4	±2	TC = (0 ±200) × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12	–	TC = (0 ±200) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C4, C5, C14, C19	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C13	±20	

Note

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz.

PINNING (LQFP32)

SYMBOL	PIN	DESCRIPTION
TS	1	test switch; connection to ground for normal operation
BLI	2	battery LOW indicator output
DO	3	data output
RE	4	receiver enable input
TPI	5	IF test point; I channel
TPQ	6	IF test point; Q channel
VI1RF	7	pre-amplifier RF input 1
VI2RF	8	pre-amplifier RF input 2
n.c.	9	not connected
RRFA	10	external emitter resistor for pre-amplifier
GND1	11	ground 1 (0 V)
VO2RF	12	pre-amplifier RF output 2
VO1RF	13	pre-amplifier RF output 1
V_P	14	supply voltage
VI2MI	15	I channel mixer input 2
VI1MI	16	I channel mixer input 1
n.c.	17	not connected
VI1MQ	18	Q channel mixer input 1
VI2MQ	19	Q channel mixer input 2
GND2	20	ground 2 (0 V)
COM	21	gyrator filter resistor; common line
RGYR	22	gyrator filter resistor
n.c.	23	not connected
VO1MUL	24	frequency multiplier output 1
VO2MUL	25	frequency multiplier output 2
RMUL	26	external emitter resistor for frequency multiplier
SENSE	27	battery LOW detector sense input
OSC	28	oscillator collector
n.c.	29	not connected
GND3	30	ground 3 (0 V)
OSB	31	oscillator base; crystal input
OSE	32	oscillator emitter

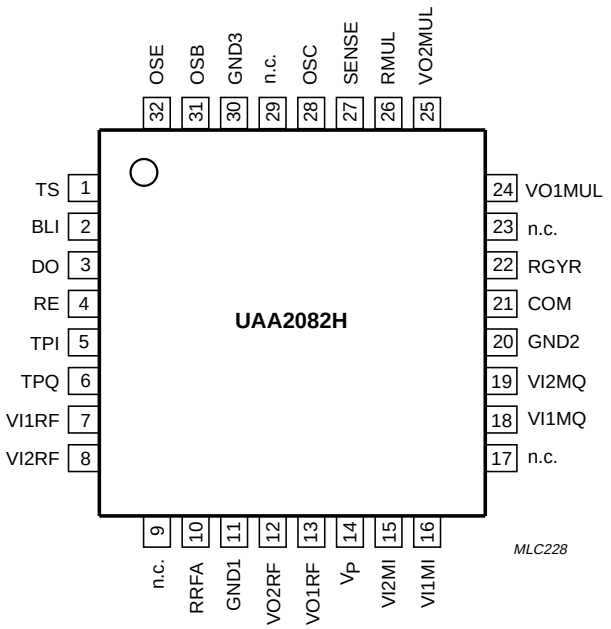
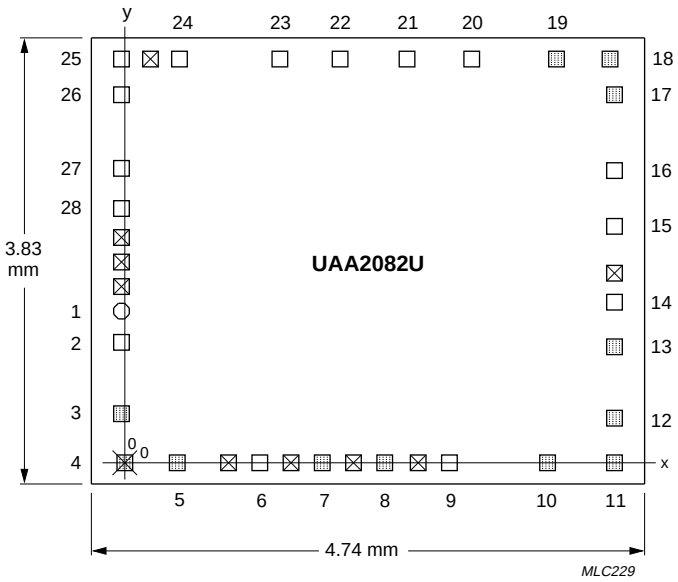


Fig.7 Pin configuration; LQFP32.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

See Table 4 for bonding pad description and locations for x/y co-ordinates.



Where:

- ○ Pad number 1 (diameter 124 μm)
- □ Pad 124 μm x 124 μm
- ⊠ Pad not used
- ▨ Pad 100 μm x 100 μm
- ⊠ Pad 100 μm x 100 μm with reference point

Chip area: 18.15 mm^2
Chip thickness: 380 ±20 μm.
Drawing not to scale.

Fig.8 Bonding pad locations.

Table 4 Bonding pad centre locations (dimensions in μm)

SYMBOL	PAD	DESCRIPTION	x	y
TPI	1	IF test point; I channel	−32	1296
TPQ	2	IF test point; Q channel	−32	1000
VI1RF	3	pre-amplifier RF input 1	−32	360
VI2RF	4	pre-amplifier RF input 2; note 1	0	0
RRFA	5	external emitter resistor for pre-amplifier	472	0
GND1	6	ground 1 (0 V)	1160	0
VO2RF	7	pre-amplifier RF output 2	1688	0
VO1RF	8	pre-amplifier RF output 1	2232	0
V_P	9	supply voltage	2760	0
VI2MI	10	I channel mixer input 2	3608	0
VI1MI	11	I channel mixer input 1	4216	0
VI1MQ	12	Q channel mixer input 1	4216	360
VI2MQ	13	Q channel mixer input 2	4216	960
GND2	14	ground 2 (0 V)	4216	1360
COM	15	gyrator filter resistor; common line	4216	2024
RGYR	16	gyrator filter resistor	4216	2496
VO1MUL	17	frequency multiplier output 1	4216	3136
VO2MUL	18	frequency multiplier output 2	4176	3456
RMUL	19	external emitter resistor for frequency multiplier	3668	3458
SENSE	20	battery LOW detector sense input	2952	3456
OSC	21	oscillator collector	2312	3456
GND3	22	ground 3 (0 V)	1832	3456
OSB	23	oscillator base; crystal input	1328	3456
OSE	24	oscillator emitter	432	3456
TS	25	test switch; connection to ground for normal operation	−32	3456
BLI	26	battery LOW indicator output	−32	3136
DO	27	data output	−32	2512
RE	28	receiver enable input	−32	2152
		lower left corner of chip (typical values)	−278	−186

Note

1. All x/y co-ordinates are referenced to the centre of pad 4 (VI2RF); see Fig.8.

INTERNAL CIRCUITS

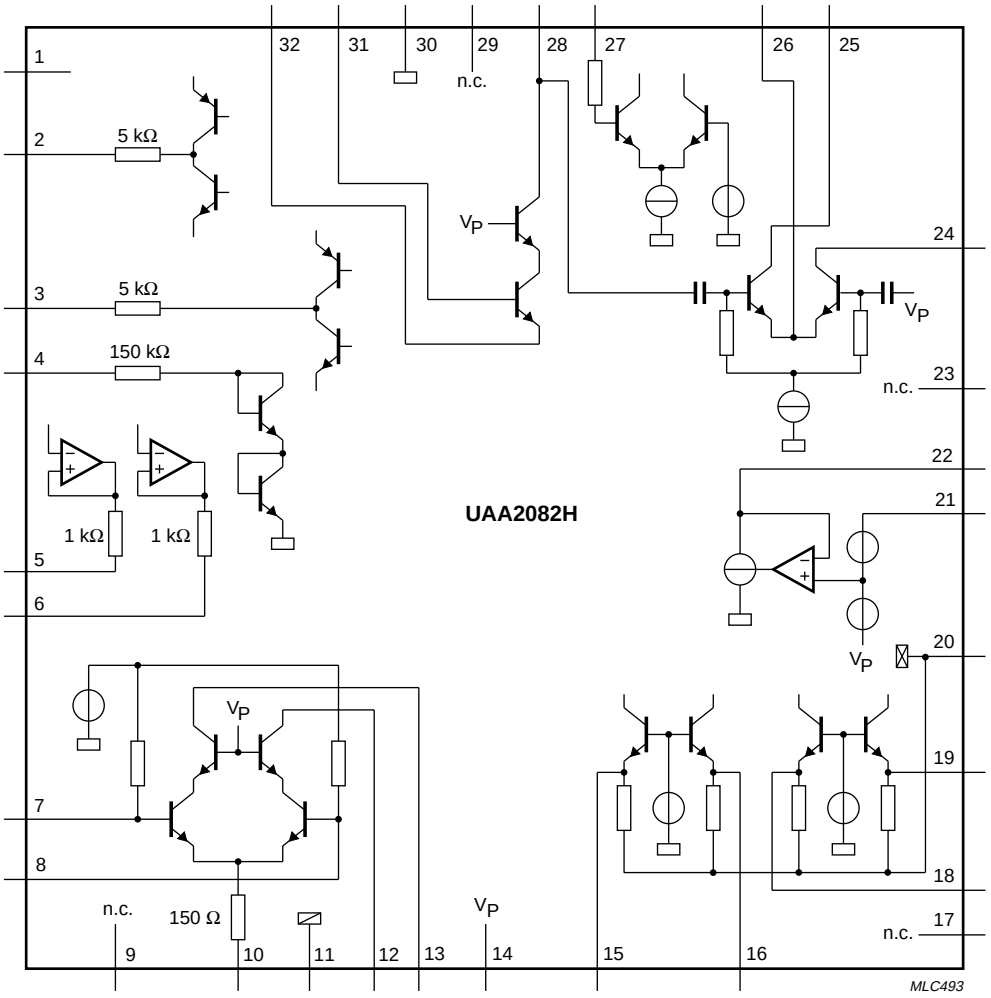


Fig.9 Internal circuits drawn for LQFP32.

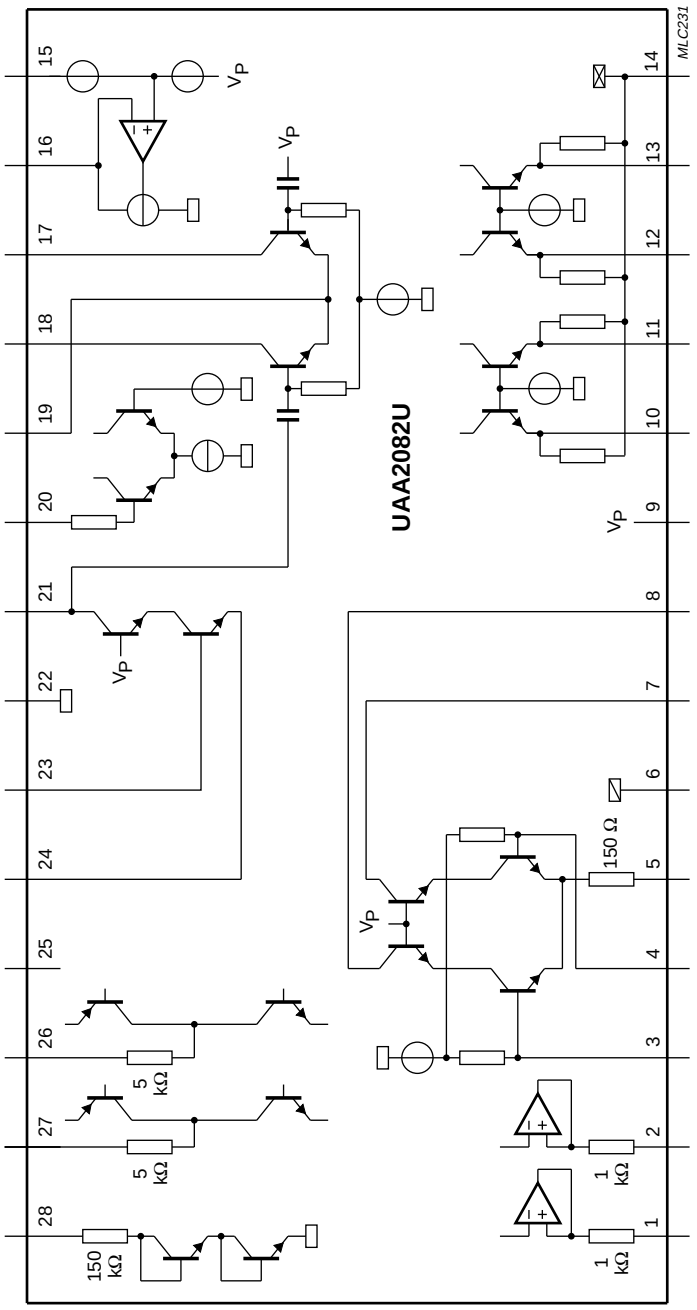


Fig.10 Internal circuits drawn for naked die.

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Figs 1 to 6.

Radio frequency amplifier

The RF amplifier is an emitter-coupled pair driving a balanced cascode stage, which drives an external balanced tuned circuit. Its bias current is set by an external 300 Ω resistor R1 to typically 770 μA. With this bias current the optimum source resistance is 1.3 kΩ at VHF and 1.0 kΩ at UHF. At 930 MHz a higher bias current is required to achieve optimum gain. A value of 120 Ω is used for R1, which corresponds with a bias current of approximately 1.3 mA and an optimum source resistance of approximately 600 Ω.The capacitors C1 and C2 transform a 50 Ω source resistance to this optimum value. The output drives a tuned circuit with capacitive divider (C7, C8 and C9) to provide maximum power transfer to the phase-splitting network and the mixers.

Mixers

The double balanced mixers consist of common base input stages and upper switching stages driven from the frequency multiplier. The 300 Ω input impedance of each mixer acts together with external components (C10, C11; L4, L5 respectively) as phase shifter/power splitter to provide a differential phase shift of 90 degrees between the I channel and the Q channel. At 930 MHz all external phase shifter components are inductive (L10, L11; L4, L5).

Oscillator

The oscillator is based on a transistor in common collector configuration. It is followed by a cascode stage driving a tuned circuit which provides the signal for the frequency multiplier. The oscillator transistor requires an external bias voltage $V_{bias(osc)}$ (1.22 V typ.). The oscillator bias current (typically 250 μA) is determined by the 1.5 kΩ external resistor R5. The oscillator frequency is controlled by an external 3rd overtone crystal in parallel resonance mode. External capacitors between base and emitter (C17) and from emitter to ground (C16) make the oscillator transistor appear as having a negative resistance for small signals; this causes the oscillator to start. Inductance L9 connected in parallel with capacitor C16 to the emitter of the oscillator transistor prevents oscillation at the fundamental frequency of the crystal.

The resonant circuit at output pin OSC selects the second harmonic of the oscillator frequency. In other applications a different multiplication factor may be chosen.

At 930 MHz an external oscillator circuit is required to provide sufficient local oscillator signal for the frequency multiplier.

Frequency multiplier

The frequency multiplier is an emitter-coupled pair driving an external balanced tuned circuit. Its bias current is set by external resistor R4 to typically 190 μA (173 MHz), 350 μA (470 MHz) and 1 mA (930 MHz). The oscillator signal is internally AC coupled to one input of the emitter-coupled pair while the other input is internally grounded via a capacitor. The frequency multiplier output signal between pins VO1MUL and VO2MUL drives the upper switching stages of the mixers. The bias voltage on pins VO1MUL and VO2MUL is set by external resistor R3 to allow sufficient voltage swing at the mixer outputs. The value of R3 depends on the operating frequency: 1.5 kΩ (173 MHz), 820 Ω (470 MHz) and 330 Ω (930 MHz).

Low noise amplifiers, active filters and gyrator filters

The low noise amplifiers ensure that the noise of the following stages does not affect the overall noise figure. The following active filters before the gyrator filters reduce the levels of large signals from adjacent channels. Internal AC couplings block DC offsets from the gyrator filter inputs.

The gyrator filters implement the transfer function of a 7th order elliptic filter. Their cut-off frequencies are determined by the 47 kΩ external resistor R2 between pins RGYR and COM. The gyrator filter output signals are available on IF test pins TPI and TPQ.

Limiters

The gyrator filter output signals are amplified in the limiter amplifiers to obtain IF signals with removed amplitude information.

Demodulator

The limiter amplifier output signals are fed to the demodulator. The demodulator output DO is going LOW or HIGH depending upon which of the input signals has a phase lead.

Battery LOW indicator

The battery LOW indicator senses the supply voltage and sets its output HIGH when the voltage at input SENSE is less than V_{th} (typically 1.10 V). Low battery warning is available at BLI.

Band gap reference

The whole chip except the oscillator section can be powered-up and powered-down by enabling and disabling the band gap reference via the receiver enable pin RE.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).
Ground pins GND1, GND2 and GND3 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	–0.3	+8.0	V
T_{stg}	storage temperature	–55	+125	°C
T_{amb}	operating ambient temperature	–10	+70	°C
V_{es}	electrostatic handling; note 1			
	pins VI1RF and VI2RF	–1500	+2000	V
	pin RRFA	–500	+2000	V
	pins VO1RF and VO2RF	–2000	+250	V
	pins V_P and OSB	–500	+500	V
	pins OSC and OSE	–2000	+500	V
	other pins	–2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor.

DC CHARACTERISTICS

V_P = 2.05 V; T_{amb} = −10 to +70 °C (typical values at T_{amb} = 25 °C); measurements taken in test circuit Figs 1, 2, 3 or 4 with crystal at pin OSB disconnected; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current	V_{RE} = HIGH; $f_{i(RF)}$ = 173 and 470 MHz	2.3	2.7	3.2	mA
		V_{RE} = HIGH; $f_{i(RF)}$ = 930 MHz	2.9	3.4	3.9	mA
$I_{P(off)}$	stand-by current	V_{RE} = LOW	–	–	3	µA
$V_{bias(osc)}$	oscillator bias voltage		1.20	1.22	1.24	V
Receiver enable input (pin RE)						
V_{IH}	HIGH level input voltage		1.4	–	V_P	V
V_{IL}	LOW level input voltage		0	–	0.3	V
I_{IH}	HIGH level input current	V_{IH} = V_P = 3.5 V	–	–	20	µA
V_{IL}	LOW level input current	V_{IL} = 0 V	0	–	−1.0	µA
Battery LOW indicator output (pin BLI)						
V_{OH}	HIGH level output voltage	V_{SENSE} < V_{th}; I_{BLI} = −10 µA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	V_{SENSE} > V_{th}; I_{BLI} = +10 µA	–	–	0.5	V
V_{th}	voltage threshold for battery LOW indicator	V_P = 2.05 V; T_{amb} = 25 °C	1.05	1.10	1.15	V
		V_P = 2.05 to 3.5 V; T_{amb} = −10 to +70 °C	1.03	1.10	1.17	V
Demodulator output (pin DO)						
V_{OH}	HIGH level output voltage	I_{DO} = −10 µA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	I_{DO} = +10 µA	–	–	0.5	V

AC CHARACTERISTICS (173 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Figs 1 or 2; $f_{i(RF)}$ = 172.941 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ±25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–126.5	–123.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–120.5	dBm
		V_P = 1.9 V	–	–	–117.5	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	69	72	–	dB
		T_{amb} = –10 to +70 °C	67	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	$\Delta f > \pm 1$ MHz; note 3	78	85	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (470 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Figs 3 or 4; $f_{i(RF)}$ = 469.950 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–124.5	–121.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–118.5	dBm
		V_P = 1.9 V	–	–	–115.5	dBm
Mixer input						
$P_{i(mix)}$	input sensitivity	BER ≤ $^3/_{100}$; note 3	–	–115.0	–110.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	67	70	–	dB
		T_{amb} = –10 to +70 °C	65	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	$\Delta f > \pm 1$ MHz; note 4	75	82	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 5	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Test circuit Fig.5. $P_{i(mix)}$ is the maximum available power at the input of the test board. The bit error rate BER is measured using the test facility shown in Fig.12.
4. Δf is the frequency offset between the required signal and the interfering signal.
5. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (930 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.6; note 1; $f_{i(RF)}$ = 930.500 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 2	–	–120.0	–114.0	dBm
		V_P = 1.9 V	–	–	–108.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	60	69	–	dB
α_c	co-channel rejection		–	5	10	dB
α_{sp}	spurious immunity		40	60	–	dB
α_{im}	intermodulation immunity		53	60	–	dB
α_{bl}	blocking immunity	$\Delta f > \pm 1$ MHz; note 3	65	74	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz and a level of –15 dBm.
2. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

TEST INFORMATION

Tuning procedure for AC tests

1. Turn on the signal generator: $f_{gen} = f_{i(RF)} + 4$ kHz, no modulation, $V_{i(RF)} = 1$ mV (RMS).
2. Measure the IF with a counter connected to test pin TPI. Tune C16 to set the crystal oscillator to achieve $f_{IF} = 4$ kHz Change the generator frequency to $f_{gen} = f_{i(RF)} - 4$ kHz and check that f_{IF} is also 4 kHz. For a received input frequency $f_{i(RF)} = 172.941$ MHz the crystal frequency is $f_{XTAL} = 57.647$ MHz, while for $f_{i(RF)} = 469.950$ MHz the crystal frequency is $f_{XTAL} = 78.325$ MHz. For a received input frequency $f_{i(RF)} = 930.500$ MHz an external oscillator signal must be used with $f_{i(OSC)} = 310.1667$ MHz and a level of –15 dBm (for definition of crystal frequency, see Table 1).
3. Set the signal generator to nominal frequency ($f_{i(RF)}$) and turn on the modulation deviation ±4.0 kHz, 600 Hz square wave modulation, $V_{i(RF)} = 1$ mV (RMS). Note that the RF signal should be reduced in the following tests, as the receiver is tuned, to ensure $V_{o(IF)} = 10$ to 50 mV (p-p) on test pins TPI or TPQ.
4. Tune C15 (oscillator output circuit) and C12 (frequency multiplier output) to obtain a peak audio voltage on pin TPI.
5. Tune C3 and C6 (RF input and mixer input) to obtain a peak audio voltage on pin TPI. When testing the mixer input sensitivity tune C23 instead of C3 and C6 (test circuit Fig.5).
6. Check that the output signal on pin TPQ is within 3 dB in amplitude and at 90° (±20°) relative phase of the signal on pin TPI.
7. Check that data signal appears on output pin DO and proceed with the AC test.

AC test conditions

Table 5 Definitions for AC test conditions (see Table 6)

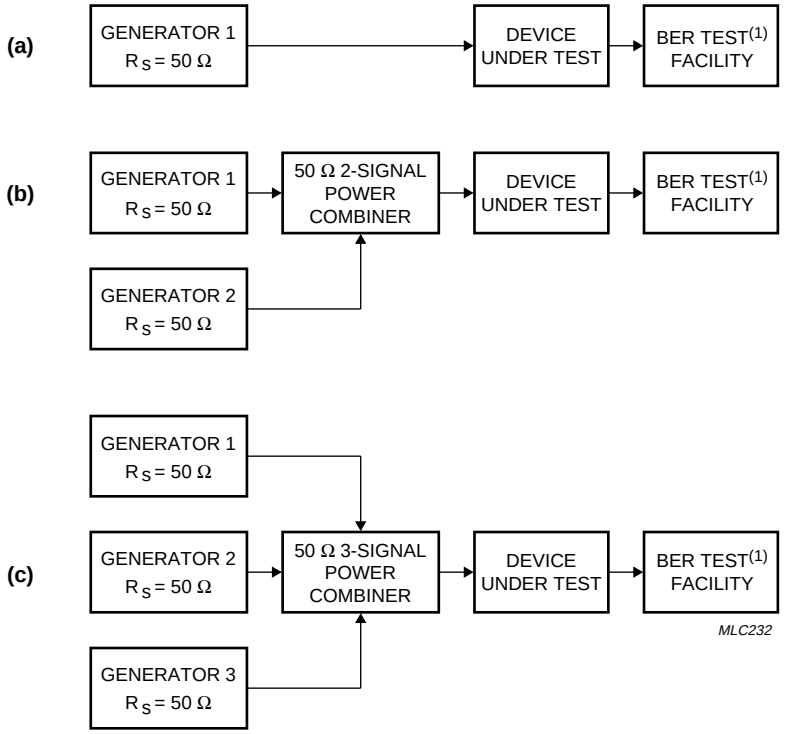
SIGNAL	DESCRIPTION
Modulated test signal 1	
Frequency	172.941, 469.950 or 930.500 MHz
Deviation	±4.0 kHz
Modulation	1200 baud pseudo random bit sequence
Rise time	250 ±25 µs (between 10% and 90% of final value)
Modulated test signal 2	
Deviation	±2.4 kHz
Modulation	400 Hz sine wave
Other definitions	
f_1	frequency of signal generator 1
f_2	frequency of signal generator 2
f_3	frequency of signal generator 3
Δf_{cs}	channel spacing (20 kHz)
P_1	maximum available power from signal generator 1 at the test board input
P_2	maximum available power from signal generator 2 at the test board input
P_3	maximum available power from signal generator 3 at the test board input
$P_{i(ref)}$	maximum available power at the test board input to give a Bit Error Rate (BER) $\leq 3/100$ for the modulated test signal 1, in the absence of interfering signals and under the conditions as specified in Chapters “AC characteristics (173 MHz)”, “AC characteristics (470 MHz)” and “AC characteristics (930 MHz)”

Table 6 AC test conditions; notes 1 and 2

SYMBOL	PARAMETER	CONDITIONS	TEST SIGNALS
α_a	adjacent channel selectivity; Fig.11(b)	$f_2 = f_1 \pm \Delta f_{CS}$	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{a(min)}$
α_c	co-channel rejection; Fig.11(b)	$f_2 = f_1 \pm$ up to 3 kHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 - \alpha_{c(max)}$
α_{sp}	spurious immunity; Fig.11(b)	f_2 = 100 kHz to 2 GHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{sp(min)}$
α_{im}	intermodulation immunity; Fig.11(c)	$f_2 = f_1 \pm \Delta f_{cs}$; $f_3 = f_1 \pm 2\Delta f_{cs}$	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: unmodulated	$P_2 = P_1 + \alpha_{im(min)}$
		generator 3: modulated test signal 2	$P_3 = P_2$
α_{bl}	blocking immunity; Fig.11(b)	$f_2 = f_1 \pm 1$ MHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{bl(min)}$
f_{offset}	frequency offset range; Fig.11(a)	deviation = ±4.0 kHz, $f_1 = f_{i(RF)} \pm 2$ kHz ($f_{offset(min)}$)	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
Δf_{dev}	deviation range; Fig.11(a)	deviation = ±2.5 to ±7 kHz; ($\Delta f_{dev(min)}$ to $\Delta f_{dev(max)}$)	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
t_{on}	receiver turn-on time; Fig.11(a)	note 3	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 10$ dB

Notes

1. The tests are executed without load on pins TPI and TPQ.
2. All minimum and maximum values correspond to a bit error rate (BER) $\leq 3/100$ in the wanted signal (P_1).
3. The BER measurement is started 5 ms ($t_{on(max)}$) after V_{RE} goes HIGH; BER is then measured for 100 bits (BER $\leq 3/100$).



(a) One generator.
(b) Two generators.
(c) Three generators.
(1) See Fig.12.

Fig.11 Test configurations.

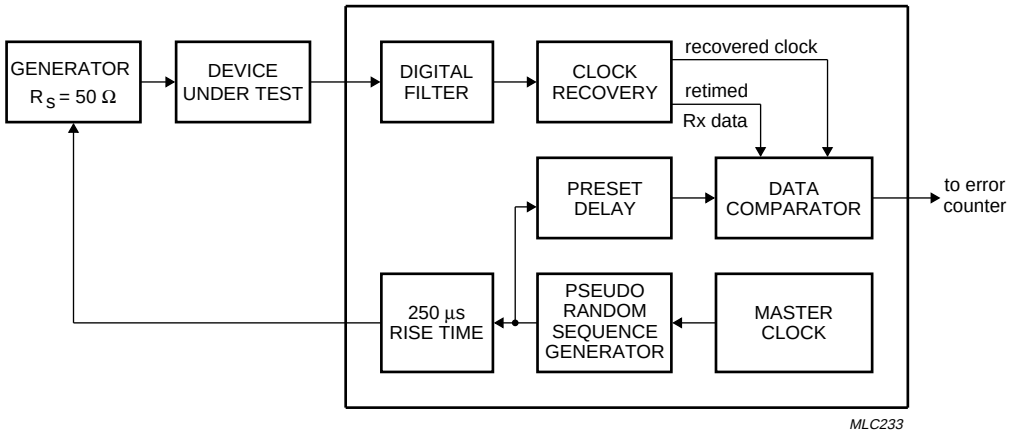
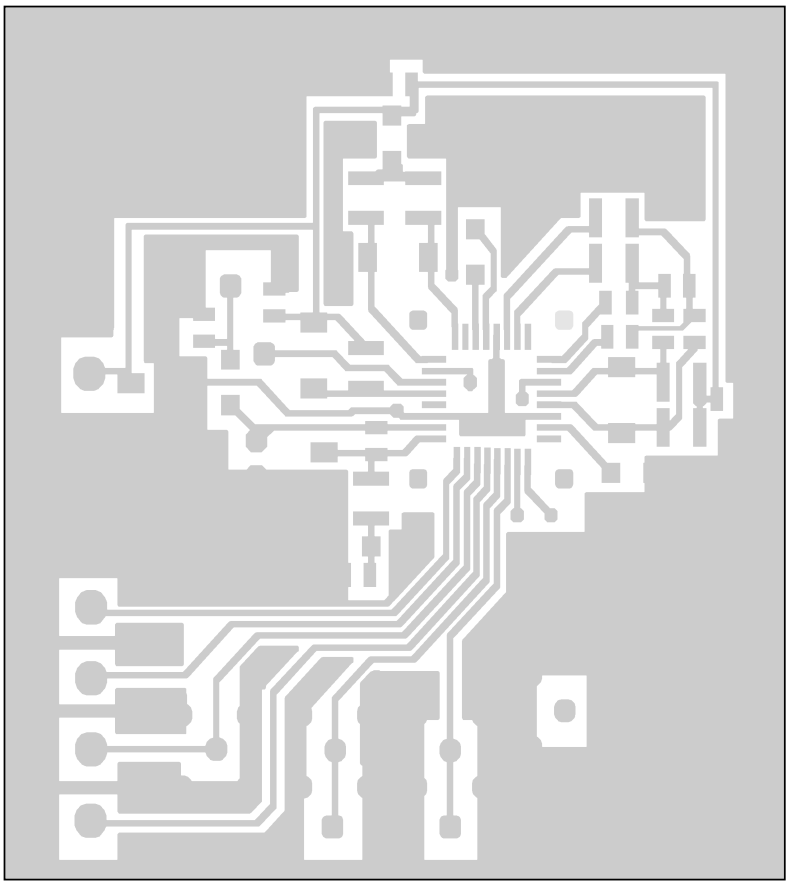


Fig.12 BER test facility.

PRINTED-CIRCUIT BOARDS



MBD562

Fig.13 PCB top view for LQFP32; test circuit Figs 1 and 3.

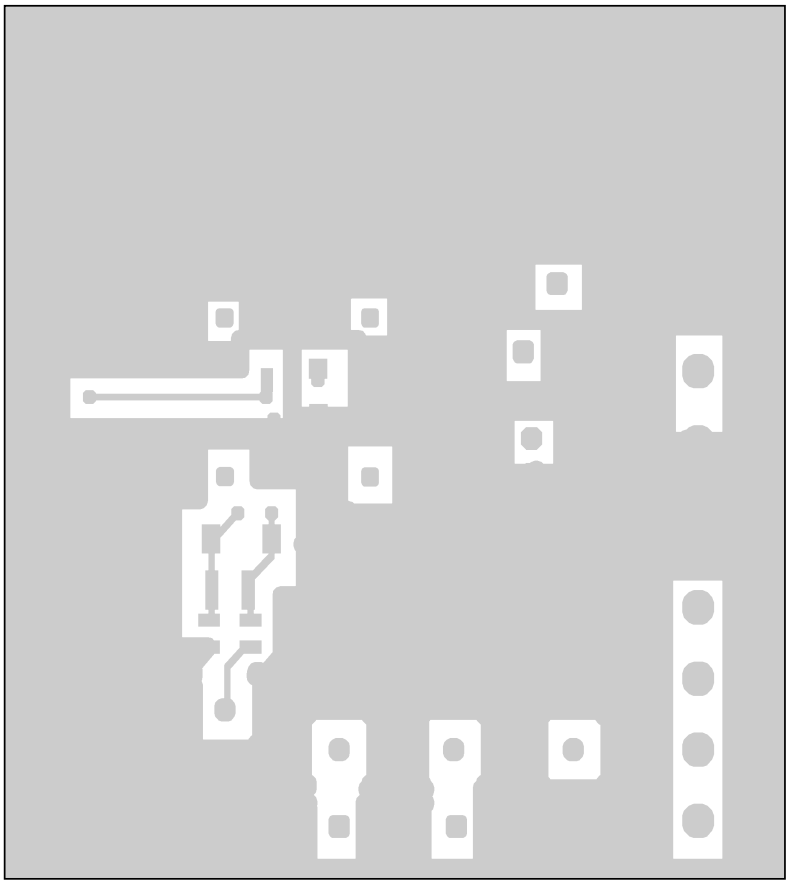
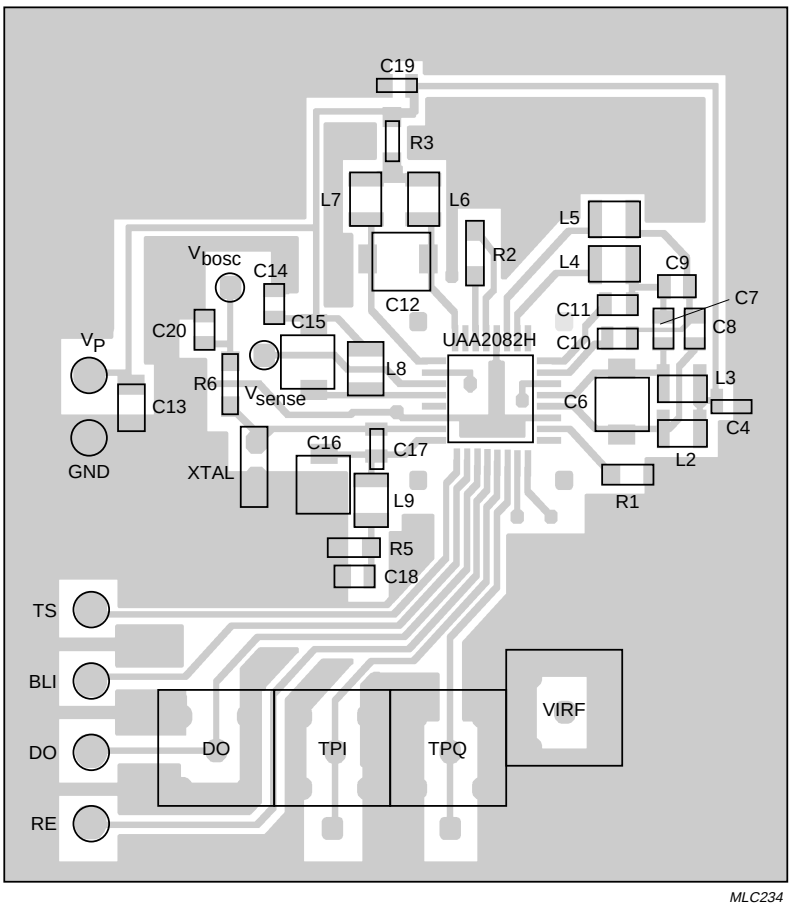


Fig.14 PCB bottom view for LQFP32; test circuit Figs 1 and 3.



V_{EE} = GND; V_C = V_P.

Fig.15 PCB top view with components for LQFP32; test circuit Fig.3.

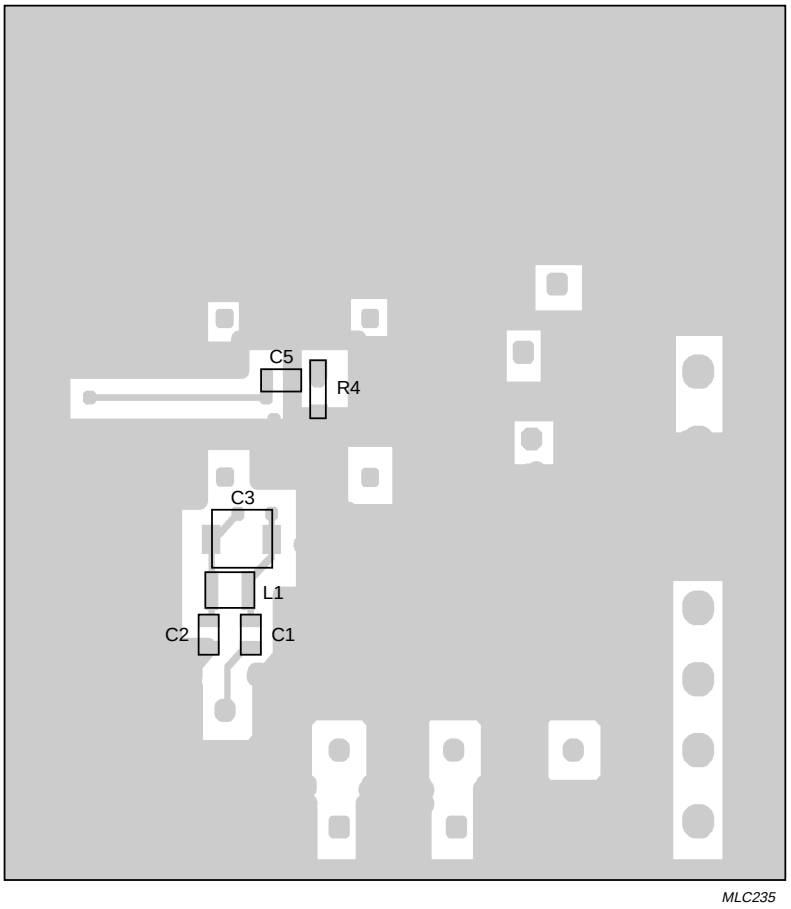


Fig.16 PCB bottom view with components for LQFP32; test circuit Fig.3.

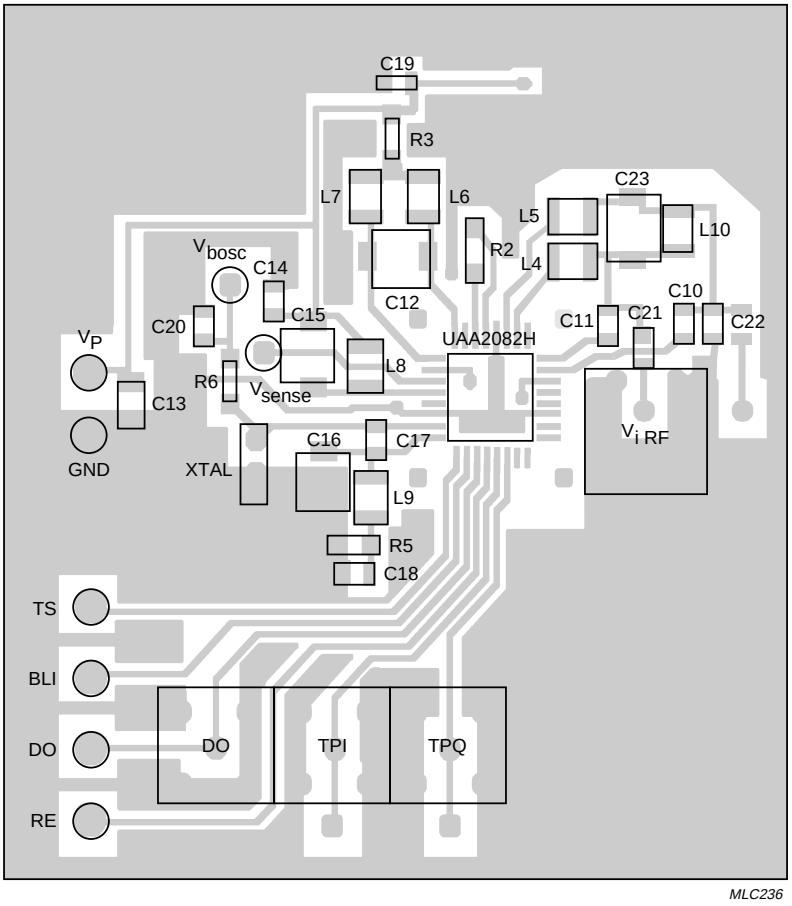


Fig.17 PCB top view with components for LQFP32; test circuit Fig.5.

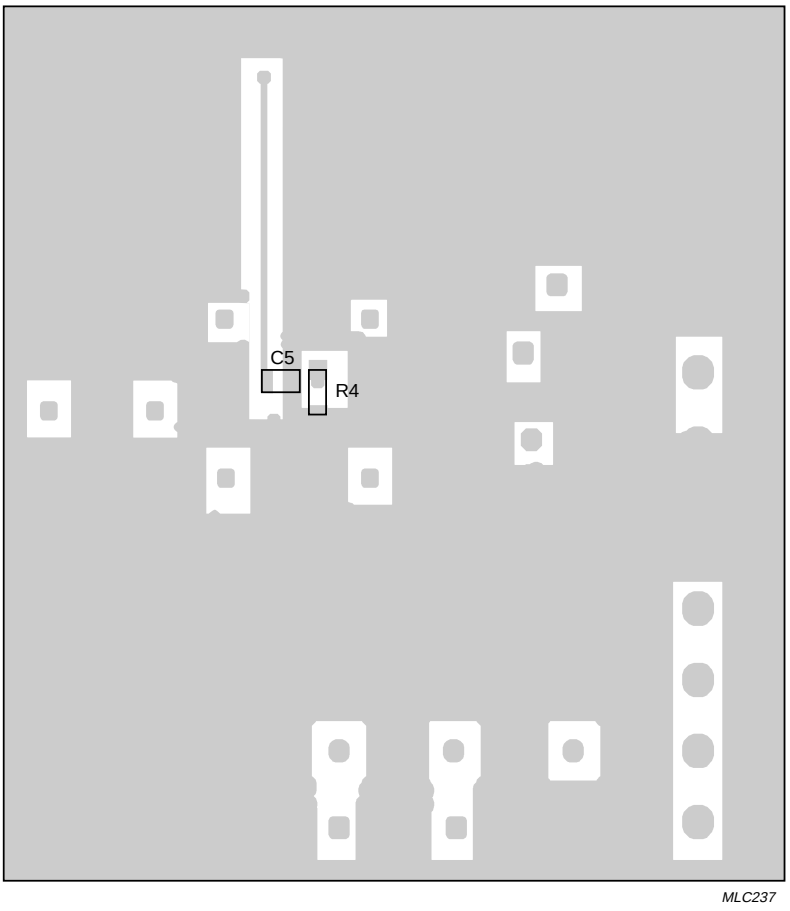


Fig.18 PCB bottom view with components for LQFP32; test circuit Fig.5.

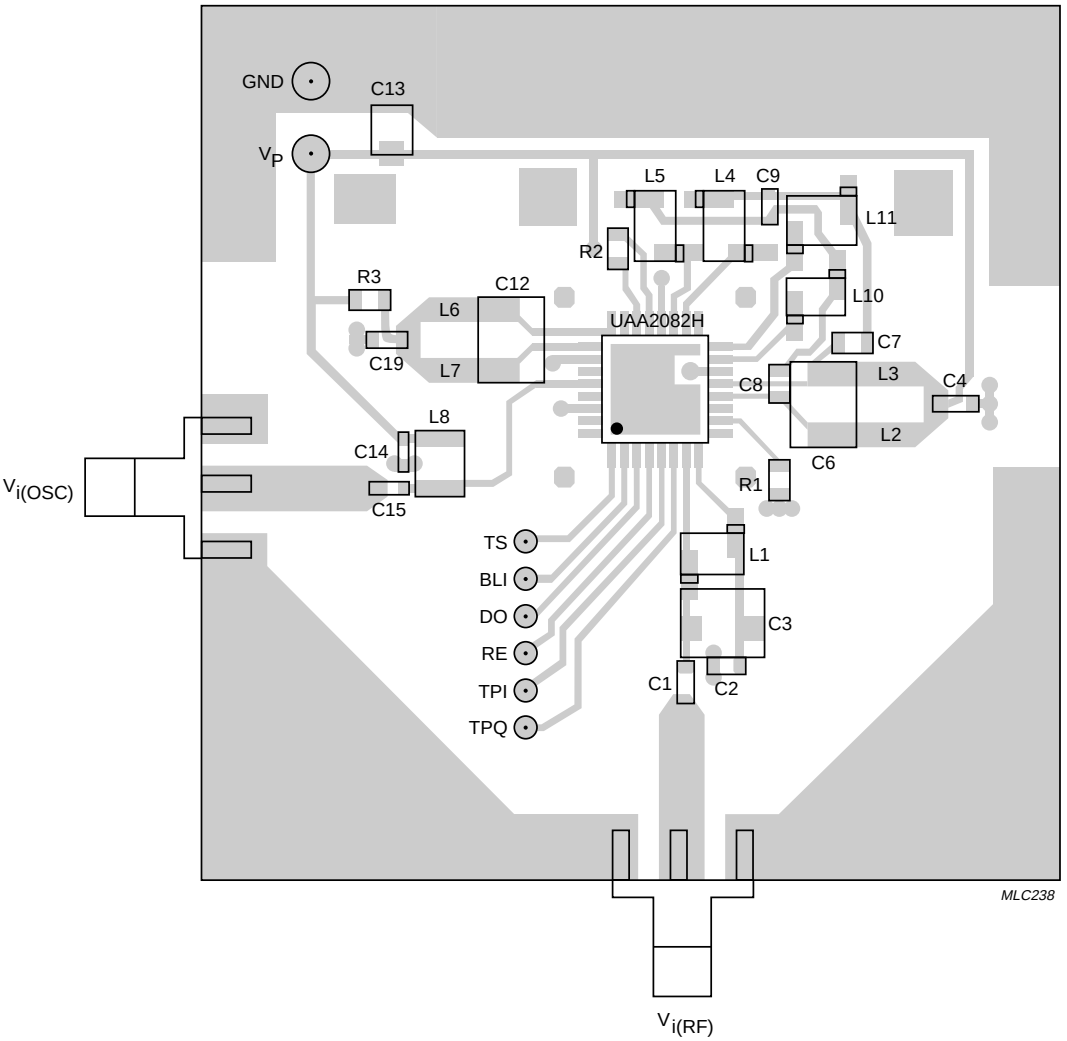


Fig.19 PCB top view with components for LQFP32; test circuit Fig.6.

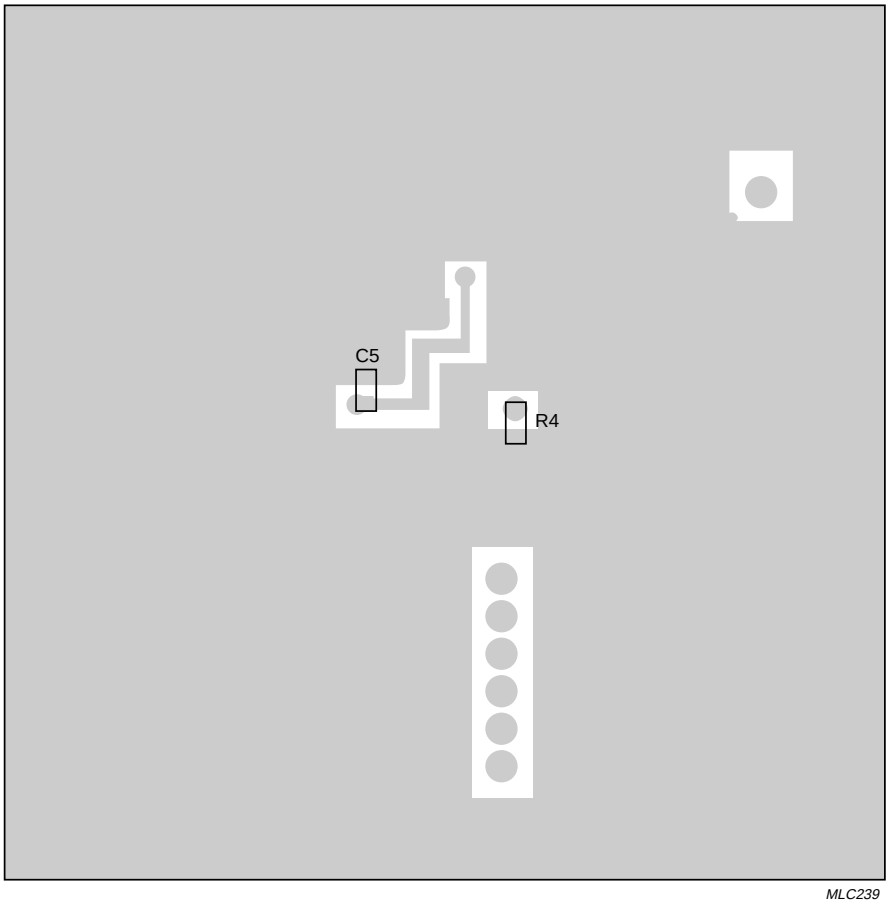
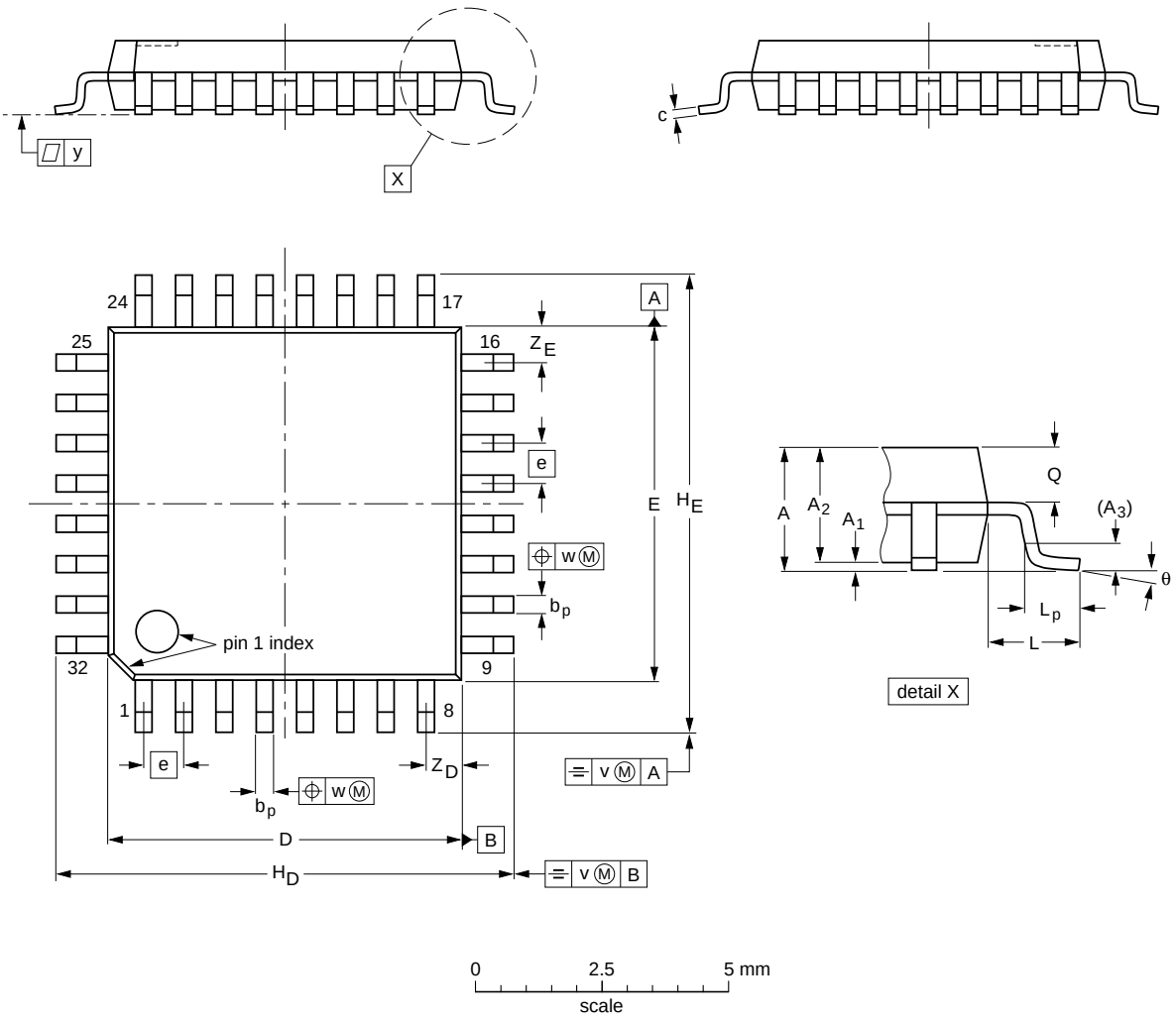


Fig.20 PCB bottom view with components for LQFP32; test circuit Fig.6.

PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1						~~93-06-29~~ 95-12-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

NOTES

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