

FDLL457A



LL-34

THE PLACEMENT OF THE EXPANSION GAP
HAS NO RELATIONSHIP TO THE LOCATION
OF THE CATHODE TERMINAL

COLOR BAND MARKING

DEVICE	1ST BAND	2ST BAND
FDLL457A	RED	BLACK

Small Signal Diode

Absolute Maximum Ratings (Note 1) $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{RRM}	Maximum Repetitive Reverse Voltage	70	V
$I_{F(AV)}$	Average Rectified Forward Current	200	MA
I_{FSM}	Peak Forward Surge Current Pulse width = 1.0 second Pulse width = 1.0 microsecond	1.0 4.0	A A
T_{stg}	Storage Temperature Range	-65 to +200	$^\circ\text{C}$
T_J	Operating Junction Temperature	175	$^\circ\text{C}$

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:

Note 1) These ratings are limiting values above which serviceability of any semiconductor device may be impaired.

Note 2) Measured on 8.3ms single half-sine wave or equivalent square wave. Duty cycle=4 pulses per minute maximum.

Thermal Characteristics

Symbol	Characteristic	Value	Units
P_D	Total Device Dissipation	500	mW
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	300	$^\circ\text{C/W}$

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
V_R	Breakdown Voltage	$I_R = 100 \mu\text{A}$	85		V
V_F	Forward Voltage	$I_F = 10 \text{ mA}$ $I_F = 100 \text{ mA}$		1.0 1.0	V V
I_R	Reverse Current	$V_R = 60 \text{ V}$ $V_R = 60 \text{ V}, T_A = 150^\circ\text{C}$		25 5.0	nA μA
C_T	Total Capacitance	$V_R = 0, f = 1.0 \text{ MHz}$		6.0	pF

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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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