HMC835LP6GE

v04.1113

FRACTIONAL-N PLL WITH INTEGRATED VCO 33 - 4100 MHz

Features

Wideband: 33 - 4100 MHz

Maximum Phase Detector Rate: 100 MHz

Low Phase Noise: -110 dBc/Hz in Band @2GHz

PLL FOM:

-230 dBc/Hz Integer Mode, -227 dBc/Hz Fractional Mode

< 94 fs Integrated RMS Jitter (1 kHz to 100 MHz)

Low Noise Floor: -167 dBc/Hz

2 Differential RF outputs

External LO Input

Exact Frequency Mode:
0 Hz Fractional Frequency Error

Programmable RF Output Phase

Output Phase Synchronous Frequency Changes

Output Phase Synchronization

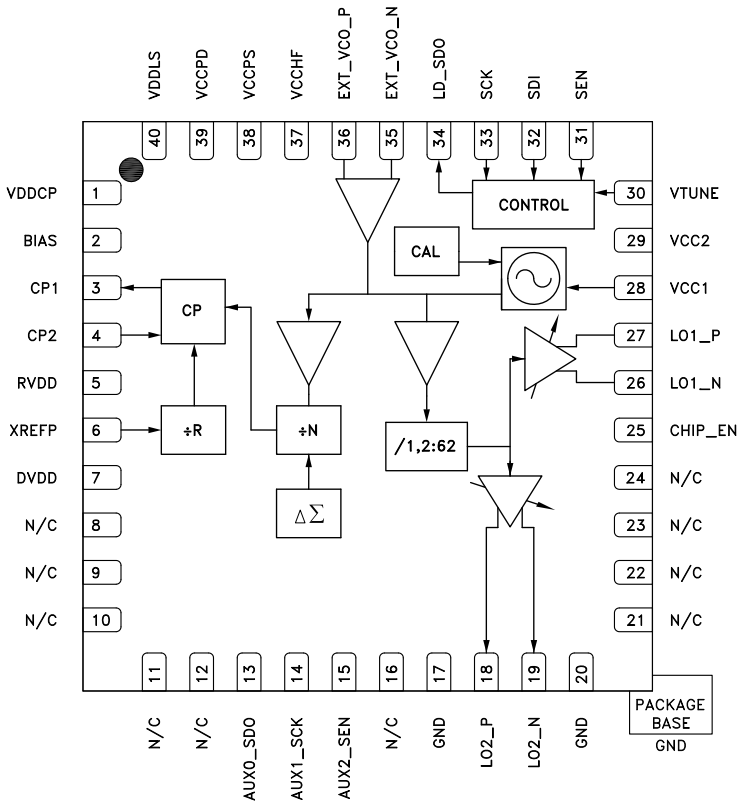
RF Output Mute Function

40 Lead 6x6 mm SMT Package: 36 mm^2

Typical Applications

- MIMO Radio Architectures
- Cellular Infrastructure
- Cellular backhaul
- Communication Test Equipment
- CATV Equipment
- Phased Array Applications
- DDS Replacement

Functional Diagram



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General Description

The HMC835LP6GE is a low noise, wide band, Fractional-N PLL that features an integrated VCO with a fundamental frequency of 2050 to 4100 MHz, and an integrated VCO Output Divider (divide by 2/4/6/.../60/62) that together enable the HMC835LP6GE to generate frequencies from 33 MHz to 4100 MHz. Integrated Phase Detector (PD) and a delta-sigma modulator capable of operating at up to 100 MHz enable wider loop-bandwidths, faster frequency changes along with excellent spectral performance.

Two independent RF outputs, with independent gain control, enable the HMC835LP6GE to distribute identical frequency and phase signals to multiple destinations, at optimal signal levels tailored to each output.

An external VCO input allows the HMC835LP6GE to lock external VCOs, and enables cascaded LO architectures for MIMO radio applications. Two separate Charge Pump (CP) outputs enable separate loop filters optimized for both integrated and external VCOs, and seamless switching between integrated or external VCOs during operation. Programmable RF output phase feature can further phase adjust and synchronize multiple HMC835LP6GEs enabling scalable MIMO and beam-forming radio architectures.

Additional features include configurable output mute function that mutes RF outputs during frequency changes, Exact Frequency Mode that enables the HMC835LP6GE to generate fractional frequencies with 0 Hz frequency error, and the ability to synchronously change frequencies without changing the phase of the output signal.

Electrical Specifications

VPPCP, VDDLS, VCC1, VCC2 = 5 V; RVDD, AVDD, DVDD, VCCPD, VCCHF, VCCPS = 3.3 V Min and Max Specified across Temp -40 °C to 85 °C

Parameter	Condition	Min.	Typ.	Max.	Units
RF Output Characteristics					
Output Frequency		33		4100	MHz
VCO Frequency at PLL Input		2050		4100	MHz
RF Output Frequency at f_{VCO}		2050		4100	MHz
Output Power					
RF Output Power at fundmental frequency at 2050 MHz	Max Gain Setting Reg 16h[7:6]=11 Differential (100 Ohm load). Output power varies with frequency and output configu-ration. See Figures 11, 12, 13, 14		5		dBm
Output Power Control range	3 dB Steps		9		dB
Harmonics for Fundamental Mode					
fo Mode at 2 GHz	2nd / 3rd / 4th		-26/-20/-39		dBc
fo/2 Mode at 2GHz/2 = 1 GHz	2nd / 3rd / 4th		-27/-17/-35		dBc
fo/30 Mode at 3 GHz/30 = 100 MHz	2nd / 3rd / 4th		-26/-10/-38		dBc

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Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
fo/62 Mode at 3999 MHz/62 = 64.5 MHz	2nd / 3rd / 4th		-23/-10/-31		dBc
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,...,62	1		62	

Parameter	Condition	Min.	Typ.	Max.	Units
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (+/- 4) dynamically max	20		524,283	
REF Input Characteristics					
Max Ref Input Frequency				350	MHz
Ref Input Level	AC Coupled [1]	-6		12	dBm
Ref Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	
Phase Detector (PD) [2]					
PD Frequency Fractional Mode	[3]	DC		100	MHz
PD Frequency Integer Mode		DC		100	MHz
Charge Pump					
Output Current		0.02		2.54	mA
Charge Pump Gain Step Size			20		µA
PD/Charge Pump SSB Phase Noise	50 MHz Ref, Input Referred				
1 kHz			-143		dBc/Hz
10 kHz	Add 2 dB for Fractional		-150		dBc/Hz
100 kHz	Add 3 dB for Fractional		-153		dBc/Hz
Logic Inputs					
Vsw			0.9		V
Logic Outputs					
VOH Output High Voltage			1.8/3.3		V
VOL Output Low Voltage			0		V
Output Impedance		100		200	Ω
Maximum DC current to a load				1.5	mA

[1] Measured with 100 Ω external termination. See "1.3.2 Reference Input Stage" section for more details.

[2] Slew rate of ≥ 0.5 ns/V is recommended, see "1.3.2 Reference Input Stage" section for more details. Frequency is guaranteed across process voltage and temperature from -40 °C to +85 °C.

[3] This maximum PD frequency can only be achieved if the minimum N value is respected. eg. In the case of fractional mode, the maximum PD frequency = fvco/20 or 100 MHz, whichever is less.

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Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Voltages					
3.3 V Supplies	AVDD, VCCHF, VCCPS, 3VRVDD,DVDD3V,VCCPD	3.1	3.3	3.5	V
5 V Supplies	VCC1,VCC2,VDDLS, VDDCP	4.8	5	5.2	V
Power Supply Currents					
+5V Analog Charge Pump (VDDCP)			6		mA
+5V VCO core + LO1 Buffer Only (VCC2)	Single-Ended Output[4]	99		110	
	Differential Output [4]	104		129	
+5V VCO core + LO2 Buffer Only (VCC2)	Single-Ended Output[4]	99		110	
	Differential Output [4]	104		129	
+5V VCO core + LO1 Buffer + LO2 Buffer (VCC2)	Single-Ended Output[4]	108		130	
	Differential Output [4]	118		168	
+5V VCO Divider and RF/PLL Buffer (VCC1)	Fo/1 Mode		27		
	Fo/N (2,4...62) Mode	52		73	
+3.3V VCCPD, VCCPS, VCCHF, DVDD, RVDD			48		
Power Down - Crystal Off	Reg 01h=0, Crystal Not Clocked (5V and 3.3V combined)		1		µA
Power Down - Crystal On, 100 MHz	Reg 01h=0, Crystal Clocked 100 MHz		5		mA
Power on Reset					
Typical Reset Voltage on DVDD			700		mV
Min DVDD Voltage for No Reset		1.5			V
Power on Reset Delay			250		µs
VCO Open Loop Phase Noise at fo @ 4 GHz					
10 kHz Offset			-78		dBc/Hz
100 kHz Offset			-108		dBc/Hz
1 MHz Offset			-134.5		dBc/Hz
10 MHz Offset			-156		dBc/Hz
100 MHz Offset			-171		dBc/Hz
VCO Open Loop Phase Noise at fo @ 3 GHz/2 = 1.5 GHz					
10 kHz Offset			-89		dBc/Hz
100 kHz Offset			-119		dBc/Hz
1 MHz Offset			-143.7		dBc/Hz
10 MHz Offset			-160.7		dBc/Hz
100 MHz Offset			-167		dBc/Hz

[4] Minimum and Maximum current various by different Gain settings from 0 to 3

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Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
VCO Open Loop Phase Noise at fo @3 GHz/30 = 100 MHz					
10 kHz Offset			-111		dBc/Hz
100 kHz Offset			-142		dBc/Hz
1 MHz Offset			-167		dBc/Hz
10 MHz Offset			-170		dBc/Hz
100 MHz Offset			-171		dBc/Hz
PLL Figure of Merit (FOM)					
Floor Integer Mode (Fig 28)	Normalized to 1 Hz		-230		dBc/Hz
Floor Fractional Mode (Fig 28)	Normalized to 1 Hz		-227		dBc/Hz
Flicker (Both Modes) (Fig 28)	Normalized to 1 Hz		-268		dBc/Hz
VCO Characteristics					
VCO Tuning Sensitivity at 3862 MHz	Measured with 2.5 V on VTUNE; see Fig 7		15		MHz/V
VCO Tuning Sensitivity at 3643 MHz	Measured with 2.5 V on VTUNE; see Fig 7		14.5		MHz/V
VCO Tuning Sensitivity at 3491 MHz	Measured with 2.5 V on VTUNE; see Fig 7		16.2		MHz/V
VCO Tuning Sensitivity at 3044 MHz	Measured with 2.5 V on VTUNE; see Fig 7		14.6		MHz/V
VCO Tuning Sensitivity at 2558 MHz	Measured with 2.5 V on VTUNE; see Fig 7		15.4		MHz/V
VCO Tuning Sensitivity at 2129 MHz	Measured with 2.5 V on VTUNE; see Fig 7		14.8		MHz/V
VCO Supply Pushing	Measured with 2.5 V on VTUNE		2		MHz/V

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Typical Performance Characteristics

Figure 1. Closed Loop Fractional Phase Noise at 4100 MHz, Divided by 1 to 62 [1][5]

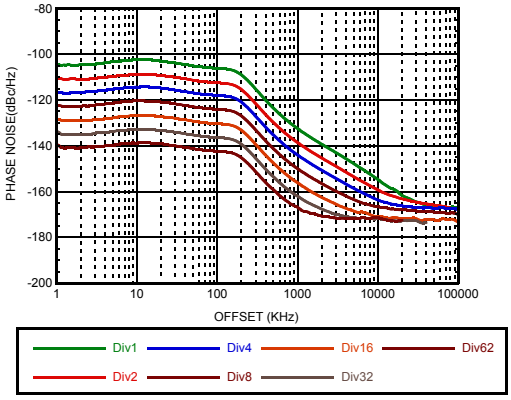


Figure 2. Closed Loop Fractional Phase Noise at 3600 MHz, Divided by 1 to 62 [1][5]

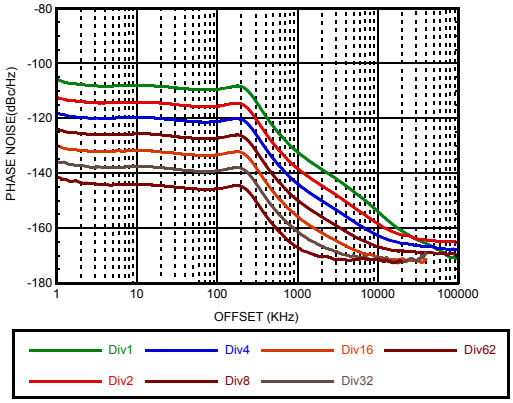


Figure 3. Closed Loop Phase Noise at 3300 MHz, Divided by 1 to 62 [2][5]

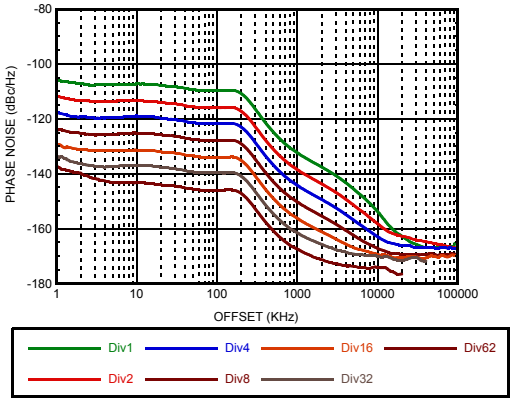


Figure 4. Closed Loop Phase Noise at 3300 MHz, Divided by 1 to 62 [3][5]

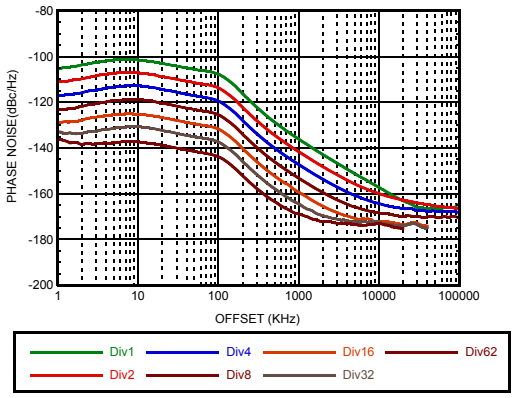


Figure 5. Closed Loop Phase Noise at 3300MHz for different Loop Filter [4][5]

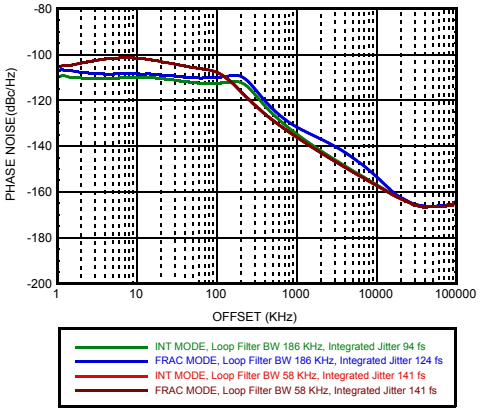
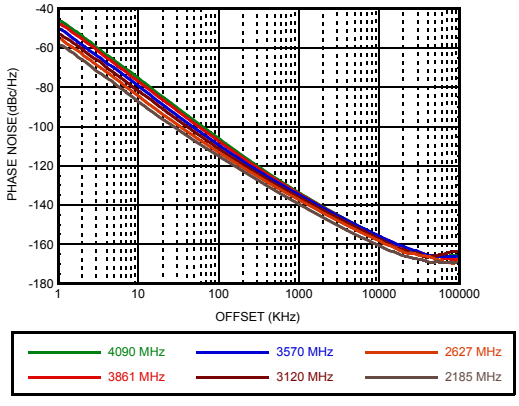


Figure 6. Free Running VCO Phase Noise



[1] Measured with 122.88 MHz Xtal, 61.44 MHz PD frequency, Loop Filter #1, CP = 2.54 mA, Offset Dn = 435 uA.
[2] Measured with 100 MHz Xtal, 50 MHz PD frequency, Loop Filter #1, CP = 2.54 mA, Offset Dn = 435 uA.
[3] Measured with 100 MHz Xtal, 50 MHz PD frequency, Loop Filter #2, CP = 2.54 mA, Offset Dn = 435 uA.
[4] Measured with 100 MHz Xtal, 50 MHz PD frequency, Loop Filter #1 and Loop Filter #2, CP= 2.54 mA. Offset Dn = 435 uA. Phase Noise integrated from 1 kHz to 100 MHz
[5] Loop Filter designs are provided in Table 1

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Figure 7. Typical VCO Sensitivity

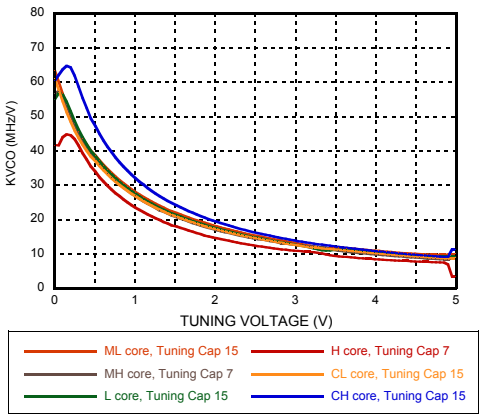


Figure 8. Typical Tuning Voltage After Calibration [6]

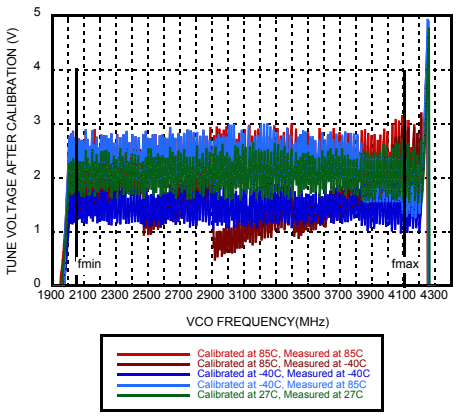


Figure 9. Open Loop Phase Noise vs. Temp

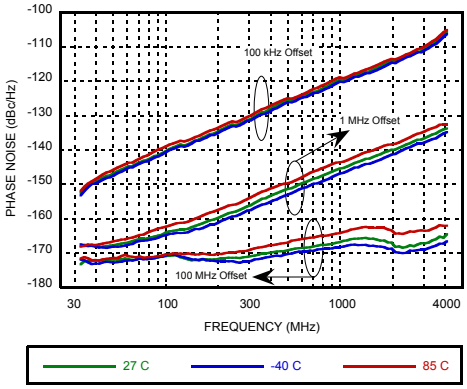


Figure 10. Single Sideband Integrated Phase Noise [7]

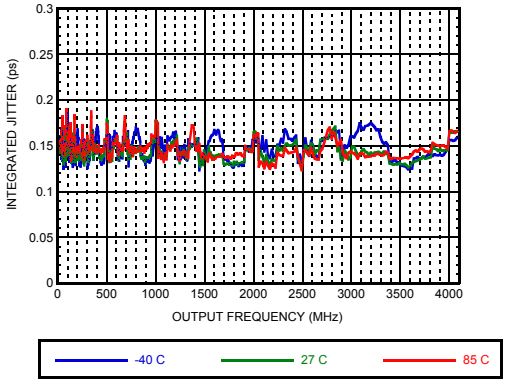


Figure 11. Differential Output Power (LO1, LO2) [8] [9]

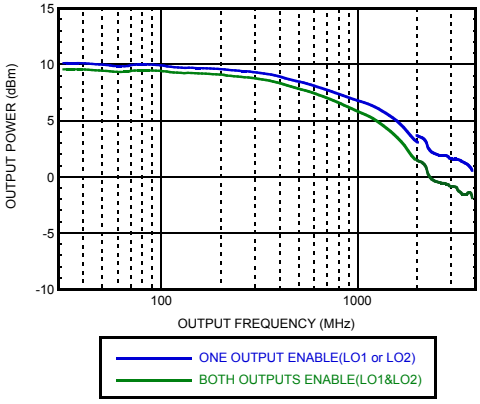
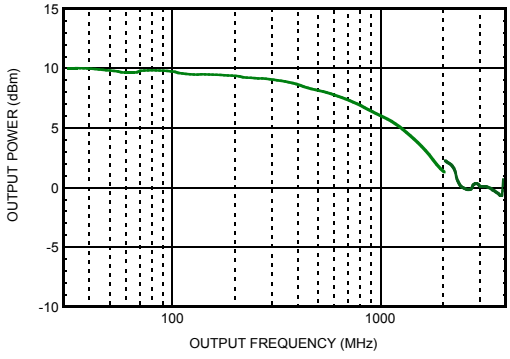


Figure 12. Single-Ended Output Power (LO1_N, LO2_P) [9]



[6] The HMC835LP6GE features an internal AutoCal process that seamlessly calibrates the HMC835LP6GE when a frequency change is executed. Once calibrated, at any temperature, the calibration setting holds across the entire operating range of the HMC835LP6GE (-40 ˚C to +85 ˚C). Fig 10 shows that the tuning voltage of the HMC835LP6GE is maintained within a narrow operating range for worst case scenarios where calibration was executed at one temperature extreme and the HMC835LP6GE is operating at the other extreme.

[7] 100 MHz Xtal, 50 MHz PD frequency. Loop Filter #1 with CP and Offset scaling. Phase Noise integrated from 1 kHz to 100 MHz

[8] This is the measured power into 50 Ohm load to ground on each of the differential output legs, LO_N & LO_P. Output power into differential 100 Ohm load is ~3dB higher.

[9] Gain Setting: Reg 16h[7:6] = 11 and Reg 16h[9:8] = 11; Divider Boost setting: Reg 16h[10] = 1 measured at 27C

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Figure 13. Single-Ended Output Power LO1_N or LO2_P When Other Port operating Differential [9]

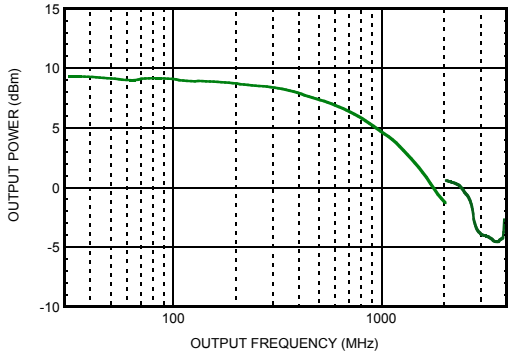


Figure 14. Typical Differential Output Power vs Frequency and Temp(Max Gain 11) [8] [9]

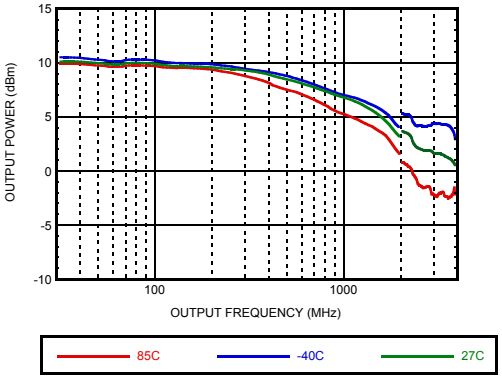


Figure 15. Typical Differential Output Power vs Frequency and Gain [8]

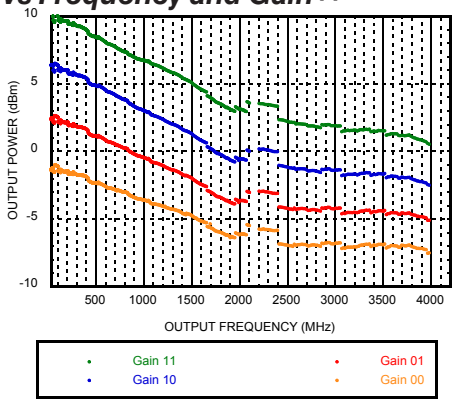


Figure 16. Fractional Spurious Performance at 904 MHz, Exact Frequency Mode ON [10]

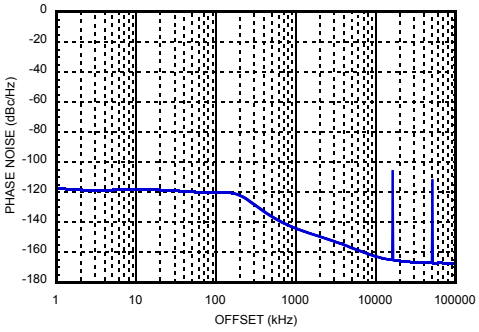


Figure 17. Fractional Spurious Performance at 1804 MHz, Exact Frequency Mode ON [10]

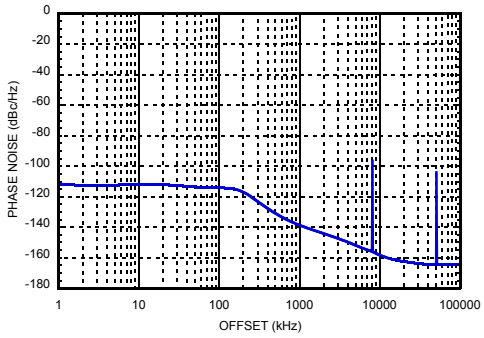
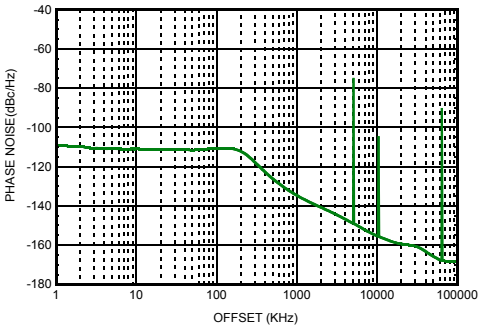


Figure 18. Fractional Spurious Performance at 2646.96 MHz, Exact Frequency Mode ON [11]



[10] 100 MHz Xtal, PD 50 MHz, Channel Spacing = 200 KHz, Loop Filter #1 from Table 1. Exact Frequency Mode ON.
[11] 122.88 Xtal, PD 61.44. Loop Filter #1 from Table 1 is used. Channel spacing 240 KHz. Exact Frequency Mode ON

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Figure 19. Fractional Spurious Performance at 2646.96 MHz, Exact Frequency Mode OFF [12]

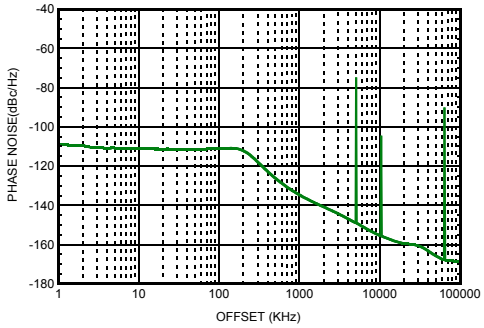


Figure 20. Low Frequency Performance [13]

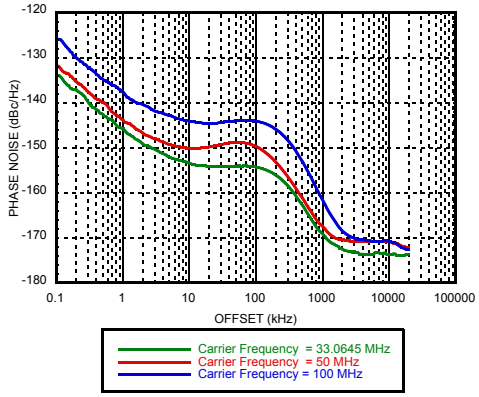


Figure 21. Typical Spurious Emissions at 3000.1 MHz, Fixed Reference [14]

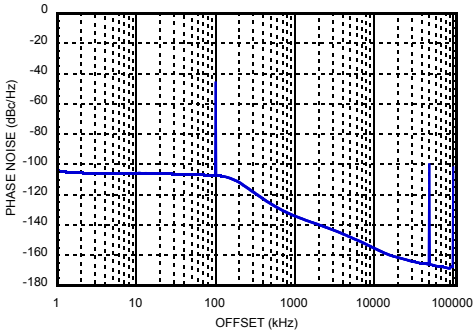


Figure 22. Typical Spurious Emissions at 3000.1 MHz, Tunable Reference [15]

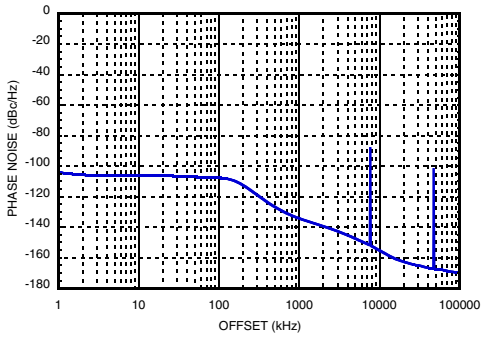


Figure 23. Typical Spurious vs Offset from 3 GHz, Fixed vs. Tunable Reference [16]

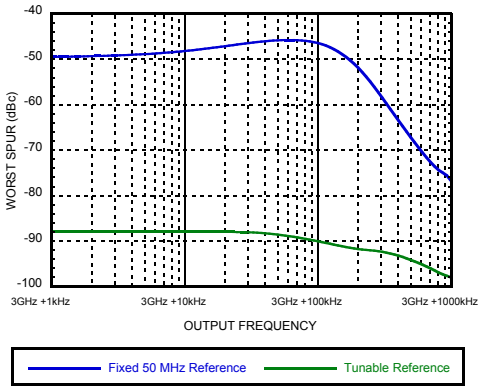
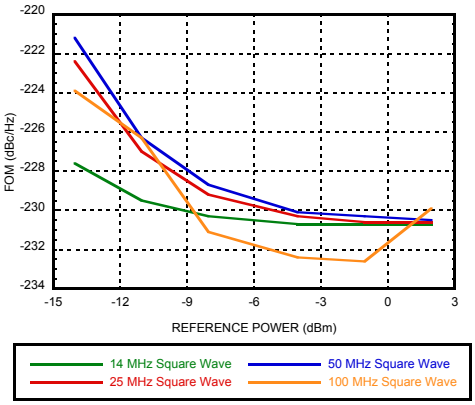


Figure 24. Reference Input Sensitivity, Square Wave [17]



[12] 122.88 Xtal, PD 61.44. Loop Filter #1 from Table 1 is used. Channel spacing 240 KHz. Exact Frequency Mode OFF
[13] 100 MHz Xtal, PD Frequency 50 MHz, Loop Filter #3 from Table 1 is used. CP = 2.54 mA. Set to Integer Mode.
[14] 100 MHz Xtal, PD Frequency 50 MHz,Loop Filter #1 from Table 1 is used. The plot shows an integer boundary spur inside the loop filter bandwidth.
[15] The tunable reference is used to change the reference frequency from 50 MHz in Fig 22 to 47.5 MHz in Fig 23 in order to distance the integer boundary spur away from the carrier frequency so that it is filtered by the loop filter. Loop Filter Type 1 from Table 1 is used.
[16] The plot is generated by recoding the magnitude of the largest spur only at any offset, at each output frequency, while using a fixed 50MHz reference, and a tunable 47.5 MHz reference.See detail procedure discussed in [17]. Contact Hittite Apps Support to obtain the required configuration to achieve similar spurious performance throughout the operating range of the HMC835LP6GE.
[17] Measured from a 50 Ω source with a 100 Ω external resistor termination.

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Figure 25. Reference Input Sensitivity, Sinusoidal Wave [17]

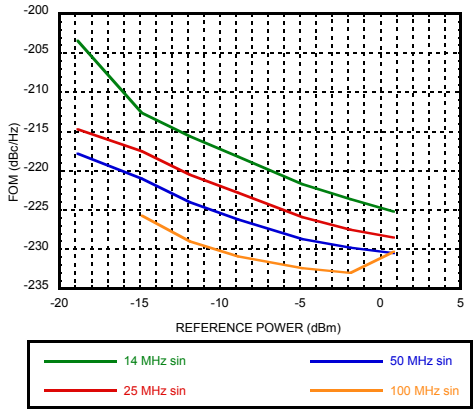


Figure 26. Phase Adjust at 0 degree[18]

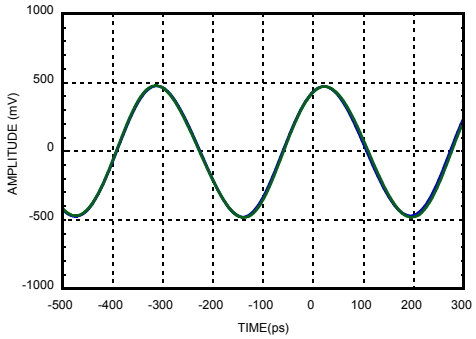


Figure 27. Phase Adjust at 90 degree [19]

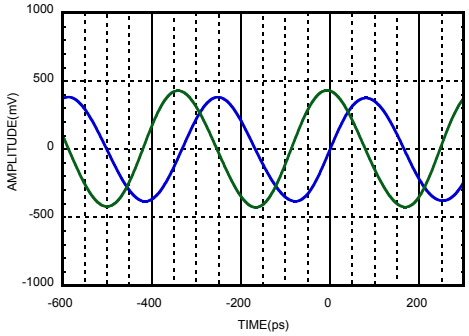


Figure 28. Phase Adjust at 180 degree [20]

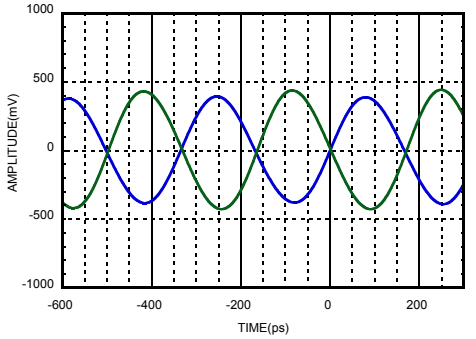


Figure 29. Figure of Merit

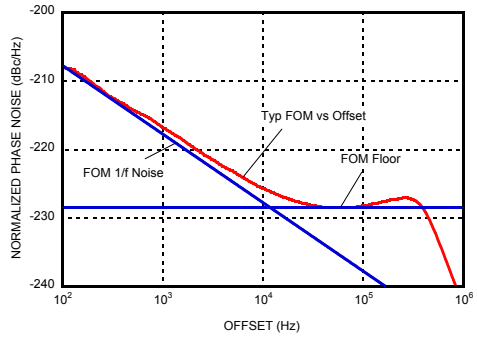
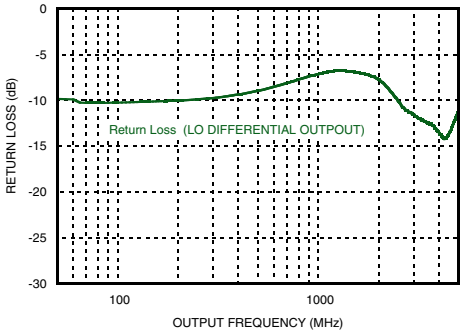


Figure 30. RF Output Return Loss Diff [21]



[18] Loop Filter #1 from Table 1 used. Phase adjust feature limited to Fundamental Mode operation (2050 to 4100MHz). The plot is capture by using two identical HMC835LP6GE eval boards driven by the same 10MHz external reference source from instrument via on board HMC1031MS8E to generate a 50 MHz reference frequency to lock with HMC835LP6GE, and captured with 26GHz 50 Ω high speed Oscilloscope. Seed value in Reg1A for both HMC835LP6GE initially set to 0. Then Reg1A was adjusted in HMC835LP6GE #1 to bring the phase into alignment with HMC835LP6GE #2.

[19] Phase adjust feature limited to Fundamental Mode operation (2050 to 4100MHz). Starting condition as stated in [18] then HMC835LP6GE #2 seed value Reg 1Ah set to 400000h. Required seed value calculated from (Phase Adjust (degrees)/360˚ x 2^{24}.

[20] Phase adjust feature limited to Fundamental Mode operation (2050 to 4100MHz). Starting condition as stated in [18] then HMC835LP6GE #2 seed value Reg 1Ah set to 800000h.

[21] Both LO1 and LO2 Output Buffer Enabled in Reg 17h[5:4] as 11.Differential or single-ended mode programmed in Reg 17h[9:8].

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Figure 31. RF Output Return Loss Diff [21]

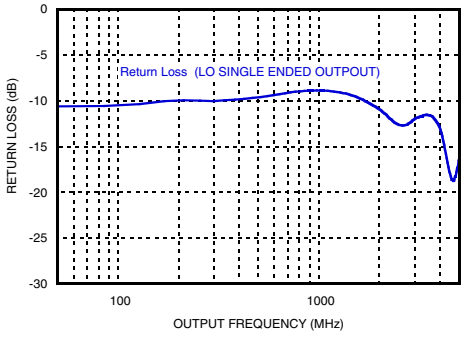


Figure 32. Frequency Settling After Frequency Change, AutoCal Enabled [22]

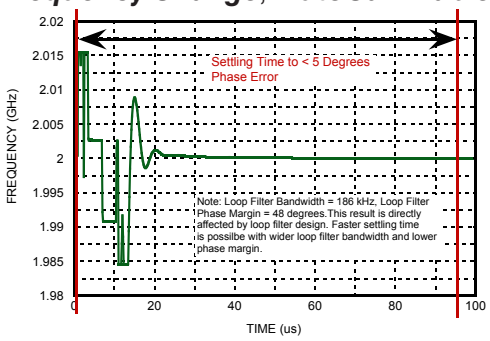


Figure 33. Phase Settling After Frequency Change, AutoCal Enabled [22]

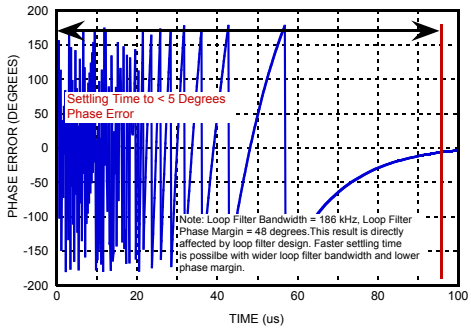


Figure 34. Frequency Settling After Frequency Change, Manual Calibration [23]

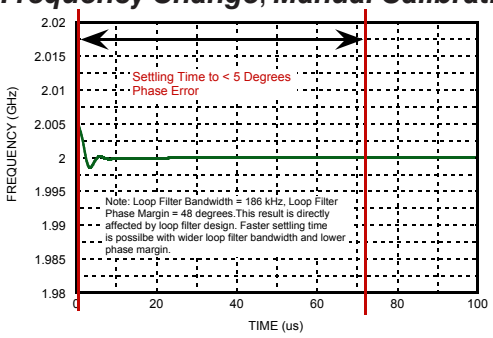


Figure 35. Phase Settling After Frequency Change, Manual Calibration [23]

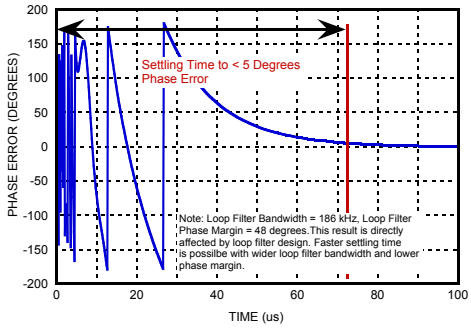
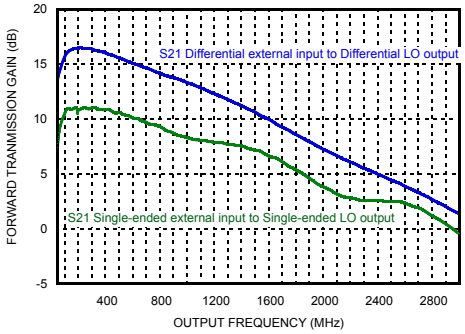


Figure 36. External VCO Port Gain (Ext VCO In to LO Out) [24]



[22] The HMC835LP6GE features an internal AutoCal process that seamlessly calibrates the HMC835LP6GE when a frequency change is executed. Typical frequency settling time that can be expected after any frequency change (Reg 03h or Reg 04h writes) is shown in Fig 31 with AutoCal enabled (Reg 0Ah[11] = 0). Frequency hop of 5 MHz is shown in Fig 31, however the settling time is independent of the size of the frequency change. Any size frequency size hop will have a similar settling time with AutoCal enabled. Loop BW = 186 kHz (Loop Filter #1 in Table 1).

[23] For applications that require fast frequency changes, the HMC835LP6GE supports manual calibration that enables faster settling times. Manual calibration needs to be executed only once for each individual HMC835LP6GE, at any temperature, and is valid across all temperature operating range of the HMC835LP6GE. More information about manual calibration is available in section 1.2.1.6. Frequency hop of 5 MHz is shown in Fig 33 and Fig 34 however the settling time is independent of the size of the frequency change. Any size frequency size hop will have a similar settling time with AutoCal disabled (Reg 0Ah[11] = 1). Loop BW = 186 kHz (Loop Filter #1 in Table 1).

[24] 0dbm IN. External Buffer Bias is configured in Reg 18h[20:19] as 11. Both LO1 and LO2 Output Buffer Enabled in Reg 17h[5:4] as 11.Differential or single-ended mode programmed in Reg 17h[9:8].

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Figure 37. HMC835LP6GE with External VCO HMC384LP4E at 2213MHz [25]

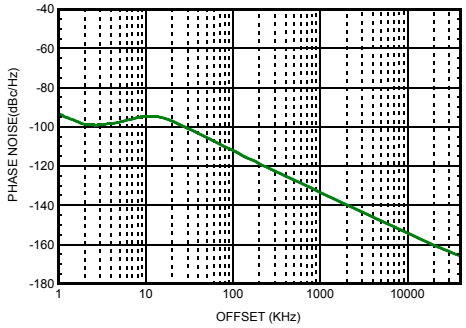


Figure 38. HMC835LP6GE Mute and Isolations

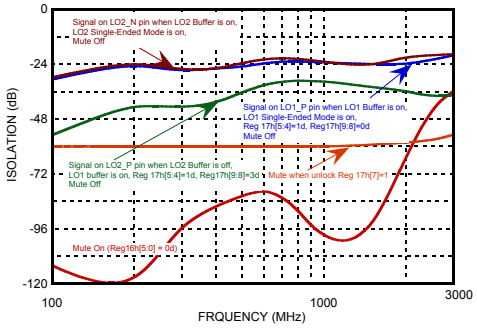
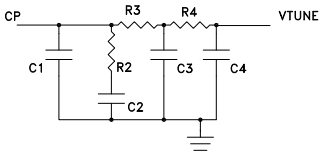
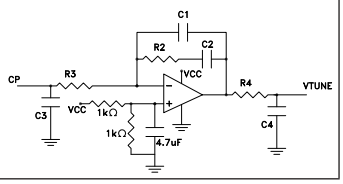


Table 1. Loop Filter Designs Used in Typical Performance Characteristics Graphs

Loop Filter ID	Loop BW (kHz)	Loop Phase Margin	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (Ω)	R3 (Ω)	R4 (Ω)	Loop Filter Design
#1 [26]	161	53°	180	6.8	47	47	2200	1000	1000	
#2 [27]	80	56°	56	22	220	220	1000	1000	1000	
#3 [28]	214	61°	56	1.8	NA	NA	2200	0	0	
#4 [29]	17	66°	3300	330	1500	4700	75	75	12	

[25] 50MHz PFD with Loop Filter Type 4 is used. In order to configure HMC835LP6GE to use with external VCO, Reg 17h need to be configured to disable the on chip VCO and VCO to PLL path while enable External Buffer, second CP link and External IO switch. Reg 17h [0:11] as 3157d. Reg 0Bh[4] =1: PFD SWAP might be needed to be selected for active loop filter. Reg 0Bh[4] = 0: For use with positive tuning slope VCO and PASSIVE loop filter. Reg 0Bh[4] = 1: For use with a NEGATIVE slope VCO or with a ACTIVE loop filter.

[26] Loop Filter #1 is suggested to use for best integrated phase noise. It is designed for 50 MHz PD frequency, CP =2 mA in Fractional Mode.

[27] Loop Filter #2 is suggested to use for best far out phase noise. It is designed for 50 MHz PD frequency, CP =2 mA in Fractional Mode.

[28] Loop Filter #3 is suggested to use for best low frequency phase noise used as reference source. It is designed for 50 MHz PD frequency, CP =2 mA in Integer Mode.

[29] Loop Filter #4 is a example to use HMC835LP6GE as a PLL and connect with external VCO.

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Table 2. Pin Descriptions

Pin Number	Function	Description
1	VDDCP	Power Supply for charge pump analog section, 5.0V Nominal
2	BIAS	External bypass decoupling for precision bias circuits, 3.5 V NOTE: BIAS ref voltage cannot drive an external load. Must be measured with 10 GΩ meter such as Agilent 34410A, normal 10 MΩ DVM will read erroneously.
3	CP1	Charge Pump output 1
4	CP2	Charge Pump output 2
5	RVDD	Reference supply, 3.3 V nominal.
6	XREFP	Reference Input. DC bias is generated internally. Normally AC coupled externally.
7	DVDD	Digital supply, 3.3 V nominal
8, 9, 10, 11, 12, 16, 21, 22, 23, 24	N/C	No Connect
13	AUX0_SDO	Auxiliary SDO, digital output
14	AUX1_SCK	Auxiliary SCK, digital output
15	AUX2_SEN	Auxiliary SEN, digital output
17	GND	Ground
18	LO2_P	RF Output LO2_P, positive side, used for differential or dual outputs only.
19	LO2_N	RF Output LO2_N, negative side, used in single-ended, differential, or dual output mode
20	GND	Ground
25	CHIP_EN	Chip Enable input.
26	LO1_N	RF output LO_N, negative side, used for single-ended, differential, or dual output mode
27	LO1_P	RF output LO_P, positive side, used for differential or dual outputs only.
28	VCC1	VCO analog supply 1.
29	VCC2	VCO analog supply 2.
30	VTUNE	VCO varactor tuning port input.
31	SEN	Serial Port Enable (CMOS) logic input
32	SDI	Serial Port Data (CMOS) logic input
33	SCK	Serial Port Clock (CMOS) logic input
34	LD_SDO	Lock Detect or Serial Data Output (CMOS) logic output.
35	EXT_VCO_N	External VCO negative input.
36	EXT_VCO_P	External VCO positive input.
37	VCCHF	Analog supply, 3.3 V nominal
38	VCCPS	Analog supply, Prescaler, 3.3 V nominal
39	VCCPD	Analog supply, Phase Detector, 3.3 V nominal
40	VDDLS	Analog supply, Charge Pump, 5.0 V nominal

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Absolute Maximum Ratings

AVDD, RVDD, DVDD, VCCPD, VCCHF, VCCPS	-0.3 V to +3.6 V
VPPCP, VDDLS, VCC1	-0.3 V to +5.5 V
VCC2	-0.3 V to +5.5 V
Operating Temperature	-40 °C to +85 °C
Storage Temperature	-65 °C to 150 °C
Maximum Junction Temperature	150 °C
Thermal Resistance (Θ_{JC}) (junction to case (ground paddle))	9 °C/W
Reflow Soldering	
Peak Temperature	260 °C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Condition	Min.	Typ.	Max.	Units
Temperature					
Ambient backside metal ground pad Temperature[1]		-40		85	°C
Supply Voltage					
AVDD, RVDD, DVDD, VCCPD, VCCHF, VCCPS		3.1	3.3	3.5	V
VPPCP, VDDLS, VCC1, VCC2,VDDCP		4.8	5	5.2	V

[1] Layout design guidlines set out in Qualification Test Report are strongly recommended with paddle at 85°C.

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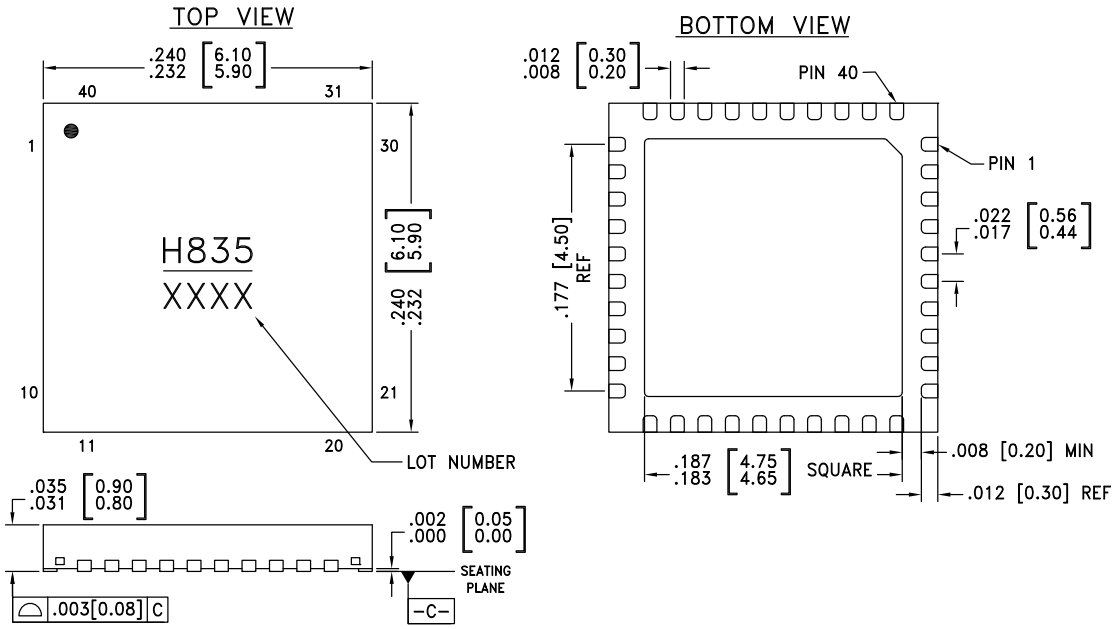
FRACTIONAL-N PLL WITH INTEGRATED VCO 33 - 4100 MHz

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC835LP6GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H835 XXXX

[1] 4-Digit lot number XXXX

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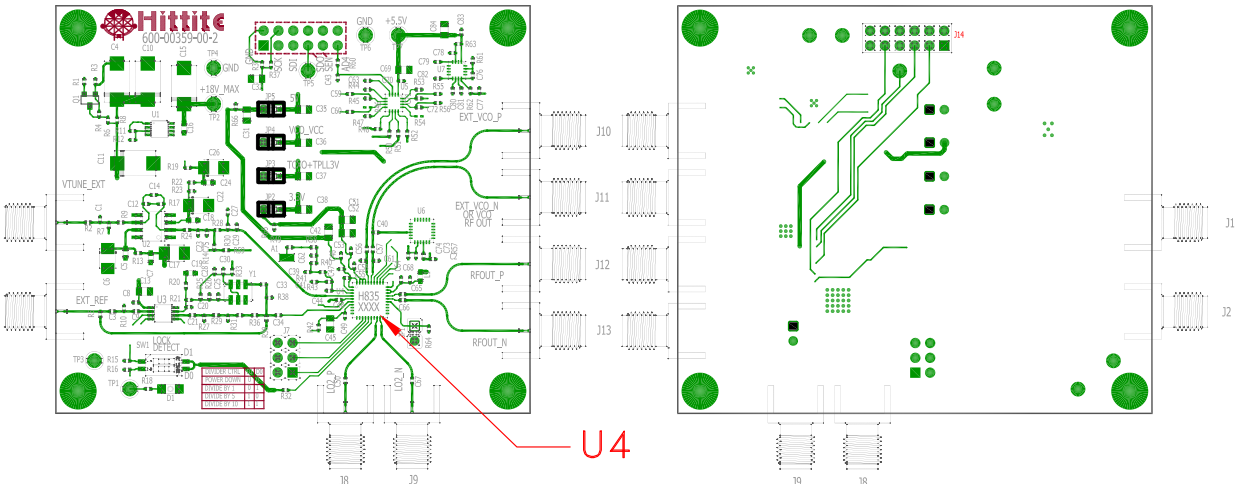
Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC835LP6GE from the "Search by Part Number" pull down menu to view the product splash page.

Evaluation Order Information

Item	Contents	Part Number
Evaluation Kit	HMC835LP6GE Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC835LP6G

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Changing Evaluation Board Reference Frequency & CP Current Configuration

The evaluation board is provided with a 50 MHz on-board reference oscillator, and loop filter #1 configuration shown in Table 1 (~161 kHz bandwidth). The default register configuration file included in the Hittite PLL Evaluation software sets the comparison frequency to 50 MHz (R=1, ie. Reg 02h = 1).

As with all PLL's and PLL with Integrated VCOs, modifying the comparison frequency or Charge Pump (CP) current will result in changes to the loop dynamics and ultimately, phase noise profile. When making these changes there are several items to keep in mind:

- CP Offset Current setting - Refer to Section 1.3.1.
- LD Configuration - Refer to Section 1.3.5.

To redesign the loop filter for a particular application, download Hittite's PLL Design software tool by clicking on the "Software Download" link on the HMC835LP6GE product page at www.hittite.com. Hittite PLL Design enables users to accurately model and analyze performance of all Hittite PLLs, PLLs with Integrated VCOs, and Clock Generators. It supports various loop filter topologies, and enables users to design custom loop filters and accurately simulate resulting performance.

For evaluation purposes, the HMC835LP6GE evaluation board is shipped with an on-board, low cost, reasonable noise 100 ppm, 50 MHz VCXO, enabling evaluation of most parameters including phase noise without any external references.

Exact phase or frequency measurements require the HMC835LP6GE to use the same reference as the measuring instrument. To accommodate this requirement, the HMC835LP6GE evaluation board includes the HMC1031MS8E; a simple low current integer-N PLL that can lock the on-board VCXO to an external 10 MHz reference input commonly provided by most test equipment. To lock the HMC835LP6GE to external 10 MHz reference simply connect the external reference output to J2 input of the HMC835LP6GE evaluation board and change the HMC1031MS8E integer divider value to 5 by changing the switch settings D1 = 1 (SW1-4 closed), and D0 = 0 (SW2-3 open), for more information please see the HMC1031MS8E data sheet.

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Use HMC835LP6GE as PLL with external VCO Configuration

In general, in order to configure HMC835 with external VCO, Reg17h needs to be configured to disable the on chip VCO and VCO to PLL path while enable external buffer, CP2 link and External IO switch. The recommended value for Reg 17h is to be set as 3157d. Reg 19h[20:19] is also available to adjust the EXT VCO amp Input depending on the external VCO RF output level.

Use HMC835LP6GE as PLL with on board external VCO

In order to demonstrate the ablity of using HMC835LP6GE as a PLL alone with external VCO, the evaluation board is provided with a on board external VCO HMC384LP4E and Loop Filter Type 4 configuration shown in Table 1(~17 kHz bandwidth). A 0 Ω resister on C40 and a 0.001 uF capcitor on C58 need to be soldered in order to convert the standard HMC835LP6GE evaluation board to work with on board external VCO configuration.Jumper J4 needs to be put on for HMC384LP4E power supply. Reg 0Bh[4] PFD invert needs to be set to 1 in order to work with on board active loop filter. (0=For use with positive tuning slope VCO and PASSIVE loop filter. 1=For use with a NEGATIVE slope VCO or with a ACTIVE loop filter)

Use HMC835LP6GE as PLL with off board external VCO

The evaluation board is provided with external VCO input ports (J10: EXT_VCO_P and J11: EXT_VCO_N). Prepopulated loop filter can be modified according to external VCO characteristics.

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HMC835LP6GE Application Information

Large bandwidth (33 MHz to 4100 MHz), excellent phase noise and spurious performance, and phase noise floor (-167 dBc/Hz), coupled with a high level of integration make the HMC835LP6GE ideal for a variety of applications; as an RF or IF stage LO.

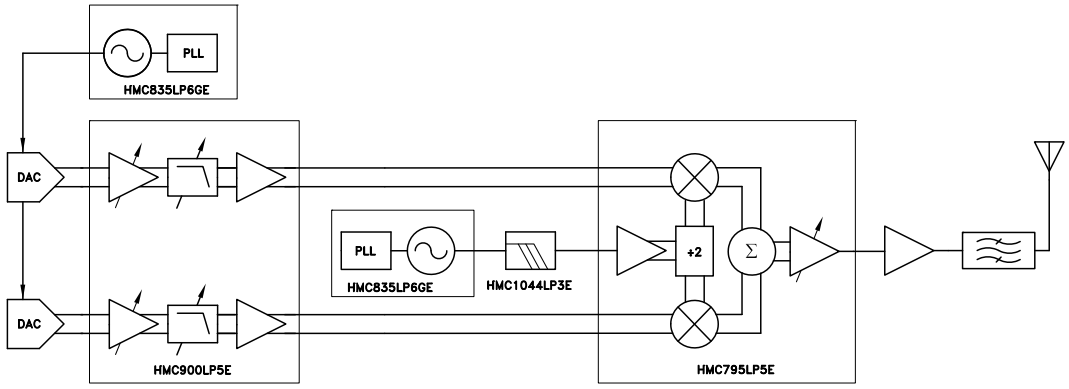

Figure 36. HMC835LP6GE in a typical transmit chain

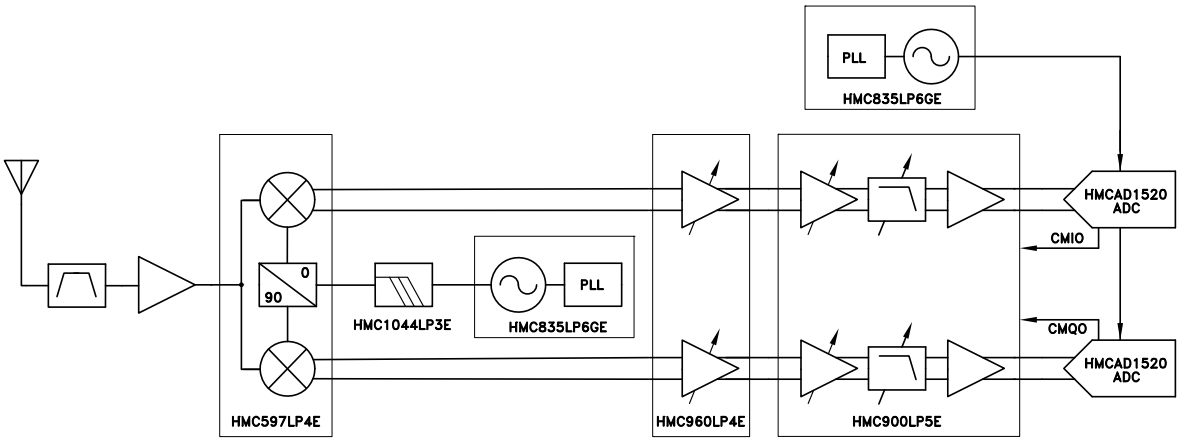

Figure 37. HMC835LP6GE in a typical receive chain

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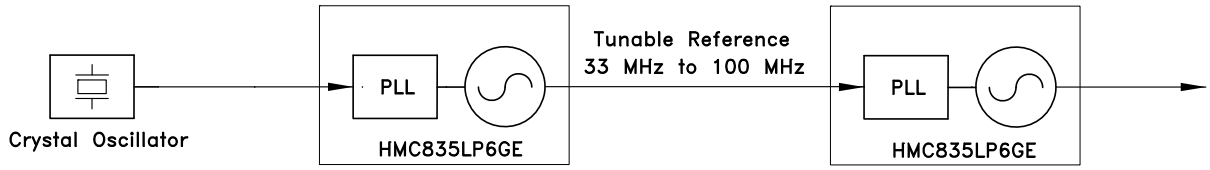

Figure 38. FRACTIONAL-N PLL WITH INTEGRATED VCO used as a tunable reference for HMC835LP6GE

Using the HMC835LP6GE with a tunable reference as shown in Fig 38, it is possible to drastically improve spurious emissions performance across all frequencies. Example shown in Fig 23 Fig 24 shows that it is possible to achieve spurious emissions as low as -95 dBc/Hz at 3 GHz. Please contact Hittite's application support to obtain detailed tunable reference information.

Power Supply

The HMC835LP6GE is a high performance low-noise device. In some cases phase noise and spurious performance may be degraded by noisy power supplies. To achieve maximum performance and ensure that power supply noise does not degrade the performance of the HMC835LP6GE it is highly recommended to use Hittite's low noise high PSRR (Power Supply Rejection Ratio) regulator, the HMC1060LP3E. Using the HMC1060LP3E lowers the design risk and cost, and ensures that the performance shown in "Typical Performance Characteristics" can be achieved.

Power supply noise contribution to the PLL output phase noise can easily be modelled in the Hittite PLL Design tool. To download Hittite's PLL Design software tool, click on the "Software Download" link on the HMC835LP6GE product page at www.hittite.com

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1.0 Theory of Operation

The block diagram of HMC835LP6GE PLL with Integrated VCO is shown in Figure 39.

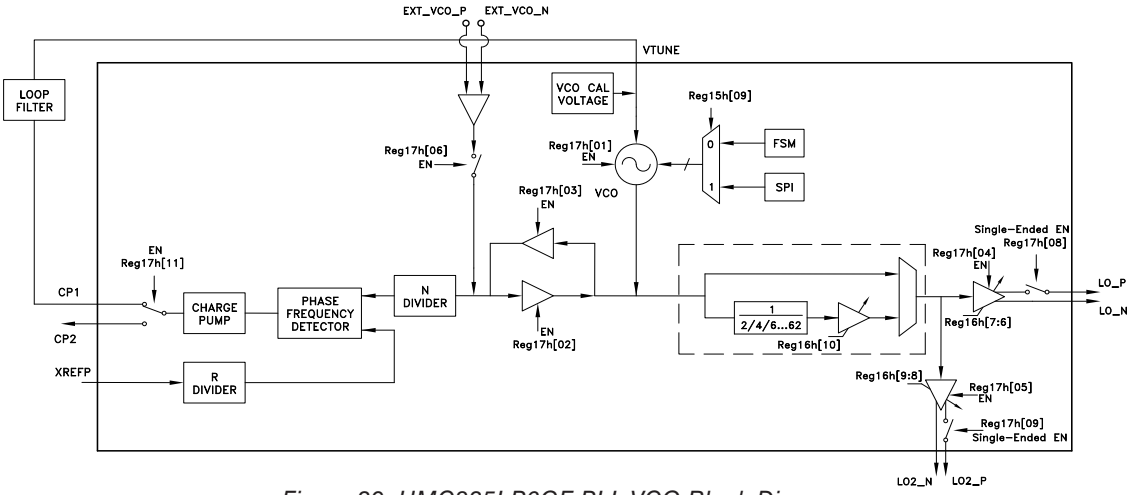

Figure 39. HMC835LP6GE PLL VCO Block Diagram

1.1 Overview

The PLL divides down the VCO output to the desired comparison frequency via the N-divider (integer value set in Reg 03h, fractional value set in Reg 04h), compares the divided VCO signal to the divided reference signal (reference divider set in Reg 02h) in the Phase Detector (PD), and drives the VCO tuning voltage via the Charge Pump (CP) (configured in Reg 09h) to the VCO subsystem. Some of the additional PLL subsystem functions include:

- Delta Sigma configuration (Reg 06h)
- Exact Frequency Mode (Configured in Reg 0Ch, Reg 06h,Reg 03h, and Reg 04h)
- Lock Detect (LD) Configuration (Reg 07h to configure LD, and Reg 0Fh to configure LD_SDO output pin)
- External CEN pin used as hardware enable pin.

Typically, only writes to the divider registers (integer part Reg 03h, fractional part Reg 04h,VCO Divide Ratio part Reg 04h) are required for HMC835LP6GE output frequency changes.

Divider registers of the PLL (Reg 03h, and Reg 04h), set the fundamental frequency (2050 MHz to 4100 MHz) of the VCO. Output frequencies ranging from 33 MHz to 2050 MHz are generated by tuning to the appropriate fundamental VCO frequency (2050 MHz to 4100 MHz) by programming N divider (Reg 03h, and Reg 04h), and programming the output divider (divide by 1/2/4/6.../60/62, programmed in Reg 16h) in the VCO register.

For detailed frequency tuning information and example, please see "1.3.7 Frequency Tuning" section.

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1.2 VCO Subsystem

The VCO consists of a capacitor switched step tuned VCO and an output stage. In typical operation, the VCO is programmed with the appropriate capacitor switch setting which is executed automatically by the PLL AutoCal state machine if AutoCal is enabled (Reg 0Ah[11] = 0, see section "1.2.1 VCO Calibration" for more information). The VCO tunes to the fundamental frequency (2050 MHz to 4100 MHz), and is locked by the CP output from the PLL subsystem. The VCO controls the output stage of the HMC835LP6GE enabling configuration of:

- VCO Output divider settings configured in Reg 16h (divide by 2/4/6...60/62 to generate frequencies from 33 MHz to 2050 MHz, or divide by 1 to generate fundamental frequencies between 2050 MHz and 4100 MHz)
- Output gain settings (Reg 16h[7:6], Reg 16h[9:8])
- Single-ended or differential output operation (Reg 17h[9:8])
- Always Mute (Reg 16h[5:0])
- Mute when unlock (Reg 17h[7])

1.2.1 VCO Calibration

1.2.1.1 VCO Auto-Calibration (AutoCal)

The HMC835LP6GE uses a step tuned type VCO. A step tuned VCO is a VCO with a digitally selectable capacitor bank allowing the nominal center frequency of the VCO to be adjusted or 'stepped' by switching in/out VCO tank capacitors. A step tuned VCO allows the user to center the VCO on the required output frequency while keeping the varactor tuning voltage optimized near the mid-voltage tuning point of the HMC835LP6GE's charge pump. This enables the PLL charge pump to tune the VCO over the full range of operation with both a low tuning voltage and a low tuning sensitivity (kvco).

The VCO switches are normally controlled automatically by the HMC835LP6GE using the Auto-Calibration feature. The Auto-Calibration feature is implemented in the internal state machine. It manages the selection of the VCO sub-band (capacitor selection) when a new frequency is programmed. The VCO switches may also be controlled directly via register Reg 15h for testing or for other special purpose operation.

To use a step tuned VCO in a closed loop, the VCO must be calibrated such that the HMC835LP6GE knows which switch position on the VCO is optimum for the desired output frequency. The HMC835LP6GE supports Auto-Calibration (AutoCal) of the step tuned VCO. The AutoCal fixes the VCO tuning voltage at the optimum mid-point of the charge pump output, then measures the free running VCO frequency while searching for the setting which results in the free running output frequency that is closest to the desired phase locked frequency. This procedure results in a phase locked oscillator that locks over a narrow voltage range on the varactor. A typical tuning curve for a step tuned VCO is shown in Fig 40.Note how the tuning voltage stays in a narrow range over a wide range of output frequencies such as fast frequency hopping.

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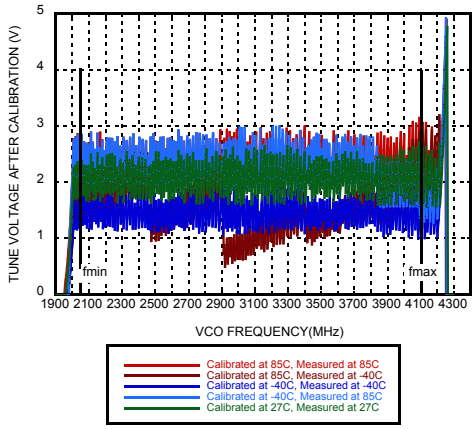

Figure 40. Typical VCO Tuning Voltage After Calibration

The calibration is normally run automatically once for every change of frequency. This ensures optimum selection of VCO switch settings vs. time and temperature. The user does not normally have to be concerned about which switch setting is used for a given frequency as this is handled by the AutoCal routine. The accuracy required in the calibration affects the amount of time required to tune the VCO. The calibration routine searches for the best step setting that locks the VCO at the current programmed frequency, and ensures that the VCO will stay locked and perform well over it's full temperature range without additional calibration, regardless of the temperature that the VCO was calibrated at.

Auto-Calibration can also be disabled allowing manual VCO tuning. Refer to section 1.2.1.6 for a description of manual tuning.

1.2.1.2.2 Auto-reLock on Lock Detect Failure

It is possible by setting Reg 0Ah[17] to have the VCO subsystem automatically re-run the calibration routine and re-lock itself if Lock Detect indicates an unlocked condition for any reason. With this option the system will attempt to re-Lock only once.

1.2.1.3.3 VCO AutoCal on Frequency Change

Assuming Reg 0Ah[11]=*0*, the VCO calibration starts automatically whenever a frequency change is requested. If it is desired to rerun the AutoCal routine for any reason, at the same frequency, simply rewrite the frequency change with the same value and the AutoCal routine will execute again without changing final frequency.

1.2.1.4.4 VCO AutoCal Time & Accuracy

The VCO frequency is counted for T_{mmt}, the period of a single AutoCal measurement cycle.

$$T_{mmt} = T_{xtal} \cdot R \cdot 2^n \quad \text{(EQ 1)}$$

n — is set by Reg 0Ah[2:0] and results in measurement periods which are multiples of the PD period, $T_{xtal}R$.

R — is the reference path division ratio currently in use, Reg 02h

T_{xtal} — is the period of the external reference (crystal) oscillator.

The VCO AutoCal counter will, on average, expect to register N counts, rounded down (floor) to the nearest integer, every PD cycle.

N — is the ratio of the target VCO frequency, f_{vco}, to the frequency of the PD, f_{pd}, where N can

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be any rational number supported by the N divider.

N is set by the integer (N_{int} = Reg 03h) and fractional (N_{frac} = Reg 04h) register contents

$$N = N_{int} + N_{frac} / 2^{24} \quad \text{(EQ 2)}$$

The AutoCal state machine runs at the rate of the FSM clock, T_{FSM}, where the FSM clock frequency cannot be greater than 50 MHz.

$$T_{FSM} = T_{xtal} \cdot 2^{m} \quad \text{(EQ 3)}$$

m is 0, 2, 4 or 5 as determined by Reg 0Ah[14:13]

The expected number of VCO counts, V, is given by

$$V = floor\ (N \cdot 2^{n}) \quad \text{(EQ 4)}$$

The nominal VCO frequency measured, f_{vcom}, is given by

$$f_{vcom} = V \cdot f_{xtal} / (2^{n} \cdot R) \quad \text{(EQ 5)}$$

where the worst case measurement error, f_{err} , is:

$$f_{err} \approx \pm f_{pd} / 2^{n+1} \quad \text{(EQ 6)}$$

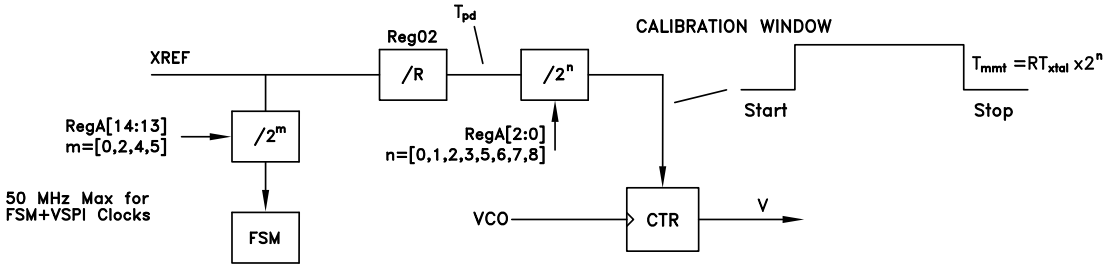

Figure 41. VCO Calibration

A 5-bit step tuned VCO, for example, nominally requires 5 measurements for calibration, worst case 6 measurements, and hence 7 VSPI data transfers of 20 clock cycles each. Total calibration time, worst case, is given by:

$$T_{cal} = k128T_{FSM} + 6T_{PD}\ 2^{n} + 7 \cdot 20T_{FSM} \quad \text{(EQ 7)}$$

or equivalently

$$T_{cal} = T_{xtal}\ (6R \cdot 2^{n} + (140+(3 \cdot 128)) \cdot 2^{m}) \quad \text{(EQ 8)}$$

For guaranteed hold of lock, across temperature extremes, the resolution should be better than 1/8th the frequency step caused by a VCO sub-band switch change. Better resolution settings will show no improvement.

1.2.1.4.1.1 VCO AutoCal Example

The HMC835LP6GE must satisfy the maximum f_{pd} limited by the two following conditions:

a. N ≥ 16 (f_{int}), N ≥ 20.0 (f_{frac}), where N = f_{VCO}/ f_{pd}

b. f_{pd} ≤ 100 MHz

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Suppose the HMC835LP6GE output frequency is to operate at 2.01 GHz. Our example crystal frequency is f_{xtal} = *50 MHz, R=1, and m=0 (*Fig 41*)*, hence T_{FSM} = 20 ns (50 MHz). Note, when using AutoCal, the maximum AutoCal Finite State Machine (FSM) clock cannot exceed 50 MHz (see Reg 0Ah[14:13]). The FSM clock does not affect the accuracy of the measurement, it only affects the time to produce the result. This same clock is used to clock the 16 bit VCO serial port.

If time to change frequencies is not a concern, then one may set the calibration time for maximum accuracy, and therefore not be concerned with measurement resolution.

Using an input crystal of 50 MHz (R=1 and fpd=50 MHz) the times and accuracies for calibration using (EQ 6) and (EQ 8) are shown in Table 3. Where minimal tuning time is 1/8th of the VCO band spacing.

Across all VCOs, a measurement resolution better than 800 kHz will produce correct results. Setting m = 0, n = 5, provides 781 kHz of resolution and adds 8.6 µs of AutoCal time to a normal frequency hop. Once the AutoCal sets the final switch value, 8.64 µs after the frequency change command, the fractional register will be loaded, and the loop will lock with a normal transient predicted by the loop dynamics. Hence as shown in this example that AutoCal typically adds about 8.6 µs to the normal time to achieve frequency lock. Hence, AutoCal should be used for all but the most extreme frequency hopping requirements.

Table 3. AutoCal Example with F_{xtal} = 50 MHz, R = 1, m = 0

Control Value *Reg0Ah[2:0]*	n	2^n	T_{mmt} (µs)	T_{cal} (µs)	F_{err} Max
0	0	1	0.02	4.92	± 25 MHz
1	1	2	0.04	5.04	± 12.5 MHz
2	2	4	0.08	5.28	± 6.25 MHz
3	3	8	0.16	5.76	± 3.125 MHz
4	5	32	0.64	8.64	± 781 kHz
5	6	64	1.28	12.48	± 390 kHz
6	7	128	2.56	20.16	± 195 kHz
7	8	256	5.12	35.52	± 98 kHz

1.2.1.5 Manual VCO Calibration for Fast Frequency Hopping

If it is desirable to switch frequencies quickly it is possible to eliminate the AutoCal time by calibrating the VCO in advance and storing the switch number vs frequency information in the host. This can be done by initially locking the HMC835LP6GE on each desired frequency using AutoCal, then reading, and storing the selected VCO switch settings. The VCO switch settings are available inReg 15h[8:1] after every AutoCal operation. The host must then program the VCO switch settings directly when changing frequencies. Manual writes to the VCO switches are executed immediately as are writes to the integer and fractional registers when AutoCal is disabled. Hence frequency changes with manual control and AutoCal disabled, requires a minimum of two serial port transfers to the HMC835LP6GE, once to set the VCO switches, and once to set the PLL frequency.

If AutoCal is disabled Reg 0Ah[11]=1, the VCO will update its registers with the value written via Reg 15h[8:1] immediately.

1.2.2 Registers required for Frequency Changes in Fractional Mode

A large change of frequency, in fractional mode (Reg 06h[11]=1), may require Main Serial Port writes to:

1. The integer register intg, Reg 03h *(only required if the integer part changes)*
2. Manual VCO Tuning Reg 15h only required for manual control of VCO if Reg 0Ah[11]=1 *(AutoCal*

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disabled)

3. VCO Divide Ratio and Gain Register
   - Reg 16h[5:0] is required to change the VCO Output Divider value if needed.
   - Reg 16h[10:6] is required to change the Output Gain if needed.
4. The fractional register, Reg 04h. The fractional register write triggers AutoCal if Reg 0Ah[11]=0, and is loaded into the Delta Sigma modulator automatically after AutoCal runs. If AutoCal is disabled, Reg 0Ah[11]=1, the fractional frequency change is loaded into the Delta Sigma modulator immediately when the register is written with no adjustment to the VCO.

Small steps in frequency in fractional mode, with AutoCal enabled (Reg 0Ah[11]=0), usually only require a single write to the fractional register. Worst case, 3 Main Serial Port transfers to the HMC835LP6GE could be required to change frequencies in fractional mode. If the frequency step is small and the integer part of the frequency does not change, then the integer register is not changed. In all cases, in fractional mode, it is necessary to write to the fractional register Reg 04h for frequency changes.

1.2.3 Registers Required for Frequency Changes in Integer Mode

A change of frequency, in integer mode (Reg 06h[11]=0), requires Main Serial Port writes to:

1. VCO register
   - Reg 15h only required for manual control of VCO if Reg 0Ah[11]=1 (AutoCal disabled)
   - Reg 16h is required to change the VCO Output Divider value if needed
2. The integer register Reg 03h.
   - In integer mode, an integer register write triggers AutoCal if Reg 0Ah[11]=0, and is loaded into the prescaler automatically after AutoCal runs. If AutoCal is disabled, Reg 0Ah[11]=1, the integer frequency change is loaded into the prescaler immediately when written with no adjustment to the VCO. Normally changes to the integer register cause large steps in the VCO frequency, hence the VCO switch settings must be adjusted. AutoCal enabled is the recommended method for integer mode frequency changes. If AutoCal is disabled (Reg 0Ah[11]=1), a prior knowledge of the correct VCO switch setting and the corresponding adjustment to the VCO is required before executing the integer frequency change.

1.2.4 VCO Output Mute Function

The HMC835LP6GE features an intelligent output mute function with the capability to disable the VCO output while maintaining the PLL and VCO subsystems fully functional. The mute function is automatically controlled by the HMC835LP6GE, and provides a number of mute control options including:

1. Always mute (Reg 16h[5:0] = 0d). This mode is used for manual mute control.
2. Automatically mute the outputs during VCO calibration (Reg 17h[7] = 1) that occurs during output frequency changes.

This mode can be useful in eliminating any out of band emissions during freqeuncy changes, and ensuring that the system emits only desired frequencies. It is enabled by writing Reg 17h[7] = 1. Typical isolation when the HMC835LP6GE is muted is always better than 60 dB, and is ~ 30 dB better than disabling the output buffers of the HMC835LP6GE via Reg 17h[5:4].

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1.3 PLL Overview

1.3.1 Phase Detector (PD)

The Phase detector (PD) has two inputs, one from the reference path divider and one from the RF path divider. When in lock these two inputs are at the same average frequency and are fixed at a constant average phase offset with respect to each other. We refer to the frequency of operation of the PD as f_{pd}. Most formulae related to step size, delta-sigma modulation, timers etc., are functions of the operating frequency of the PD, f_{pd}. f_{pd} is also referred to as the comparison frequency of the PD.

The PD compares the phase of the RF path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies linearly over a full ±2π radians (±360°) of input phase difference.

1.3.1.1 Charge Pump

A simplified diagram of the charge pump is shown in Fig 42. The CP consists of 4 programmable current sources, two controlling the CP Gain (Up Gain Reg 09h[13:7], and Down Gain Reg 09h[6:0]) and two controlling the CP Offset, where the magnitude of the offset is set by Reg 09h [20:14], and the direction is selected by Reg 09h [21]=1 for up and Reg 09h [22]=1 for down offset.

CP Gain is used at all times, while CP Offset is only recommended for fractional mode of operation. Typically the CP Up and Down gain settings are set to the same value (Reg 09h[13:7] = Reg 09h[6:0]).

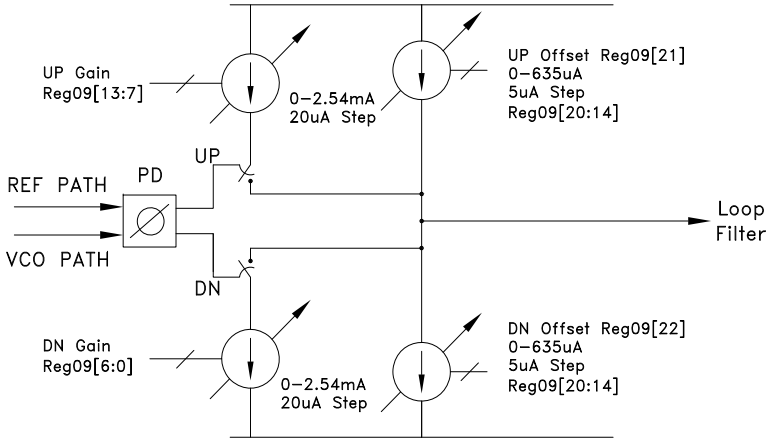

Figure 42. Charge Pump Gain & Offset Control

1.3.1.2.2 Charge Pump Switch

Charge pump Up and Down gains are set by Reg 09h[13:7] and Reg 09h[6:0] respectively. The current gain of the pump in Amps/radian is equal to the gain setting of this register divided by 2π.

Typical CP gain setting is set to 2 to 2.5 mA, however lower values can also be used. Values < 1 mA may result in degraded Phase Noise performance.

For example, if both Reg 09h[13:7] and Reg 09h[6:0] are set to '50d' the output current of each pump will be 1 mA and the phase frequency detector gain k_p = 1 mA/2π radians, or 159 µA/rad.

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1.3.1.3.3 Charge Pump Phase Offset

In Integer Mode, the phase detector operates with zero offset. The divided reference and the divided VCO arrive at the phase detector at the same time. Integer mode does not require any CP Offset current. When operating in Integer Mode simply disable CP offset in both directions (Up and down), by writing Reg 09h[22:21] = '00'b.

In Fractional Mode CP linearity is of paramount importance. Any non-linearity degrades phase noise and spurious performance. These non-linearities are eliminated by operating the PD with an average phase offset, either positive or negative (either the reference or the VCO edge always arrives first at the PD).

In non-inverting configurations, a programmable CP offset current source is used to add DC current to the loop filter and create the desired phase offset. Positive current causes the VCO to lead, negative current causes the reference to lead.

The CP offset is controlled via Reg 09h[20:14]. The phase offset is scaled from 0 degrees, that is the reference and the VCO path arrive in phase, to 360 degrees, where they arrive a full cycle late.

The recommended charge pump offset current a function of the PFD period and CP gain, and is provided in (EQ 9). It is also plotted in Fig 43 vs. PD frequency for typical CP Gain currents.

$$\text{Recommended CP Offset} = \min\left[\left(4.3\times10^{-9}\times F_{PD}\times I_{CP}\right), 0.25\times I_{CP}\right] \quad \text{(EQ 9)}$$

where:

F_{PD}*: Comparison frequency of the Phase Detector (Hz)*

I_{CP}*: is the full scale current setting (A) of the switching charge pump (set in Reg 09h[6:0], [13:7]*

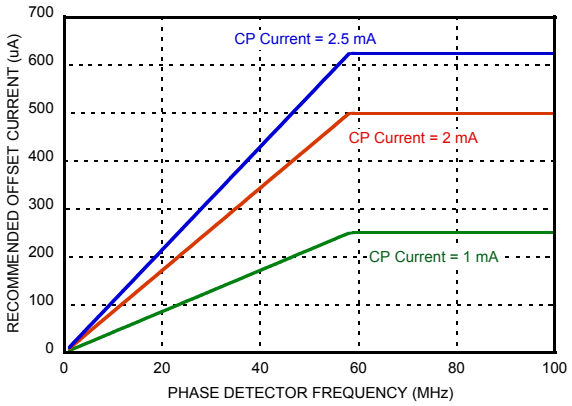

Figure 43.Recommended CP offset current vs PD frequency for typical CP gain currents. Calculated using (EQ 9)

The required CP offset current should never exceed 25 % of the programmed CP current. It is recommended to enable the Up Offset and disable the Down Offset by writing Reg 09h[22:21] = '10'b.

Operation with CP offset influences the configuration of the Lock Detect function. Refer to the description of Lock Detect function in section 1.3.5.

When operating with PD frequency >=80MHz, the CP Offset current should be disabled for the frequency change and then re-enabled after the PLL has settled. If the CP Offset current is enabled during a frequency change it may not lock.

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1.3.1.4 Phase Detector Functions

Phase detector register Reg 0Bh allows manual access to control special phase detector features.

Setting Reg 0Bh[5] = 0, masks the PD up output, which prevents the charge pump from pumping up.`

Setting (Reg 0Bh[6]) = 0, masks the PD down output, which prevents the charge pump from pumping down.

Clearing both Reg 0Bh[5] and Reg 0Bh[6] tri-states the charge pump while leaving all other functions operating internally.

PD Force UP Reg 0Bh[9] = 1 and PD Force DN Reg 0Bh[10] = 1 allows the charge pump to be forced up or down respectively. This will force the VCO to the ends of the tuning range which can be useful in VCO testing.

1.3.2 Reference Input Stage

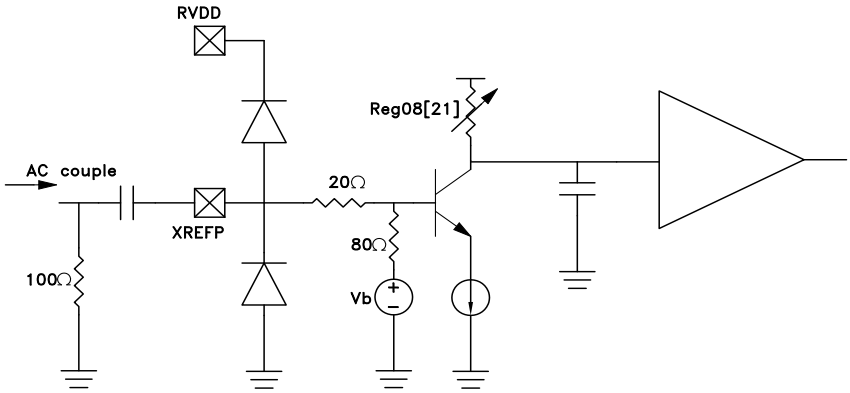

Figure 44. Reference Path Input Stage

The reference buffer provides the path from an external reference source (generally crystal based) to the R divider, and eventually to the phase detector. The buffer has two modes of operation controlled by Reg 08h[21]. High Gain (Reg 08h[21] = 0), recommended below 200 MHz, and High frequency (Reg 08h[21] = 1), for 200 to 350 MHz operation. The buffer is internally DC biased, with 100 Ω internal termination. For 50 Ω match, an external 100 Ω resistor to ground should be added, followed by an AC coupling capacitor (impedance < 1 Ω), then to the XREFP pin of the part.

At low frequencies, a relatively square reference is recommended to keep the input slew rate high. At higher frequencies, a square or sinusoid can be used. The following table shows the recommended operating regions for different reference frequencies. If operating outside these regions the part will normally still operate, but with degraded reference path phase noise performance.

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Table 4. Reference Sensitivity Table

	Square Input			Sinusoidal Input		
Reference Input Frequency (MHz)	Slew > 0.5V/ns	Recommended Swing (Vpp)			Recommended Power Range (dBm)	
	Recommended	Min	Max	Recommended	Min	Max
< 10	YES	0.6	2.5	x	x	x
10	YES	0.6	2.5	x	x	x
25	YES	0.6	2.5	ok	8	15
50	YES	0.6	2.5	YES	6	15
100	YES	0.6	2.5	YES	5	15
150	ok	0.9	2.5	YES	4	12
200	ok	1.2	2.5	YES	3	8

Input referred phase noise of the PLL when operating at 50 MHz is between -148 and -150 dBc/Hz at 10 kHz offset depending upon the mode of operation. The input reference signal should be 10 dB better than this floor to avoid degradation of the PLL noise contribution. It should be noted that such low levels are only necessary if the PLL is the dominant noise contributor and these levels are required for the system goals.

1.3.3 Reference Path 'R' Divider

The reference path "R" divider is based on a 14-bit counter and can divide input signals by values from 1 to 16,383 and is controlled via Reg 02h.

1.3.4 RF Path 'N' Divider

The main RF path divider is capable of average divide ratios between 2^{19}-5 (524,283) and 20 in fractional mode, and 2^{19}-1 (524,287) to 16 in integer mode.

1.3.5 Lock Detect

The Lock Detect (LD) function indicates that the HMC835LP6GE is indeed generating the desired frequency. It is enabled by writing Reg 07h[11]=1. The HMC835LP6GE provides LD indicator in one of two ways:

- As an output available on the LD_SDO pin of the HMC835LP6GE, (Configuration is required to use the LD_SDO pin for LD purpose, for more information please see "1.8 Serial Port Open Mode" and "1.3.5.3 Configuring LD_SDO Pin for LD Output" section).
- Or reading from Reg 12h[1], where Reg 12h[1] = 1 indicates locked and Reg 12h[1] = 0 indicates an unlocked condition.

The device incorporates a self-calibrating or automatic 'training' feature to manage the LD configuration. The simplest configuration is to use the training feature. If the training feature is not used, the user must calculate the required configuration for reliable LD indication. Described below are details for LD configuration with and without the training feature.

1.3.5.1 Lock Detect Configuration using Training

The HMC835LP6GE lock-detect functionality is self-calibrating. Typically the lock-detect training is only required once on power-up, or each time the reference frequency or the R divider value (Reg 02h) is changed.

To train the lock-detect circuitry of the HMC835LP6GE on power-up, set:

- set Reg 07h [11] = 1 to enable lock-detect counters
- set Reg 07h [14] = 1 to enable the lock-detect timer

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• set Reg 07h [20] = 1 to train the lock-detect timer

These bits can all be written simultaneously.

On any change of the PD frequency (via either the external reference frequency, or the R divider setting (Reg 02h)), the lock-detect circuit should be retrained by toggling Reg 07h [20] Off and then back On.

1.3.5.2 Lock Detect Configuration without Training (Manual)

The LD circuit expects the divided VCO edge and the divided reference edge to appear at the PD within a user specified time period (window), repeatedly. Either signal may arrive first, only the difference in arrival times is significant. The arrival of the two edges within the designated window increments an internal counter. Once the count reaches and exceeds a user specified value (Reg 07h[2:0]) the HMC835LP6GE declares lock.

Failure in registering the two edges in any one window resets the counter and immediately declares an un-locked condition. Lock is deemed to be reestablished once the counter reaches the user specified value (Reg 07h[2:0]) again.

Optimal spectral performance in fractional mode requires CP current and CP offset current configuration discussed in detail in section "1.3.1".

These settings in Reg 09h impact the required LD window size in fractional mode of operation. To function, the required lock detect window size is provided by (EQ 10).

$$\text{LD Window (seconds)} = \frac{\left(\frac{I_{CP\,Offset}(A)}{F_{PD}(Hz)\times I_{CP}(A)} + 2.66\times10^{-9}(\text{sec}) + \frac{1}{F_{PD}(Hz)}\right)}{2} \text{ in Fractional Mode} \quad \text{(EQ 10)}$$

$$\text{LD Window (seconds)} = \frac{1}{2\times F_{PD}} \text{ in Integer Mode}$$

where:

F_{PD}*: is the comparison frequency of the Phase Detector*

$I_{CP\ Offset}$*: is the Charge Pump Offset Current* Reg 09h*[20:14]*

I_{CP}*: is the full scale current setting of the switching charge pump* Reg 09h*[6:0], or* Reg 09h*[13:7]*

Table 5 provides the required Reg 07h settings to appropriately program the LD window size. From Table 5, simply select the closest value in the "LD Window Size" columns to the one calculated in (EQ 10) and program Reg 07h[9:8] and Reg 07h[7:5] accordingly.

Table 5. Typical Lock Detect Window

LD Timer Speed Reg07[9:8]	Lock Detect Window Size Nominal Value (ns)							
Fastest 00	6.5	8	11	17	29	53	100	195
01	7	8.9	12.8	21	36	68	130	255
10	7.1	9.2	13.3	22	38	72	138	272
Slowest 11	7.6	10.2	15.4	26	47	88	172	338
LD Timer Divide Setting Reg07[7:5]	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**

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1.3.5.3 LD Window Configuration Example

Assuming, fractional mode, with a 50 MHz PD and

- Charge Pump gain of 2 mA (Reg 09h[13:7] = 64h, Reg 09h[6:0] = 64h),
- Down Offset (Reg 09h[22:21] = '10'b)
- Offset current magnitude of +400 µA (Reg 09h[20:14] = 50h)

Applying (EQ 11), the required LD window size is:

$$\text{LD Window (seconds)} = \frac{\left(\frac{0.4x10^{-3}(A)}{50\times10^{6}(Hz)\times2x10^{-3}(A)} + 2.66\times10^{-9}(\text{sec}) + \frac{1}{50\times10^{6}(Hz)}\right)}{2} = 13.33 \text{ nsec} \quad \text{(EQ 11)}$$

Locating the Table 5 value that is closest to the (EQ 11) result, in this case 13.3 ≈ 13.33. To set the LD window size, simply program Reg 07h[9:8] = '10'b and Reg 07h[7:5] = '010'b according to Table 5.

There is always a good solution for the lock detect window for a given operating point. The user should understand however that one solution does not fit all operating points. As observed from (EQ 11), If charge pump offset or PD frequency are changed significantly then the lock detect window may need to be adjusted.

1.3.5.4 Configuring LD_SDO Pin for LD Output

Setting Reg 0Fh*[4:0]=1* will display the Lock Detect Flag on LD_SDO pin of the HMC835LP6GE. If locked, LD_SDO will be high. As the name suggests, LD_SDO pin is multiplexed between LD and SDO (Serial Data Out) signals. Hence LD is available on the LD_SDO pin at all times except when a serial port read is requested, in which case the pin reverts temporarily to the Serial Data Out pin, and returns to the Lock Detect Flag after the read is completed.

LD can be made available on LD_SDO pin at all times by writing Reg 0Fh*[6]* = 1. In that case the HMC835LP6GE will not provide any read-back functionality because the SDO signal is not available.

1.3.6 Cycle Slip Prevention (CSP)

When changing VCO frequency and the VCO is not yet locked to the reference, the instantaneous frequencies of the two PD inputs are different, and the phase difference of the two inputs at the PD varies rapidly over a range much greater than ±2π radians. Since the gain of the PD varies linearly with phase up to ±2π, the gain of a conventional PD will cycle from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than a multiple of 0 radians. The output current from the charge pump will cycle from maximum to minimum even though the VCO has not yet reached its final frequency.

The charge on the loop filter small cap may actually discharge slightly during the low gain portion of the cycle. This can make the VCO frequency actually reverse temporarily during locking. This phenomena is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically. Cycle Slipping increases the time to lock to a value greater than that predicted by normal small signal Laplace analysis.

The HMC835LP6GE PD features an ability to reduce cycle slipping during frequency tunning. The Cycle Slip Prevention (CSP) feature increases the PD gain during large phase errors.

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1.3.7 Frequency Tuning

HMC835LP6GE VCO subsystem always operates in fundamental frequency of operation (2050 MHz to 4100 MHz). The HMC835LP6GE generates frequencies below its fundamental frequency (33 MHz to 2050 MHz) by tuning to the appropriate fundamental frequency and selecting the appropriate Output Divider setting (divide by 2/4/6.../60/62) in Reg 16h[5:0].

The HMC835LP6GE automatically controls frequency tuning in the fundamental band of operation, for more information see "1.2.1 VCO Calibration".

To tune to frequencies below the fundamental frequency range (<2050 MHz) it is required to tune the HMC835LP6GE to the appropriate fundamental frequency, then select the appropriate output divider setting (divide by 2/4/6.../60/62) in Reg 16h[5:0].

1.3.7.1 Integer Mode

The HMC835LP6GE is capable of operating in integer mode. For Integer mode set the following registers

a. Disable the Fractional Modulator, Reg 06h*[11]=0*

b. Bypass the Modulator circuit, Reg 06h*[7]=1*

In integer mode the VCO step size is fixed to that of the PD frequency. Integer mode typically has 3 dB lower phase noise than fractional mode for a given PD operating frequency. Integer mode, however, often requires a lower PD frequency to meet step size requirements. The fractional mode advantage is that higher PD frequencies can be used, hence lower phase noise can often be realized in fractional mode. Charge Pump offset should be disabled in integer mode Reg 09h[22:14] = 0h.

1.3.7.2.2 Integer Frequency Tuning

In integer mode the digital ΔΣ modulator is shut off and the N divider (Reg 03h) may be programmed to any integer value in the range 16 to 2^{19}-1. To run in integer mode configure Reg 06h as described, then program the integer portion of the frequency as explained by (EQ 12), ignoring the fractional part.

a. Disable the Fractional Modulator, Reg 06h[11] = 0
b. Bypass the delta-sigma modulator Reg 06h[7] = 1
c. To tune to frequencies (<2050 MHz), select the appropriate output divider valueReg 16h[5:0].

1.3.7.3 Fractional Mode

The HMC835LP6GE is placed in fractional mode by setting the following registers:

a. Enable the Fractional Modulator, Reg 06h*[11]=1*

b. Connect the delta sigma modulator in circuit, Reg 06h*[7]=0*

1.3.7.4.4 Fractional Frequency Tuning

This is a generic example, with the goal of explaining how to program the output frequency. Actual variables are dependant upon the reference in use.

The HMC835LP6GE in fractional mode can achieve frequencies at fractional multiples of the reference. The frequency of the HMC835LP6GE, f_{vco}, is given by

$$f_{vco} = \frac{f_{xtal}}{R} (N_{int} + N_{frac}) = f_{int} + f_{frac} \quad \text{(EQ 12)}$$

$$f_{out} = f_{vco} / k \quad \text{(EQ 13)}$$

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Where:

f_{out}	is the output frequency after any potential dividers.
k	is 1 for fundamental, or k = 2,4,6,…58,60,62 depending on the selected output divider value (Reg 16h[5:0])
N_{int}	is the integer division ratio, Reg 03h, an integer number between 20 and 524,284
N_{frac}	is the fractional part, from 0.0 to 0.99999...,N_{frac}=Reg 04h/2^{24}
R	is the reference path division ratio, Reg 02h
f_{xtal}	is the frequency of the reference oscillator input
f_{pd}	is the PD operating frequency, f_{xtal}/R

As an example:

f_{out}	1402.5 MHz
k	2
f_{vco}	2,805 MHz
f_{xtal}	= 50 MHz
R	= 1
f_{pd}	= 50 MHz
N_{int}	= 56
N_{frac}	= 0.1
Reg 04h	= round(0.1 x 2^{24}) = round(1677721.6) = 1677722

$$f_{VCO} = \frac{50e6}{1} \left(56 + \frac{1677722}{2^{24}}\right) = 2805\ MHz + 1.192\ Hz\ error \qquad \text{(EQ 14)}$$

$$f_{out} = \frac{f_{VCO}}{2} = 1402.5\ MHz + 0.596\ Hz\ error \qquad \text{(EQ 15)}$$

In this example the output frequency of 1402.5 MHz is achieved by programming the 19-bit binary value of 56d = 38h into *intg_reg* in Reg 03h, and the 24-bit binary value of 1677722d = 19999Ah into *frac_reg* in Reg 04h. The 0.596 Hz quantization error can be eliminated using the exact frequency mode if required. In this example the VCO output fundamental 2805 MHz is divided by 2 (Reg 16h[5:0] = 2h) = 1402.5 MHz.

1.3.7.5.5 Exact Frequency Tuning

Due to quantization effects, the absolute frequency precision of a fractional PLL is normally limited by the number of bits in the fractional modulator. For example, a 24 bit fractional modulator has frequency resolution set by the phase detector (PD) comparison rate divided by 2^{24}. The value 2^{24} in the denominator is sometimes referred to as the modulus. Hittite PLLs use a fixed modulus which is a binary number. In some types of fractional PLLs the modulus is variable, which allows exact frequency steps to be achieved with decimal step sizes. Unfortunately small steps using small modulus values results in large spurious outputs at multiples of the modulus period (channel step size). For this reason Hittite PLLs use a large fixed modulus. Normally, the step size is set by the size of the fixed modulus. In the case of a 50 MHz PD rate, a modulus of 2^{24} would result in a 2.98 Hz step resolution, or 0.0596 ppm. In some applications it is necessary to have exact frequency steps, and even an error of 3 Hz cannot be tolerated.

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Fractional PLLs are able to generate exact frequencies (with zero frequency error) if N can be exactly represented in binary (eg. N = 50.0,50.5,50.25,50.75 etc.). Unfortunately, some common frequencies cannot be exactly represented. For example, N_{frac} = 0.1 = 1/10 must be approximated as round((0.1 x 2^{24})/ 2^{24}) ≈ 0.100000024. At f_{PD} = 50 MHz this translates to 1.2 Hz error. Hittite's exact frequency mode addresses this issue, and can eliminate quantization error by programming the channel step size to F_{PD}/10 in Reg 0Ch to 10 (in this example). More generally, this feature can be used whenever the desired frequency, f_{VCO}, can be exactly represented on a step plan where there are an integer number of steps (<2^{24}) across integer-N boundaries. Mathematically, this situation is satisfied if:

$$f_{VCOk} \bmod\left(f_{gcd}\right) = 0 \quad \text{where} f_{gcd} = \gcd(f_{VCO1}, f_{PD}) \text{and} f_{gcd} \geq \left(\frac{f_{PD}}{2^{24}}\right) \qquad \text{(EQ 16)}$$

Where:

gcd stands for Greatest Common Divisor

f_N = maximum integer boundary frequency < f_{VCO1}

f_{PD} = frequency of the Phase Detector

and f_{VCOk} are the channel step frequencies where 0 < k < 2^{24}-1, As shown in Fig 44.

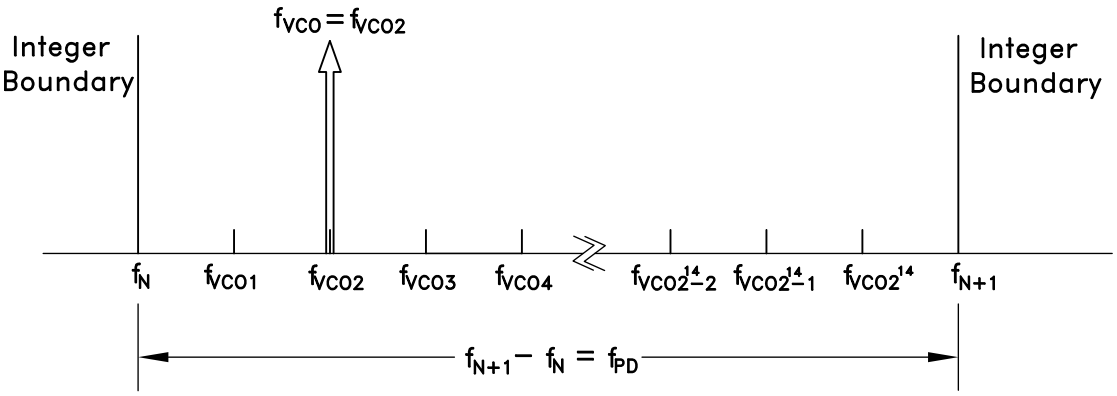

Figure 45. Exact Frequency Tuning

Some fractional PLLs are able to achieve this by adjusting (shortening) the length of the Phase Accumulator (the denominator or the modulus of the Delta-Sigma modulator) so that the Delta-Sigma modulator phase accumulator repeats at an exact period related to the interval frequency (f_{VCOk} - $f_{VCO(k-1)}$) in Fig 44. Consequently, the shortened accumulator results in more frequent repeating patterns and as a result often leads to spurious emissions at multiples of the repeating pattern period, or at harmonic frequencies of f_{VCOk} - $f_{VCO(k-1)}$. For example, in some applications, these intervals might represent the spacing between radio channels, and the spurious would occur at multiples of the channel spacing.

The Hittite method on the other hand is able to generate exact frequencies between adjacent integer-N boundaries while still using the full 24 bit phase accumulator modulus, thus achieving exact frequency steps with a high phase detector comparison rate, which allows Hittite PLLs to maintain excellent phase noise and spurious performance in the Exact Frequency Mode.

1.3.7.6.6 Using Hittite Exact Frequency Mode

If the constraint in (EQ 16) is satisfied, HMC835LP6GE is able to generate signals with zero frequency error at the desired VCO frequency. Exact Frequency Mode may be re-configured for each target frequency, or be set-up for a fixed f_{gcd} which applies to all channels.

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1.3.7.6.1.1 Configuring Exact Frequency Mode For a Particular Frequency

1. Calculate and program the integer register setting Reg 03h = N_{INT} = floor(f_{VCO}/f_{PD}), where the floor function is the rounding down to the nearest integer. Then the integer boundary frequency $f_N = N_{INT} \cdot f_{PD}$
2. Calculate and program the exact frequency register value Reg 0Ch = f_{PD}/f_{gcd}, where f_{gcd} = gcd(f_{VCO},f_{PD})
3. Calculate and program the fractional register setting Reg 04h $N_{FRAC} = \text{ceil}\left(\frac{2^{24}\left(f_{VCOk} - f_N\right)}{f_{PD}}\right)$, where ceil is the ceiling function meaning "round up to the nearest integer."

Example: To configure the HMC835LP6GE for exact frequency mode at f_{VCO} = 2800.2 MHz where Phase Detector (PD) rate f_{PD} = 61.44 MHz Proceed as follows:

Check (EQ 16) to confirm that the exact frequency mode for this f_{VCO} is possible.

$$f_{gcd} = \text{gcd}(f_{VCO}, f_{PD}) \; and \; f_{gcd} \geq \left(\frac{f_{PD}}{2^{24}}\right)$$

$$f_{gcd} = \text{gcd}\left(2800.2\times10^6, 61.44\times10^6\right) = 120\times10^3 > \frac{61.44\times10^6}{2^{24}} = 3.662$$

Since (EQ 16) is satisfied, the HMC835LP6GE can be configured for exact frequency mode at f_{VCO} = 2800.2 MHz as follows:

1. N_{INT} = Reg 03h = $floor\left(\frac{f_{VCO1}}{f_{PD}}\right) = floor\left(\frac{2800.2\times10^6}{61.44\times10^6}\right) = 45d = 2Dh$

2. Reg 0Ch = $\frac{f_{PD}}{\text{gcd}\left(\left(f_{VCOk+1} - f_{VCOk}\right), f_{PD}\right)} = \frac{61.44\times10^6}{\text{gcd}\left(100\times10^3, 61.44\times10^6\right)} = \frac{61.44\times10^6}{20000} = 3072d = C00h$

3. To program Reg 04h, the closest integer-N boundary frequency f_N that is less than the desired VCO frequency f_{VCO} must be calculated. $f_N = f_{PD} \cdot N_{INT}$. Using the current example:

$$f_N = f_{PD} \times N_{INT} = 45\times61.44\times10^6 = 2764.8\,MHz.$$

$$\text{Then Reg04h} = ceil\left(\frac{2^{24}\left(f_{VCO} - f_N\right)}{f_{PD}}\right) = ceil\left(\frac{2^{24}\left(2800.2\times10^6 - 2764.8\times10^6\right)}{61.44\times10^6}\right) = 9666560d = 938000h$$

1.3.7.7.7 Hittite Exact Frequency Channel Mode

If it is desirable to have multiple, equally spaced, exact frequency channels that fall within the same interval (ie. $f_N \leq f_{VCOk} < f_{N+1}$) where f_{VCOk} is shown in Fig 44 and $1 \leq k \leq 2^{24}$, it is possible to maintain the same integer-N (Reg 03h) and exact frequency register (Reg 0Ch) settings and only update the fractional register (Reg 04h) setting. The Exact Frequency Channel Mode is possible if (EQ 16) is satisfied for at least two equally spaced adjacent frequency channels, i.e. the channel step size.

To configure the HMC835LP6GE for Exact Frequency Channel Mode, initially and only at the beginning, integer (Reg 03h) and exact frequency (Reg 0Ch) registers need to be programmed for the smallest f_{VCO} frequency (f_{VCO1} in Fig 44), as follows:

1. Calculate and program the integer register setting Reg 03h = N_{INT} = floor(f_{VCO1}/f_{PD}), where f_{VCO1} is shown in Fig 44 and corresponds to minimum channel VCO frequency. Then the lower integer boundary frequency is given by $f_N = N_{INT} \cdot f_{PD}$.
2. Calculate and program the exact frequency register value Reg 0Ch = f_{PD}/f_{gcd}, where f_{gcd} = gcd((f_{VCOk+1} - f_{VCOk}),f_{PD}) = greatest common divisor of the desired equidistant channel spacing and the PD frequency ((f_{VCOk+1} - f_{VCOk}) and f_{PD}).

Then, to switch between various equally spaced intervals (channels) only the fractional register (Reg 04h) needs to be programmed to the desired VCO channel frequency f_{VCOk} in the following manner:

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Reg 04h = $N_{FRAC} = \text{ceil}\left(\frac{2^{24}\left(f_{VCOk} - f_N\right)}{f_{PD}}\right)$ where $f_N = \text{floor}(f_{VCO1}/f_{PD})$, and f_{VCO1}, as shown in Fig 44, represents the smallest channel VCO frequency that is greater than f_N.

Example: To configure the HMC835LP6GE for Exact Frequency Mode for equally spaced intervals of 100 kHz where first channel (Channel 1) = f_{VCO1} = 2800.200 MHz and Phase Detector (PD) rate f_{PD} = 61.44 MHz proceed as follows:

First check that the exact frequency mode for this f_{VCO1} = 2800.2 MHz (Channel 1) and f_{VCO2} = 2800.2 MHz + 100 kHz = 2800.3 MHz (Channel 2) is possible.

$$f_{gcd1} = \gcd(f_{VCO1}, f_{PD}) \; and \; f_{gcd1} \geq \left(\frac{f_{PD}}{2^{24}}\right) \; and \; f_{gcd2} = \gcd(f_{VCO2}, f_{PD}) \; and \; f_{gcd2} \geq \left(\frac{f_{PD}}{2^{24}}\right)$$

$$f_{gcd1} = \gcd\left(2800.2\times10^6, 61.44\times10^6\right) = 120\times10^3 > \frac{61.44\times10^6}{2^{24}} = 3.662$$

$$f_{gcd2} = \gcd\left(2800.3\times10^6, 61.44\times10^6\right) = 20\times10^3 > \frac{61.44\times10^6}{2^{24}} = 3.662$$

If (EQ 16) is satisfied for at least two of the equally spaced interval (channel) frequencies $f_{VCO1}, f_{VCO2}, f_{VCO3}, \ldots f_{VCON}$, as it is above, Hittite Exact Frequency Channel Mode is possible for all desired channel frequencies, and can be configured as follows:

1. Reg 03h = $floor\left(\frac{f_{VCO1}}{f_{PD}}\right) = floor\left(\frac{2800.2\times10^6}{61.44\times10^6}\right) = 45d = 2Dh$
2. Reg 0Ch = $\frac{f_{PD}}{\gcd\left(\left(f_{VCOk+1} - f_{VCOk}\right), f_{PD}\right)} = \frac{61.44\times10^6}{\gcd\left(100\times10^3, 61.44\times10^6\right)} = \frac{61.44\times10^6}{20000} = 3072d = C00h$

   where (f_{VCOk+1} - f_{VCOk}) is the desired channel spacing (100 kHz in this example).
3. To program Reg 04h the closest integer-N boundary frequency f_N that is less than the smallest channel VCO frequency f_{VCO1} must be calculated. $f_N = \text{floor}(f_{VCO1}/f_{PD})$. Using the current example:

   $$f_N = f_{PD} \times floor\left(\frac{2800.2\times10^6}{61.44\times10^6}\right) = 45\times61.44\times10^6 = 2764.8\,MHz$$ Then

   Reg 04h $= ceil\left(\frac{2^{24}\left(f_{VCO1} - f_N\right)}{f_{PD}}\right)$ for channel 1 where $f_{VCO1} = 2800.2\,MHz$

   $$= ceil\left(\frac{2^{24}\left(2800.2\times10^6 - 2764.8\times10^6\right)}{61.44\times10^6}\right) = 9666560d = 938000h$$
4. To change from channel 1 (f_{VCO1} = 2800.2 MHz) to channel 2 (f_{VCO2} = 2800.3 MHz), only Reg 04h needs to be programmed, as long as all of the desired exact frequencies f_{VCOk} (Fig 44) fall between the same integer-N boundaries ($f_N < f_{VCOk} < f_{N+1}$). In that case

   Reg 04h = $ceil\left(\frac{2^{24}\left(2800.3\times10^6 - 2764.8\times10^6\right)}{61.44\times10^6}\right) = 9693867d = 93EAABh$, and so on.

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1.3.8 Seed Register

The start phase of the fractional modulator digital phase accumulator (DPA) may be set to any desired phase relative to the reference frequency, The phase is programmed in Reg 1Ah, and Exact Frequency Mode is required. Phase = 2π x Reg1Ah/(2^{24}) via the seed register Reg 1Ah[23:0]. The HMC835LP6GE will automatically reload the start phase (seed value) into the DPA every time a new fractional frequency is selected. Certain zero or binary seed values may cause spurious energy correlation at specific frequencies. For most cases a random, or non zero, non-binary start seed is recommended.

1.4 Soft Reset & Power-On Reset

The HMC835LP6GE features a hardware Power on Reset (POR). All chip registers will be reset to default states approximately 250 µs after power up.

The PLL subsystem SPI registers may also be soft reset by an SPI write to register Reg 00h.

1.5 Power Down Mode

Power down the HMC835LP6GE by pulling CEN pin (pin 17) low (assuming no SPI overrides(Reg 01h[0]=1)). This will result in all analog functions and internal clocks disabled. Current consumption will typically drop below 10 µA in Power Down state. The serial port will still respond to normal communication in Power Down mode.

It is possible to ignore the CEN pin, by setting Reg 01h[0]=0. Control of Power Down Mode then comes from the serial port register Reg 01h[1].

It is also possible to leave various blocks on when in Power Down *(see* Reg 01h*)*, including:

a. Internal Bias Reference Sources	Reg 01h*[2]*
b. PD Block	Reg 01h*[3]*
c. CP Block	Reg 01h*[4]*
d. Reference Path Buffer	Reg 01h*[5]*
e. VCO Path buffer	Reg 01h*[6]*
f. Digital I/O Test pads	Reg 01h*[7]*

To mute the output but leave the PLL and VCO locked please refer to 1.2.4 section.

1.6 General Purpose Output (GPO) Pin

The PLL shares the LD_SDO (Lock-Detect/Serial Data Out) pin to perform various functions. While the pin is most commonly used to read back registers from chip via the SPI, it is also capable of exporting a variety of signals and real time test waveforms (including Lock Detect). It is driven by a tri-state CMOS driver with ~200 Ω Rout. It has logic associated with it to dynamically select whether the driver is enabled, and to decide which data to export from the chip.

In its default configuration, after power-on-reset, the output driver is disabled, and only drives during appropriately addressed SPI reads. This allows it to share the output with other devices on the same bus.

The pin driver is enabled if the chip is addressed - ie. The last 3 bits of SPI cycle = '000'b before the rising edge of SEN. If SEN rises before SCK has clocked in an 'invalid' (non-zero) chip -address, the HMC835LP6GE will start to drive the bus.

The FRACTIONAL-N PLL WITH INTEGRATED VCO will naturally switch away from the GPO data and export the SDO during an SPI read. To prevent this automatic data selection, and always select the GPO signal, set "Prevent AutoMux of SDO" (Reg 0Fh[6] = 1). The phase noise performance at this output is poor and uncharacterized. The GPO output should not be toggling during normal operation because it may degrade the spectral performance.

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Note that there are additional controls available, which may be helpful if sharing the bus with other devices:

- To disable the driver completely, set Reg 08h[5] = 0 (it takes precedence over all else).
- To disable either the pull-up or pull-down sections of the driver, Reg 0Fh[8] = 1 or Reg 0Fh[9] = 1 respectively.

Example Scenarios:

- Drive SDO during reads, tri-state otherwise (to allow bus-sharing)
  - No action required.
- Drive SDO during reads, Lock Detect otherwise
  - Set GPO Select Reg 0Fh [4:0] = '00001'b (which is default)
  - Set "Prevent GPO driver disable" (Reg 0Fh[7] = 1)
- Always drive Lock Detect
  - Set " Prevent AutoMux of SDO" Reg 0Fh[6] = 1
  - Set GPO Select Reg 0Fh[4:0]= 00001 (which is default)
  - Set "Prevent GPO driver disable" (Reg 0Fh[7] = 1))

The signals available on the GPO are selected in Reg 0Fh[4:0].

1.7 Chip Identification

The chip id information may be read by reading the content of read only register, chip_ID in Reg 00h. For HMC835LP6GE, chip id is C7701Ah.

1.8 SERIAL PORT Overview

The SPI protocol has the following general features:

a. 3-bit chip address , enable the use of up to 8 devices connected to the serial bus

b. Simultaneous Write/Read during the SPI cycle

c. 5-bit address space

d. 3 wire for Write Only capability, 4 wire for Read/Write capability

Typical serial port operation can be run with SCLK at speeds up to 50 MHz.

1.8.1 Serial Port WRITE Operation

AVDD = DVDD = 3V, AGND = DGND = 0V

Table 6. SPI WRITE Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SDI setup time to SCLK Rising Edge	3			ns
t_2	SCLK Rising Edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCLK 32 Rising Edge to SEN Rising Edge	10			ns
t_6	Recovery Time	10			ns
	Max Serial port Clock Speed		50		MHz

A typical WRITE cycle is shown in Fig 45.

a. The Master (host) places 24-bit data, d23:d0, MSB first, on SDI on the first 24 falling edges of SCLK.

b. the slave (HMC835LP6GE) shifts in data on SDI on the first 24 rising edges of SCLK

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c. Master places 5-bit register address to be written to, r4:r0, MSB first, on the next 5 falling edges of SCLK (25-29)

d. Slave shifts the register bits on the next 5 rising edges of SCLK (25-29).

e. Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (30-32). Hittite reserves chip address a2:a0 = 000 for HMC835LP6GE.

f. Slave shifts the chip address bits on the next 3 rising edges of SCLK (30-32).

g. Master asserts SEN after the 32nd rising edge of SCLK.

h. Slave registers the SDI data on the rising edge of SEN.

i. Master clears SEN to complete the WRITE cycle.

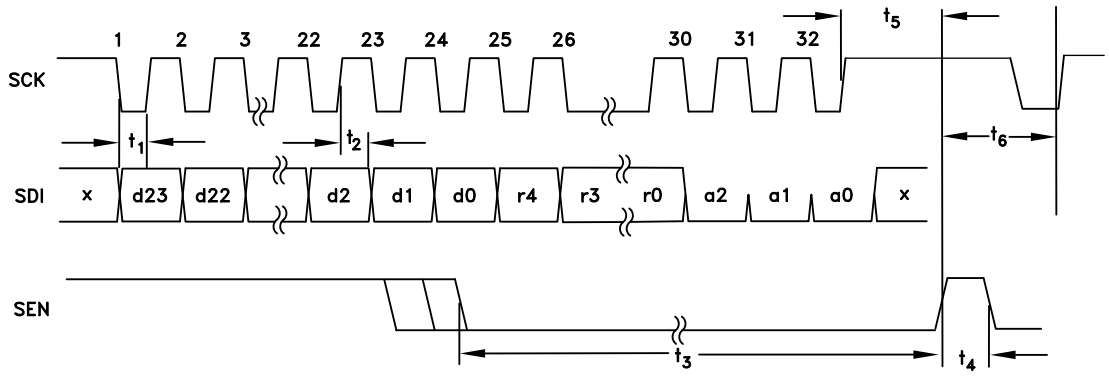

Figure 46. Serial Port Timing Diagram - WRITE

1.8.2 Serial Port READ Operation

A typical READ cycle is shown in Fig 46.

In general, the LD_SDO line is always active during the WRITE cycle. During any SPI cycle LD_SDO will contain the data from the current address written in Reg 00h[4:0]. If Reg 00h[4:0] is not changed then the same data will always be present on LD_SDO when an Open Mode cycle is in progress. If it is desired to READ from a specific address, it is necessary in the first SPI cycle to write the desired address to Reg 00h[4:0], then in the next SPI cycle the desired data will be available on LD_SDO.

An example of the two cycle procedure to read from any address follows:

a. The Master (host), on the first 24 falling edges of SCLK places 24-bit data, d23:d0, MSB first, on SDI as shown in Fig 46. d23:d5 should be set to zero. d4:d0 = address of the register to be READ on the next cycle.

b. the slave (HMC835LP6GE) shifts in data on SDI on the first 24 rising edges of SCK

c. Master places 5-bit register address , r4:r0, (the READ ADDRESS register), MSB first, on the next 5 falling edges of SCK (25-29). r4:r0=00000.

d. Slave shifts the register bits on the next 5 rising edges of SCK (25-29).

e. Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCK (30-32). Chip address is always '000'b.

f. Slave shifts the chip address bits on the next 3 rising edges of SCK (30-32).

g. Master asserts SEN after the 32nd rising edge of SCK.

h. Slave registers the SDI data on the rising edge of SEN.

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i. Master clears SEN to complete the the address transfer of the two part READ cycle.

j. If one does not wish to write data to the chip during the second cycle , then it is recommended to simply rewrite the same contents on SDI to Register zero on the READ back part of the cycle.

k. Master places the same SDI data as the previous cycle on the next 32 falling edges of SCK.

l. Slave (HMC835LP6GE) shifts the SDI data on the next 32 rising edges of SCK. On these same edges, the slave places the desired read data (ie. data from the address specified in Reg 00h[4:0] of the first cycle) on LD_SDO which automatically switches to SDO mode from LD mode, disabling the LD output.

m. Master asserts SEN after the 32nd rising edge of SCK to complete the cycle and revert back to Lock Detect on LD_SDO.

Table 7. SPI Read Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SDI setup time to SCK Rising Edge	3			ns
t_2	SCK Rising Edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCK Rising Edge to SDO time		8.2ns+0.2ns/pF		ns
t_6	Recovery TIme	10			ns
t_7	SCK 32 Rising Edge to SEN Rising Edge	10			ns

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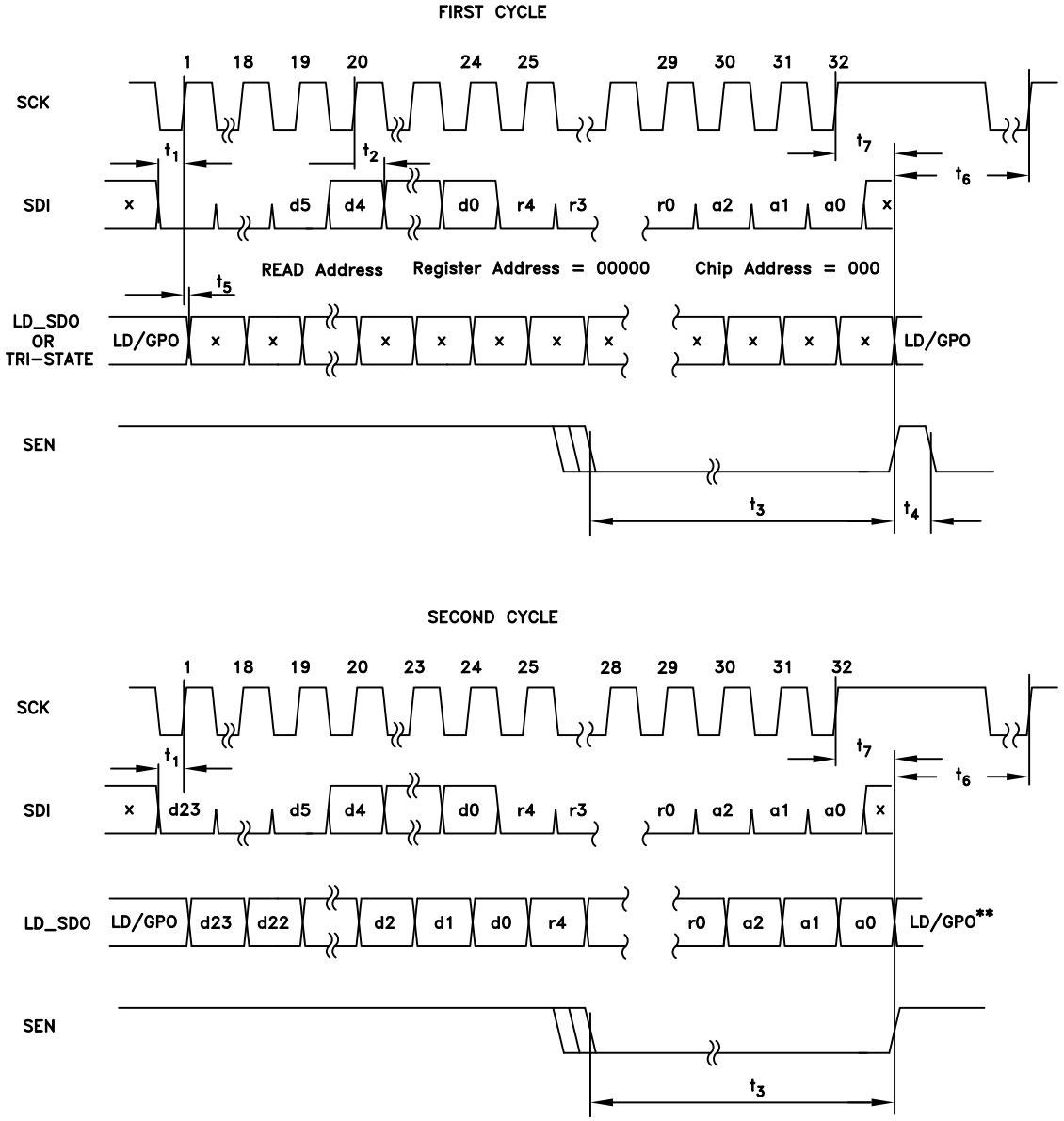

Figure 47. Serial Port Timing Diagram - READ

For more information on using the GPO pin while in SPI Mode please see section 1.8 Serial Port Overview

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2.0 PLL Register Map

2.1 Reg 00h ID Register (Read Only) DEFAULT C7701A h

Bit	Type	Name	Width	Default	Description
[23:0]	RO	chip_ID	24	C7701A	Chip ID Number

2.2 Reg 00h Open Mode Read Address/RST Strobe Register (Write Only)

Bit	Type	Name	Width	Default	Description
[4:0]	WO	Read Address	5	-	(WRITE ONLY) Read Address for next cycle
[5]	WO	Soft Reset	1	-	(WRITE ONLY) Soft Reset - (set to 0 during operation)
[23:6]	WO	Not Defined	18	-	Not Defined (set to write 0h)

2.3 Reg 01h Chip Enable Register DEFAULT 3h

Bit	Type	Name	Width	Default	Description
[0]	R/W	Chip Enable Pin Select	1	1	1 = Chip enable via CHIP_EN pin, Reg 01h[0]=1 and CHIP_EN pin low places the HMC835LP6GE in Power Down Mode 0 = Chip enable via SPI - Reg 01h[0] = 0, CHIP_EN pin ignored (see Power Down Mode description for more details)
[1]	R/W	SPI Chip Enable	1	1	Controls Chip Enable (Power Down) if Reg 01h[0] =0 Reg 01h[0]=0 and Reg 01h[1]=1 - chip is enabled, CHIP_EN pin don't care Reg 01h[0]=0 and Reg 01h[1]=0 - chip disabled, CHIP_EN pin don't care (see Power Down Mode description for more information)
[2]	R/W	Keep Bias On	1	0	keeps internal bias generators on, ignores Chip enable control
[3]	R/W	Keep PFD Pn	1	0	keeps PFD circuit on, ignores Chip enable control
[4]	R/W	Keep CP On	1	0	keeps Charge Pump on, ignores Chip enable control
[5]	R/W	Keep Reference Buffer ON	1	0	keeps Reference buffer block on, ignores Chip enable control
[6]	R/W	Keep VCO Buffer ON	1	0	keeps VCO divider buffer on, ignores Chip enable control
[7]	R/W	Keep GPO Driver ON	1	0	keeps GPO output Driver ON, ignores Chip enable control
[9:8]	R/W	Reserved	2	0	Reserved
[23:10]	R/W	Spare	14	0	Don't Care

2.4 Reg 02h REFDIV Register DEFAULT 1h

Bit	Type	Name	Width	Default	Description
[13:0]	R/W	rdiv	14	1	Reference Divider 'R' Value (EQ 8) min 1 max max 2^{14}-1 = 3FFFh = 16383d
[23:14]	R/W	Spare	10	0	Don't Care

2.5 Reg 03h Frequency Register - Integer Part DEFAULT 19h

Bit	Type	Name	Width	Default	Description
[18:0]	R/W	Integer Setting	19	25d 19h	Divider Integer part, used in all modes, see (EQ 10) Fractional Mode min 20d max 2^{19} - 4 = 7FFFCh = 524,284d Integer Mode min 16d max 2^{19}-1 = 7FFFFh = 524,287d
[23:19]	R/W	Spare	5	0	Don't Care

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2.6 Reg 04h Frequency Register - Fractional Part DEFAULT 0h

Bit	Type	Name	Width	Default	Description
[23:0]	R/W	Fractional Setting	24	0	Divider Fractional part (24 bit unsigned) see Fractional Frequency Tuning Fractional Division Value = Reg4[23:0]/2^24 Used in Fractional Mode only min 0 max 2^{24}-1 = FFFFFFh = 16,777,215d

2.7 Reg 05h Reserved DEFAULT 0h

Bit	Type	Name	Width	Default	Description
[23:0]	RO	Reserved	24	0	Reserved

2.8 Reg 06h Delta Sigma Modulator Register DEFAULT 30F0Ah

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[1:0]	R/W	Reserved	2	2	Reserved, don't care
[3:2]	R/W	DSM Order	2	2	Select the Delta Sigma Modulator Type 0: 1st order 1: 2nd Order 2: 3rd Order - Recommended 3: Reserved
[4]	R/W	Synchronous SPI Mode	1	0	0: Normal SPI Load - all register load on rising edge of SEN 1: Synchronous SPI - registers Reg 03h, Reg 04h , Reg 1Ah, Reg 0Ch wait to load synchronously on the next internal clock cycle. Normally (When this bit is 0) SPI writes into the internal state machines/counters happen asynchronously relative to the internal clocks. This can create freq/phase disturbances if writing register 3, 4, 1A or 0C. When this bit is enabled, the internal SPI registers are loaded synchronously with the internal clock. This means that the data in the SPI shifter should be held constant for at least 2 PFD clock periods after SEN is asserted to allow this retiming to happen cleanly.
[5]	R/W	Exact Frequency Mode Enable	1	0	1: Exact Frequency Mode Enabled 0: Exact Frequency Mode Disabled
[6]	R/W	Reserved	1	0	Reserved
[7]	R/W	Fractional Bypass	1	0	0: Use Modulator, Required for Fractional Mode, 1: Bypass Modulator, Required for Integer Mode Note: When enabled fractional modulator output is ignored, but fractional modulator continues to be clocked if Reg 06h[11] =1. This feature can be used to test the isolation of the digital fractional modulator from the VCO output in integer mode.
[8]	R/W	Autoseed EN	1	1	1: loads the modulator seed (start phase) whenever the fractional register (Reg 04h) is written 0: when fractional register (Reg 04h) write changes frequency, modulator starts at previous value (phase)
[10:9]	R/W	Reserved	2	3	Reserved
[11]	R/W	Delta Sigma Modulator Enable	1	1	0: Disable DSM, used for Integer Mode 1: Enable DSM Core, required for Fractional Mode
[22:12]	R/W	Reserved	11	48d 30h	Reserved
[23]	R/W	Spare	1	0	Don't Care

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2.9 Reg 07h Lock Detect Register Check DEFAULT 200844h

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	lkd_wincnt_max	3	4	lock detect window sets the number of consecutive counts of divided VCO that must land inside the Lock Detect Window to declare LOCK 0: 5 1: 32 2: 96 3: 256 4: 512 5: 2048 6: 8192 7: 65535
[4:3]	R/W	Reserved	2	00	Program 00
[7:5]	R/W	LD Timer Divide Setting	3	100	Only used with Manual LD Mode. See Table 5
[9:8]	R/W	LD Timer Speed	2	00	Only used with Manual LD Mode. See Table 5
[10]	R/W	Reserved	1	0	Program 0
[11]	R/W	LD Enable	1	1	0: LD disable 1: LD enable
[13:12]	R/W	Reserved	2	00	Program 00
[14]	R/W	LD Mode	1	0	0: Manual LD Mode 1: Automatic Training Mode
[15]	R/W	CSP Enable	1	0	0: Disabled 1: Enabled
[18:16]	R/W	Reserved	3	000	Program 000
[19]	R/W	Reserved	1	0	Program 0
[20]	R/W	Lock Detect Training	9	0	0 to 1 transition triggers the training. Lock Detect Training is only required after changing Phase Detector frequency. After changing PD frequency a toggle Reg 07h[20] from 0 to 1 retrains the Lock Detect.
[21]	R/W	Reserved	1	1	Program 1
[23:22]	R/W	Spare	2	0	Don't Care

2.10 Reg 08h Analog EN Register Check DEFAULT 1BFFFh

Bit	Type	Name	Width	Default	Description
[4:0]	R/W	Reserved	5	1Fh	Reserved
[5]	R/W	LD_SDO Driver Enable	1	1d	0 - Pin LD_SDO disabled (Hi Z) 1 - and RegFh[7]=1 , Pin LD_SDO is always driven. This is required for use as a GPO port 1 - and RegFh[7]=0 LD_SPI is off if the last Rx chip address is not equal to '000'b, allowing a shared SPI with other compatible parts
[9:6]	R/W	Reserved	4	Fh	Reserved
[10]	R/W	VCO Buffer and Prescaler Bias Enable	1	1d	0: VCO Prescaler Bias Disable 1: VCO Prescaler Bias Enable Only applies to External VCO
[20:11]	R/W	Reserved	10	37h	Reserved
[21]	R/W	High Frequency Reference	1	0	Program to 1 for XTAL > 200 MHz, 0 otherwise
[22]	R/W	SDO Output Level	1	0	Output Logic Level on LD/SDO pin 0: 1.8 V Logic Levels 1: DVDD3V Logic Level
[23]	R/W	Reserved	1	0	Reserved

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2.11 Reg 09h Charge Pump Register 547264h

Bit	Type	Name	Width	Default	Description
[6:0]	R/W	CP DN Gain	7	100d 64h	Charge Pump DN Gain Control 20 µA/step Affects fractional phase noise and lock detect settings 0d = 0 µA 1d = 20 µA 2d = 40 µA ... 127d = 2.54mA Default 2mA
[13:7]	R/W	CP UP Gain	7	100d 64h	Charge Pump UP Gain Control 20 µA per step Affects fractional phase noise and lock detect settings 0d = 0 µA 1d = 20 µA 2d = 40 µA ... 127d = 2.54mA Default 2mA
[20:14]	R/W	Offset Magnitude	7	81d	Charge Pump Offset Control 5 µA/step Affects fractional phase noise and lock detect settings 0d = 0 µA 1d = 5 µA 2d = 10 µA ... 127d = 635 µA Default 405µA
[21]	R/W	Offset UP enable	1	0	Sets Direction of Reg 09h[20:14] Up, 0- UP Offset Off
[22]	R/W	Offset DN enable	1	1	Sets Direction of Reg 09h[20:14] Down, 0- DN Offset Off
[23]	R/W	HiK charge pump Mode	1	0	Only recommended with external VCOs and Active Loop Filters. When enabled the HMC835LP6GE increases CP current by 3 mA, thereby improving phase noise performance, and increasing loop bandwidth

2.12 Reg 0Ah VCO AutoCal Configuration Register DEFAULT 2046h

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	Vtune Resolution	3	6d	Used by internlan AutoCal state machine R Divider Cycles 0 - 1 1 - 2 2 - 4 3 - 8 4 - 32 5 - 64 6 - 128 7 - 256 Ref div cycles for frequency measurement. Measurement should last > 4 µsec. Note: 1 does not work if R divider = 1.
[10:3]	R/W	Reserved	8	8d	Reserved
[11]	R/W	AutoCal Disable	1	0	0 = AutoCal Enabled 1 = AutoCal disabled
[12]	R/W	Reserved	1	0	Reserved
[14:13]	R/W	FSM/VSPI Clock Select	2	1	Set the AutoCal FSM and VSPI Clock (50 MHz maximum) 0: Input Crystal Reference 1: Input Crystal Reference/4 2: Input Crystal Reference/16 3: Input Crystal Reference/32
[16:15]	R/W	Reserved	2	0	Reserved
[17]	R/W	Reserved	1	0	Reserved
[23:18]	R/W	Reserved	5	0	Reserved

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2.13 Reg 0Bh PD/CP Register DEFAULT 7C021h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[3:0]	R/W	Reserved	4	1	Reserved
[4]	R/W	PD Phase Select	1	0	Inverts the PD polarity (program to 0) 0- Use with a positive tuning slope VCO and Passive Loop Filter (default when using internal VCO) 1- Use with a Negative Slope VCO or with an inverting Active Loop Filter with a Positive Slope VCO (Only recommended when using an External VCO, and an active loop filter)
[5]	R/W	PD Up Output Enable	1	1	Enables the PD UP output, see also Reg 0Bh[9]
[6]	R/W	PD Down Output Enable	1	1	Enables the PD DN output, see also Reg 0Bh[10]
[8:7]	R/W	Reserved	2	0	Reserved, Program to 0d.
[9]	R/W	Force CP UP	1	0	Forces CP UP output on if CP is not forced down - Use for Test only
[10]	R/W	Force CP DN	1	0	Forces CP DN output on if CP is not forced up - Use for Test only
[11]	R/W	Force CP Mid Rail	1	0	Force CP MId Rail - Use for Test only (if Force CP UP or Force CP DN are enabled they have precedence)
[23:12]	R/W	Reserved	12	7Ch	Reserved

2.14 Reg 0Ch Exact Frequency Register DEFAULT 0h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[23:0]	R/W	Number of Channels per Fpd	24	0	Comparison Frequency divided by the correction rate. Must be an integer. Frequencies at integer multiples of the correction rate will have zero frequency error. 0: Disabled 1: Invalid ≥ 2 valid max 2^{24}-1 = FFFFFFh = 16,777,215d

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2.15 Reg 0Fh GPO Register DEFAULT 1h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[4:0]	R/W	GPO	5	1	Select signal to be output to SDO pin when enabled DEFAULT LOCK DETECT 0: Data from Reg0F[5] 1: Lock Detect Output 2. Lock Detect Trigger 3: Lock Detect Window Output 4: Ring Osc Test 5. Pullup Hard from CSP 6. PullDN hard from CSP 7. Reserved 8: Reference Buffer Output 9: Ref Divider Output 10: VCO divider Output 11. Modulator Clock from VCO divider 12. Auxiliary Clock 13. Aux SPI Clock 14. Aux SPI Enable 15. Aux SPI Data Out 16. PD DN 17. PD UP 18. SD3 Clock Delay 19. SD3 Core Clock 20. AutoStrobe Integer Write 21. Autostrobe Frac Write 22. Autostrobe Aux SPI 23. SPI Latch Enable 24. VCO Divider Sync Reset 25. Seed Load Strobe 26.-29 Not Used 30. SPI Output Buffer En 31. Soft RSTB Note: Only the default condition is tested during production.
[5]	R/W	GPO Test Data	1	0	1 - GPO Test Data when GPO_Select = 0
[6]	R/W	Prevent Automux SDO	1	0	1- Outputs GPO data only 0- Automuxes between SDO and GPO data
[7]	R/W	Prevent Auto tri-state SDO	1	0	Keep LD_SDO enabled, despite Rx chip address
[8]	R/W	Reserved	1	0	Reserved
[9]	R/W	Reserved	1	0	Reserved
[23:10]	R/W	Reserved	14	0	Reserved

2.16 Reg 10h Tuning Register (Read Only) DEFAULT 80h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[7:0]	R	VCO Tune Curve	8	0	VCO selection resulting from AutoCalibration. 0- maximum frequency '1111 1111'b- minimum frequency
[8]	R	VCO Tuning Busy	1	1	Indicates if the VCO tuning is in process 1- Busy 0- Not Busy

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2.17 Reg 11h SAR Register (Read Only)

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[18:0]	R	SAR Error Magnitude Count	19	2^{19}- 1d 7FFFFh	SAR Error Magnitude Count
[19]	R	SAR Error Sign	1	0	SAR Error Sign 0: positive 1: negative
[23:20]	R	Reserved	4	0	Reserved

2.18 Reg 12h GPO/LD Register (Read Only)

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[0]	R	GPO Out	1	0	GPO Output
[1]	R	Lock Detect Out	1	0	Lock Detect Output
[23:2]	R	Reserved	22	7h	Reserved. May return different values after lock detect training

2.19 Reg 13h BIST Register (Read Only)

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[16:0]	R	Reserved	16	4697d 1259h	Reserved

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2.20 Reg 14h Auxiliary SPI Register DEFAULT 220h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[0]	R/W	Aux SPI Mode	1	0	1- Use the 3 outputs as an SPI port 0- Use the 3 outputs as a static GPO port along with Reg 14h[3:1]
[3:1]	R/W	Aux GPO Values	3	0	3 Output values can be set indivually when Reg 14h[0] = 1
[4]	R/W	Aux GPO 3.3 V	1	0	0- 1.8 V output out of the Auxiliary GPO pins 1- 3.3 V output out of the Auxiliary GPO pins
[8:5]	R/W	Reserved	4	1	Reserved
[9]	R/W	Phase Sync	1	1	When set, CHIP_EN pin is used as a trigger for phase synchronization. Can be used to synchronize multiple HMC835LP6GE, or, along with the Reg 1Ah value to phase step the output. (Exact Frequency Mode must be enabled)
[11:10]	R/W	Aux SPI GPO Output	2	0	Option to send GPO multiplexed data (eg. Lock Detect) to one of the auxiliary outputs 0- None 1 - to [0] 2 - to [1] 3 - to [2]
[13:12]	R/W	Aux SPI Outputs	2	0	When the chip is disabled, the Aux SPI Outputs: 0 - Hi Z 1 - Continue driving 2 - Drive high 3 - Drive low
[23:14]	R/W	Reserved	10	0	Reserved

2.21 Reg 15h Manual VCO Config Register DEFAULT F48A0h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[0]	R/W	Vtune Preset Enable	1	0	1-Vtune Preset enabled (for manual VCO) 0-Vtune Preset controlled by VCO Auto-calibration state machine
[5:1]	R/W	Capacitor Switch Setting	5	16d 10h	capacitor switch setting
[8:6]	R/W	Manual VCO Selection	3	2	selects the VCO core sub-band
[9]	R/W	Manual VCO Tune Enable	1	0	1-Manual VCO tuning enabled. Bits[8:0] are active for manual VCO tuning. 0-Manual VCO tuning disabled. Bits[8:0] are ignored (under the control of VCO Auto-calibration state machine)
[15:10]	R/W	Reserved	6	18d 12h	Reserved
[16]	R/W	Enable Auto-Scale CP current	1	1	1 - Automatically scale CP current based on VCO frequency and capacitor setting 0- Don't scale CP current
[19:17]	R/W	Reserved	3	7d	Reserved
[23:20]	R/W	Spare	4	0	Don't Care

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2.22 Reg 16h Gain Divider Register DEFAULT 6C1h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[5:0]	R/W	RF Divide Ratio	6	1	0 - Mute, VCO and PLL buffer On, RF output stages Off 1 - Fo 2 - Fo/2 3 - invalid, defaults to 2 4 - Fo/4 5 - invalid, defaults to 4 6 - Fo/6 ... 60 - Fo/60 61 - invalid, defaults to 60 62 - Fo/62 > 62 - invalid, defaults to 62
[7:6]	R/W	LO Output Buffer Gain Control	2	3	3 - Max Gain 2 - Max Gain - 3 dB 1 - Max Gain - 6 dB 0 - Max Gain - 9 dB
[9:8]	R/W	LO2 Output Buffer gain Control	2	2	3 - Max Gain 2 - Max Gain - 3 dB 1 - Max Gain - 6 dB 0 - Max Gain - 9 dB
[10]	R/W	Divider Output Stage Gain Control	1	1	1 - Max Gain 0 - Max Gain - 3 dB
[23:11]	R/W	Spare	13	0	Don't Care

2.23 Reg 17h Modes Register DEFAULT 1ABh (See Figure 39)

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[0]	R/W	VCO SubSys Master Enable	1	1	Master enable for the entire VCO Subsystem 1 - Enabled (Chip Enable required) 0 - Disabled
[1]	R/W	VCO Enable	1	1	
[2]	R/W	External VCO Buffer Enable	1	0	External VCO Buffer to output stage enable. Only used when locking an external VCO.
[3]	R/W	PLL Buffer Enable	1	1	PLL Buffer Enable. Used when using an internal VCO.
[4]	R/W	LO1 Output Buffer Enable	1	0	Enables LO1 (LO_P & LO_N pins) output buffer.
[5]	R/W	LO2 Output Buffer Enable	1	1	Enables the LO2 (LO2_N & LO2_P pins) output buffer
[6]	R/W	External Input Enable	1	0	Enables External VCO input
[7]	R/W	Pre Lock Mute Enable	1	1	Mute both output buffers until the PLL is locked
[8]	R/W	LO1 Output Single-Ended Enable	1	1	Enables Single-Ended output mode for LO output 1- Single-ended mode, LO_N pin is enabled, and LO_P pin is disabled 0- Differential mode, both LO_N and LO_P pins enabled Please note that single-ended output is only available on LO_N pin.
[9]	R/W	LO2 Output Single-Ended Enable	1	0	Enables Single-Ended output mode for LO2 output 1- Single-ended mode, LO2_P pin is enabled, and LO2_N pin is disabled 0- Differential mode, both LO2_N and LO2_P pins enabled Please note that single-ended output is only available on LO2_N pin.
[10]	R/W	Reserved	1	0	Reserved
[11]	R/W	Charge Pump Output Select	1	0	Connects CP to CP1 or CP2 output. 0: CP1 1: CP2
[23:12]	R/W	Spare	12	0	Don't Care

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2.24 Reg 18h Bias Register DEFAULT 54C1h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[18:0]	R/W	Reserved	19	21697d 54C1h	Program to 54C3h
[20:19]	R/W	External Input Buffer Bias	2	00	External input buffer bias setting. >=1.5GHz program 11 <1.5GHz program 10
[23:21]	R/W	Spare	3	0	Don't Care

2.25 Reg 19h Cals Register DEFAULT AAAh

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[23:0]	R/W	Reserved	24	2730d AAAh	Reserved. Program to AB2h.

2.26 Reg 1Ah Seed Register DEFAULT B29D0Bh

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[23:0]	R/W	Delta Sigma Modulator Seed	24	11705611d B29D0Bh	Used to program output phase relative to the reference frequency. (Exact Frequency Mode required). When not using Exact Frequency Mode and Auto seed Enable Reg06h[8] =1, Reg1Ah sets the start phase of output signal. If AutoSeed disable Reg06h[8] =0, Reg1Ah is the start phase of the signal after every frequency change. (LO Phase = 2π x Reg1Ah/(2^{24}).

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