NB6L295MNGEVB, NB6L295MMNGEVB

NB6L295MNG/ NB6L295MMNG Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Introduction and Board Description

The NB6L295M Evaluation Board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the operation and performance of either the NB6L295MMNG (CML) or the NB6L295MNG (LVPECL) Dual Channel Programmable Delay.

This evaluation board manual contains:

- Information on the NB6L295M Evaluation Board
- Appropriate Lab Setup
- Detailed Board Features
- Bill of Materials

This manual should be used in conjunction with the device datasheet NB6L295M/D or NB6L295/D which contains full technical details on the device specifications and operation.

The NB6L295M Evaluation Board was also designed to accommodate a custom QFN−24 socket. Therefore, some external components were installed on the bottom side of the board.

Board Features

- On board programmable SDI circuitry minimizing cabling, or, external SDI accessed through SMA connectors.
- Convenient and compact board layout
- 2.5 V or 3.3 V single or split−power supply operation (banana jack connectors for VCC, SMAGND and DUTGND; Separate PLDVCC power supply for on board PLD
- CML or LVPECL differential output signals are accessed via SMA connectors with provision for load termination resistors
- SMA connectors are provided for 1) all high−speed differential input & (CML or LVPECL) output signals and 2) for external SDI & control signals access

Board Layout

The evaluation board is constructed in four layers. The top layer is the primary trace layer and is made with polyimide material. This layer provides a high−bandwidth 50 Ω controlled trace impedance environment for the equal length inputs and outputs. The second layer is a copper ground plane.

Layer Stack

L1 Signal − "High and Low Speed"
L2 SMA Ground
L3 VCC (Device positive power supply) and DUTGND (Device negative power supply)
L4 Signal − "Low Speed"

What measurements can you expect to make?

With this evaluation board, the following measurements could be performed in single ended or differential modes of operation.

- Propagation and Programmed Delay
- Output Rise and Fall Time
- Frequency Performance
- Jitter
- VCMR − Common Mode Range

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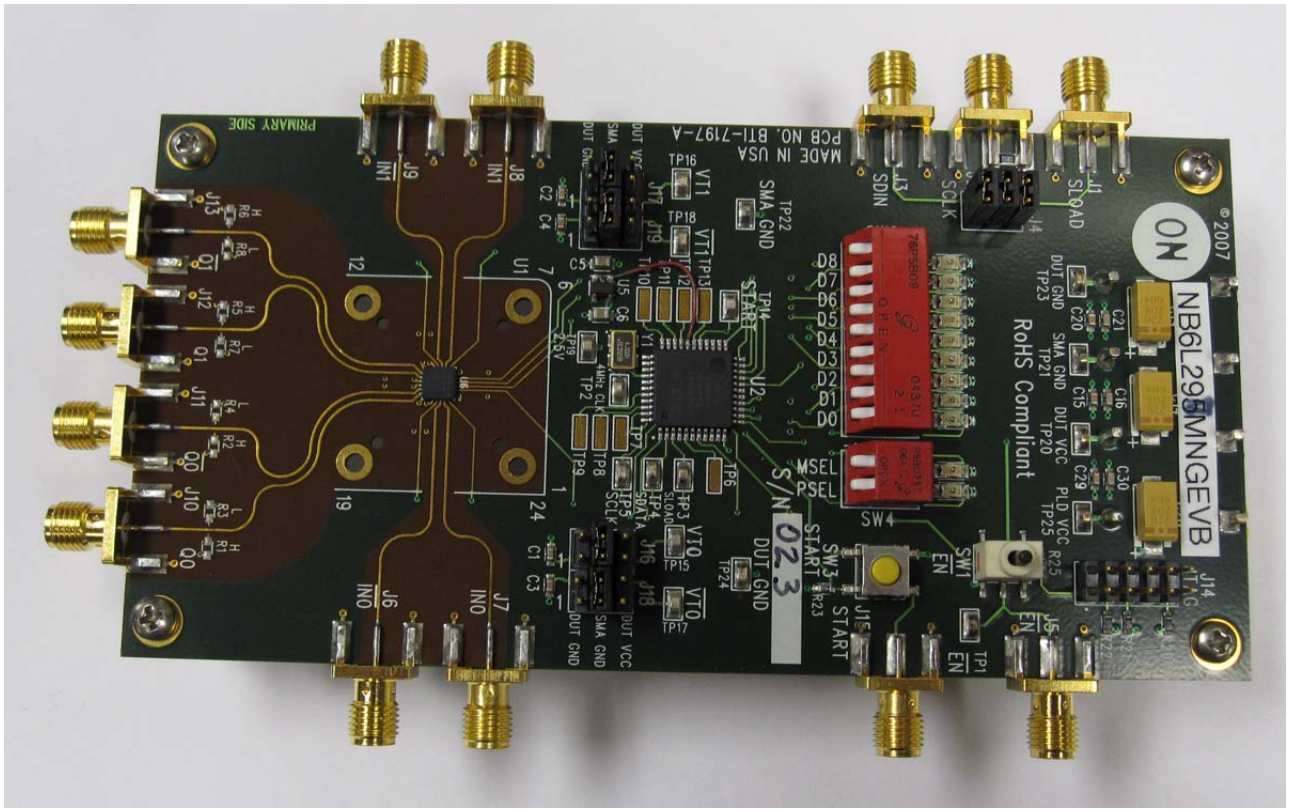


Figure 1. NB6L295MNGEVB Evaluation Board Photo

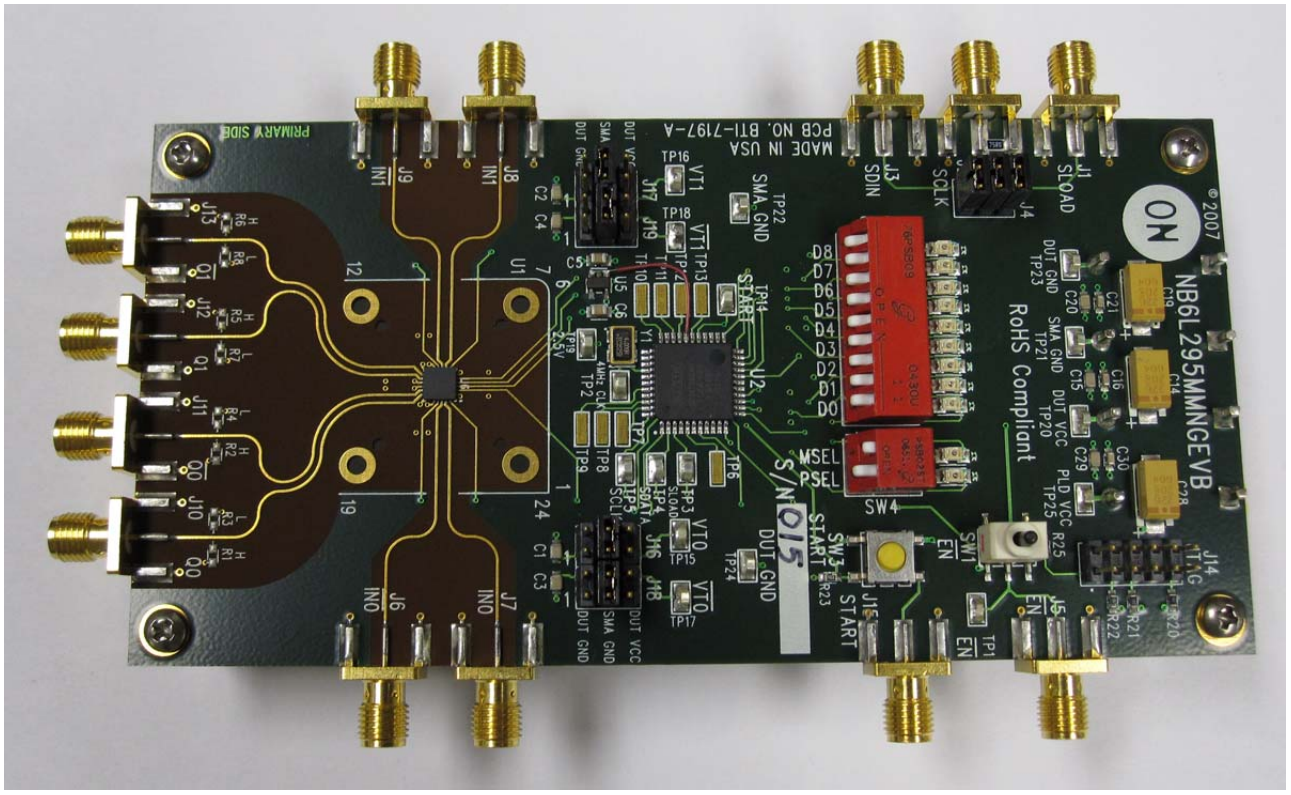


Figure 2. NB6L295MMNGEVB Evaluation Board Photo

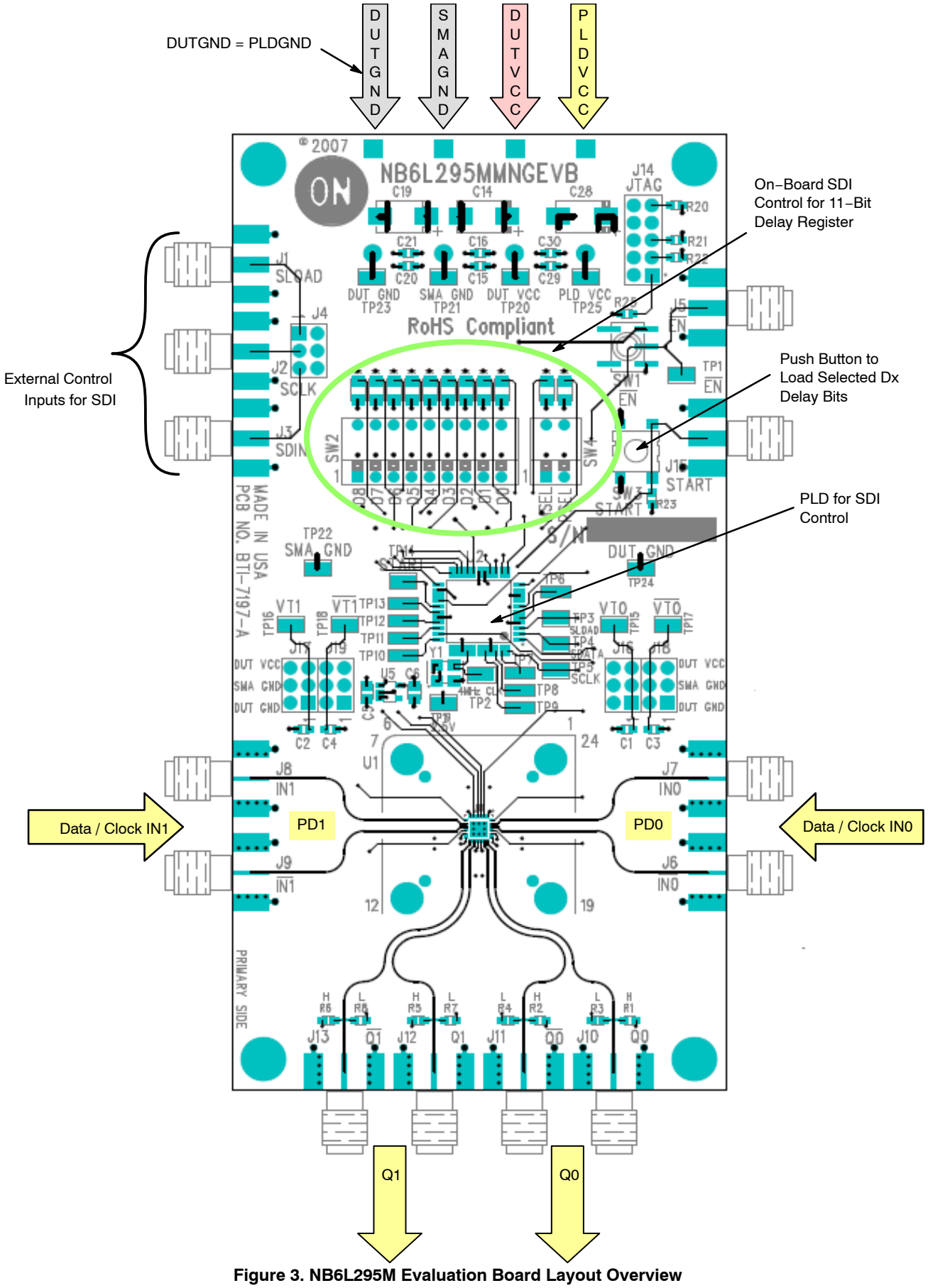


Figure 3. NB6L295M Evaluation Board Layout Overview

TEST AND MEASUREMENT SETUP AND PROCEDURE

Basic Lab Equipment (or Equivalent)

- Agilent Signal Generator #8133A for INx / $\overline{\text{INx}}$, external Clock or Data source
- Tektronix TDS8000 Oscilloscope or Frequency Counter
- Agilent #6624A DC Power Supply
- Digital Voltmeter
- Matched high−speed cables with SMA connectors

Lab Setup

A typical lab setup for taking time domain measurements in differential mode operation is shown in Figures 6 and 7. The following steps should be followed for proper equipment setup:

Step 1: Connect Power Supply

The NB6L295M and NB6L295 have positive supply pins, VCC, VCC0 and VCC1, and negative supply pins, (DUT)GND. The SMAGND (V_{TT}) terminal is the isolated termination ground plane for the outputs, only, and is not to be confused with the device ground pin, (DUT)GND.

Three power levels must be provided to the board, VCC, DUTGND, and SMAGND. Connect a power supplies to banana jack connectors for VCC, PLDVCC, DUTGND and SMAGND, which are provided on the bottom of the board. By−pass capacitors have been installed from VCC to SMAGND and from DUTGND to SMAGND at the banana jacks.

DUTGND = PLDGND, therefore, when device power supply is 2.5 V or 3.3 V, PLDVCC = DUTVCC. The exposed pad on the PCB for the QFN−24 package is connected to DUTGND.

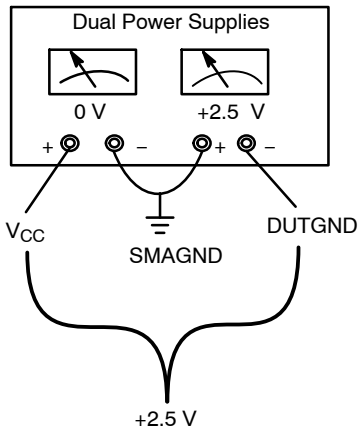


Figure 4. “Split” or Dual Power Supply Connections for NB6L295M, CML Outputs

Table 1. NB6L295M, CML OUTPUTS OFFSET POWER SUPPLY CONFIGURATIONS

Device Pin	Power Supply Connector Color	“Spilt” Power Supply
PLDVCC	Yellow	PLDVCC = 0 V
VCC	Red	V_{CC} = 0 V
SMAGND	Black	V_{TT} = 0 V
DUTGND	Black	DUTGND = −2.5 V or −3.3 V

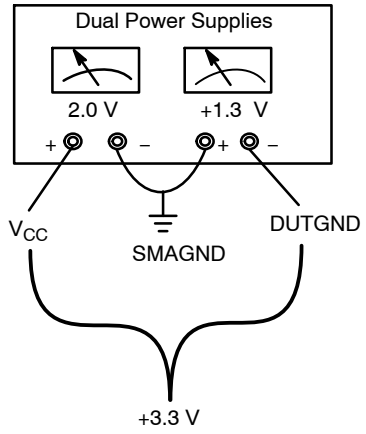


Figure 5. “Split” or Dual Power Supply Connections for NB6L295, LVPECL Outputs

Table 2. NB6L295, LVPECL OUTPUTS “SPLIT” POWER SUPPLY CONFIGURATIONS

Device Pin	Power Supply Connector Color	“Spilt” Power Supply
PLDVCC	Yellow	PLDVCC = +2.0 V
VCC	Red	V_{CC} = +2.0 V
SMAGND	Black	V_{TT} = 0 V
DUTGND	Black	DUTGND = −0.5 V or −1.3 V

Step 2: CML & LVPECL Output Load Termination

NB6L295M – CML Outputs (see Figures 4 and 7)

The CML Qx and $\overline{Qx}$ outputs must be externally DC loaded and AC terminated. A "split" or dual power supply technique can be used to take advantage of terminating the CML outputs into 50 Ω to Ground of an oscilloscope or a frequency counter. Since $V_{TT} = V_{CC}$, offsetting V_{CC} to 0 V yields V_{TT} = 0 V or Ground (SMAGND).

NB6L295 – LVPECL Outputs (see Figures 5 and 6)

The LVPECL Qx and $\overline{Qx}$ outputs have standard, open emitter outputs and must be externally DC loaded and AC terminated.

Taking advantage of the internal 50 Ω to ground of the test equipment, a split power supply technique will assure the equal output loading and termination of both outputs. Connect the Qx and $\overline{Qx}$ outputs of the device to the oscilloscope with equally matched cables. Both outputs must be equally loaded and terminated. The outputs are now DC loaded and AC terminated with 50 Ω to V_{TT}, which is the Ground internal to the oscilloscope. Since $V_{TT} = V_{CC} - 2$ V, offsetting V_{CC} to +2.0 V yields V_{TT} = 0 V or Ground (SMAGND).

The V_{TT} terminal connects to the isolated SMAGND connector ground plane, and is not to be confused with the device ground pin, DUTGND.

NOTE: When a single−ended output is being used, the unconnected output for the pair **must be** terminated to V_{TT} through a 50 Ω resistor for best operation. Unused output pairs may be left unconnected. Since V_{TT} = 0 V, a standard 50 Ω SMA termination plug can be used.

Step 3: Connect and Setup Inputs

Set the signal generator amplitude to appropriate logic levels For Clock, set the generator output for a square wave clock signal with a 50% duty cycle.

For Differential Mode

Connect the differential outputs of the generator with equally matched cables to the differential inputs of the device (INx and $\overline{INx}$). The differential inputs of the NB6L295 incorporate internal 50 Ω termination resistors.

For Single−Ended Mode

Connect the single−ended output of the generator to the INx input of the device. V_{th} must be applied to the complementary input ($\overline{INx}$) when operating in single−ended mode. Refer to the device datasheet for details on single−ended operation.

The VTx and $\overline{VTx}$ termination pins each have a trace from package pin to a node where it can be connected to either VCC, DUTGND or SMAGND, depending on the user's need.

Step 4: Program the SDI

The internal delay registers of the NB6L295/NB6L295M may be programmed by a) the onboard PLD or b) by using the three−lines for an external Serial Data Interface (SDI) consisting of a SERIAL DATA (SDATA) input, a SERIAL CLOCK (SCLK) input, and a SERIAL LOAD (SLOAD) as follows:

a) **Onboard PLD**

When using the onboard PLD for the SDI source,

1. Install the three jumpers located at J4
2. Insure PLDVCC power is applied
3. The 11−bit switches will program the NB6L295's 11−bit shift register. Set SW2 and SW4 switches to the desired values for the 11−bit word
4. Load the program values by depressing momentary switch SW3, or send a pulse signal (125 ns min) through J1.

Refer to the NB6L295 datasheet for details on the proper settings for these switches.

b. **External SDI**

An external SDI source can also program the NB6L295/NB6L295M. See datasheet DC Table, AC Table, as well as Figures 7 and 8. When using an external SDI source, remove the three jumpers at J4.

To use the SDI ports, generate input SCLK, SDATA, and SLOAD signals via the appropriate SMA connectors with OFFSET LVCMOS/LVTTL LEVELS, i.e. +2.0 V HIGH and −1.3 V LOW for a 3.3 V LVPECL power supply. The SCLK signal will sample the information presented on SDATA line. Values are loaded and indexed into a 11−bit shift register. The register shifts once per rising edge of the SCLK input. The serial input SDATA bits must each meet setup and hold timing to the respective SCLK rising edge as specified in the AC Characteristics section of the datasheet document. The LEAST Significant Bit (LSB), PSEL, is indexed in first followed by MSEL and D0, D1, D2, D3, D4, D5, D6, and D7, through MOST Significant Bit (MSB), D8, indexed in last. A Pulse on the SLOAD pin after the SHIFT register is fully indexed (11 clocks) will load and latch the data values for the internal registers.

The SLOAD pulse Low to HIGH rising edge transition transfers the data from the SHIFT register to the LATCH register. The SLOAD Pulse HIGH to LOW transition will lock the new data values into the LATCH register.

After the PLD programs the NB6L295/NB6L295M, PLDVCC can be disconnected.

Input/Output Enable –$\overline{EN}$: When switch SW1 is in the UP position or is externally connected to a LOW through J15 SMA connector, the outputs are ENABLED.

To monitor the Qx and $\overline{Qx}$ outputs on an oscilloscope or frequency counter:

- The power supply needs to be DC offset
- Assure that the instrument has internal 50 Ω termination impedance to ground
- Ensure the oscilloscope is triggered properly

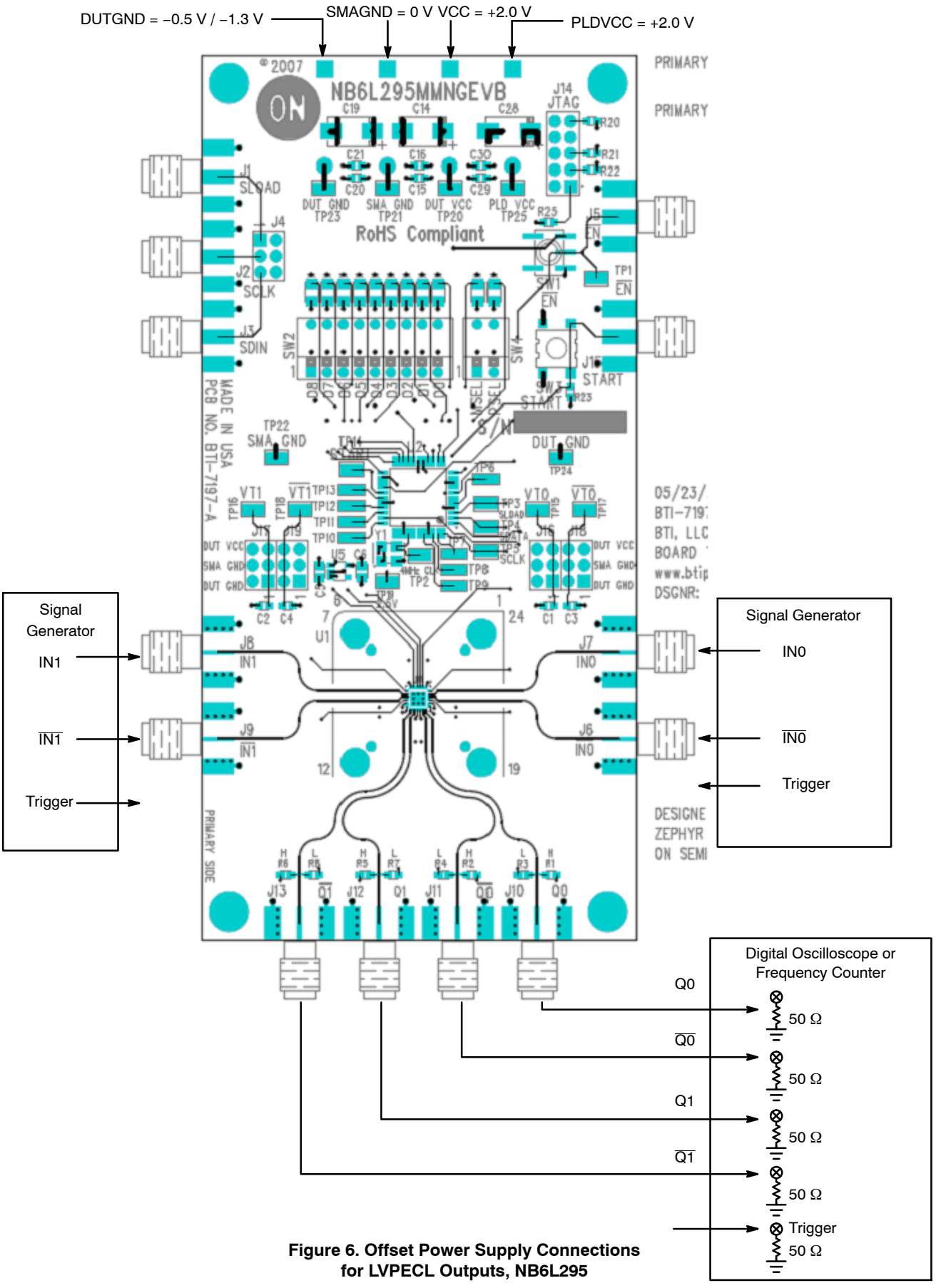


Figure 6. Offset Power Supply Connections for LVPECL Outputs, NB6L295

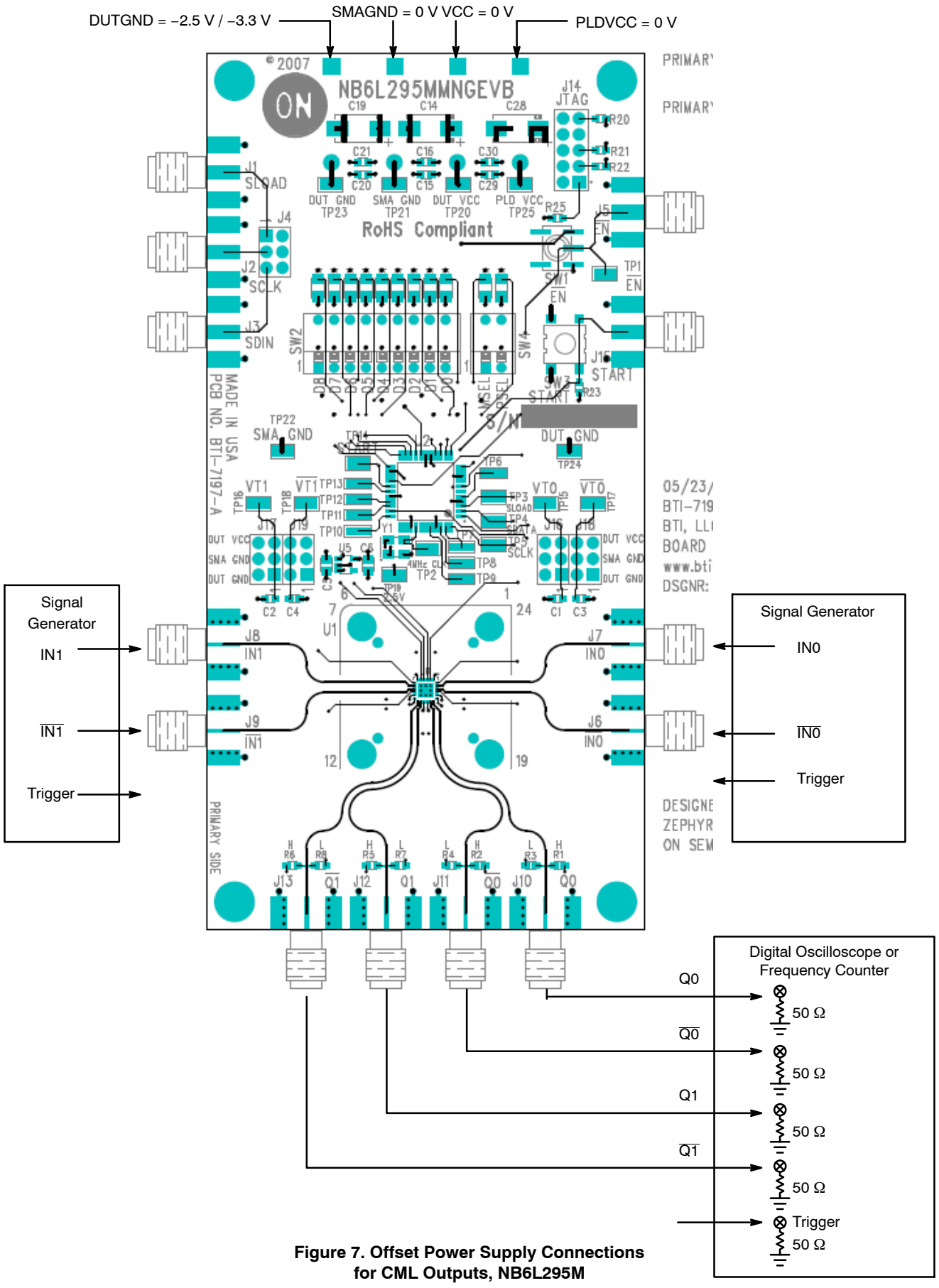
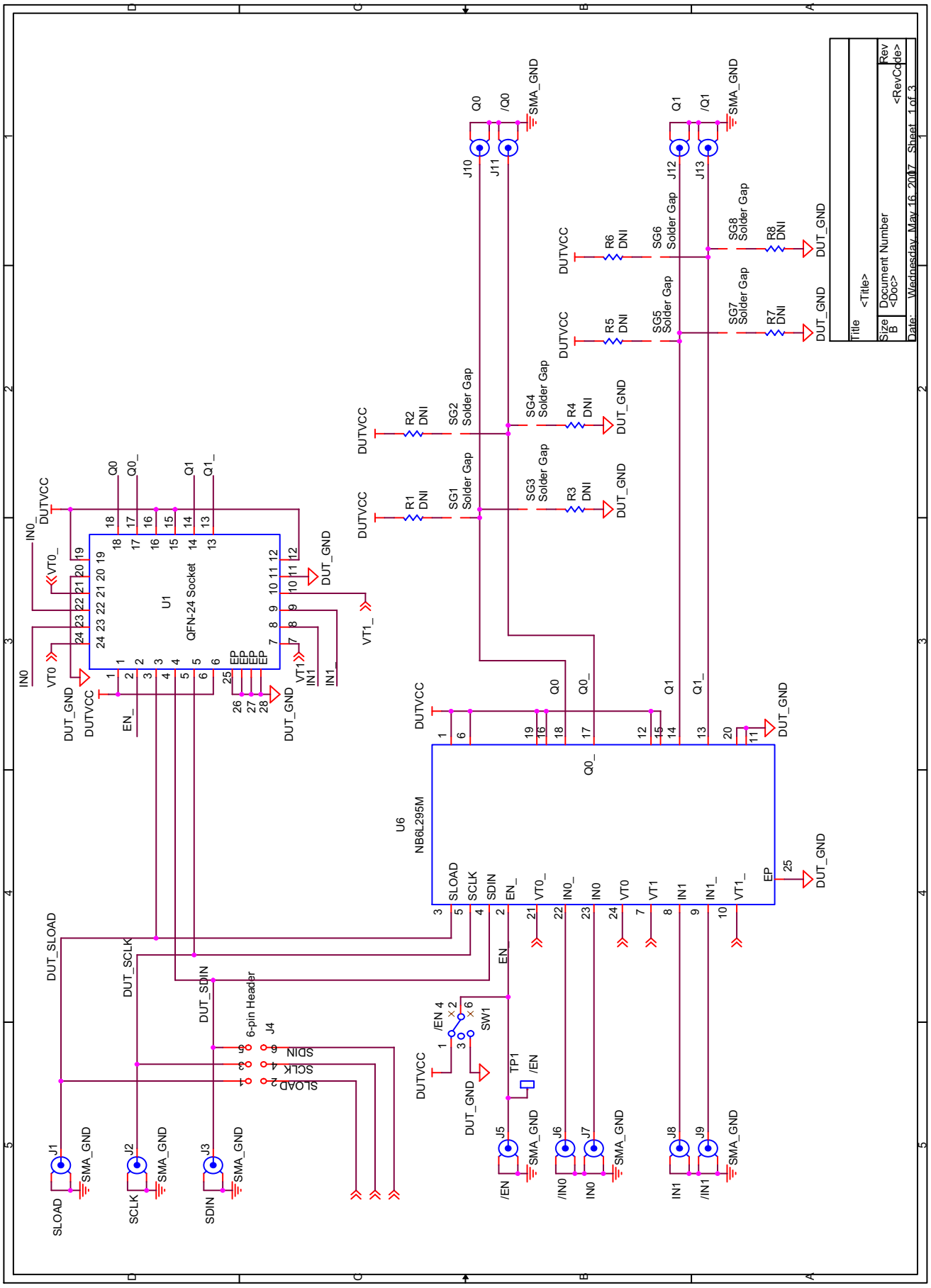


Figure 7. Offset Power Supply Connections for CML Outputs, NB6L295M


U6
NB6L295M
SLOAD
SCLK
SDIN
EN_
VT0_
IN0_
IN0
VT0
VT1
IN1
IN1_
VT1_
EP
Q0
Q0_
Q1
Q1_
DUTVCC
DUT_GND
U1
QFN-24 Socket
EP
EP
EP
EP
IN0_
VT0_
EN_
VT1_
IN1
IN1_
J1
J2
J3
J4
6-pin Header
SLOAD
SCLK
SDIN
J5
J6
J7
J8
J9
J10
J11
J12
J13
SMA_GND
SW1
/EN 4
TP1
/EN
/IN0
IN0
IN1
/IN1
SG1 Solder Gap
SG2 Solder Gap
SG3 Solder Gap
SG4 Solder Gap
SG5 Solder Gap
SG6 Solder Gap
SG7 Solder Gap
SG8 Solder Gap
R1 DNI
R2 DNI
R3 DNI
R4 DNI
R5 DNI
R6 DNI
R7 DNI
R8 DNI
DUT_SLOAD
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DUT_SDIN
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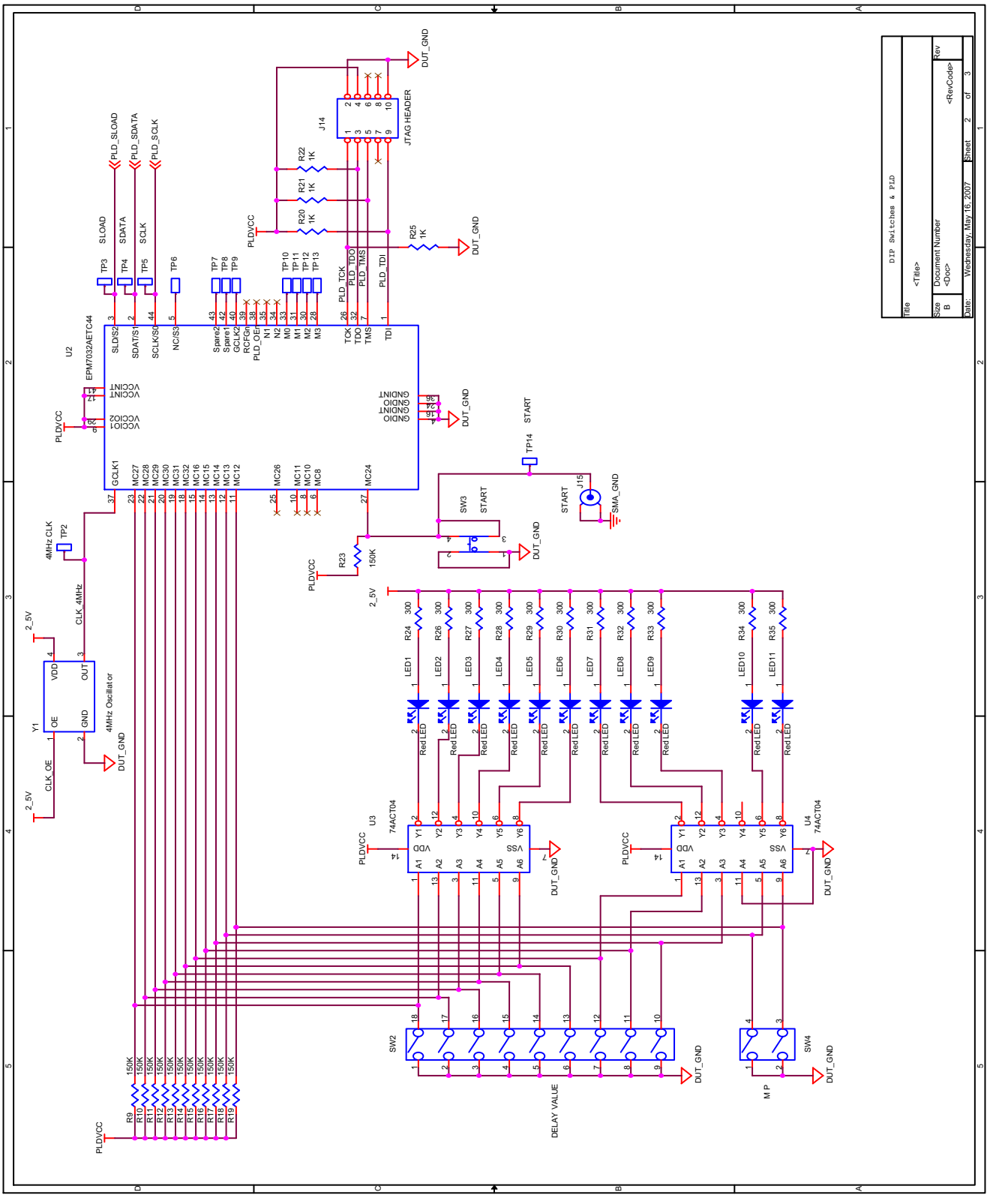
Date: Wednesday, May 16, 2007 Sheet 1 of 3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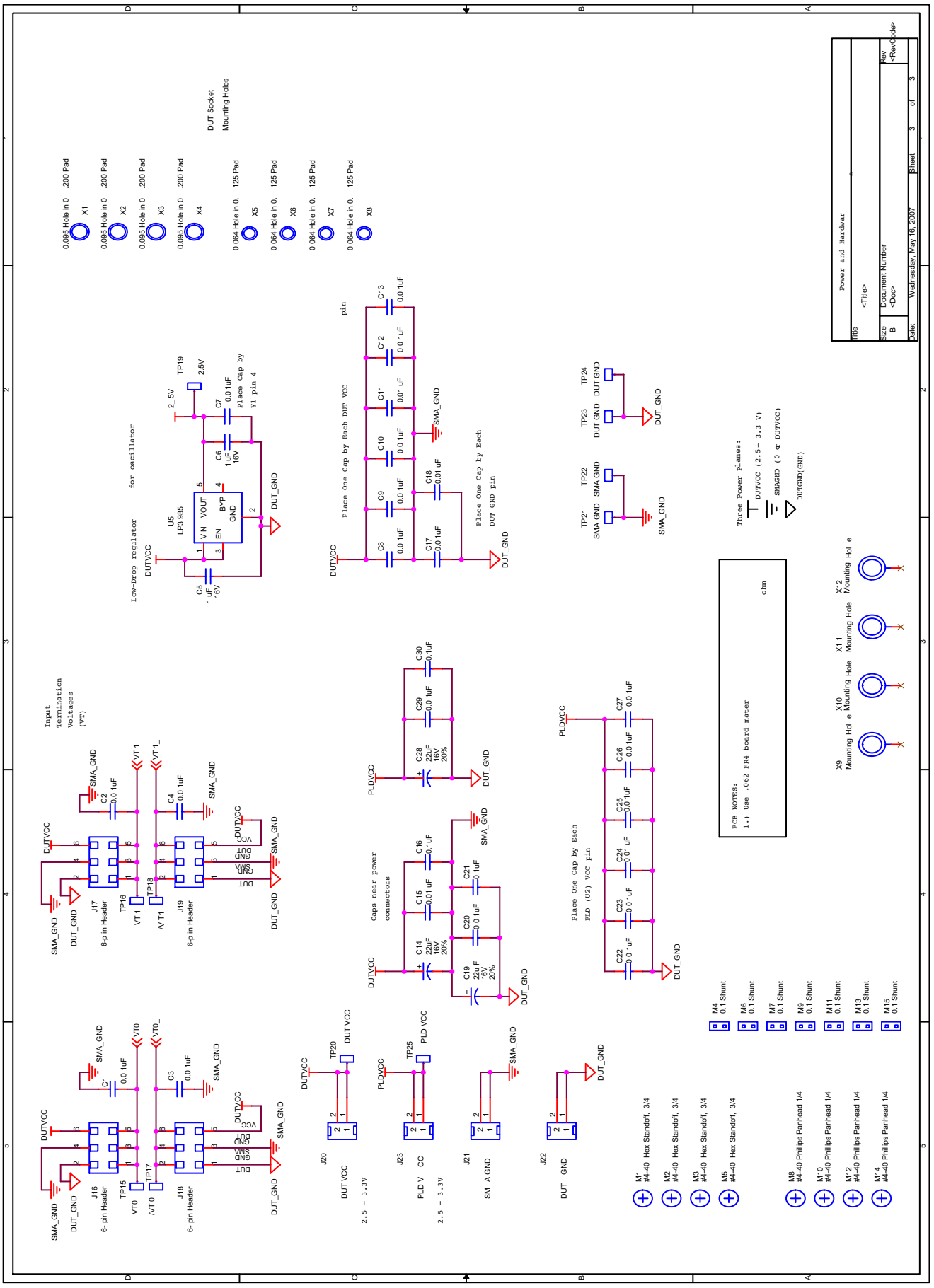
Wednesday, May 16, 2007
JTAG HEADER
EPM7032AETC44
4MHz Oscillator
74ACT04
RedLED
DELAY VALUE
M P
SMA_GND
DUT_GND
PLDVCC
2_5V


Power and Hardwar e
Title
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Date: Wednesday, May 16, 2007
Sheet 3 of 3
Low-Drop regulator for oscillator
Input Termination Voltages (VT)
Place One Cap by Each DUT VCC pin
Place One Cap by Each DUT GND pin
Caps near power connectors
Place One Cap by Each PLD (U2) VCC pin
Three Power planes:
DUTVCC (2.5~ 3.3 V)
SMAGND (0 or DUTVCC)
DUTGND(GND)
PCB NOTES:
1.) Use .062 FR4 board mater
ohm
DUT Socket Mounting Holes
Mounting Hol e
Mounting Hole
Hex Standoff, 3/4
Phillips Panhead 1/4
0.1 Shunt
6-p in Header
6- pin Header
DUT VCC
PLD V CC
SM A GND
DUT GND

Table 3. NB6L295MMNGEVB BILL OF MATERIALS

Item	Qty	Part Number	Value	Ref. Des.	PCB Footprint	Vendor	Vendor PN	Manufacturer
1	22	C0603C103K5RACTU	0.01 μF	C1,C2,C3,C4,C7,C8,C9,C10,C11 C12,C13,C15,C17,C18,C20,C22 C23,C24,C25,C26,C27,C29	603	Digikey	399−1091−1−ND	Kemet
2	2	C0805C105K4RACTU	1 μF	C6,C5	805	Digikey	399−1284−1−ND	Kemet
3	3	T494D226K016AS	22 μF	C14,C19,C28	EIA−7343−31	Digikey	399−1782−1−ND	Kemet
4	3	ECJ−1VB1C104K	0.1 μF	C16,C21,C30	603	Digikey	PCC1762CT−ND	Panasonic
5	13	142−0701−801	SMA	J1,J2,J3,J5,J6,J7,J8,J9, J10,J11,J12,J13,J15	CON_SMA_142−0701−80x JOHNSON	Digi−Key	J502−ND	Johnson Components
6	5	10−89−1061	6−pin Header	J4,J16,J17,J18,J19		Digikey	WM6806−ND	Molex
7	1	10−89−1101	JTAG HEADER	J14		Digikey	WM6810−ND	Molex
8	1	571−0500	Red BANANA JACK	J20	CON2_571−0500 DELTRON	Mouser	164−6219	Deltron
9	2	571−0100	BLK BANANA JACK	J22,J21	CON2_571−0500 DELTRON	Mouser	164−6218	Deltron
10	1	571−0700	Yellow BANANA JACK	J23	CON2_571−0500 DELTRON	Mouser	164−7170	Deltron
11	11	597−3111−407F	Red LED	LED1,LED2,LED3,LED4,LED5, LED6,LED7,LED8,LED9, LED10,LED11	LED_1206_AK	Digikey	350−1565−1−ND	Dialight
12	4	1895	#4−40 Hex Standoff, 3/4	M1,M2,M3,M5		Digikey	1895K−ND	Keystone
13	7	382811−5	0.1 Shunt	M4,M6,M7,M9,M11,M13,M15		Digikey	A26229−ND	AMP/Tyco
14	4	PMS 440 0025 PH	#4−40 Phillips Panhead 1/4	M8,M10,M12,M14		Digikey	H342−ND	Building Fasteners
15	8		DNI	R1,R2,R3,R4,R5,R6,R7,R8	603			
16	12	ERJ−3GEYJ154V	150k	R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R23	603	Digikey	P150KGCT−ND	Panasonic
17	4	ERJ−3GEYJ102V	1k	R20,R21,R22,R25	603	Digikey	P1.0KGCT−ND	Panasonic
18	11	ERJ−3GEYJ301V	300	R24,R26,R27,R28,R29,R30, R31,R32,R33,R34,R35	603	Digikey	P300GCT−ND	Panasonic
20	1	GT13MSCBE	SW SPDT	SW1	SWS_GT13MSCBE_ITT	Digikey	CKN2092CT−ND	C&K
21	1	76PSB09ST	SW PianoDIP−9	SW2	SW_DIP_76PSB09 GRAYHILL	Digikey	GH7145−ND	Grayhill
22	1	B3S−1002	Push Button Switch	SW3	SW_EVQPLD_PAN	Digi−Key	SW416−ND	Omron
23	1	76PSB02ST	SW PianoDIP−2	SW4	SW_DIP_76PSB02 GRAYHILL	Digikey	GH7131−ND	Grayhill
24	17	5015	TP_5015_KEYSTONE	TP1,TP2,TP3,TP4,TP5,TP14, TP15,TP16,TP17,TP18,TP19, TP20,TP21,TP22,TP23,TP24, TP25	TP_5015_KEYSTONE	Digikey	5015KCT−ND	Keystone
26	1	NB6L295 or NB6L295M	DUT	U1	QFN−24			ON Semiconductor
27	1	EPM7032AETC44−10	EPM7032AETC44	U2	TQFP80P1200X1200X120−44N	Arrow	EPM7032AETC44−10	Altera
28	2	74ACT04SC	74ACT04	U3,U4	SO14	Digi−Key	74ACT04SC−ND	Fairchild
29	1	LP3985IM5−2.5/NOPB	LP3985	U5	SOT23−5	Digi−Key	LP3985IM5−2.5CT−ND	National Semi
33	1	ECS−3525−040−B−TR	4MHz Oscillator	Y1	OSCS_3525_ECS	Digikey	XC1047CT−ND	ECS

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