

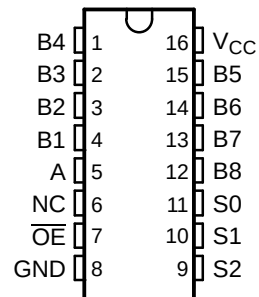
FEATURES

- Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range ($r_{on} = 3\ \Omega$ Typ)
- 0- to 10-V Switching on Data I/O Ports
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)} = 20\text{ pF}$ Max, B Port)
- V_{CC} Operating Range From 4.75 V to 5.25 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications

APPLICATIONS

- PCI Interface
- Differential Signal Interface
- Memory Interleaving
- Bus Isolation
- Low-Distortion Signal Gating

DBQ OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The TS5N118 is a high-bandwidth FET bus switch

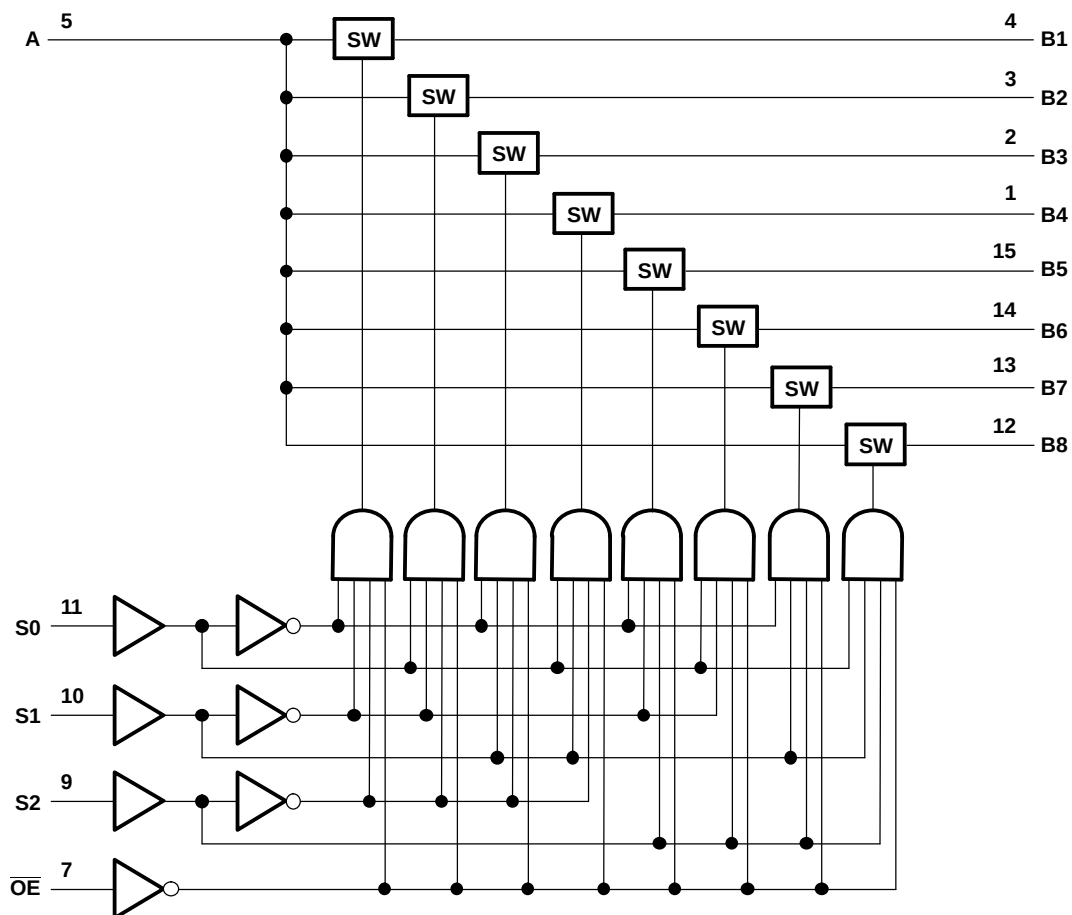
TS5N118
1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER
HIGH-BANDWIDTH BUS SWITCH

SCDS205–AUGUST 2005

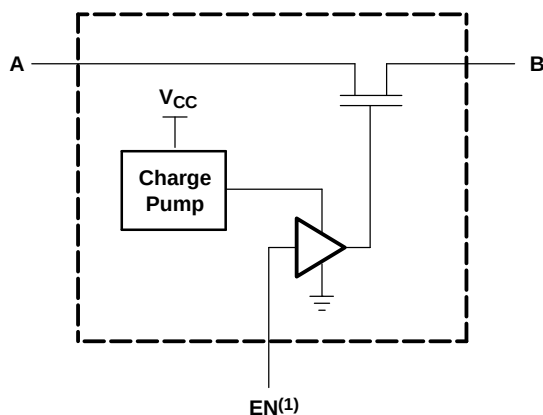
FUNCTION TABLE

INPUTS				INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S2	S1	S0		
L	L	L	L	B1	A port = B1 port
L	L	L	H	B2	A port = B2 port
L	L	H	L	B3	A port = B3 port
L	L	H	H	B4	A port = B4 port
L	H	L	L	B5	A port = B5 port
L	H	L	H	B6	A port = B6 port
L	H	H	L	B7	A port = B7 port
L	H	H	H	B8	A port = B8 port
H	X	X	X	Z	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	7	V
V_{IN}	Control input voltage range ⁽²⁾⁽³⁾	–0.5	7	V
$V_{I/O}$	Switch I/O voltage range ⁽²⁾⁽³⁾⁽⁴⁾	–0.5	11	V
$I_{I/O}$	ON-state switch current ⁽⁵⁾		±100	mA
	Continuous current through V_{CC} or GND		±100	mA
θ_{JA}	Package thermal impedance ⁽⁶⁾	DBQ package		90
		PW package		108
				°C/W
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
- (5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
$V_{$				

TS5N118

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Electrical Characteristics⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽²⁾	MAX	UNIT
I_{IN}	Control inputs	$V_{CC} = 5.25\text{ V}$,	$V_{IN} = 0\text{ to }V_{CC}$				10	μA
I_{OZ} ⁽³⁾		$V_{CC} = 5.25\text{ V}$,	$V_O = 0\text{ to }10\text{ V}$, $V_I = 0$,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$			10	μA
		$V_{CC} = 0\text{ V}$,	$V_O = \text{Open}$,	$V_I = 0\text{ to }10\text{ V}$			10	
I_{CC}		$V_{CC} = 5.25\text{ V}$,	$I_{I/O} = 0$, Switch ON or OFF,	$V_{IN} = V_{CC}\text{ or GND}$			10	mA
C_{in}	Control inputs	$V_{CC} = 5\text{ V}$,	$V_{IN} = 10\text{ V or }0$				10	pF
$C_{io(OFF)}$	A port	$V_{CC} = 5\text{ V}$,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$,	$V_{I/O} = 10\text{ V or }0$			120	pF
	B port	$V_{CC} = 5\text{ V}$,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$,	$V_{I/O} = 10\text{ V or }0$			20	
$C_{io(ON)}$		$V_{CC} = 5\text{ V}$,	Switch ON, $V_{IN} = V_{CC}\text{ or GND}$,	$V_{I/O} = 10\text{ V or }0$			160	pF
r_{on} ⁽⁴⁾		$V_{CC} = 4.75\text{ V}$, TYP at $V_{CC} = 5\text{ V}$	$V_I = 0$,	$I_O = 50\text{ mA}$		3		

TYPICAL PERFORMANCE

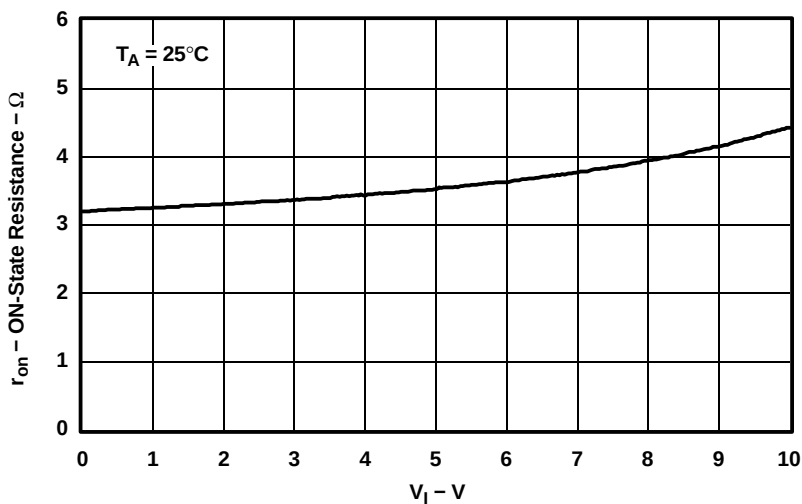


Figure 1. Typical r_{on} vs V_I , $V_{CC} = 5\text{ V}$ and $I_O = -50\text{ mA}$

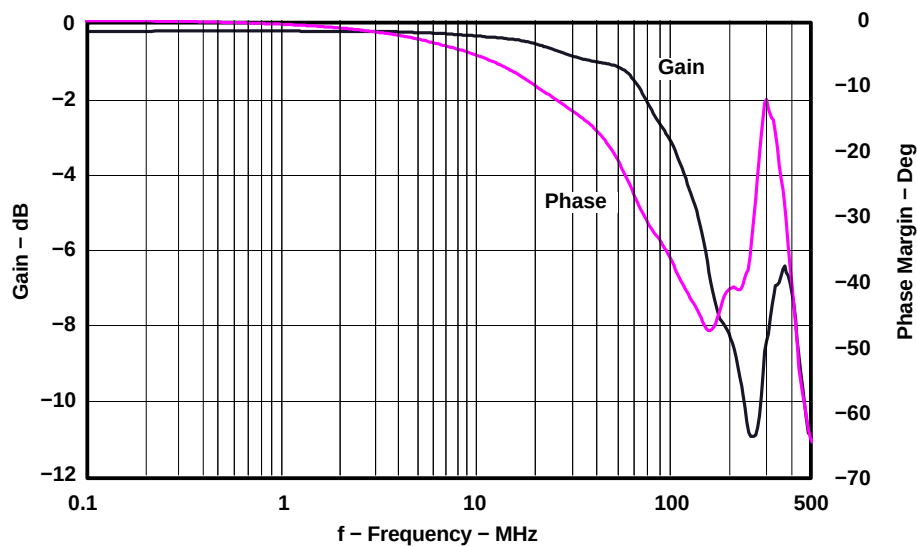


Figure 2. Frequency Response vs Bandwidth

TYPICAL PERFORMANCE

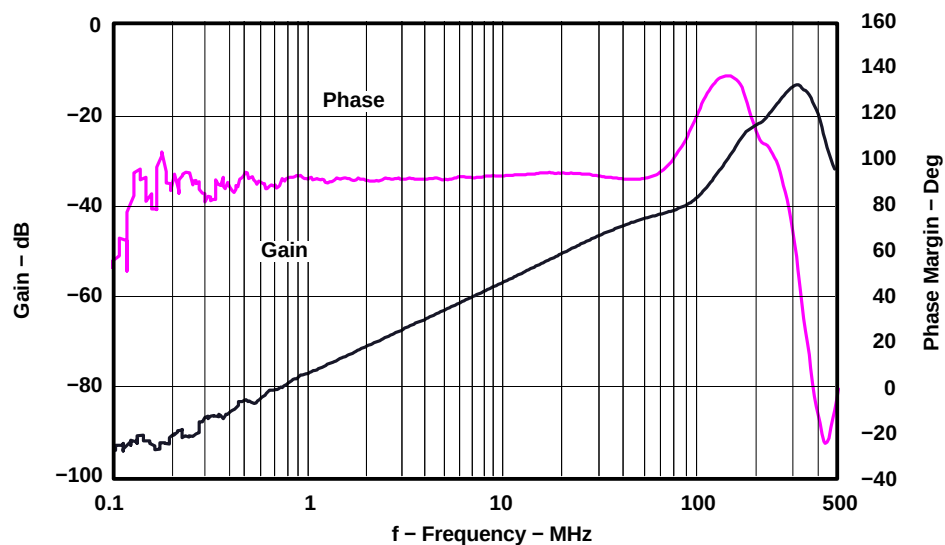


Figure 3. Frequency Response vs OFF Isolation

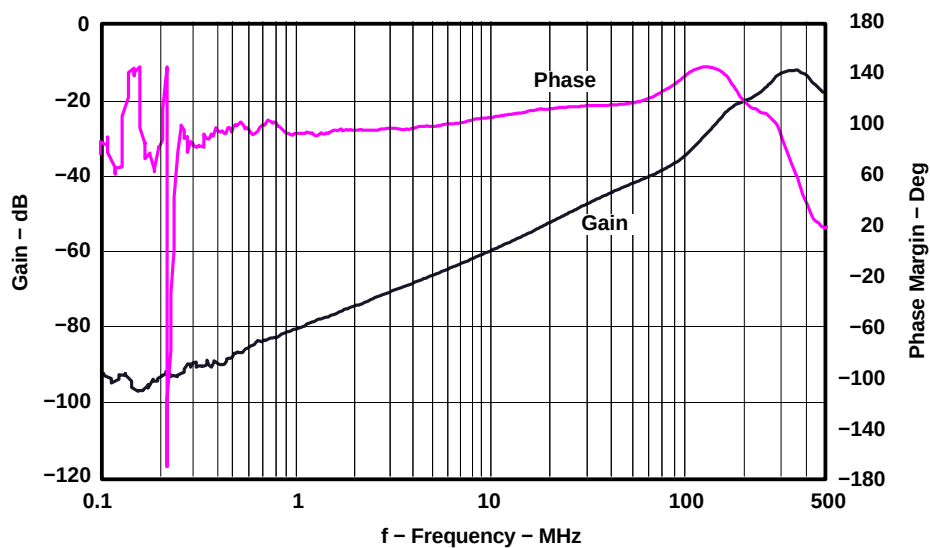
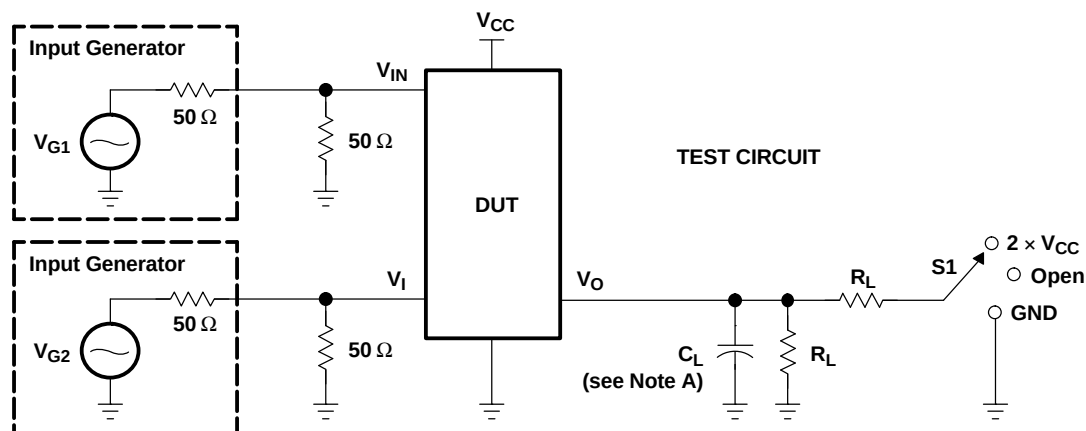


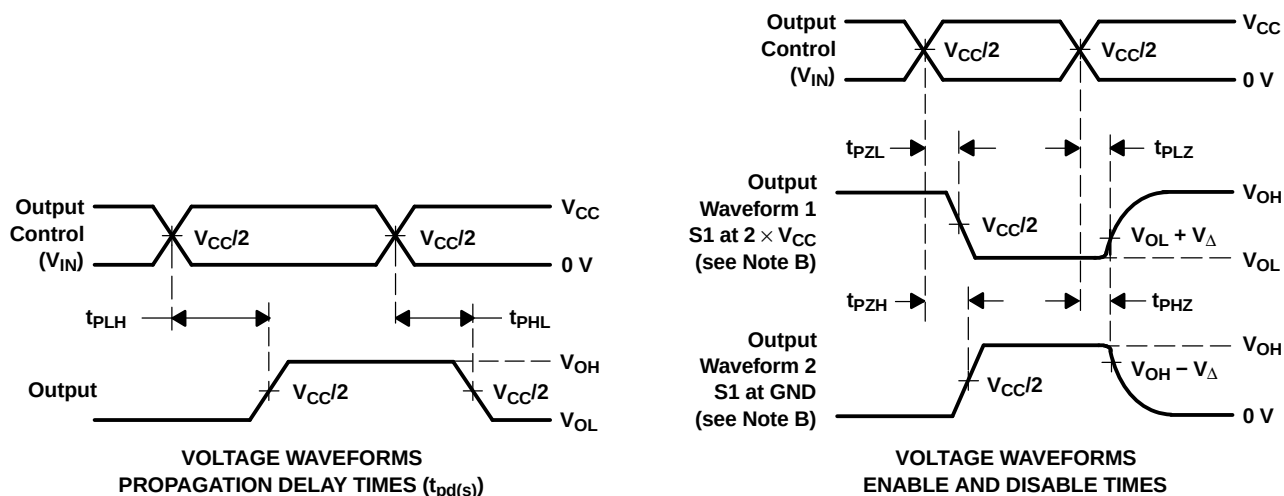
Figure 4. Frequency Response vs Crosstalk

PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd(s)} [†]	5 V ± 0.25 V	Open	100 Ω	V _{CC}	35 pF	
t _{PLZ} /t _{PZL}	5 V ± 0.25 V	2 × V _{CC}	100 Ω	GND	35 pF	0.3 V
t _{PHZ} /t _{PZH}	5 V ± 0.25 V	GND	100 Ω	V _{CC}	35 pF	0.3 V

[†] t_{pd(s)} is measured with Demux inputs at opposite voltage levels, i.e. V_{B1} = 5 V, V_{B2} = GND.



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 25 ns, t_f < 25 ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - t_{PZL} and t_{PZH} are the same as t_{en}.
 - t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output

PARAMETER MEASUREMENT INFORMATION

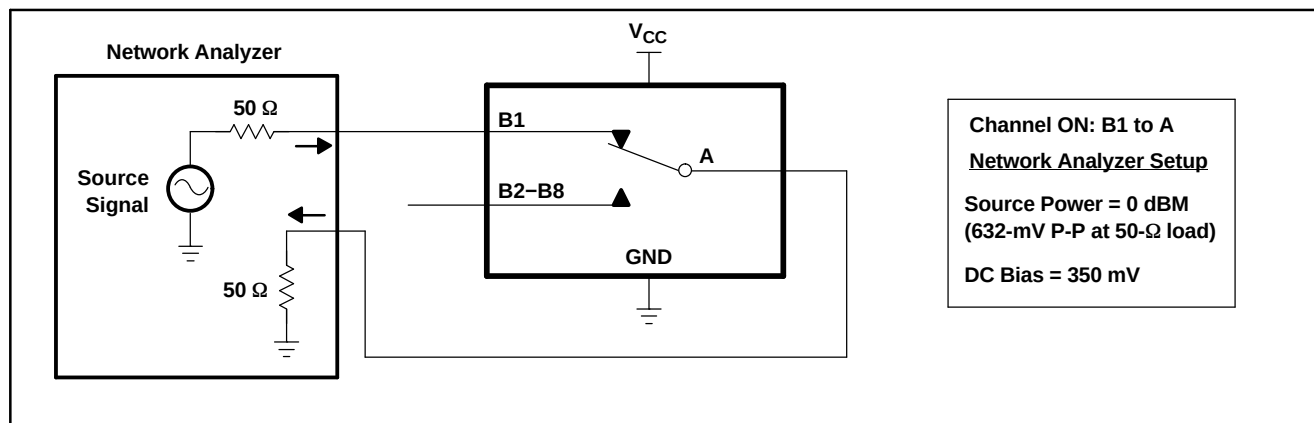


Figure 6. Bandwidth (BW)

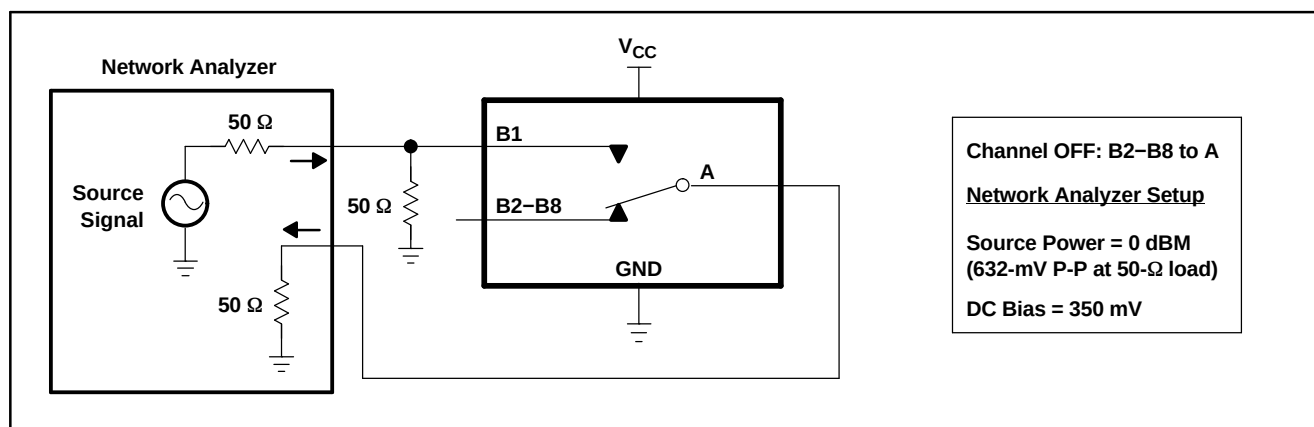


Figure 7. OFF Isolation (O_{ISO})

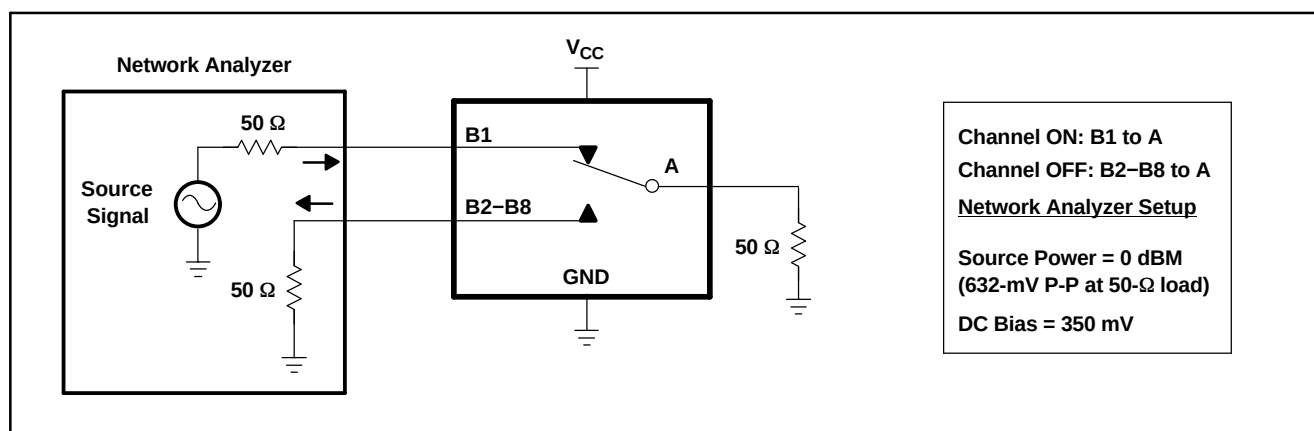
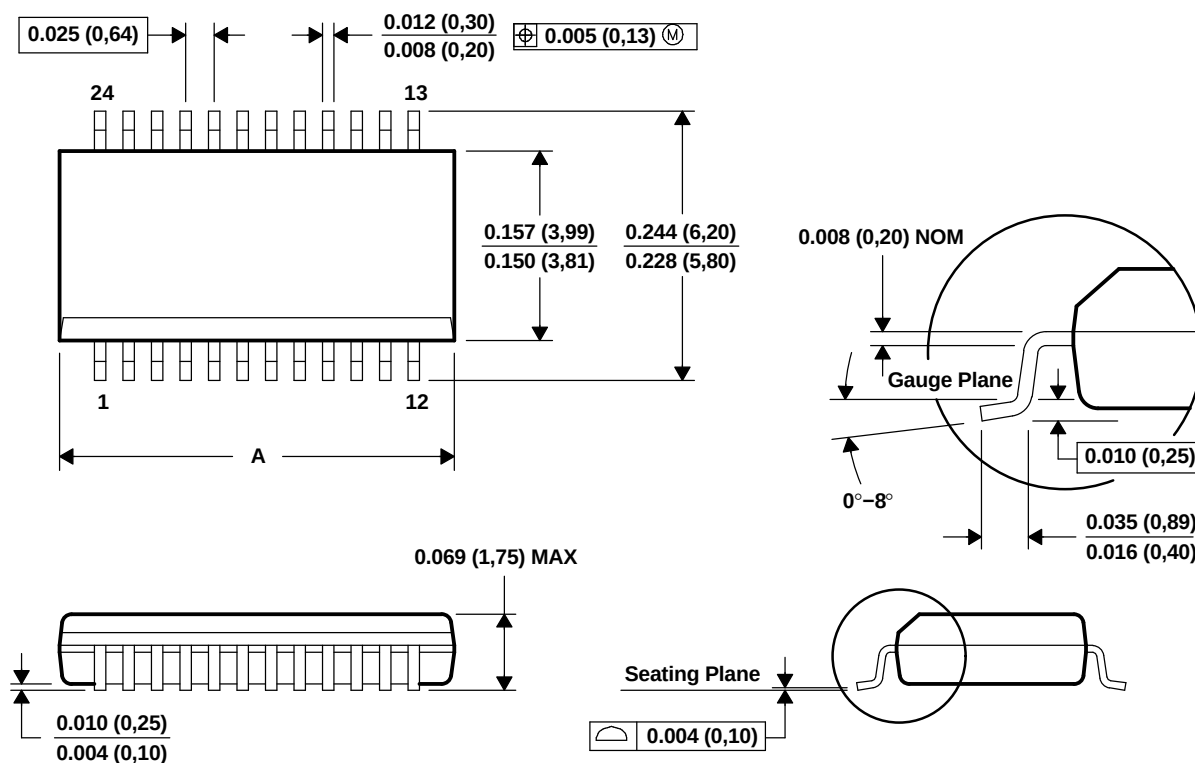


Figure 8. Crosstalk (X_{TALK})

MECHANICAL DATA

DBQ (R-PDSO-G**)



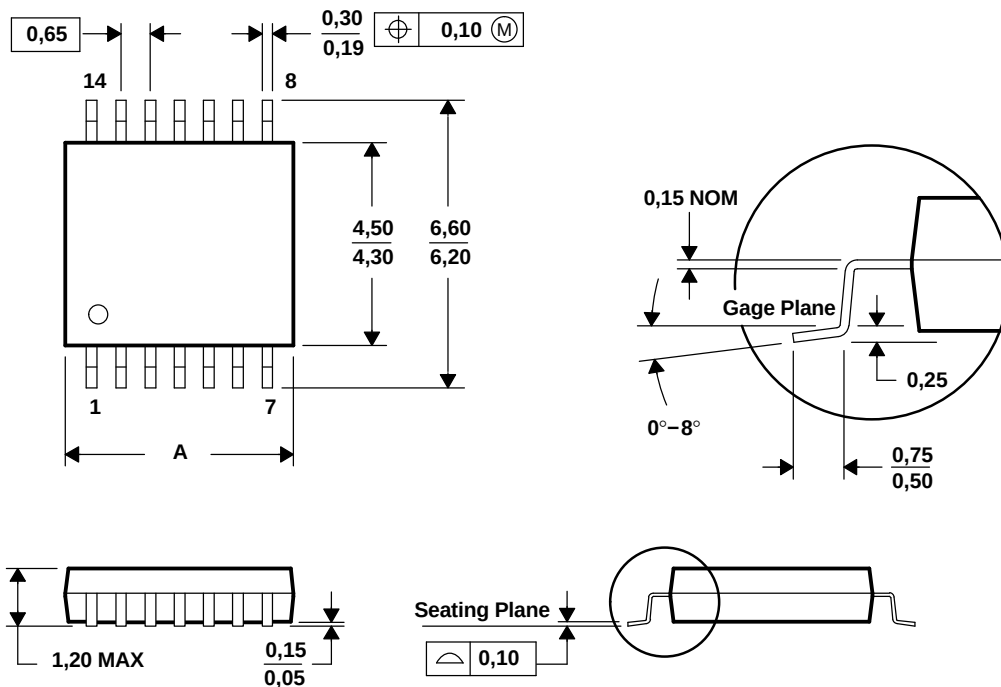
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MECHANICAL DATA

PW (R-PDSO-G)**

14 PINS SHOWN



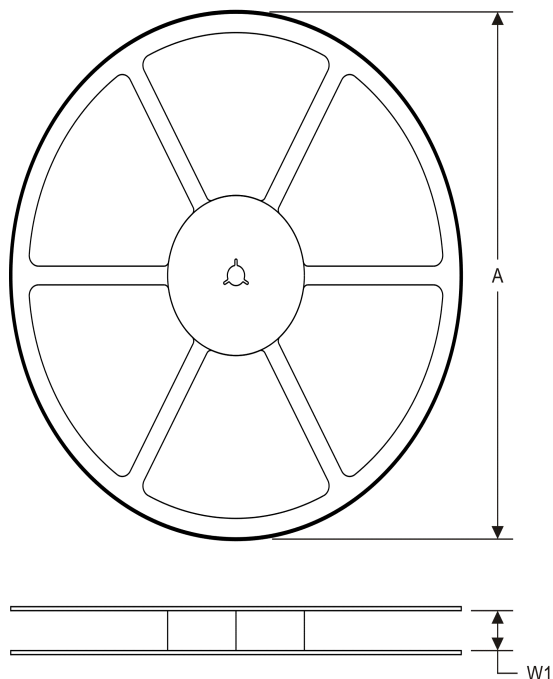
PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TS5N118DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS5N118DBQRE4	ACTIVE	SSOP							

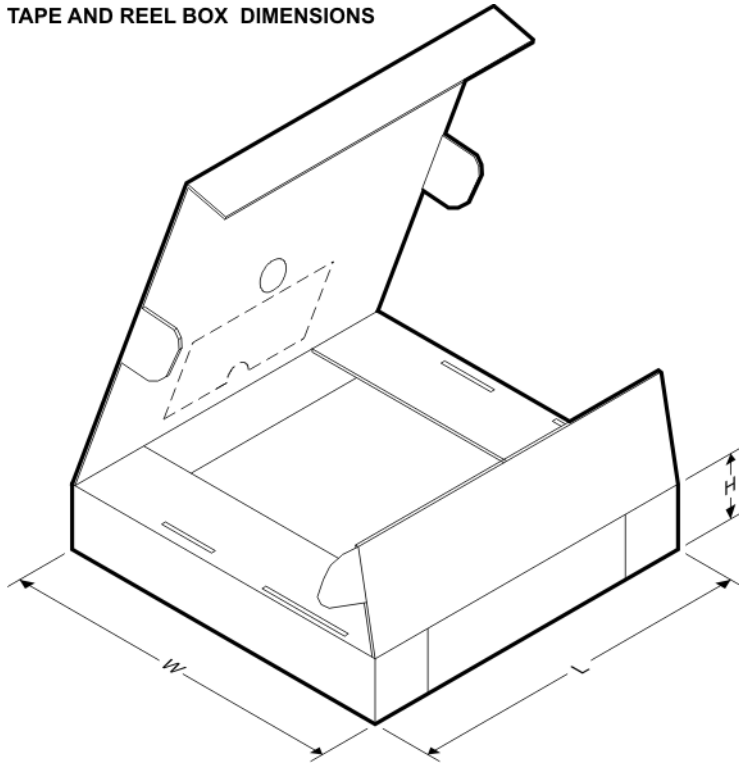
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS
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TAPE AND REEL BOX DIMENSIONS

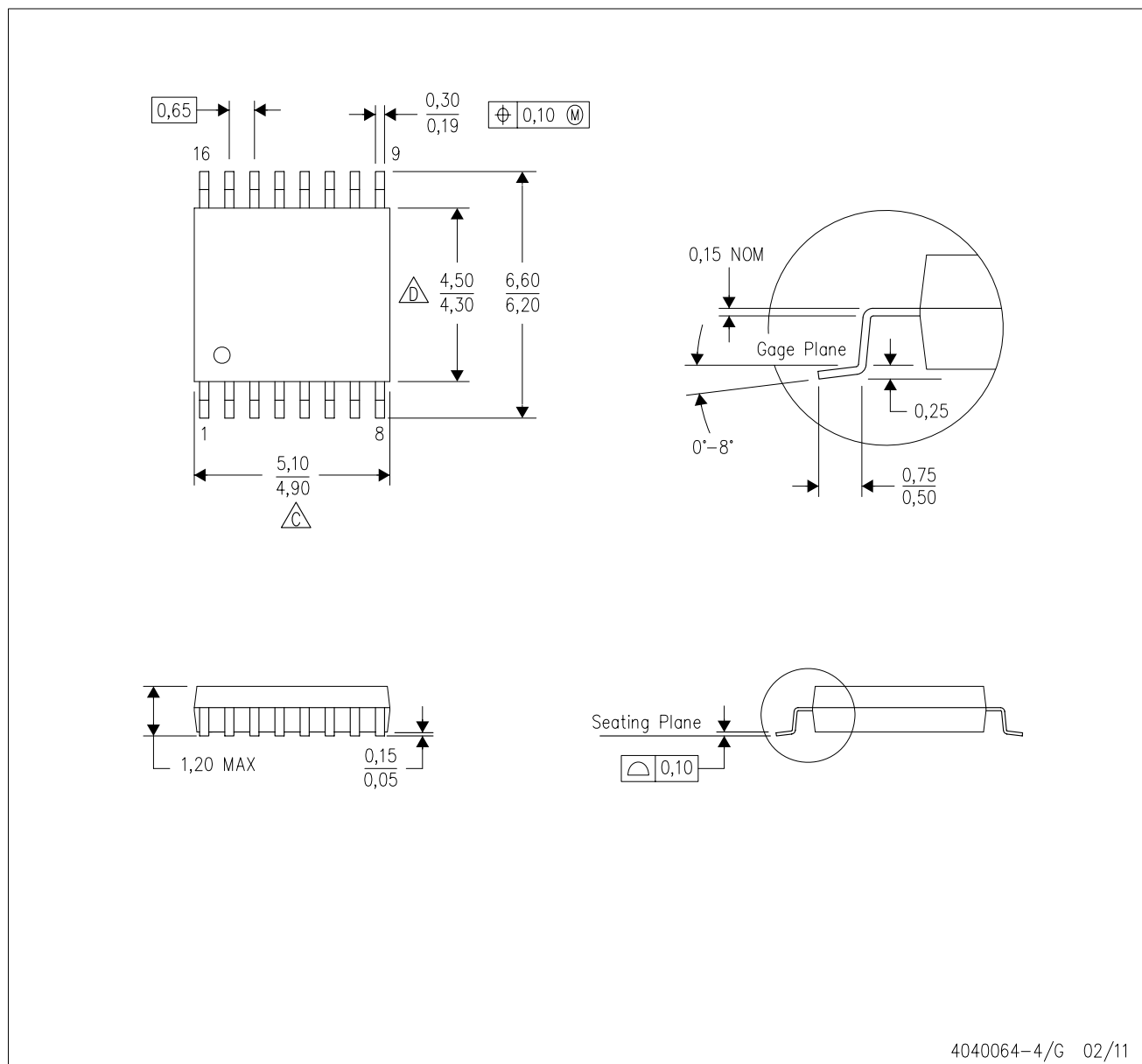


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins</
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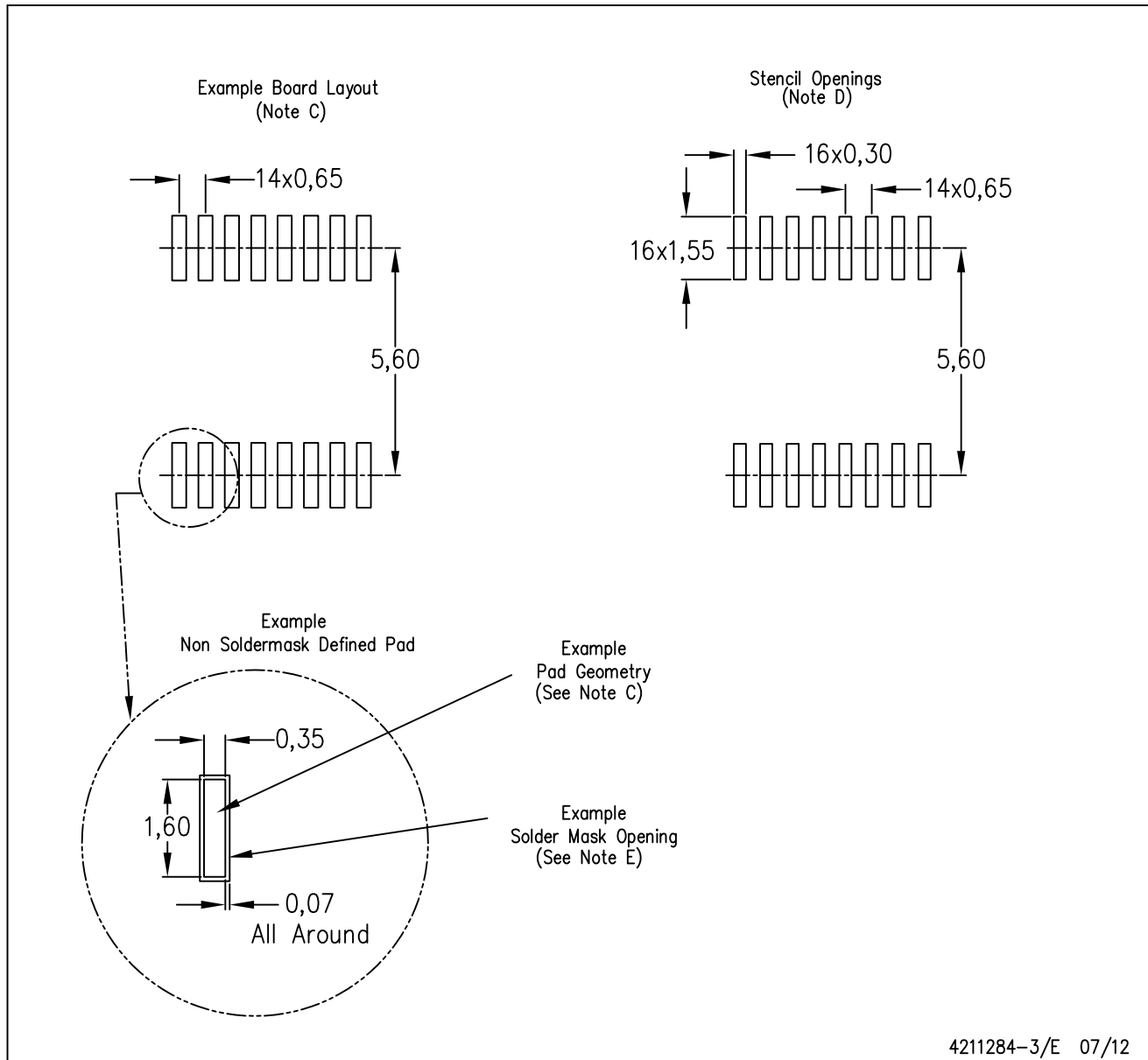
PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



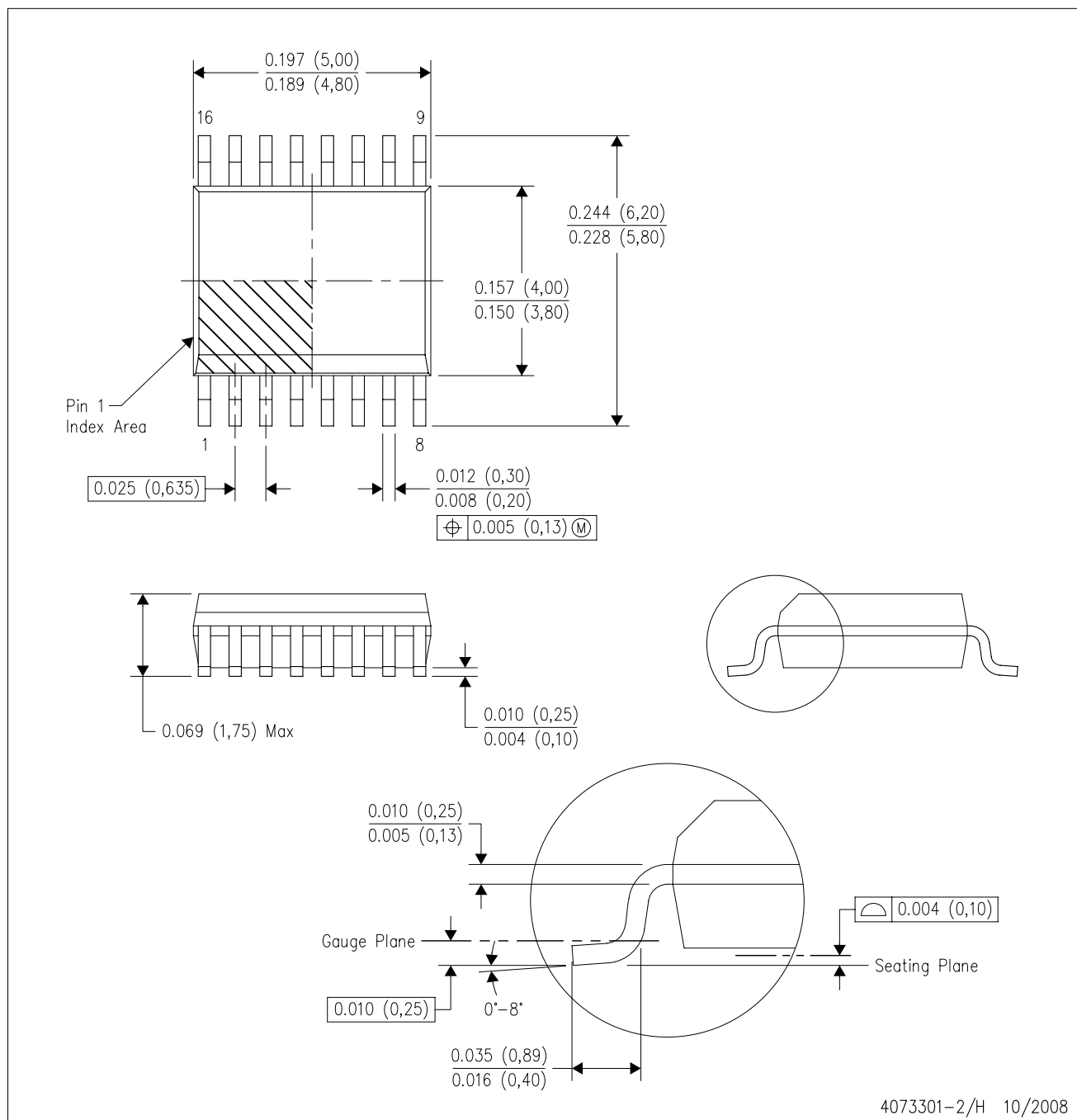
PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



DBQ (R-PDSO-G16)

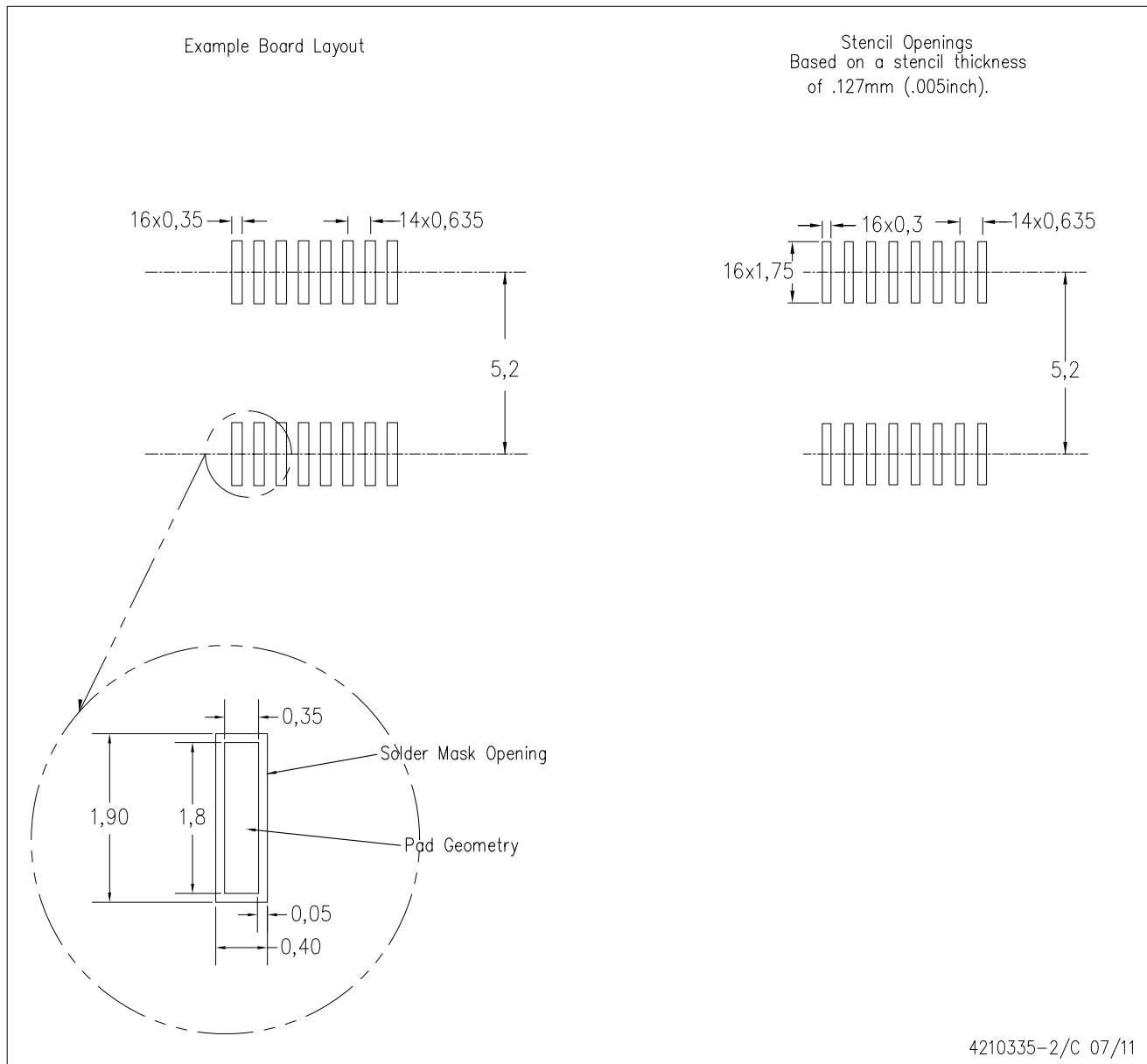
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AB.

DBQ (R-PDSO-G16)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
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