3.3V MULTIMEDIA FIFO
16 BIT V-III, 32 BIT Vx-III FAMILY
UP TO 1 Mb DENSITY

IDT72V15160 *IDT72V14320*
IDT72V16160 *IDT72V15320*
IDT72V17160 *IDT72V16320*
IDT72V18160 *IDT72V17320*
IDT72V19160 *IDT72V18320*
IDT72V19320

FEATURES:

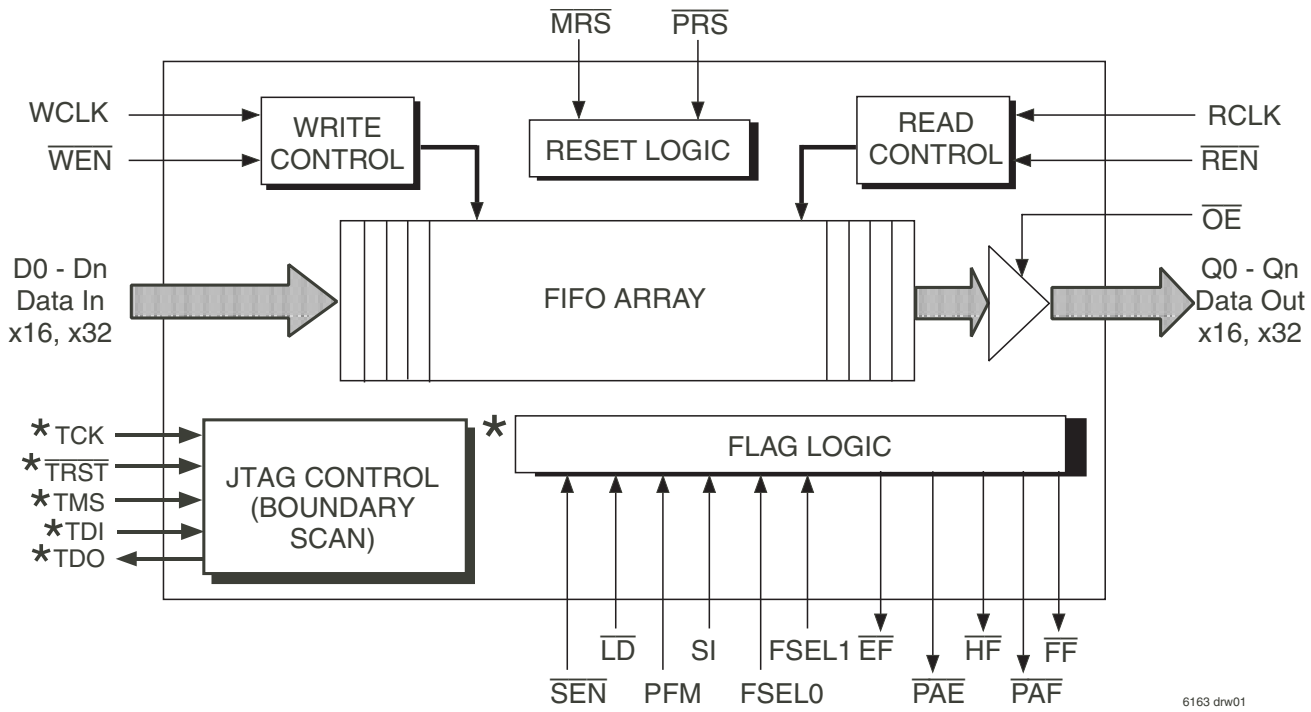
- Choose among the following memory organizations: Commercial

V-III	Vx-III
IDT72V15160 - 4,096 x 16	IDT72V14320 - 1,024 x 32
IDT72V16160 - 8,192 x 16	IDT72V15320 - 2,048 x 32
IDT72V17160 - 16,384 x 16	IDT72V16320 - 4,096 x 32
IDT72V18160 - 32,768 x 16	IDT72V17320 - 8,192 x 32
IDT72V19160 - 65,536 x 16	IDT72V18320 - 16,384 x 32
	IDT72V19320 - 32,768 x 32

- Up to 100 MHz Operation of the Clocks
- 5V input tolerant
- Auto power down minimizes standby power consumption
- Master Reset clears entire FIFO
- Partial Reset clears data, but retains programmable settings
- Empty, Full and Half-Full flags signal FIFO status
- Programmable Almost-Empty and Almost-Full flags, each flag can default to one of eight preselected offsets
- Program programmable flags through serial input
- Output enable puts data outputs into high impedance state
- JTAG port, provided for Boundary Scan function (PBGA Only)
- Available in a 80-pin (V-III) Thin Quad Flat Pack, 128-pin(Vx-III) Thin Quad Flat Pack (TQFP) or a 144-pin (Vx-III) Plastic Ball Grid Array (PBGA) (with additional features)
- Industrial temperature range (–40°C to +85°C)
- High-performance submicron CMOS technology

FUNCTIONAL BLOCK DIAGRAM

*Available on the Vx-III PBGA package only.



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DESCRIPTION:

The IDT V-III and Vx-III Multimedia FIFOs are exceptionally deep, high speed, CMOS First-In-First-Out (FIFO) memories with independent clocked read and write controls and high density offerings up to 1 Mbit.

Each FIFO has a data input port (D_n) and a data output port (Q_n). The frequencies of both the RCLK (read port clock) and the WCLK (write port clock) signals may vary from 0 to $f_{S(MAX)}$ with complete independence. There are no restrictions on the frequency of the one clock input with respect to the other.

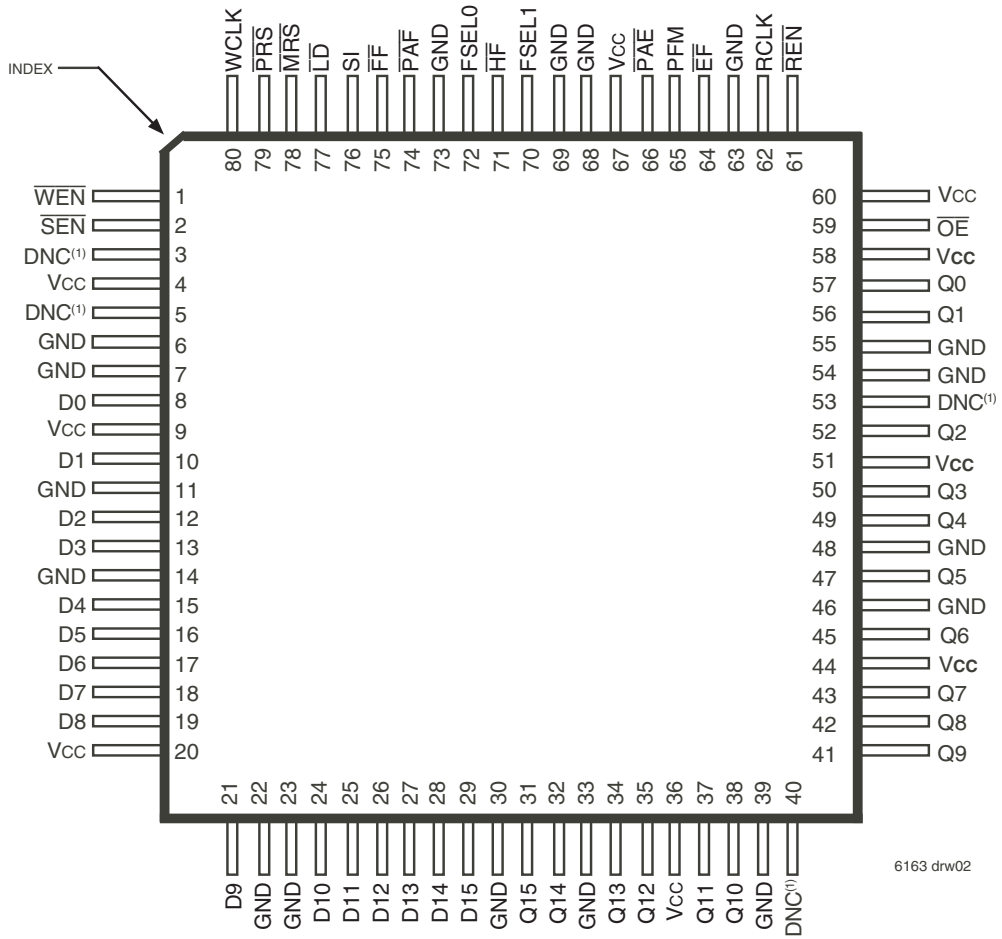
These FIFOs have five flag pins, $\overline{EF}$ (Empty Flag), $\overline{FF}$ (Full Flag), $\overline{HF}$ (Half-full Flag), $\overline{PAE}$ (Programmable Almost-Empty flag) and $\overline{PAF}$ (Programmable Almost-Full flag).

$\overline{PAE}$ and $\overline{PAF}$ can be programmed independently to switch at any point in memory. Programmable offsets determine the flag switching threshold and can be loaded with the serial interface to any user desired value or by default values. Eight default offset settings are provided, so that $\overline{PAE}$ can be set to switch at a predefined number of locations from the empty boundary and the $\overline{PAF}$ threshold can also be set at similar predefined values from the full boundary. The default offset values are set during Master Reset by the state of the FSEL0, FSEL1, and $\overline{LD}$ pins.

For serial programming, $\overline{SEN}$ together with $\overline{LD}$ on each rising edge of WCLK, are used to load the offset registers via the Serial Input (SI).

During Master Reset ($\overline{MRS}$) the read and write pointers are set to the first location of the FIFO.

PIN CONFIGURATIONS (16-BIT V-III FAMILY)



NOTE:
1. DNC = Do Not Connect.

TQFP (PN80-1, order code: PF)
TOP VIEW

The Partial Reset ($\overline{PRS}$) also sets the read and write pointers to the first location of the memory. However, the programmable flag settings existing before Partial Reset remain unchanged. $\overline{PRS}$ is useful for resetting a device in mid-operation, when reprogramming programmable flags would be undesirable.

It is also possible to select the timing mode of the $\overline{PAE}$ (Programmable Almost-Empty flag) and $\overline{PAF}$ (Programmable Almost-Full flag) outputs. The timing modes can be set to be either asynchronous or synchronous for the $\overline{PAE}$ and $\overline{PAF}$ flags.

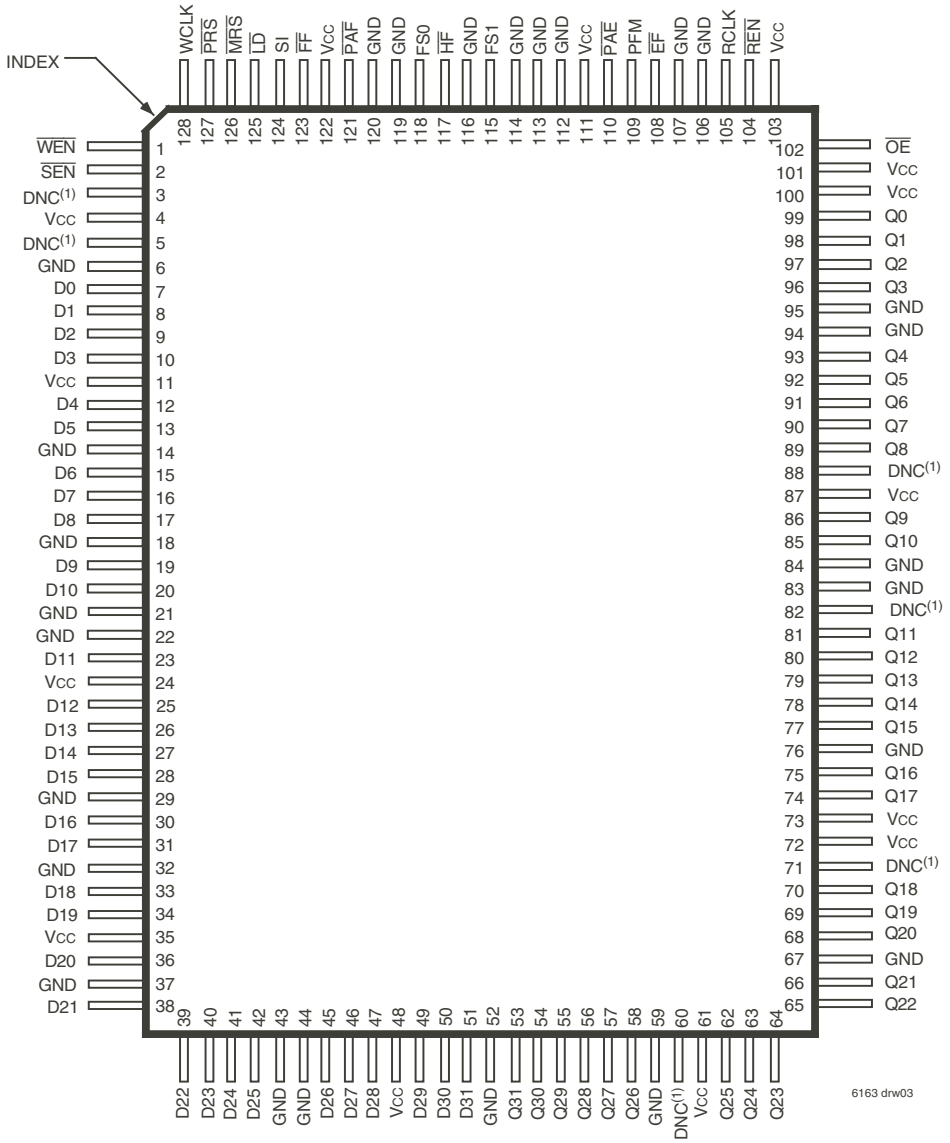
If asynchronous $\overline{PAE}$/$\overline{PAF}$ configuration is selected, the $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of WCLK. Similarly, the $\overline{PAF}$ is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of RCLK.

If synchronous $\overline{PAE}$/$\overline{PAF}$ configuration is selected, the $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only and not WCLK. Similarly, $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only and not RCLK. The mode desired is configured during Master Reset by the state of the Programmable Flag Mode (PFM) pin.

If, at any time, the FIFO is not actively performing an operation, the chip will automatically power down. Once in the power down state, the standby supply current consumption is minimized. Initiating any operation (by activating control inputs) will immediately take the device out of the power down state.

The IDT V-III and Vx-III family of FIFOs are fabricated using IDT's high speed submicron CMOS technology.

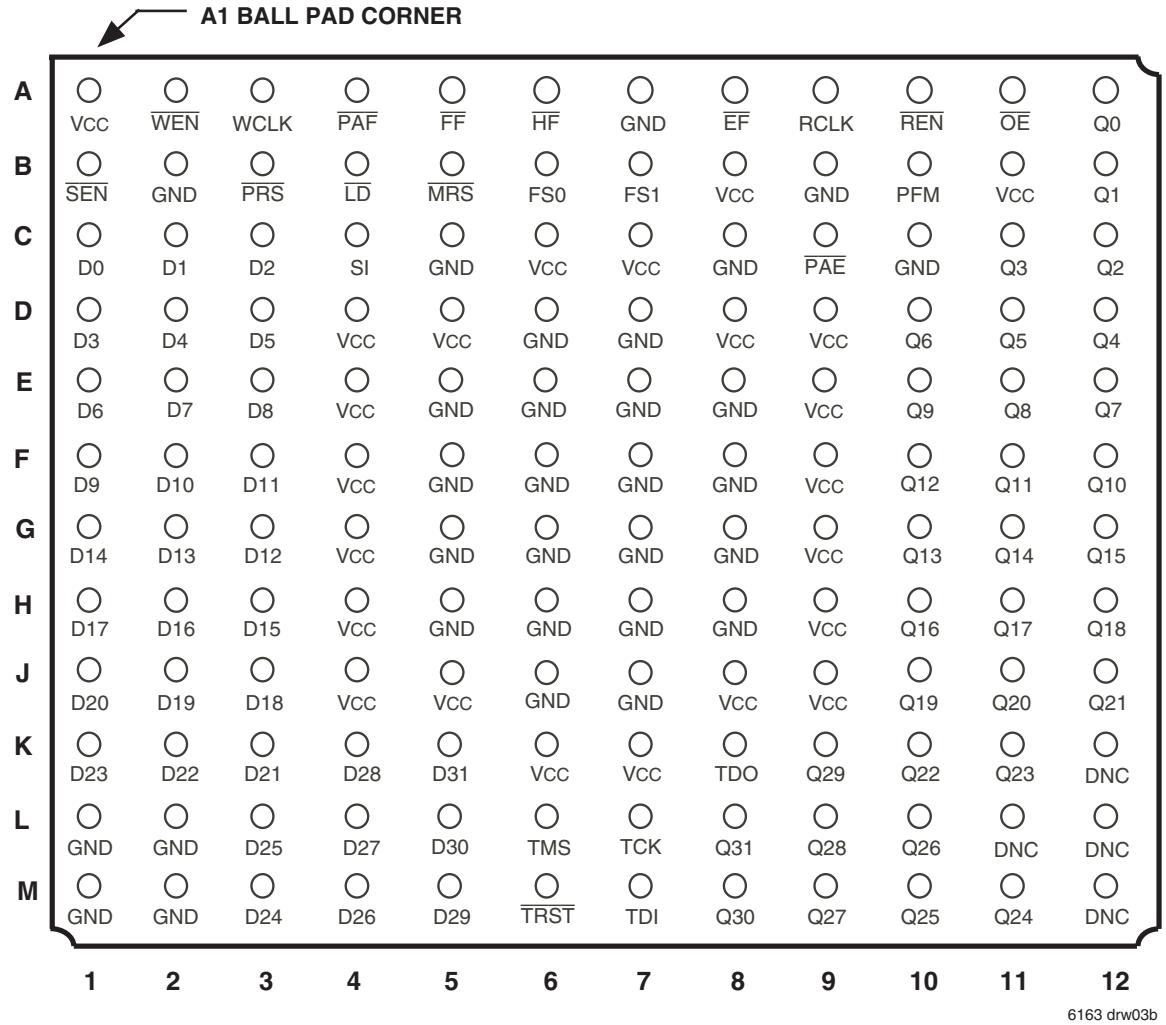
PIN CONFIGURATIONS (32-BIT Vx-III FAMILY)



NOTE:
1. DNC - Do Not Connect.

TQFP: (PK128-1, order code: PF)
TOP VIEW

PIN CONFIGURATIONS-CONTINUED (32-BIT VX-III FAMILY)



6163 drw03b

NOTE:
1. DNC - Do Not Connect.

PBGA: 1mm pitch, 13mm x 13mm (BB144-1, order code: BB)
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
D0–Dn	Data Inputs	I	Data inputs for a 16 or 32-bit bus
$\overline{EF}$	Empty Flag	O	$\overline{EF}$ indicates the FIFO memory is empty. See Table 2.
$\overline{FF}$	Full Flag	O	$\overline{FF}$ indicates the FIFO memory is full. See Table 2.
FSEL0[1]	Flag Select Bit 0	I	During Master Reset, this input along with FSEL1 and the $\overline{LD}$ pin, will select the default offset values for the programmable flags $\overline{PAE}$ and $\overline{PAF}$. There are up to eight possible settings available.
FSEL1[1]	Flag Select Bit 1	I	During Master Reset, this input along with FSEL0 and the $\overline{LD}$ pin will select the default offset values for the programmable flags $\overline{PAE}$ and $\overline{PAF}$. There are up to eight possible settings available.
$\overline{HF}$	Half-Full Flag	O	$\overline{HF}$ indicates the FIFO memory is more than half-full. $\overline{HF}$ is asserted when the number of words written into the FIFO reaches N÷2+1, where N is the total depth of the FIFO. See Table 2.
$\overline{LD}$	Load	I	During Master Reset, the state of the $\overline{LD}$ input along with FSEL0 and FSEL1, determines one of eight default offset values for the $\overline{PAE}$ and $\overline{PAF}$ flags and serial programming mode. After Master Reset, $\overline{LD}$ must be high and should only toggle LOW together with $\overline{SEN}$ to start serial loading of the flag offsets.
$\overline{MRS}$	Master Reset	I	$\overline{MRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Master Reset, the FIFO is configured for one of eight programmable flag default settings, serial programming of the offset settings and synchronous versus asynchronous programmable flag timing modes.
$\overline{OE}$	Output Enable	I	$\overline{OE}$ controls the output line drivers.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	$\overline{PAE}$ goes LOW if the number of words in the FIFO memory is less than offset n, which is stored in the Empty Offset register. $\overline{PAE}$ goes HIGH if the number of words in the FIFO memory is greater than or equal to offset n.
$\overline{PAF}$	Programmable Almost-Full Flag	O	$\overline{PAF}$ goes HIGH if the number of free locations in the FIFO memory is more than offset m, which is stored in the Full Offset register. $\overline{PAF}$ goes LOW if the number of free locations in the FIFO memory is less than or equal to m.
PFM[1]	Programmable Flag Mode	I	During Master Reset, a LOW on PFM will select Asynchronous Programmable flag timing mode. A HIGH on PFM will select Synchronous Programmable flag timing mode.
$\overline{PRS}$	Partial Reset	I	$\overline{PRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Partial Reset, the serial programming method or programmable flag settings are all retained.
Q0–Qn	Data Outputs	O	Data outputs for an 16 or 32-bit bus. Outputs are not 5V tolerant regardless of the state of $\overline{OE}$.
RCLK	Read Clock	I	When enabled by $\overline{REN}$, the rising edge of RCLK reads data from the FIFO memory.
$\overline{REN}$	Read Enable	I	$\overline{REN}$ enables RCLK for reading data from the FIFO memory.
$\overline{SEN}$	Serial Enable	I	$\overline{SEN}$ enables serial loading of programmable flag offsets. $\overline{SEN}$ must be high during Master Reset and should only toggle LOW together with $\overline{LD}$ to start serial loading of the flag offsets.
SI	Serial In	I	At Maser Reset this pin is LOW. After Master Reset, this pin functions as a serial input for loading offset registers.
WCLK	Write Clock	I	Enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the FIFO.
$\overline{WEN}$	Write Enable	I	$\overline{WEN}$ enables WCLK for writing data into the FIFO memory.
VCC	+3.3V Supply	I	These are VCC supply inputs and must be connected to the 3.3V supply rail.
GND	Ground	I	Ground Pins.

NOTE:
1. Inputs should not change state after Master Reset.

Please continue to next page for more Pin descriptions for PBGA package.

PIN DESCRIPTION (32-BIT VX-III PBGA PACKAGE ONLY)

Symbol	Name	I/O	Description
TCK[1]	JTAG Clock	I	Clock input for JTAG function. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data from TMS and TDI are sampled on the rising edge of TCK and outputs change on the falling edge of TCK. If the JTAG function is not used this signal needs to be tied to GND.
TDI[1]	JTAG Test Data Input	I	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded via the TDI on the rising edge of TCK to either the Instruction Register, ID Register and Bypass Register. An internal pull-up resistor forces TDI HIGH if left unconnected.
TDO[1]	JTAG Test Data Output	O	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded output via the TDO on the falling edge of TCK from either the Instruction Register, ID Register and Bypass Register. This output is high impedance except when shifting, while in SHIFT-DR and SHIFT-IR controller states.
TMS[1]	JTAG Mode Select	I	TMS is a serial input pin. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pull-up resistor forces TMS HIGH if left unconnected.
$\overline{TRST}$[1]	JTAG Reset	I	$\overline{TRST}$ is an asynchronous reset pin for the JTAG controller. The JTAG TAP controller does not automatically reset upon power-up, thus it must be reset by either this signal or by setting TMS= HIGH for five TCK cycles. If the TAP controller is not properly reset then the FIFO outputs will always be in high-impedance. If the JTAG function is used but the user does not want to use $\overline{TRST}$, then $\overline{TRST}$ can be tied with $\overline{MRS}$ to ensure proper FIFO operation. If the JTAG function is not used then this signal needs to be tied to GND. An internal pull-up resistor forces $\overline{TRST}$ HIGH if left unconnected.

NOTE:
1. These pins are for the JTAG port. Please refer to pages 15-19 and Figures 2-4.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Industrial	Unit
V_{TERM}[2]	Terminal Voltage with respect to GND	–0.5 to +4.5	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminal only.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}[1]	Supply Voltage Industrial	3.15	3.3	3.45	V
GND	Supply Voltage Industrial	0	0	0	V
V_{IH}[2]	Input High Voltage Industrial	2.0	—	5.5	V
V_{IL}[3]	Input Low Voltage Industrial	—	—	0.8	V
T_A	Operating Temperature Industrial	-40	—	85	°C

NOTES:

1. V_{CC} = 3.3V ± 0.15V, JEDEC JESD8-A compliant.
2. Outputs are not 5V tolerant.
3. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Industrial: V_{CC} = 3.3V ± 0.15V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

		IDT72V15160, IDT72V16160, IDT72V17160, IDT72V18160, IDT72V19160, IDT72V14320 IDT72V15320 IDT72V16320 IDT72V17320 IDT72V18320 IDT72V19320 Industrial t_{CLK} = 10ns		
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
I_{LI}[1]	Input Leakage Current	–1	1	µA
I_{LO}[2]	Output Leakage Current	–10	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	0.4	V
I_{CC1}[3,4,5]	Active Power Supply Current	—	40	mA
I_{CC2}[3,6]	Standby Current	—	15	mA

NOTES:

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested with outputs open (I_{OUT} = 0).
4. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
5. Typical I_{CC1} = 4.2 + 1.4*fs + 0.02*C_L*fs (in mA) with V_{CC} = 3.3V, t_A = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L = capacitive load (in pF).
6. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}[2]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:

1. With output deselected, ($\overline{OE}$ ≥ V_{IH}).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Industrial: V_{CC} = 3.3V ± 0.15V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

		Industrial		
		IDT72V15160L10 IDT72V16160L10 IDT72V17160L10 IDT72V18160L10 IDT72V19160L10	IDT72V14320L10 IDT72V15320L10 IDT72V16320L10 IDT72V17320L10 IDT72V18320L10 IDT72V19320L10	
Symbol	**Parameter**	**Min.**	**Max**	**Unit**
f_S	Clock Cycle Frequency	—	100	Mhz
t_A	Data Access Time	2	6.5	ns
t_{CLK}	Clock Cycle Time	10	—	ns
t_{CLKH}	Clock High Time	4.5	—	ns
t_{CLKL}	Clock Low Time	4.5	—	ns
t_{DS}	Data Setup Time	3.5	—	ns
t_{DH}	Data Hold Time	0.5	—	ns
t_{ENS}	Enable Setup Time	3.5	—	ns
t_{ENH}	Enable Hold Time	0.5	—	ns
t_{LDS}	Load Setup Time	3.5	—	ns
t_{LDH}	Load Hold Time	0.5	—	ns
t_{RS}	Reset Pulse Width[1]	10	—	ns
t_{RSS}	Reset Setup Time	15	—	ns
t_{RSR}	Reset Recovery Time	10	—	ns
t_{RSF}	Reset to Flag and Output Time	—	15	ns
t_{OLZ}	Output Enable to Output in Low Z[2]	0	—	ns
t_{OE}	Output Enable to Output Valid	2	6	ns
t_{OHZ}	Output Enable to Output in High-Z[2]	2	6	ns
t_{WFF}	Write Clock to $\overline{FF}$	—	6.5	ns
t_{REF}	Read Clock to $\overline{EF}$	—	6.5	ns
t_{PAFA}	Clock to Asynchronous Programmable Almost-Full Flag	—	16	ns
t_{PAFS}	Write Clock to Synchronous Programmable Almost-Full Flag	—	6.5	ns
t_{PAEA}	Clock to Asynchronous Programmable Almost-Empty Flag	—	16	ns
t_{PAES}	Read Clock to Synchronous Programmable Almost-Empty Flag	—	6.5	ns
t_{HF}	Clock to $\overline{HF}$	—	16	ns
t_{SKEW1}	Skew time between RCLK and WCLK for $\overline{EF}$ and $\overline{FF}$	7	—	ns
t_{SKEW2}	Skew time between RCLK and WCLK for $\overline{PAE}$ and $\overline{PAF}$	10	—	ns

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns(1)
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load for t_{CLK} = 10ns	See Figure 1

AC TEST LOADS

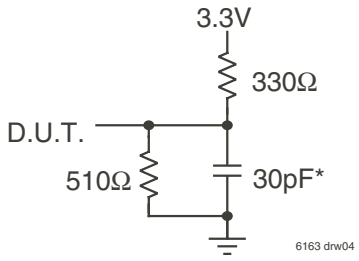
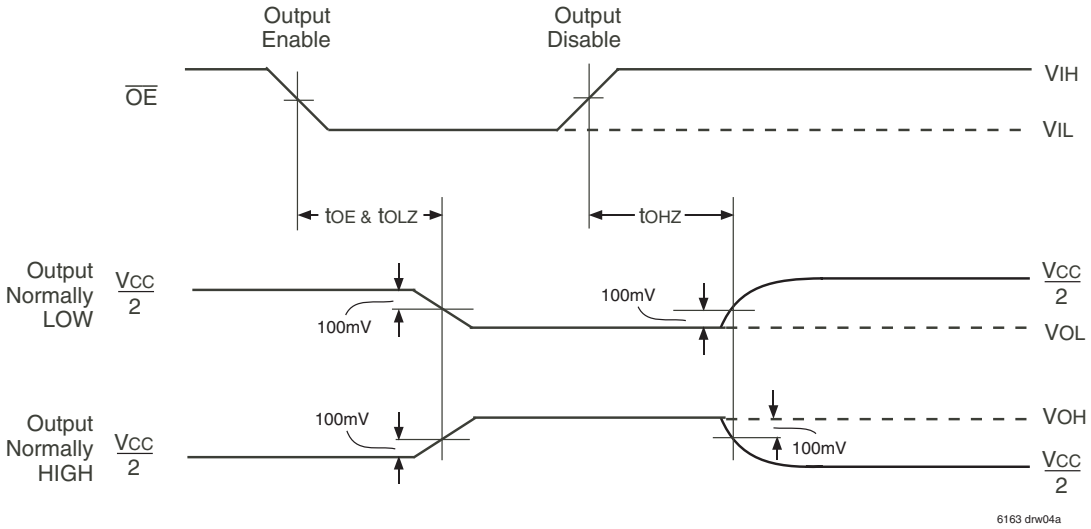


Figure 1. Output Load

* Includes jig and scope capacitances.

OUTPUT ENABLE & DISABLE TIMING



NOTE:
1. $\overline{REN}$ is HIGH.

FUNCTIONAL DESCRIPTION

To write data into to the FIFO, Write Enable ($\overline{WEN}$) must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of the Write Clock (WCLK). After the first write is performed, the Empty Flag ($\overline{EF}$) will go HIGH. Subsequent writes will continue to fill up the FIFO. The Programmable Almost-Empty flag ($\overline{PAE}$) will go HIGH after n + 1 words have been loaded into the FIFO, where "n" is the empty offset value. The default setting for these values are stated in the footnote of Table 1. This parameter is also user programmable.

If one continued to write data into the FIFO, and we assumed no read operations were taking place, the Half-Full flag ($\overline{HF}$) would toggle to LOW once D/2+1 (D= total number of words) was written into the FIFO. Continuing to write data into the FIFO will cause the Programmable Almost-Full flag ($\overline{PAF}$) to go LOW. Again, if no reads are performed, the $\overline{PAF}$ will go LOW after (D-m). The offset "m" is the full offset value. The default setting for these values are stated in the footnote of Table 1. This parameter is also user programmable.

When the FIFO is full, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. If no reads are performed after a reset, $\overline{FF}$ will go LOW after D writes to the FIFO.

If the FIFO is full, the first read operation will cause $\overline{FF}$ to go HIGH. Subsequent read operations will cause $\overline{PAF}$ and $\overline{HF}$ to go HIGH. If further read operations occur, without write operations, $\overline{PAE}$ will go LOW when there are n words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. When the last word has been read from the FIFO, the $\overline{EF}$ will go LOW inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

The $\overline{EF}$ and $\overline{FF}$ outputs are double register-buffered outputs.

PROGRAMMING FLAG OFFSETS

Full and Empty Flag offset values are user programmable. The IDT V-III and Vx-III FIFOs have internal registers for these offsets.

There are two ways to program the flag offset values. Selecting one of the eight pre-set values during master reset or serial programming.

DEFAULT FLAG OFFSETS

There are eight default offset values selectable during Master Reset. These offset values are shown in Table 1.

***Programming offsets with default values* ($\overline{LD}$, $\overline{SEN}$ pins)**: With the $\overline{LD}$ pin together with the FSEL0 and FSEL1 the user has the option to choose one of eight preset values for both offset registers. During master reset the $\overline{LD}$ pin can be either HIGH or LOW depending on the selected value. After Master Reset, $\overline{LD}$ must be high and should not change state. $\overline{SEN}$ should be high during and after Master Reset and should not change state.

SERIAL PROGRAMMING MODE

Offset values can also be programmed into the FIFO by serial loading method. The offset registers may be programmed (and reprogrammed) any time after Master Reset. Valid programming ranges are from 0 to D-1.

***Serial programming of offset values* ($\overline{LD}$,$\overline{SEN}$ pins)**: In order to select serial programming the $\overline{LD}$ pin has to be HIGH during master. Both, $\overline{LD}$ and $\overline{SEN}$ pin have to toggle to LOW in order to initial the serial programming. $\overline{LD}$ should be high during normal FIFO operation.

If Serial Programming mode has been selected then programming of $\overline{PAE}$ and $\overline{PAF}$ values can be achieved by using a combination of the $\overline{LD}$, $\overline{SEN}$, WCLK and SI input pins. Programming $\overline{PAE}$ and $\overline{PAF}$ proceeds as follows: when $\overline{LD}$ and $\overline{SEN}$ are set LOW, data on the SI input are written, one bit for each WCLK rising edge, starting with the Empty Offset LSB and ending with the Full Offset MSB.

TABLE 1 — DEFAULT PROGRAMMABLE FLAG OFFSETS

IDT72V14320, 72V15360			
$\overline{LD}$	FSEL1	FSEL0	Offsets n,m
L	H	L	511
L	L	H	255
L	L	L	127
L	H	H	63
H	L	L	31
H	H	L	15
H	L	H	7
H	H	H	3
IDT72V16320, 72V17320, 72V18320, 72V19320 IDT72V15160, 72V16160, 72V17160, 72V18160			
$\overline{LD}$	FSEL1	FSEL0	Offsets n,m
H	L	L	1,023
L	H	L	511
L	L	H	255
L	L	L	127
L	H	H	63
H	H	L	31
H	L	H	15
H	H	H	7
IDT72V19160			
$\overline{LD}$	FSEL1	FSEL0	Offsets n,m
H	L	L	1,023
L	H	L	8,191
L	L	H	16,383
L	L	L	127
L	H	H	4,095
H	H	L	511
H	L	H	2,047
H	H	H	255
All Devices			
$\overline{LD}$	FSEL1	FSEL0	Program Mode
H	X	X	Serial[3]

NOTES:
1. n = empty offset for $\overline{PAE}$.
2. m = full offset for $\overline{PAF}$.
3. As well as selecting serial programming mode, one of the default values will also be loaded depending on the state of FSEL0 & FSEL1.

A total of
20 bits for the IDT72V14320
22 bits for the IDT72V15320
24 bits for the IDT72V15160, IDT72V16320
26 bits for the IDT72V16160, IDT72V17320
28 bits for the IDT72V17160, IDT72V18320
30 bits for the IDT72V18160, IDT72V19320
32 bits for the IDT72V19160
has to be loaded serial for the two ($\overline{PAF}$, $\overline{PAE}$) registers.

TABLE 2 — STATUS FLAGS FOR IDT STANDARD MODE

			IDT72V15160						
	IDT72V14320	IDT72V15320	IDT72V16320	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
Number of Words in FIFO	0	0	0	H	H	H	L	L
	1 to n[1]	1 to n[1]	1 to n[1]	H	H	H	L	H
	(n+1) to 512	(n+1) to 1,024	(n+1) to 2,048	H	H	H	H	H
	513 to (1,024-(m+1))	1,025 to (2,048-(m+1))	2,049 to (4,096-(m+1))	H	H	L	H	H
	(1,024-m) to 1,023	(2,048-m) to 2,047	(4,096m) to 4,095	H	L	L	H	H
	1,024	2,048	4,096	L	L	L	H	H

	IDT72V16160	IDT72V17160	IDT72V18160	IDT72V19160					
	IDT72V17320	IDT72V18320	IDT72V19320		$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
Number of Words in FIFO	0	0	0	0	H	H	H	L	L
	1 to n[1]	1 to n[1]	1 to n[1]	1 to n[1]	H	H	H	L	H
	(n+1) to 4,096	(n+1) to 8,192	(n+1) to 16,384	(n+1) to 32,768	H	H	H	H	H
	4,097 to (8,192-(m+1))	8,193 to (16,384-(m+1))	16,385 to (32,768-(m+1))	32,769 to (65,536-(m+1))	H	H	L	H	H
	(8,192-m) to 8,191	(16,384-m) to 16,383	(32,768-m) to 32,767	(65,536-m) to 65,535	H	L	L	H	H
	8,192	16,384	32,768	65,536	L	L	L	H	H

6163 drw05

NOTE:
1. See Table 1 for values for n, m.

TABLE 3 — FLAG OFFSET PROGRAMMING, STATE OF $\overline{LD}$ AND $\overline{SEN}$ AFTER MASTER RESET

$\overline{LD}$	$\overline{WEN}$	$\overline{REN}$	$\overline{SEN}$	WCLK	RCLK	Operation
0	1	1	0		X	Serial Flag Programming 1 bit for each rising WCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB)
1	0	X	X		X	Write Memory
1	X	0	X	X		Read Memory
X	1	1	1	X	X	No Operation
1	1	1	X	X	X	No Operation
0	0	1	1		X	Invalid Operation
0	1	0	1	X		Invalid Operation

6163 drw06

Using the serial method, individual registers cannot be programmed selectively. $\overline{PAE}$ and $\overline{PAF}$ can show a valid status only after the complete set of bits (for all offset registers) has been entered. The registers can be reprogrammed as long as the complete set of new offset bits is entered. When $\overline{LD}$ is LOW and $\overline{SEN}$ is HIGH, no serial write to the registers can occur.

Write operations to the FIFO are allowed before and during the serial programming sequence. In this case, the programming of all offset bits does not have to occur at once. A select number of bits can be written to the SI input and then, by bringing $\overline{LD}$ and $\overline{SEN}$ HIGH, data can be written to FIFO memory via D_n by toggling $\overline{WEN}$. When $\overline{WEN}$ is brought HIGH with $\overline{LD}$ and $\overline{SEN}$ restored to a LOW, the next offset bit in sequence is written to the registers via SI. If an interruption of serial programming is desired, it is sufficient either to set $\overline{LD}$ LOW and deactivate $\overline{SEN}$ or to set $\overline{SEN}$ LOW and deactivate $\overline{LD}$. Once $\overline{LD}$ and $\overline{SEN}$ are both restored to a LOW level, serial offset programming continues.

From the time serial programming has begun, neither programmable flag will be valid until the full set of bits required to fill all the offset registers has been written. Measuring from the rising WCLK edge that achieves the above criteria; $\overline{PAF}$ will be valid after two more rising WCLK edges plus t_{PAF}, $\overline{PAE}$ will be valid after the next two rising RCLK edges plus t_{PAE} plus t_{SKEW2}.

Refer also to $\overline{LD}$ Signal description for more information on flag offset programming and state requirements for $\overline{LD}$ and $\overline{SEN}$ pins

SYNCHRONOUS vs ASYNCHRONOUS PROGRAMMABLE FLAG TIMING SELECTION

The IDT V-III and Vx-III can be configured during the Master Reset cycle with either synchronous or asynchronous timing for $\overline{PAF}$ and $\overline{PAE}$ flags by use of the PFM pin.

If synchronous $\overline{PAF}$/$\overline{PAE}$ configuration is selected (PFM, HIGH during $\overline{MRS}$), the PAF is asserted and updated on the rising edge of WCLK only and not RCLK. Similarly, $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only and not WCLK.

If asynchronous $\overline{PAF}$/$\overline{PAE}$ configuration is selected (PFM, LOW during $\overline{MRS}$), the PAF is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of RCLK. Similarly, $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of WCLK.

SIGNAL DESCRIPTION

INPUTS:

DATA IN (D_0 - D_n)

Data inputs for 16 or 32-bit wide data.

CONTROLS:

MASTER RESET ($\overline{MRS}$)

A Master Reset is accomplished whenever the $\overline{MRS}$ input is taken to a LOW state. This operation sets the internal read and write pointers to the first location of the RAM array. $\overline{PAE}$ will go LOW, $\overline{PAF}$ will go HIGH, $\overline{HF}$ will go HIGH, $\overline{EF}$ will go LOW and $\overline{FF}$ will go HIGH.

SI is supposed to be LOW during master reset.

PFM control settings are defined during the Master Reset cycle.

During a Master Reset, the output register is initialized to all zeroes. A Master Reset is required after power up, before a write operation can take place. $\overline{MRS}$ is asynchronous.

PARTIAL RESET ($\overline{PRS}$)

A Partial Reset is accomplished whenever the $\overline{PRS}$ input is taken to a LOW state. As in the case of the Master Reset, the internal read and write pointers are set to the first location of the RAM array, $\overline{PAE}$ goes LOW, $\overline{PAF}$ goes HIGH, $\overline{HF}$ goes HIGH, $\overline{FF}$ will go HIGH and $\overline{EF}$ will go LOW. The output register is initialized to all zeroes. $\overline{PRS}$ is asynchronous.

A Partial Reset is useful for resetting the device during the course of operation, when reprogramming programmable flag offset settings may not be convenient.

SERIAL IN (SI)

At the time of Master Reset, SI must be LOW.

After Master Reset, SI acts as a serial input for loading $\overline{PAE}$ and $\overline{PAF}$ offsets into the programmable registers.

WRITE CLOCK (WCLK)

A write cycle is initiated on the rising edge of the WCLK input. Data setup and hold times must be met with respect to the LOW-to-HIGH transition of the WCLK. It is permissible to stop the WCLK. Note that while WCLK is idle, the $\overline{FF}$, $\overline{PAF}$ and $\overline{HF}$ flags will not be updated. (Note that WCLK is only capable of updating $\overline{HF}$ flag to LOW). The Write and Read Clocks can either be independent or coincident.

WRITE ENABLE ($\overline{WEN}$)

When the $\overline{WEN}$ input is LOW, data may be loaded into the FIFO array on the rising edge of every WCLK cycle if the device is not full. Data is stored in the FIFO array sequentially and independently of any ongoing read operation.

When $\overline{WEN}$ is HIGH, no new data is written in the FIFO array on each WCLK cycle.

To prevent data overflow, $\overline{FF}$ will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{FF}$ will go HIGH allowing a write to occur. The $\overline{FF}$ is updated by two WCLK cycles + t_{SKEW} after the RCLK cycle.

$\overline{WEN}$ is ignored when the FIFO is full.

READ CLOCK (RCLK)

A read cycle is initiated on the rising edge of the RCLK input. Data can be read on the outputs, on the rising edge of the RCLK input. It is permissible to stop the RCLK. Note that while RCLK is idle, the $\overline{EF}$, $\overline{PAE}$ and $\overline{HF}$ flags will not be updated. (Note that RCLK is only capable of updating the $\overline{HF}$ flag to HIGH). The Write and Read Clocks can be independent or coincident.

The $\overline{OE}$ input is used to provide Asynchronous control of the three-state Qn outputs.

READ ENABLE ($\overline{REN}$)

When Read Enable is LOW, data is loaded from the FIFO array into the output register on the rising edge of every RCLK cycle if the device is not empty.

When the $\overline{REN}$ input is HIGH, the output register holds the previous data and no new data is loaded into the output register. The data outputs Q_0-Q_n maintain the previous data value.

Every word accessed at Q_n, including the first word written to an empty FIFO, must be requested using $\overline{REN}$. When the last word has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. Once a write is performed, $\overline{EF}$ will go HIGH allowing a read to occur. The $\overline{EF}$ flag is updated by two RCLK cycles + t_{SKEW} after the valid WCLK cycle.

SERIAL ENABLE ($\overline{SEN}$)

The $\overline{SEN}$ input is an enable used only for serial programming of the offset registers. The serial programming method must be selected during Master Reset. $\overline{SEN}$ is always used in conjunction with $\overline{LD}$. When these lines are both LOW, data at the SI input can be loaded into the program register one bit for each LOW-to-HIGH transition of WCLK.

When $\overline{SEN}$ is HIGH, the programmable registers retains the previous settings and no offsets are loaded. $\overline{SEN}$ functions the same way in both IDT.

Refer to LOAD ($\overline{LD}$) pin and section "Programming Flag Offsets" for more information on offset programming.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable is enabled (LOW), the parallel output buffers receive data from the output register. When $\overline{OE}$ is HIGH, the output data bus (Q_n) goes into a high impedance state.

LOAD ($\overline{LD}$)

This is a dual purpose pin. During Master Reset, the state of the $\overline{LD}$ input, along with FSEL0 and FSEL1, determines one of eight default offset values for the $\overline{PAE}$ and $\overline{PAF}$ flags, along with the serial programming option for these offset registers (see Table 3).

After Master Reset, the $\overline{LD}$ pin is used in conjunction with the $\overline{SEN}$ pin to activate the programming process of the flag offset values $\overline{PAE}$ and $\overline{PAF}$. Pulling $\overline{LD}$ LOW will begin a serial loading of these offset values.

Depending on the default or serial programming option the state of $\overline{LD}$ and $\overline{SEN}$ have to be considered before and after master reset. Refer also to section "Programming Flag Offsets" for more information on offset programming.

Programming offsets with default values: With the $\overline{LD}$ pin together with the FSEL0 and FSEL1 the user has the option to choose one of eight preset values for both offset registers. During master reset the $\overline{LD}$ pin can be either HIGH or LOW depending on the selected value. After Master Reset, $\overline{LD}$ must be high and should not change state. $\overline{SEN}$ should be high during and after Master Reset and should not change state.

Serial programming of offset values: In order to select serial programming the $\overline{LD}$ pin has to be HIGH during master. Both, $\overline{LD}$ and $\overline{SEN}$ pin have to toggle to LOW in order to initial the serial programming. $\overline{LD}$ should be high during normal FIFO operation.

PROGRAMMABLE FLAG MODE (PFM)

During Master Reset, a LOW on PFM will select Asynchronous Programmable flag timing mode. A HIGH on PFM will select Synchronous Programmable flag timing mode. If asynchronous $\overline{PAF}$/$\overline{PAE}$ configuration is selected (PFM,

LOW during $\overline{MRS}$), the $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of WCLK. Similarly, the $\overline{PAF}$ is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of RCLK.

If synchronous $\overline{PAE}$/$\overline{PAF}$ configuration is selected (PFM, HIGH during MRS) , the $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only and not WCLK. Similarly, $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only and not RCLK. The mode desired is configured during master reset by the state of the Programmable Flag Mode (PFM) pin.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

When the FIFO is full, $\overline{FF}$ will go LOW, inhibiting further write operations. When $\overline{FF}$ is HIGH, the FIFO is not full. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), $\overline{FF}$ will go LOW after D writes to the FIFO (D = total number of words).

$\overline{FF}$ is synchronous and updated on the rising edge of WCLK. $\overline{FF}$ is a double register-buffered output.

EMPTY FLAG ($\overline{EF}$)

When the FIFO is empty, $\overline{EF}$ will go LOW, inhibiting further read operations. When $\overline{EF}$ is HIGH, the FIFO is not empty.

$\overline{EF}$ is synchronous and updated on the rising edge of RCLK. $\overline{EF}$ is a double register-buffered output.

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full flag ($\overline{PAF}$) will go LOW when the FIFO reaches the almost-full condition. If no reads are performed after reset ($\overline{MRS}$), $\overline{PAF}$ will go LOW after (D - m) words are written to the FIFO. (D=total number of words, m = full offset value). The default setting for this value is stated in the footnote of Table 1.

If asynchronous $\overline{PAF}$ configuration is selected, the $\overline{PAF}$ is asserted LOW on the LOW-to-HIGH transition of the Write Clock (WCLK). $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of the Read Clock (RCLK). If synchronous $\overline{PAF}$ configuration is selected, the $\overline{PAF}$ is updated on the rising edge of WCLK.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost-Empty flag ($\overline{PAE}$) will go LOW when the FIFO reaches the almost-empty condition. $\overline{PAE}$ will go LOW when there are n words or less in the FIFO. The offset "n" is the empty offset value. The default setting for this value is stated in the footnote of Table 1.

If asynchronous $\overline{PAE}$ configuration is selected, the $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of the Read Clock (RCLK). $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of the Write Clock (WCLK). If synchronous $\overline{PAE}$ configuration is selected, the $\overline{PAE}$ is updated on the rising edge of RCLK.

HALF-FULL FLAG ($\overline{HF}$)

This output indicates a half-full FIFO. The rising WCLK edge that fills the FIFO beyond half-full sets $\overline{HF}$ LOW. The flag remains LOW until the difference between the write and read pointers becomes less than or equal to half of the total depth of the device; the rising RCLK edge that accomplishes this condition sets $\overline{HF}$ HIGH.

If no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{HF}$ will go LOW after (D/2 + 1) writes to the FIFO, where D = total number of words available in the FIFO.

Because $\overline{HF}$ is updated by both RCLK and WCLK, it is considered asynchronous.

DATA OUTPUTS (Q_0-Q_n)

(Q_0-Qn) are data outputs for 16-bit or 32-bit wide data.

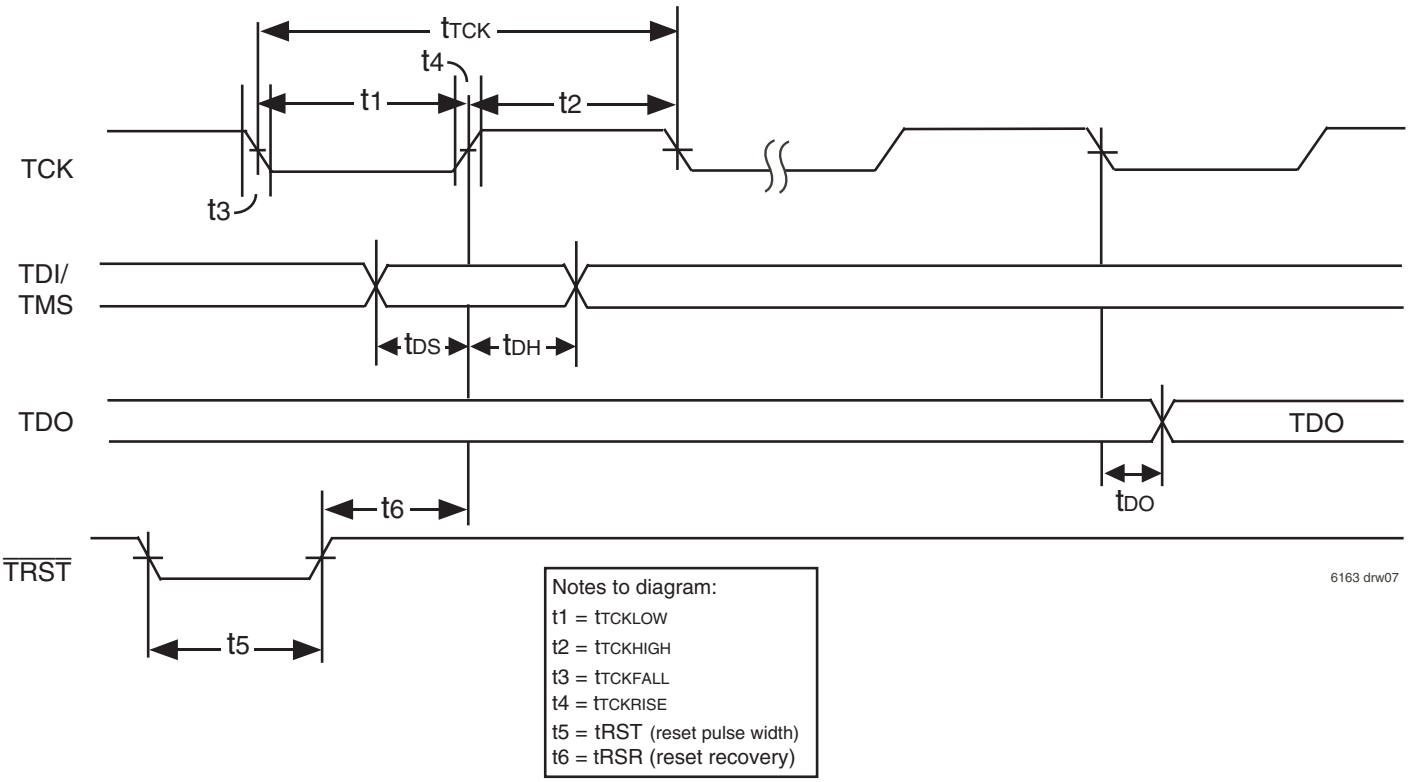


Figure 2. Standard JTAG Timing

SYSTEM INTERFACE PARAMETERS

Parameter	Symbol	Test Conditions	IDT72V14320 IDT72V15320 IDT72V16320 IDT72V17320 IDT72V18320 IDT72V19320		
			Min.	Max.	Units
Data Output	t_{DO}[1]		-	20	ns
Data Output Hold	t_{DOH}[1]		0	-	ns
Data Input	t_{DS}	trise=3ns	10	-	ns
	t_{DH}	tfall=3ns	10	-	

NOTE:
1. 50pf loading on external output signals.

JTAG AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ± 5%; Tcase = 0°C to +85°C)

Parameter	Symbol	Test Conditions			
			Min.	Max.	Units
JTAG Clock Input Period	t_{TCK}	-	100	-	ns
JTAG Clock HIGH	$t_{TCKHIGH}$	-	40	-	ns
JTAG Clock Low	t_{TCKLOW}	-	40	-	ns
JTAG Clock Rise Time	$t_{TCKRISE}$	-	-	5[1]	ns
JTAG Clock Fall Time	$t_{TCKFALL}$	-	-	5[1]	ns
JTAG Reset	t_{RST}	-	50	-	ns
JTAG Reset Recovery	t_{RSR}	-	50	-	ns

NOTE:
1. Guaranteed by design.

JTAG INTERFACE

Five additional pins (TDI, TDO, TMS, TCK and $\overline{TRST}$) are provided to support the JTAG boundary scan interface. The IDT72V14320/72V15320/72V16320/72V17320/72V18320/72V19320 incorporates the necessary tap controller and modified pad cells to implement the JTAG facility.

Note that IDT provides appropriate Boundary Scan Description Language program files for these devices.

The Standard JTAG interface consists of four basic elements:

- *Test Access Port (TAP)*
- *TAP controller*
- *Instruction Register (IR)*
- *Data Register Port (DR)*

The following sections provide a brief description of each element. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

The Figure below shows the standard Boundary-Scan Architecture

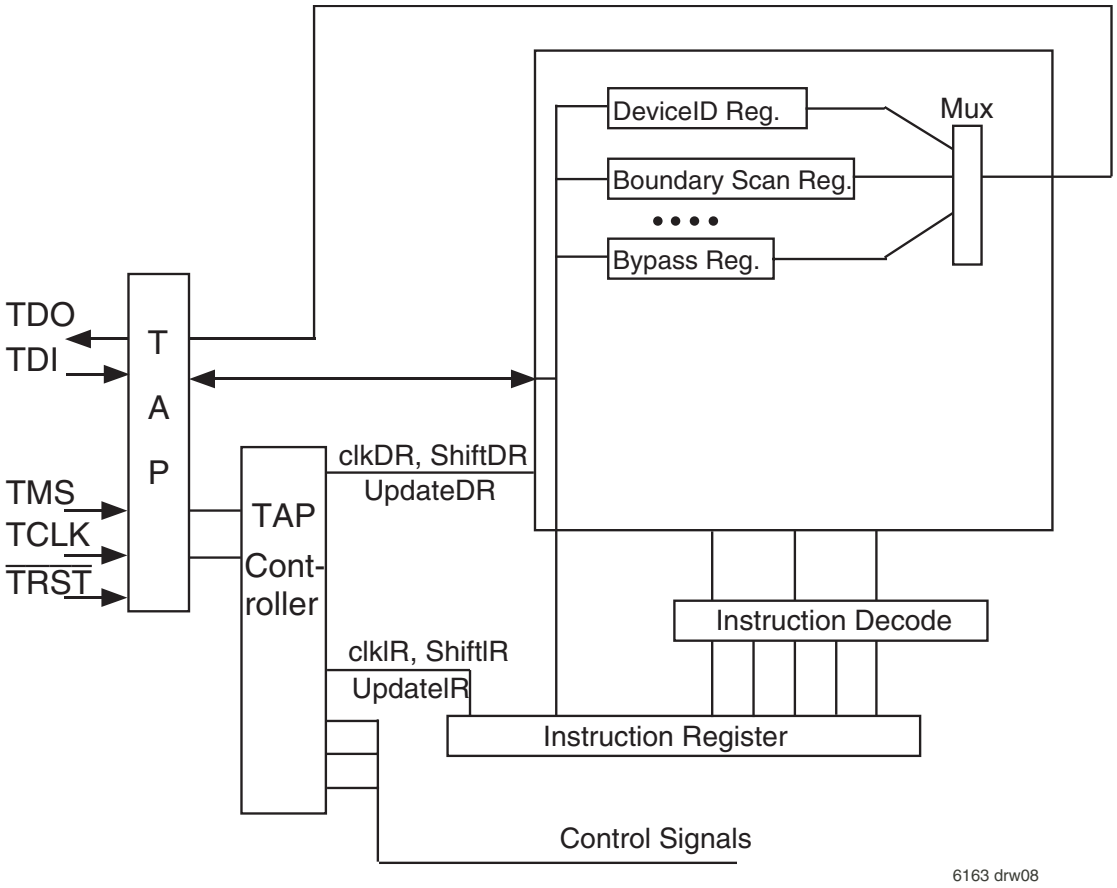


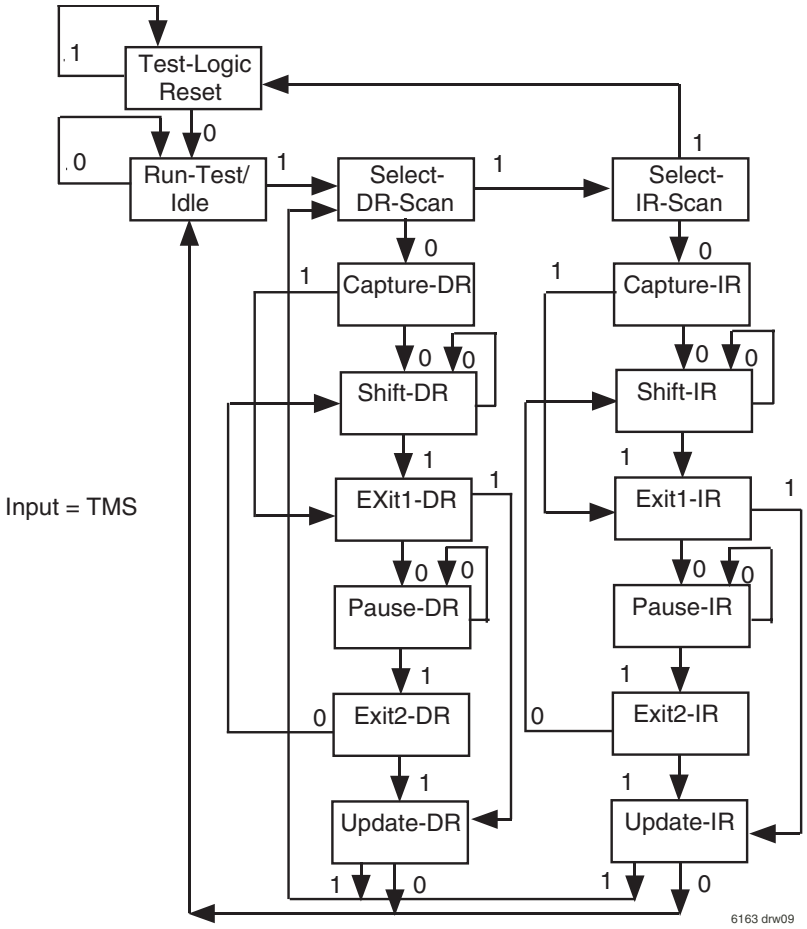
Figure 3. Boundary Scan Architecture

TEST ACCESS PORT (TAP)

The Tap interface is a general-purpose port that provides access to the internal of the processor. It consists of four input ports (TCLK, TMS, TDI, $\overline{TRST}$) and one output port (TDO).

THE TAP CONTROLLER

The Tap controller is a synchronous finite state machine that responds to TMS and TCLK signals to generate clock and control signals to the Instruction and Data Registers for capture and update of data.



NOTES:
1. Five consecutive TCK cycles with TMS = 1 will reset the TAP.
2. TAP controller does not automatically reset upon power-up. The user must provide a reset to the TAP controller (either by $\overline{TRST}$ or TMS).
3. TAP controller must be reset before normal FIFO operations can begin.

Figure 4. TAP Controller State Diagram

Refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1) for the full state diagram

All state transitions within the TAP controller occur at the rising edge of the TCLK pulse. The TMS signal level (0 or 1) determines the state progression that occurs on each TCLK rising edge. The TAP controller takes precedence over the FIFO memory and must be reset after power up of the device. See $\overline{TRST}$ description for more details on TAP controller reset.

Test-Logic-Reset All test logic is disabled in this controller state enabling the normal operation of the IC. The TAP controller state machine is designed in such a way that, no matter what the initial state of the controller is, the Test-Logic-Reset state can be entered by holding TMS at high and pulsing TCK five times. This is the reason why the Test Reset ($\overline{TRST}$) pin is optional.

Run-Test-Idle In this controller state, the test logic in the IC is active only if certain instructions are present. For example, if an instruction activates the self test, then it will be executed when the controller enters this state. The test logic in the IC is idles otherwise.

Select-DR-Scan This is a controller state where the decision to enter the Data Path or the Select-IR-Scan state is made.

Select-IR-Scan This is a controller state where the decision to enter the Instruction Path is made. The Controller can return to the Test-Logic-Reset state other wise.

Capture-IR In this controller state, the shift register bank in the Instruction Register parallel loads a pattern of fixed values on the rising edge of TCK. The last two significant bits are always required to be “01”.

Shift-IR In this controller state, the instruction register gets connected between TDI and TDO, and the captured pattern gets shifted on each rising edge of TCK. The instruction available on the TDI pin is also shifted in to the instruction register.

Exit1-IR This is a controller state where a decision to enter either the Pause-IR state or Update-IR state is made.

Pause-IR This state is provided in order to allow the shifting of instruction register to be temporarily halted.

Exit2-DR This is a controller state where a decision to enter either the Shift-IR state or Update-IR state is made.

Update-IR In this controller state, the instruction in the instruction register is latched in to the latch bank of the Instruction Register on every falling edge of TCK. This instruction also becomes the current instruction once it is latched.

Capture-DR In this controller state, the data is parallel loaded in to the data registers selected by the current instruction on the rising edge of TCK.

Shift-DR, Exit1-DR, Pause-DR, Exit2-DR and Update-DR These controller states are similar to the Shift-IR, Exit1-IR, Pause-IR, Exit2-IR and Update-IR states in the Instruction path.

THE INSTRUCTION REGISTER

The Instruction register allows an instruction to be shifted in serially into the processor at the rising edge of TCLK.

The Instruction is used to select the test to be performed, or the test data register to be accessed, or both. The instruction shifted into the register is latched at the completion of the shifting process when the TAP controller is at Update-IR state.

The instruction register must contain 4 bit instruction register-based cells which can hold instruction data. These mandatory cells are located nearest the serial outputs they are the least significant bits.

TEST DATA REGISTER

The Test Data register contains three test data registers: the Bypass, the Boundary Scan register and Device ID register.

These registers are connected in parallel between a common serial input and a common serial data output.

The following sections provide a brief description of each element. For a complete description, refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

TEST BYPASS REGISTER

The register is used to allow test data to flow through the device from TDI to TDO. It contains a single stage shift register for a minimum length in serial path. When the bypass register is selected by an instruction, the shift register stage is set to a logic zero on the rising edge of TCLK when the TAP controller is in the Capture-DR state.

The operation of the bypass register should not have any effect on the operation of the device in response to the BYPASS instruction.

THE BOUNDARY-SCAN REGISTER

The Boundary Scan Register allows serial data TDI be loaded in to or read out of the processor input/output ports. The Boundary Scan Register is a part of the IEEE 1149.1-1990 Standard JTAG Implementation.

THE DEVICE IDENTIFICATION REGISTER

The Device Identification Register is a Read Only 32-bit register used to specify the manufacturer, part number and version of the processor to be determined through the TAP in response to the IDCODE instruction.

IDT JEDEC ID number is 0xB3. This translates to 0x33 when the parity is dropped in the 11-bit Manufacturer ID field.

For the IDT72V14320/72V15320/72V16320/72V17320/72V18320/72V19320, the Part Number field contains the following values:

Device	Part# Field
IDT72V14320	04E5
IDT72V15320	04E4
IDT72V16320	04E3
IDT72V17320	04E2
IDT72V18320	04E1
IDT72V19320	04E0

31(MSB) 28	27 12	11 1	0(LSB)
Version (4 bits) 0X0	Part Number (16-bit)	Manufacturer ID (11-bit) 0X33	1

IDT72V14320/15320/16320/17320/18320/19320 JTAG Device Identification Register

JTAG INSTRUCTION REGISTER

The Instruction register allows instruction to be serially input into the device when the TAP controller is in the Shift-IR state. The instruction is decoded to perform the following:

- Select test data registers that may operate while the instruction is current. The other test data registers should not interfere with chip operation and the selected data register.
- Define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

The Instruction Register is a 4 bit field (i.e. IR3, IR2, IR1, IR0) to decode 16 different possible instructions. Instructions are decoded as follows.

Hex Value	Instruction	Function
0x00	EXTEST	Select Boundary Scan Register
0x02	IDCODE	Select Chip Identification data register
0x01	SAMPLE/PRELOAD	Select Boundary Scan Register
0x03	HIGH-IMPEDANCE	JTAG
0x0F	BYPASS	Select Bypass Register

JTAG Instruction Register Decoding

The following sections provide a brief description of each instruction. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

EXTEST

The required EXTEST instruction places the IC into an external boundary-test mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register is accessed to drive test data off-chip via the boundary outputs and receive test data off-chip via the boundary inputs. As such, the EXTEST instruction is the workhorse of IEEE. Std 1149.1, providing for probe-less testing of solder-joint opens/shorts and of logic cluster function.

IIDCODE

The optional IDCODE instruction allows the IC to remain in its functional mode and selects the optional device identification register to be connected between TDI and TDO. The device identification register is a 32-bit shift register containing information regarding the IC manufacturer, device type, and version code. Accessing the device identification register does not interfere with the operation of the IC. Also, access to the device identification register should be immediately available, via a TAP data-scan operation, after power-up of the IC or after the TAP has been reset using the optional $\overline{\text{TRST}}$ pin or by otherwise moving to the Test-Logic-Reset state.

SAMPLE/PRELOAD

The required SAMPLE/PRELOAD instruction allows the IC to remain in a normal functional mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register can be accessed via a date scan operation, to take a sample of the functional data entering and leaving the IC. This instruction is also used to preload test data into the boundary-scan register before loading an EXTEST instruction.

HIGH-IMPEDANCE

The optional High-Impedance instruction sets all outputs (including two-state as well as three-state types) of an IC to a disabled (high-impedance) state and selects the one-bit bypass register to be connected between TDI and TDO. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the IC outputs.

BYPASS

The required BYPASS instruction allows the IC to remain in a normal functional mode and selects the one-bit bypass register to be connected between TDI and TDO. The BYPASS instruction allows serial data to be transferred through the IC from TDI to TDO without affecting the operation of the IC.

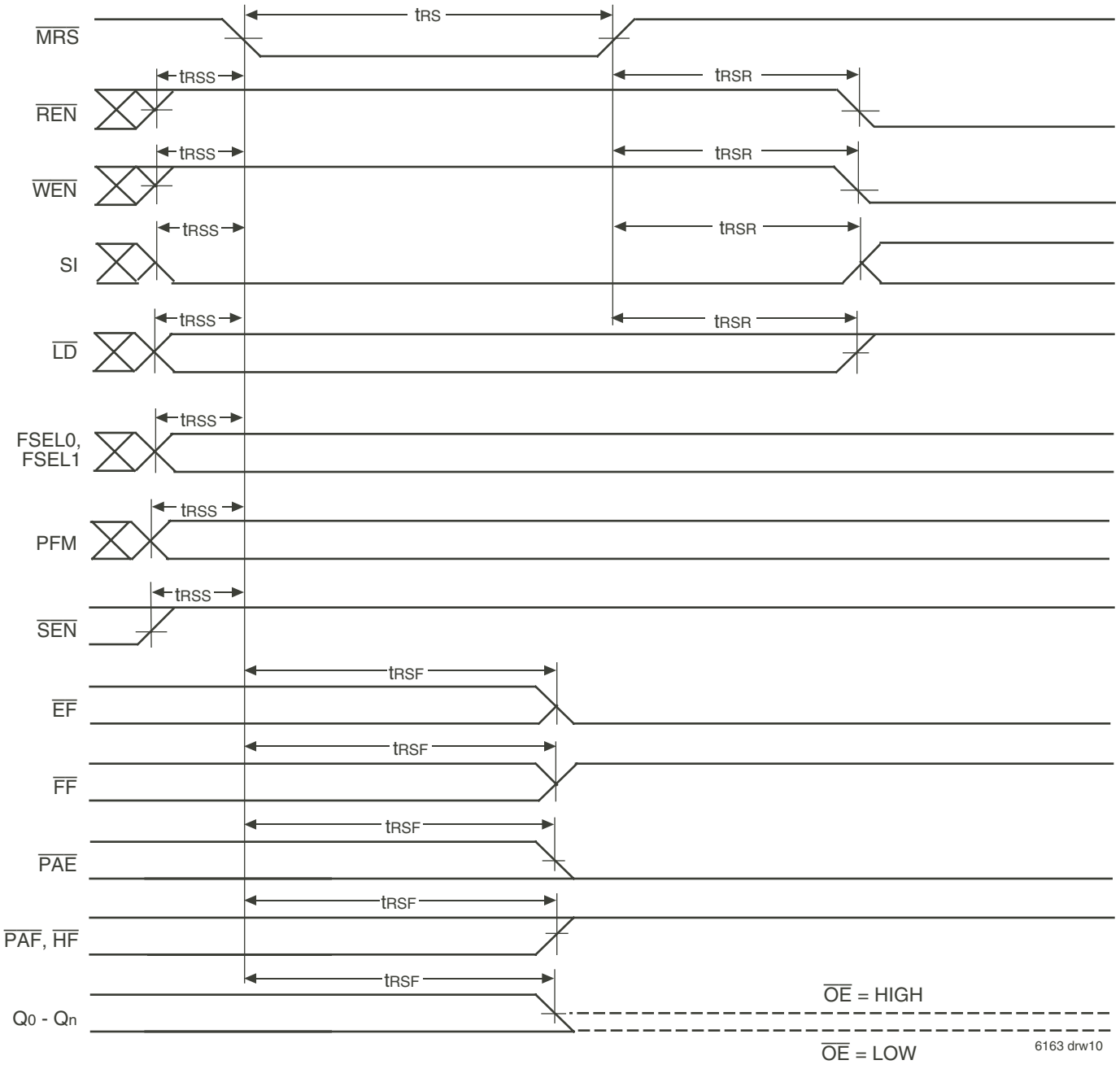


Figure 5. Master Reset Timing

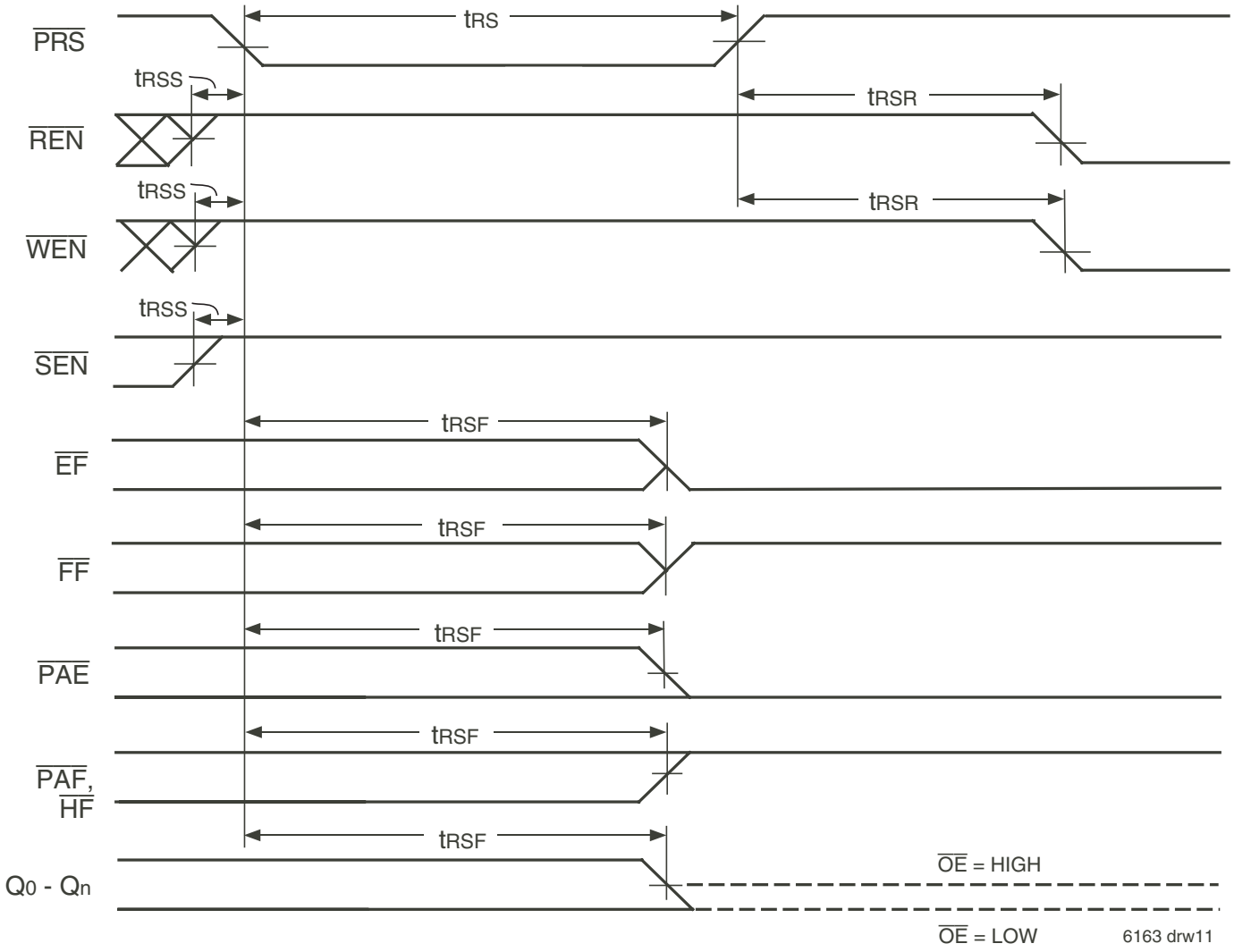
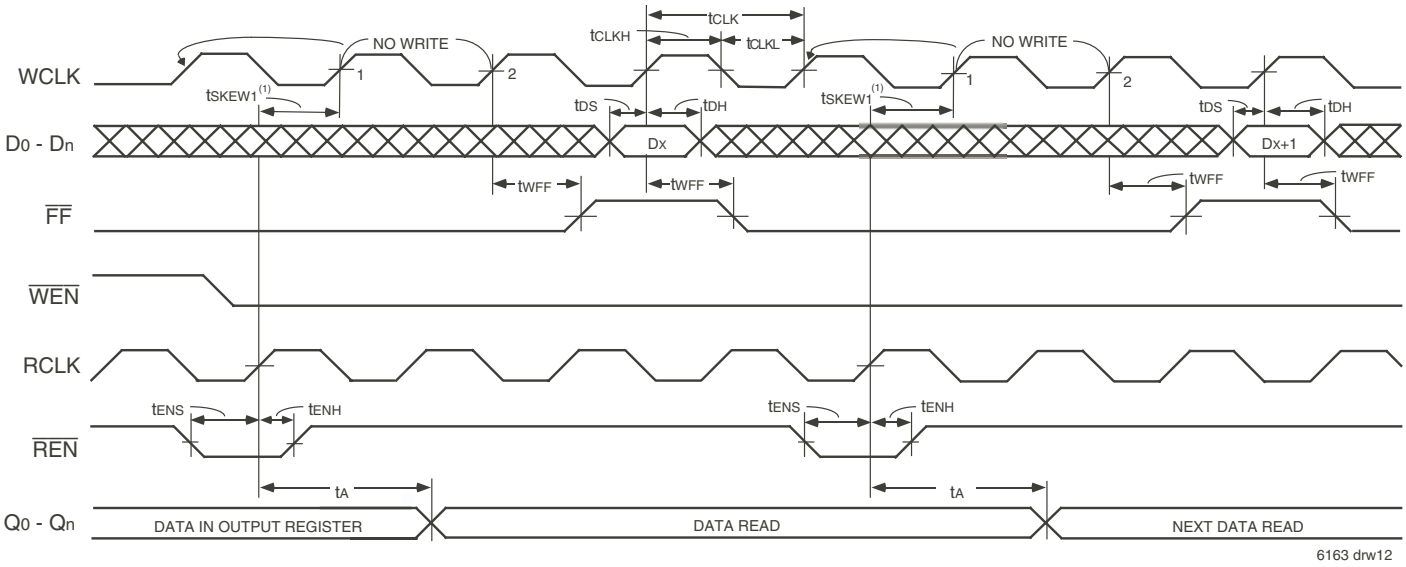
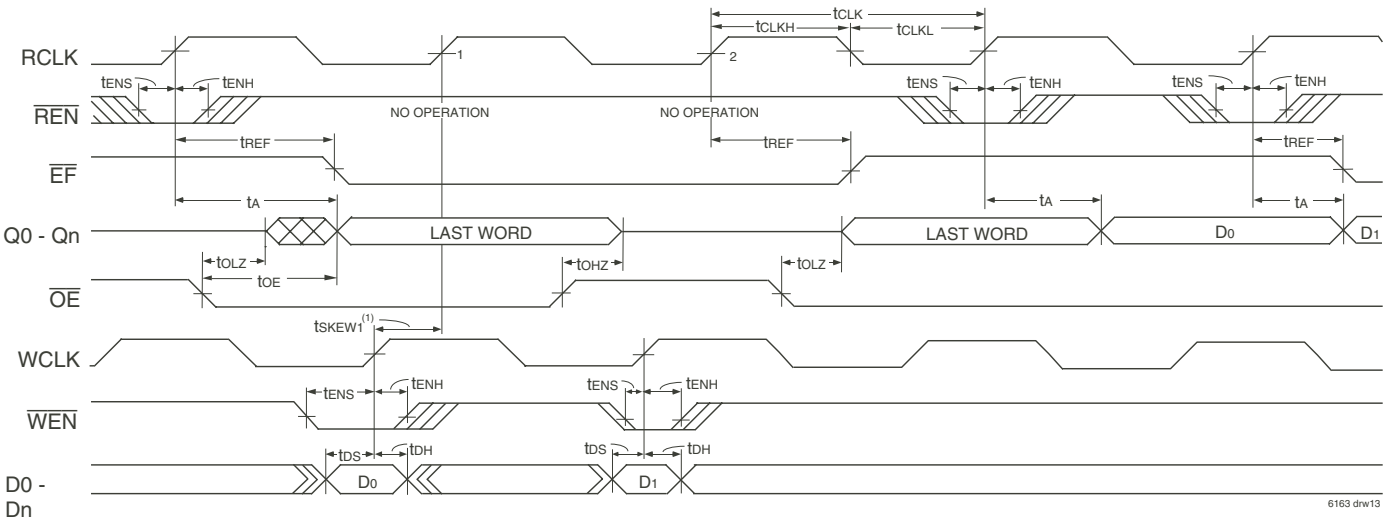


Figure 6. Partial Reset Timing



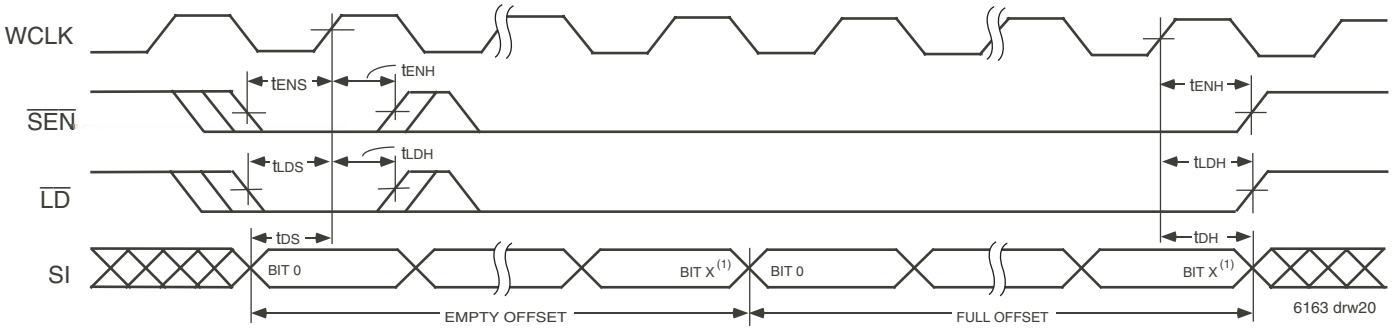
NOTES:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH (after one WCLK cycle pus t_{WFF}). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than t_{SKEW1}, then the $\overline{FF}$ deassertion may be delayed one extra WCLK cycle.
2. $\overline{LD}$ = HIGH, $\overline{OE}$ = LOW, $\overline{EF}$ = HIGH

Figure 7. Write Cycle and Full Flag Timing



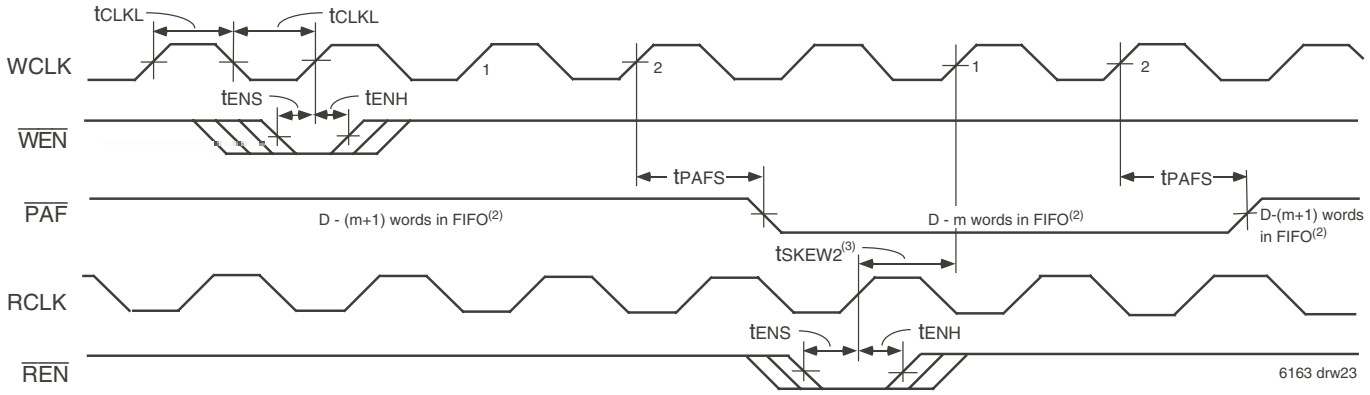
NOTES:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH (after one RCLK cycle plus t_{REF}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ deassertion may be delayed one extra RCLK cycle.
2. $\overline{LD}$ = HIGH.
3. First data word latency = $t_{SKEW1} + 1*T_{RCLK} + t_{REF}$.

Figure 8. Read Cycle, Empty Flag and First Data Word Latency Timing



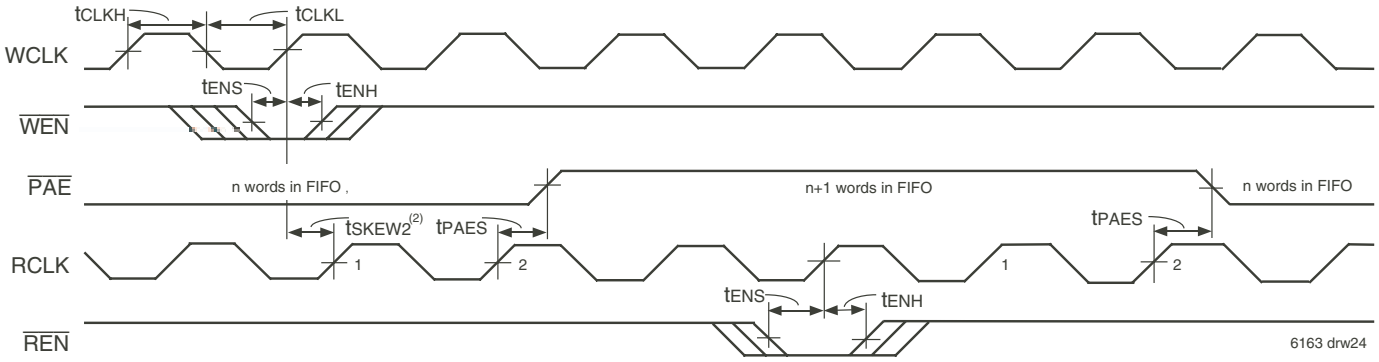
NOTE:
1. X = 9 for the IDT72V14320 (total of 20 bits), X = 10 for the IDT72V15320 (total of 22 bits), X = 11 for the IDT72V15160 and IDT72V16320 (total of 24 bits), X = 12 for the IDT72V16160, and IDT72V17320 (total of 26 bits), X = 13 for the IDT72V17160 and IDT72V18320 (total of 28 bits), X = 14 for the IDT72V18160 and IDT72V19320 (total of 30 bits), X = 15 for the IDT72V19160 (total of 32 bits).

Figure 9. Serial Loading of Programmable Flag Registers



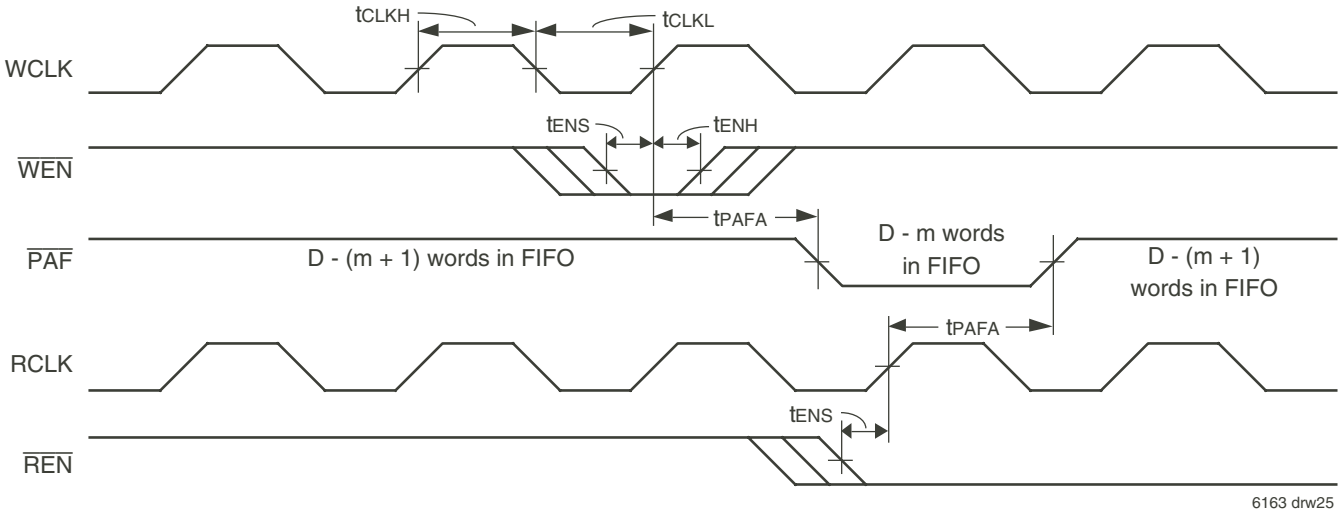
NOTES:
1. m = $\overline{PAF}$ offset.
2. D = maximum FIFO depth.
   V-III: D = 4,096 for the IDT72V15160 and 8,192 for the IDT72V16160, 16,384 for the IDT72V17160 and 32,768 for the IDT72V18160, 65,526 for the IDT72V19160.
   Vx-III: D = 1,024 for the IDT72V14320, 2,048 for the IDT72V15320, 4,096 for the IDT72V16320 and 8,192 for the IDT72V17320, 16,384 for the IDT72V18320 and 32,768 for the IDT72V19320.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{PAF}$ will go HIGH (after one WCLK cycle plus t_{PAFS}). If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then the $\overline{PAF}$ deassertion time may be delayed one extra WCLK cycle.
4. $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only.
5. Select this mode by setting PFM HIGH during Master Reset.

Figure 10. Synchronous Programmable Almost-Full Flag Timing



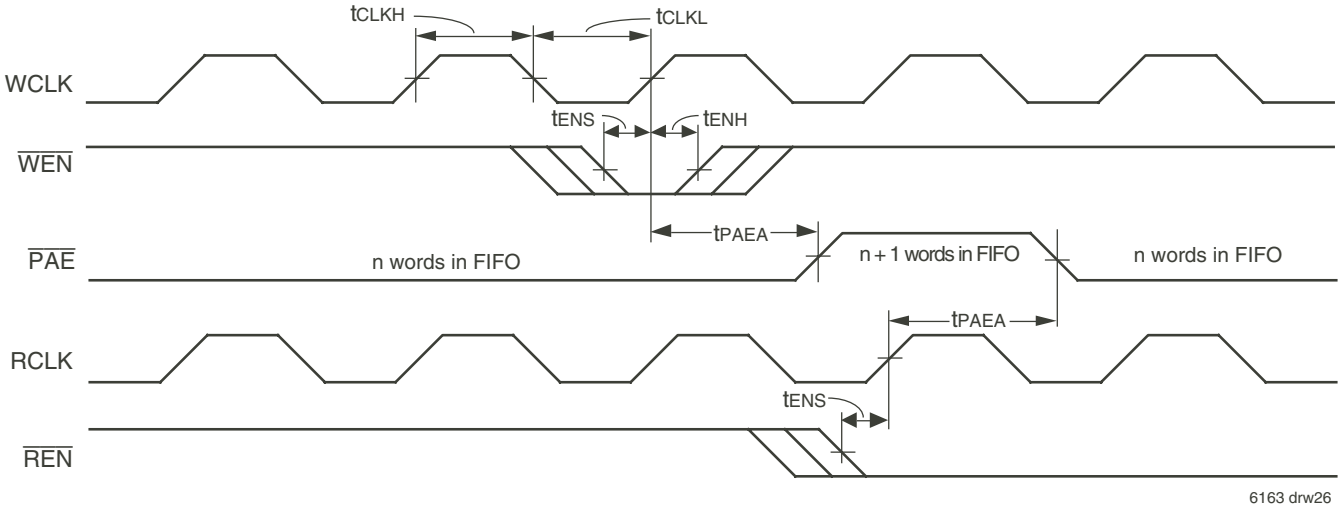
NOTES:
1. n = $\overline{PAE}$ offset.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{PAE}$ will go HIGH (after one RCLK cycle plus t_{PAES}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.
3. $\overline{PAE}$ is asserted and updated on the rising edge of WCLK only.
4. Select this mode by setting PFM HIGH during Master Reset.

Figure 11. Synchronous Programmable Almost-Empty Flag Timing



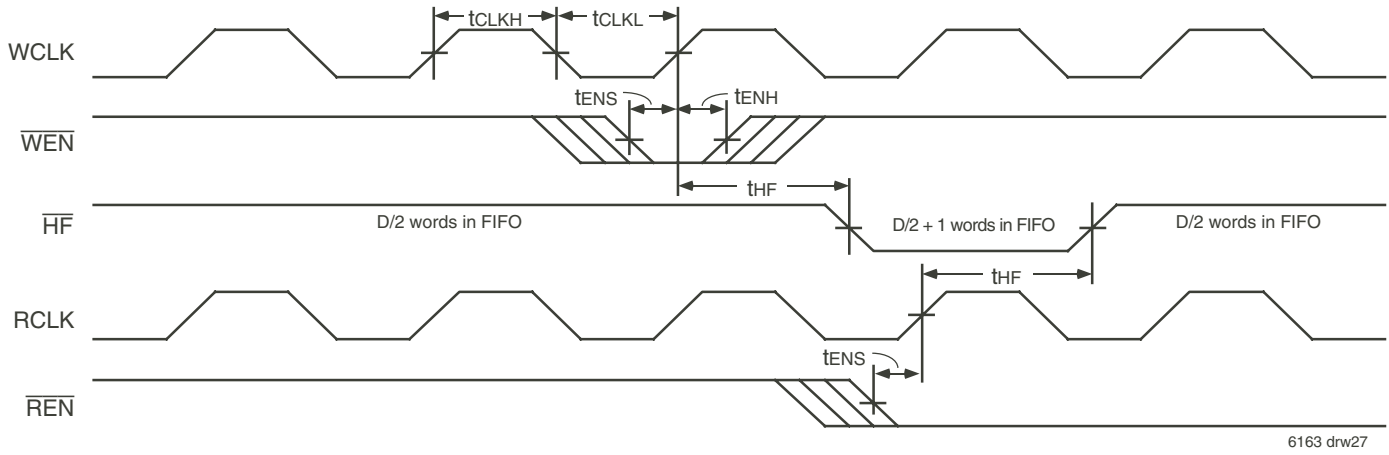
NOTES:
1. m = $\overline{PAF}$ offset.
2. D = maximum FIFO depth.
   V-III: D = 4,096 for the IDT72V15160 and 8,192 for the IDT72V16160, 16,384 for the IDT72V17160 and 32,768 for the IDT72V18160, 65,526 for the IDT72V19160.
   Vx-III: D = 1,024 for the IDT72V14320, 2,048 for the IDT72V15320, 4,096 for the IDT72V16320 and 8,192 for the IDT72V17320, 16,384 for the IDT72V18320 and 32,768 for the IDT72V19320.
3. $\overline{PAF}$ is asserted to LOW on WCLK transition and reset to HIGH on RCLK transition.
4. Select this mode by setting PFM LOW during Master Reset.

Figure 12. Asynchronous Programmable Almost-Full Flag Timing



NOTES:
1. n = $\overline{PAE}$ offset.
2. $\overline{PAE}$ is asserted LOW on RCLK transition and reset to HIGH on WCLK transition.
3. Select this mode by setting PFM LOW during Master Reset.

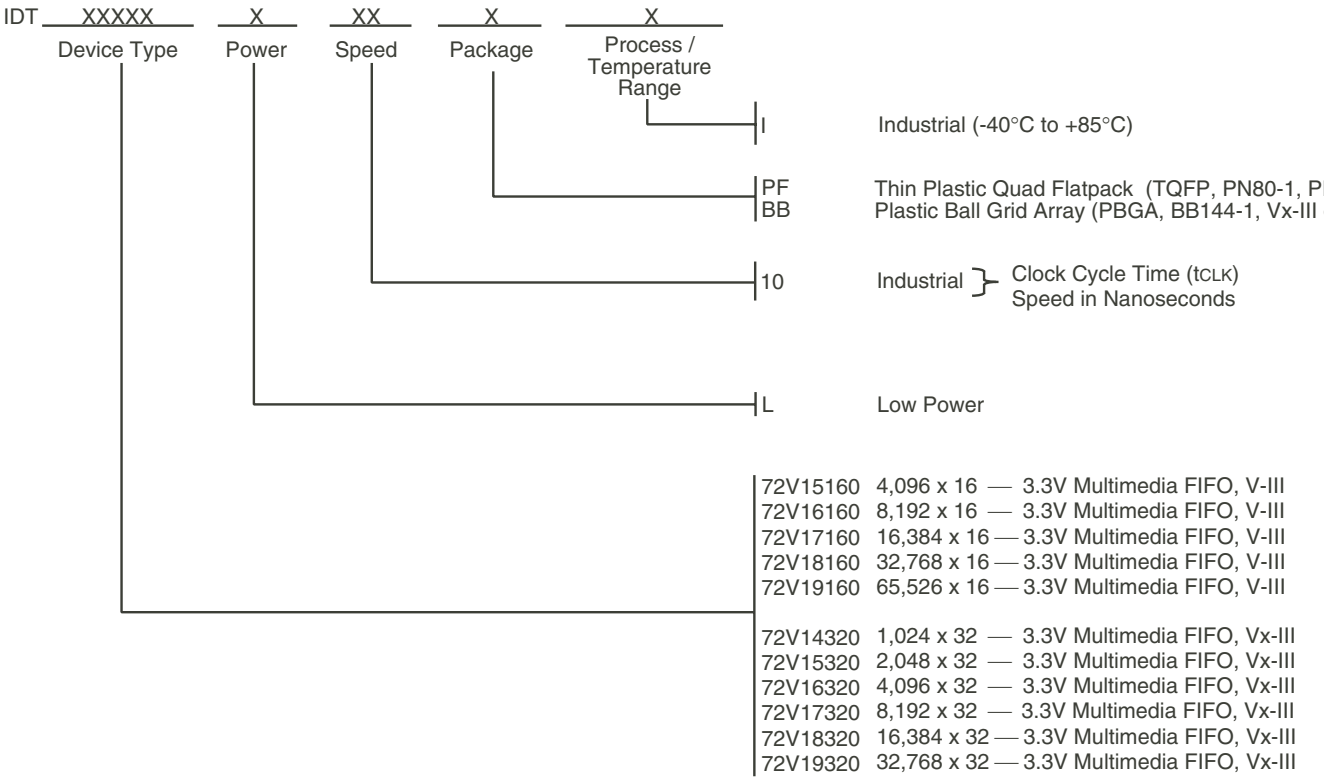
Figure 13. Asynchronous Programmable Almost-Empty Flag Timing



NOTES:
1. D = maximum FIFO depth.
   V-III: D = 4,096 for the IDT72V15160 and 8,192 for the IDT72V16160, 16,384 for the IDT72V17160 and 32,768 for the IDT72V18160, 65,526 for the IDT72V19160.
   Vx-III: D = 1,024 for the IDT72V14320, 2,048 for the IDT72V15320, 4,096 for the IDT72V16320 and 8,192 for the IDT72V17320, 16,384 for the IDT72V18320 and 32,768 for the IDT72V19320.

Figure 14. Half-Full Flag Timing

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

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www.idt.com

for Tech Support:
408-330-1753
email: FIFOhelp@idt.com

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

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- *Приемлемые сроки поставки, возможна ускоренная поставка.*
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- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

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- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
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