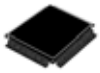
**Freescale Semiconductor**
Data Sheet: Advance Information

Document Number: MPC5646C
Rev.6, 02/2014

# MPC5646C

256 MAPBGA
(17 mm x 17 mm)

208-pin LQFP
(28 mm x 28 mm)


176-pin LQFP
(24 mm x 24 mm)

# MPC5646C
## Microcontroller Data Sheet

On-chip modules available within the family include the following features:

- e200z4d dual issue, 32-bit core Power Architecture® compliant CPU
  - — Up to 120 MHz
  - — 4 KB, 2/4-Way Set Associative Instruction Cache
  - — Variable length encoding (VLE)
  - — Embedded floating-point (FPU) unit
  - — Supports Nexus3+
- e200z0h single issue, 32-bit core Power Architecture compliant CPU
  - — Up to 80 MHz
  - — Variable length encoding (VLE)
  - — Supports Nexus3+
- Up to 3 MB on-chip flash memory: flash page buffers to improve access time
- Up to 256 KB on-chip SRAM
- 64 KB on-chip data flash memory to support EEPROM emulation
- Up to 16 semaphores across all slave ports
- User selectable MBIST
- Low-power modes supported: STOP, HALT, STANDBY
- 16 region Memory Protection Unit (MPU)
- Dual-core Interrupt Controller (INTC). Interrupt sources can be routed to e200z4d, e200z0h, or both.
- Crossbar switch architecture for concurrent access to peripherals, flash memory, and SRAM from multiple bus masters
- 32 channel eDMA controller with DMAMUX
- Timer supports input/output channels providing 16-bit input capture, output compare, and PWM functions (eMIOS)
- 2 analog-to-digital converters (ADC): one 10-bit and one 12-bit
- Cross Trigger Unit (CTU) to enable synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
- Up to 8 serial peripheral interface (DSPI) modules
- Up to 10 serial communication interface (LINFlex) modules
- Up to 6 full CAN (FlexCAN) modules with 64 MBs each
- CAN Sampler to catch ID of CAN message
- 1 inter IC communication interface ($I^2C$) module
- Up to 177 (LQFP) or 199 (BGA) configurable general purpose I/O pins
- 1 System Timer Module (STM) with four 32-bit compare channels
- Up to 8 periodic interrupt timers (PIT) with 32-bit counter resolution

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

© Freescale Semiconductor, Inc., 2009-2014. All rights reserved.

# Table of Contents


Introduction . . . . 4
1.1 Document Overview . . . . 4
1.2 Description . . . . 4
2 Block diagram . . . . 7
3 Package pinouts and signal descriptions . . . . 10
3.1 Pad types . . . . 13
3.2 System pins . . . . 14
3.3 Functional ports . . . . 14
4 Electrical Characteristics . . . . 41
4.1 Parameter classification . . . . 41
4.2 NVUSRO register . . . . 41
4.2.1 NVUSRO [PAD3V5V(0)] field description . . . . 42
4.2.2 NVUSRO [PAD3V5V(1)] field description . . . . 42
4.3 Absolute maximum ratings . . . . 42
4.4 Recommended operating conditions . . . . 44
4.5 Thermal characteristics . . . . 47
4.5.1 Package thermal characteristics . . . . 47
4.5.2 Power considerations . . . . 48
4.6 I/O pad electrical characteristics . . . . 48
4.6.1 I/O pad types . . . . 48
4.6.2 I/O input DC characteristics . . . . 49
4.6.3 I/O output DC characteristics . . . . 50
4.6.4 Output pin transition times . . . . 52
4.6.5 I/O pad current specification . . . . 53
4.7 RESET electrical characteristics . . . . 55
4.8 Power management electrical characteristics . . . . 57
4.8.1 Voltage regulator electrical characteristics . . . . 57
4.8.2 VDD_BV options . . . . 59
4.8.3 Voltage monitor electrical characteristics . . . . 60
4.9 Low voltage domain power consumption . . . . 61
4.10 Flash memory electrical characteristics . . . . 63
4.10.1 Program/Erase characteristics . . . . 63
4.10.2 Flash memory power supply DC characteristics 65
4.10.3 Flash memory start-up/switch-off timings . . . . 66
4.11 Electromagnetic compatibility (EMC) characteristics . . 66
4.11.1 Designing hardened software to avoid noise problems . . . . 66
4.11.2 Electromagnetic interference (EMI) . . . . 67
4.11.3 Absolute maximum ratings (electrical sensitivity) 67
4.12 Fast external crystal oscillator (4–40 MHz) electrical characteristics . . . . 68
4.13 Slow external crystal oscillator (32 kHz) electrical characteristics . . . . 71
4.14 FMPLL electrical characteristics . . . . 73
4.15 Fast internal RC oscillator (16 MHz) electrical characteristics . . . . 74
4.16 Slow internal RC oscillator (128 kHz) electrical characteristics . . . . 75
4.17 ADC electrical characteristics . . . . 76
4.17.1 Introduction . . . . 76
4.18 Fast Ethernet Controller . . . . 87
4.18.1 MII Receive Signal Timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK) . . . . 87
4.18.2 MII Transmit Signal Timing (TXD[3:0], TX_EN, TX_ER, TX_CLK) . . . . 87
4.18.3 MII Async Inputs Signal Timing (CRS and COL) 88
4.18.4 MII Serial Management Channel Timing (MDIO and MDC) 89
4.19 On-chip peripherals . . . . 91
4.19.1 Current consumption . . . . 91
4.19.2 DSPI characteristics . . . . 93
4.19.3 Nexus characteristics . . . . 101
4.19.4 JTAG characteristics . . . . 103
5 Package characteristics . . . . 105
5.1 Package mechanical data . . . . 105
5.1.1 176 LQFP package mechanical drawing . . . . 105
5.1.2 208 LQFP package mechanical drawing . . . . 108
5.1.3 256 MAPBGA package mechanical drawing . 113
6 Ordering information . . . . 115
7 Revision history . . . . 116

### Other Features

- System clocks sources
  - 4–40 MHz external crystal oscillator
  - 16 MHz internal RC oscillator
  - FMPLL
  - Additionally, there are two low power oscillators: 128 kHz internal RC oscillator, 32 kHz external crystal oscillator
- Real Time Counter (RTC) with clock source from internal 128 kHz or 16 MHz oscillators or external 4–40 MHz crystal
  - Supports autonomous wake-up with 1 ms resolution with max timeout of 2 seconds
  - Optional support from external 32 kHz crystal oscillator, supporting wake-up with 1 second resolution and max timeout of 1 hour
- 1 Real Time Interrupt (RTI) with 32-bit counter resolution
- 1 Safety Enhanced Software Watchdog Timer (SWT) that supports keyed functionality
- 1 dual-channel FlexRay Controller with 128 message buffers
- 1 Fast Ethernet Controller (FEC)
- On-chip voltage regulator (VREG)
- Cryptographic Services Engine (CSE)
- Offered in the following standard package types:
  - 176-pin LQFP, 24 × 24 mm, 0.5 mm Lead Pitch
  - 208-pin LQFP, 28 × 28 mm, 0.5 mm Lead Pitch
  - 256-ball MAPBGA, 17 × 17mm, 1.0 mm Lead Pitch

# 1 Introduction

## 1.1 Document Overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the MPC5646C device. To ensure a complete understanding of the device functionality, refer also to the MPC5646C Reference Manual.

## 1.2 Description

The MPC5646C is a new family of next generation microcontrollers built on the Power Architecture embedded category. This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device.

The MPC5646C family expands the range of the MPC560xB microcontroller family. It provides the scalability needed to implement platform approaches and delivers the performance required by increasingly sophisticated software architectures. The advanced and cost-efficient host processor core of the MPC5646C automotive controller family complies with the Power Architecture embedded category, which is 100 percent user-mode compatible with the original Power Architecture user instruction set architecture (UISA). It operates at speeds of up to 120 MHz and offers high performance processing optimized for low power consumption. It also capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

**Table 1. MPC5646C family comparison[1]**

| Feature | MPC5644B | | MPC5644C | | | MPC5645B | | MPC5645C | | | MPC5646B | | MPC5646C | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Package | 176 LQFP | 208 LQFP | 176 LQFP | 208 LQFP | 256 BGA | 176 LQFP | 208 LQFP | 176 LQFP | 208 LQFP | 256 BGA | 176 LQFP | 208 LQFP | 176 LQFP | 208 LQFP | 256 BGA |
| CPU | e200z4d | | e200z4d + e200z0h | | | e200z4d | | e200z4d + e200z0h | | | e200z4d | | e200z4d + e200z0h | | |
| Execution speed[2] | Up to 120 MHz (e200z4d) | | Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3] | | | Up to 120 MHz (e200z4d) | | Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3] | | | Up to 120 MHz (e200z4d) | | Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3] | | |
| Code flash memory | 1.5 MB | | | | | 2 MB | | | | | 3 MB | | | | |
| Data flash memory | 4 x16 KB | | | | | | | | | | | | | | |
| SRAM | 128 KB | | 192 KB | | | 160 KB | | 256 KB | | | 192 KB | | 256 KB | | |
| MPU | 16-entry | | | | | | | | | | | | | | |
| eDMA[4] | 32 ch | | | | | | | | | | | | | | |
| 10-bit ADC | | | | | | | | | | | | | | | |
| dedicated[5,6] | 27 ch | 33 ch | 27 ch | 33 ch | | 27 ch | 33 ch | 27 ch | 33 ch | | 27 ch | 33 ch | 27 ch | 33 ch | |
| shared with 12-bit ADC[7] | 19 ch | | | | | | | | | | | | | | |
| 12-bit ADC | | | | | | | | | | | | | | | |
| dedicated[8] | 5 ch | 10 ch | 5 ch | 10 ch | | 5 ch | 10 ch | 5 ch | 10 ch | | 5 ch | 10 ch | 5 ch | 10 ch | |
| shared with 10-bit ADC[7] | 19 ch | | | | | | | | | | | | | | |
| CTU | 64 ch | | | | | | | | | | | | | | |
| Total timer I/O[9] eMIOS | 64 ch, 16-bit | | | | | | | | | | | | | | |
| SCI (LINFlexD) | 10 | | | | | | | | | | | | | | |
| SPI (DSPI) | 8 | | | | | | | | | | | | | | |
| CAN (FlexCAN)[10] | 6 | | | | | | | | | | | | | | |
| FlexRay | Yes | | | | | | | | | | | | | | |
| STCU[11] | Yes | | | | | | | | | | | | | | |

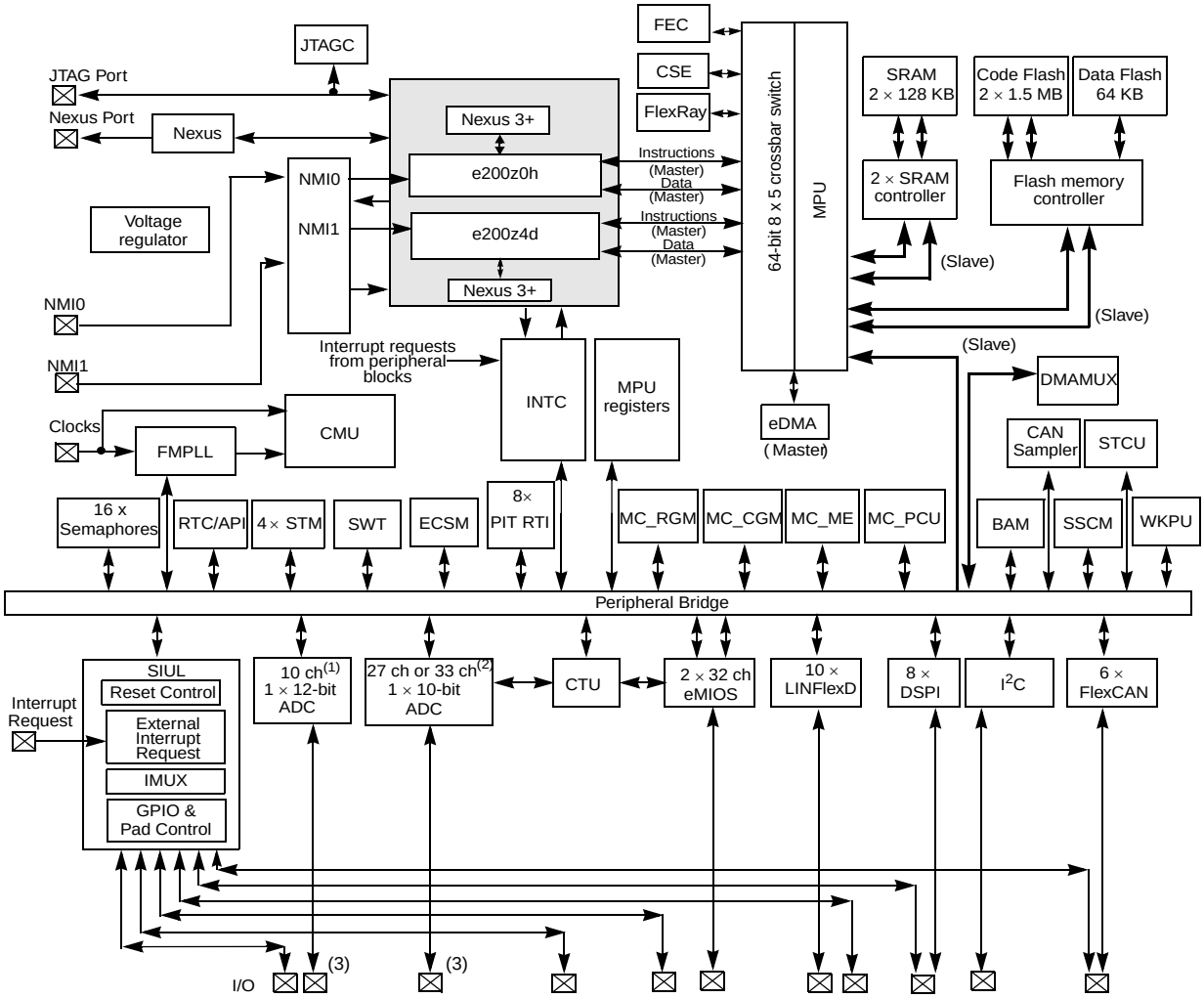
**Table 1. MPC5646C family comparison[1] (continued)**

| Feature | MPC5644B | | MPC5644C | | | MPC5645B | | MPC5645C | | | MPC5646B | | MPC5646C | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Package | 176 LQFP | 208 LQFP | 176 LQFP | 208 LQFP | 256 BGA | 176 LQFP | 208 LQFP | 176 LQFP | 208 LQFP | 256 BGA | 176 LQFP | 208 LQFP | 176 LQFP | 208 LQFP | 256 BGA |
| Ethernet | No | | Yes | | | No | | Yes | | | No | | Yes | | |
| $I^2C$ | 1 | | | | | | | | | | | | | | |
| 32 kHz oscillator (SXOSC) | Yes | | | | | | | | | | | | | | |
| GPIO[12] | 147 | 177 | 147 | 177 | 199 | 147 | 177 | 147 | 177 | 199 | 147 | 177 | 147 | 177 | 199 |
| Debug | JTAG | | | | Nexus 3+ | JTAG | | | | Nexus 3+ | JTAG | | | | Nexus 3+ |
| Cryptographic Services Engine (CSE) | Optional | | | | | | | | | | | | | | |

NOTES:
1 Feature set dependent on selected peripheral multiplexing; table shows example.
2 Based on 125 °C ambient operating temperature and subject to full device characterisation.
3 The e200z0h can run at speeds up to 80 MHz. However, if system frequency is >80 MHz (e.g., e200z4d running at 120 MHz) the e200z0h needs to run at 1/2 system frequency. There is a configurable e200z0 system clock divider for this purpose.
4 DMAMUX also included that allows for software selection of 32 out of a possible 57 sources.
5 Not shared with 12-bit ADC, but possibly shared with other alternate functions.
6 There are 23 dedicated ANS plus 4 dedicated ANX channels on LQPF176. For higher pin count packages, there are 29 dedicated ANS plus 4 dedicated ANX channels.
7 16x precision channels (ANP) and 3x standard (ANS).
8 Not shared with 10-bit ADC, but possibly shared with other alternate functions.
9 As a minimum, all timer channels can function as PWM or Input Capture and Output Control. Refer to the eMIOS section of the device reference manual for information on the channel configuration and functions.
10 CAN Sampler also included that allows ID of CAN message to be captured when in low power mode.
11 STCU controls MBIST activation and reporting.
12 Estimated I/O count for proposed packages based on multiplexing with peripherals.

# 2 Block diagram

Figure 1 shows the detailed block diagram of the MPC5646C.




| | | | | | |
|---|---|---|---|---|---|
| Legend: | ADC | Analog-to-Digital Converter | JTAGC | JTAG controller |
| | BAM | Boot Assist Module | LINFlexD | Local Interconnect Network Flexible with DMA support |
| | CSE | Cryptographic Services Engine | MC_ME | Mode Entry Module |
| | CAN | Controller Area Network (FlexCAN) | MC_CGM | Clock Generation Module |
| | CMU | Clock Monitor Unit | MC_PCU | Power Control Unit |
| | CTU | Cross Triggering Unit | MC_RGM | Reset Generation Module |
| | DMAMUX | DMA Channel Multiplexer | MPU | Memory Protection Unit |
| | DSPI | Deserial Serial Peripheral Interface | Nexus | Nexus Development Interface |
| | eDMA | enhanced Direct Memory Access | NMI | Non-Maskable Interrupt |
| | FlexCAN | Controller Area Network controller modules | PIT_RTI | Periodic Interrupt Timer with Real-Time Interrupt |
| | FEC | Fast Ethenet Controller | RTC/API | Real-Time Clock/ Autonomous Periodic Interrupt |
| | eMIOS | Enhanced Modular Input Output System | SIUL | System Integration Unit Lite |
| | ECSM | Error Correction Status Module | SRAM | Static Random-Access Memory |
| | FMPLL | Frequency-Modulated Phase-Locked Loop | SSCM | System Status Configuration Module |
| | FlexRay | FlexRay Communication Controller | STM | System Timer Module |
| | I2C | Inter-integrated Circuit Bus | SWT | Software Watchdog Timer |
| | IMUX | Internal Multiplexer | STCU | Self Test Control Unit |
| | INTC | Interrupt Controller | WKPU | Wakeup Unit |

Notes:
1) 10 dedicated channels plus up to 19 shared channels. See the device-comparison table.
2) Package dependent. 27 or 33 dedicated channels plus up to 19 shared channels. See the device-comparison table.
3) 16 x precision channels (ANP) are mapped on input only I/O cells.

**Figure 1. MPC5646C block diagram**

Table 2 summarizes the functions of the blocks present on the MPC5646C.

**Table 2. MPC5646C series block summary**

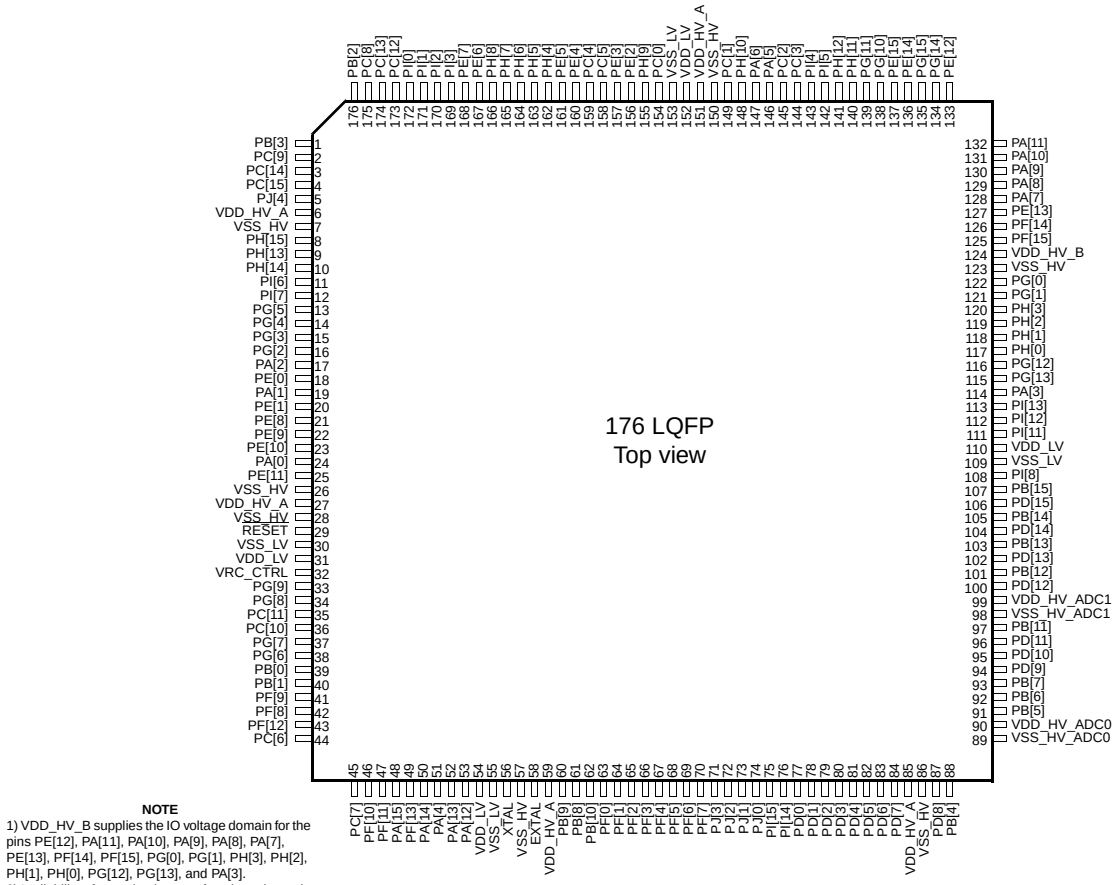
| Block | Function |
|---|---|
| Analog-to-digital converter (ADC) | Converts analog voltages to digital values |
| Boot assist module (BAM) | A block of read-only memory containing VLE code which is executed according to the boot mode of the device |
| Clock monitor unit (CMU) | Monitors clock source (internal and external) integrity |
| Cross triggering unit (CTU) | Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT |
| Cryptographic Security Engine (CSE) | Supports the encoding and decoding of any kind of data |
| Crossbar (XBAR) switch | Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width |
| DMA Channel Multiplexer (DMAMUX) | Allows to route DMA sources (called slots) to DMA channels |
| Deserial serial peripheral interface (DSPI) | Provides a synchronous serial interface for communication with external devices |
| Error Correction Status Module (ECSM) | Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes |
| Enhanced Direct Memory Access (eDMA) | Performs complex data transfers with minimal intervention from a host processor via “n” programmable channels. |
| Enhanced modular input output system (eMIOS) | Provides the functionality to generate or measure events |
| Flash memory | Provides non-volatile storage for program code, constants and variables |
| FlexCAN (controller area network) | Supports the standard CAN communications protocol |
| FMPLL (frequency-modulated phase-locked loop) | Generates high-speed system clocks and supports programmable frequency modulation |
| FlexRay (FlexRay communication controller) | Provides high-speed distributed control for advanced automotive applications |
| Fast Ethernet Controller (FEC) | Ethernet Media Access Controller (MAC) designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks |
| Internal multiplexer (IMUX) SIUL subblock | Allows flexible mapping of peripheral interface on the different pins of the device |
| Inter-integrated circuit ($I^2C$™) bus | A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices |
| Interrupt controller (INTC) | Provides priority-based preemptive scheduling of interrupt requests for both e200z0h and e200z4d cores |
| JTAG controller | Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode |

**Table 2. MPC5646C series block summary (continued)**

| Block | Function |
|---|---|
| LinFlexD (Local Interconnect Network Flexible with DMA support) | Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load |
| Memory protection unit (MPU) | Provides hardware access control for all memory references generated in a device |
| Clock generation module (MC_CGM) | Provides logic and control required for the generation of system and peripheral clocks |
| Power control unit (MC_PCU) | Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU |
| Reset generation module (MC_RGM) | Centralizes reset sources and manages the device reset sequence of the device |
| Mode entry module (MC_ME) | Provides a mechanism for controlling the device operational mode and modetransition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications |
| Non-Maskable Interrupt (NMI) | Handles external events that must produce an immediate response, such as power down detection |
| Nexus Development Interface (NDI) | Provides real-time development capabilities for e200z0h and e200z4d core processor |
| Periodic interrupt timer/ Real Time Interrupt Timer (PIT_RTI) | Produces periodic interrupts and triggers |
| Real-time counter (RTC/API) | A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode). Supports autonomous periodic interrupt (API) function to generate a periodic wakeup request to exit a low power mode or an interrupt request |
| Static random-access memory (SRAM) | Provides storage for program code, constants, and variables |
| System integration unit lite (SIUL) | Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration |
| System status and configuration module (SSCM) | Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable |
| System timer module (STM) | Provides a set of output compare events to support AutoSAR and operating system tasks |
| Semaphores | Provides the hardware support needed in multi-core systems for sharing resources and provides a simple mechanism to achieve lock/unlock operations via a single write access. |
| Wake Unit (WKPU) | Supports external sources that can generate interrupts or wakeup events, of which can cause non-maskable interrupt requests or wakeup events. |

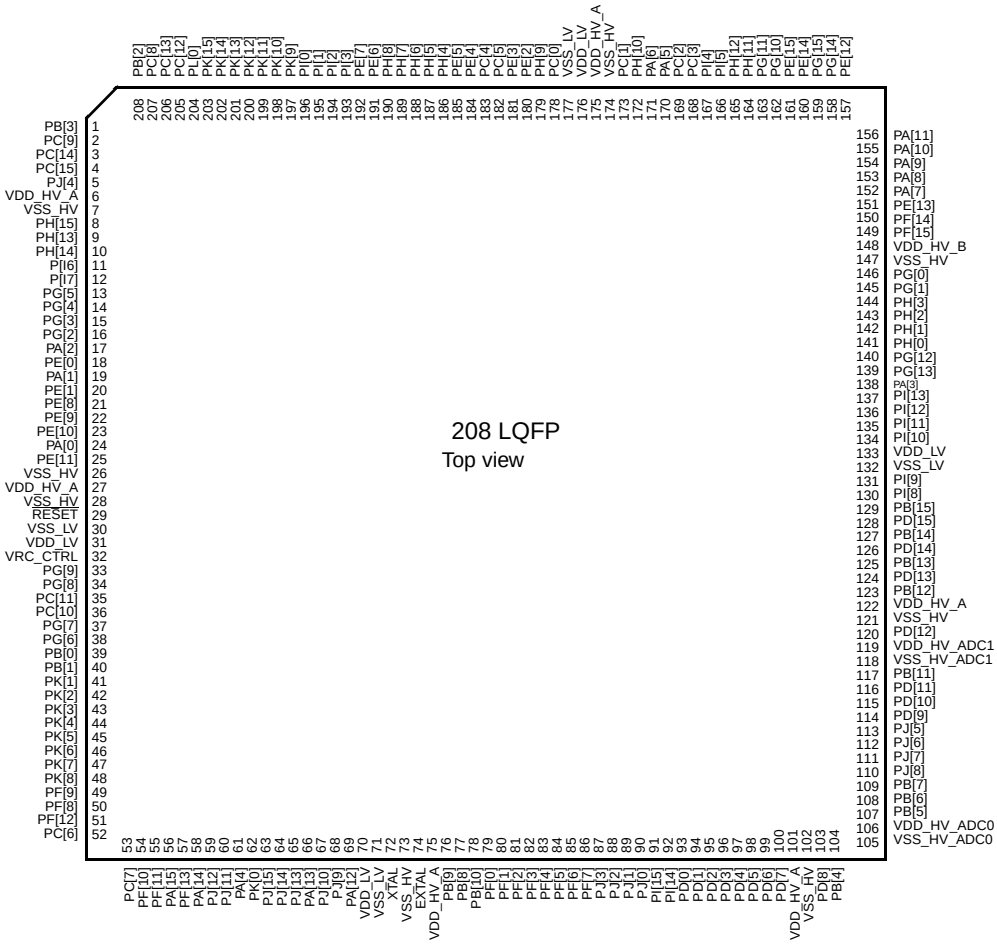
# 3 Package pinouts and signal descriptions

The available LQFP pinouts and the MAPBGA ballmaps are provided in the following figures. For functional port pin description, see Table 4.




**NOTE**
1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
2)Availability of port pin alternate functions depends on product selection.

**Figure 2. 176-pin LQFP configuration**




NOTE
1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
2) Availability of port pin alternate functions depends on product selection.

**Figure 3. 208-pin LQFP configuration**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | PC[15] | PB[2] | PC[13] | PI[1] | PE[7] | PH[8] | PE[2] | PE[4] | PC[4] | PE[3] | PH[9] | PI[4] | PH[11] | PE[14] | PA[10] | PG[11] | A |
| B | PH[13] | PC[14] | PC[8] | PC[12] | PI[3] | PE[6] | PH[5] | PE[5] | PC[5] | PC[0] | PC[2] | PH[12] | PG[10] | PA[11] | PA[9] | PA[8] | B |
| C | PH[14] | VDD_HV_A | PC[9] | PL[0] | PI[0] | PH[7] | PH[6] | VSS_LV | VDD_HV_A | PA[5] | PC[3] | PE[15] | PG[14] | PE[12] | PA[7] | PE[13] | C |
| D | PG[5] | PI[6] | PJ[4] | PB[3] | PK[15] | PI[2] | PH[4] | VDD_LV | PC[1] | PH[10] | PA[6] | PI[5] | PG[15] | PF[14] | PF[15] | PH[2] | D |
| E | PG[3] | PI[7] | PH[15] | PG[2] | | | | | | | | | PG[0] | PG[1] | PH[0] | VDD_HV_A | E |
| F | PA[2] | PG[4] | PA[1] | PE[1] | | | | | | | | | PH[1] | PH[3] | PG[12] | PG[13] | F |
| G | PE[8] | PE[0] | PE[10] | PA[0] | | | VSS_HV | VSS_HV | VSS_HV | VSS_HV | | | VDD_HV_B | PI[13] | PI[12] | PA[3] | G |
| H | PE[9] | VDD_HV_A | PE[11] | PK[1] | | | VSS_LV | VSS_HV | VSS_HV | VSS_HV | | | VDD_HV_A | VDD_LV | VSS_LV | PI[11] | H |
| J | VSS_HV | VRC_CTRL | VDD_LV | PG[9] | | | VSS_LV | VSS_LV | VSS_HV | VSS_HV | | | PD[15] | PI[8] | PI[9] | PI[10] | J |
| K | RESET | VSS_LV | PG[8] | PC[11] | | | VSS_LV | VSS_LV | VSS_LV | VDD_LV | | | PD[14] | PD[13] | PB[14] | PB[15] | K |
| L | PC[10] | PG[7] | PB[0] | PK[2] | | | | | | | | | PD[12] | PB[12] | PB[13] | VDD_HV_ADC1 | L |
| M | PG[6] | PB[1] | PK[4] | PF[9] | | | | | | | | | PB[11] | PD[10] | PD[11] | VSS_HV_ADC1 | M |
| N | PK[3] | PF[8] | PC[6] | PC[7] | PJ[13] | VDD_HV_A | PB[10] | PF[6] | VDD_HV_A | PJ[1] | PD[2] | PJ[5] | PB[5] | PB[6] | PJ[6] | PD[9] | N |
| P | PF[12] | PF[10] | PF[13] | PA[14] | PJ[9] | PA[12] | PF[0] | PF[5] | PF[7] | PJ[3] | PI[15] | PD[4] | PD[7] | PD[8] | PJ[8] | PJ[7] | P |
| R | PF[11] | PA[15] | PJ[11] | PJ[15] | PA[13] | PF[2] | PF[3] | PF[4] | VDD_LV | PJ[2] | PJ[0] | PD[0] | PD[3] | PD[6] | VDD_HV_ADC0 | PB[7] | R |
| T | PJ[12] | PA[4] | PK[0] | PJ[14] | PJ[10] | PF[1] | XTAL | EXTAL | VSS_LV | PB[9] | PB[8] | PI[14] | PD[1] | PD[5] | VSS_HV_ADC0 | PB[4] | T |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

Notes:
1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
2) Availability of port pin alternate functions depends on product selection.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | PC[15] | PB[2] | PC[13] | PI[1] | PE[7] | PH[8] | PE[2] | PE[4] | PC[4] | PE[3] | PH[9] | PI[4] | PH[11] | PE[14] | PA[10] | PG[11] | A |
| B | PH[13] | PC[14] | PC[8] | PC[12] | PI[3] | PE[6] | PH[5] | PE[5] | PC[5] | PC[0] | PC[2] | PH[12] | PG[10] | PA[11] | PA[9] | PA[8] | B |
| C | PH[14] | VDD_HV_A | PC[9] | PL[0] | PI[0] | PH[7] | PH[6] | VSS_LV | VDD_HV_A | PA[5] | PC[3] | PE[15] | PG[14] | PE[12] | PA[7] | PE[13] | C |
| D | PG[5] | PI[6] | PJ[4] | PB[3] | PK[15] | PI[2] | PH[4] | VDD_LV | PC[1] | PH[10] | PA[6] | PI[5] | PG[15] | PF[14] | PF[15] | PH[2] | D |
| E | PG[3] | PI[7] | PH[15] | PG[2] | VDD_LV | VSS_LV | PK[10] | PK[9] | PM[1] | PM[0] | PL[15] | PL[14] | PG[0] | PG[1] | PH[0] | VDD_HV_A | E |
| F | PA[2] | PG[4] | PA[1] | PE[1] | PL[2] | PM[6] | PL[1] | PK[11] | PM[5] | PL[13] | PL[12] | PM[2] | PH[1] | PH[3] | PG[12] | PG[13] | F |
| G | PE[8] | PE[0] | PE[10] | PA[0] | PL[3] | VSS_HV | VSS_HV | VSS_HV | VSS_HV | VSS_HV | VSS_HV | PK[12] | VDD_HV_B | PI[13] | PI[12] | PA[3] | G |
| H | PE[9] | VDD_HV_A | PE[11] | PK[1] | PL[4] | VSS_LV | VSS_LV | VSS_HV | VSS_HV | VSS_HV | VSS_HV | PK[13] | VDD_HV_A | VDD_LV | VSS_LV | PI[11] | H |
| J | VSS_HV | VRC_CTRL | VDD_LV | PG[9] | PL[5] | VSS_LV | VSS_LV | VSS_LV | VSS_HV | VSS_HV | VSS_HV | PK[14] | PD[15] | PI[8] | PI[9] | PI[10] | J |
| K | RESET | VSS_LV | PG[8] | PC[11] | PL[6] | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VDD_LV | VDD_LV | PM[3] | PD[14] | PD[13] | PB[14] | PB[15] | K |
| L | PC[10] | PG[7] | PB[0] | PK[2] | PL[7] | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VDD_LV | VDD_LV | PM[4] | PD[12] | PB[12] | PB[13] | VDD_HV_ADC1 | L |
| M | PG[6] | PB[1] | PK[4] | PF[9] | PK[5] | PK[6] | PK[7] | PK[8] | PL[8] | PL[9] | PL[10] | PL[11] | PB[11] | PD[10] | PD[11] | VSS_HV_ADC1 | M |
| N | PK[3] | PF[8] | PC[6] | PC[7] | PJ[13] | VDD_HV_A | PB[10] | PF[6] | VDD_HV_A | PJ[1] | PD[2] | PJ[5] | PB[5] | PB[6] | PJ[6] | PD[9] | N |
| P | PF[12] | PF[10] | PF[13] | PA[14] | PJ[9] | PA[12] | PF[0] | PF[5] | PF[7] | PJ[3] | PI[15] | PD[4] | PD[7] | PD[8] | PJ[8] | PJ[7] | P |
| R | PF[11] | PA[15] | PJ[11] | PJ[15] | PA[13] | PF[2] | PF[3] | PF[4] | VDD_LV | PJ[2] | PJ[0] | PD[0] | PD[3] | PD[6] | VDD_HV_ADC0 | PB[7] | R |
| T | PJ[12] | PA[4] | PK[0] | PJ[14] | PJ[10] | PF[1] | XTAL | EXTAL | VSS_LV | PB[9] | PB[8] | PI[14] | PD[1] | PD[5] | VSS_HV_ADC0 | PB[4] | T |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

Notes:
1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], PA[3], PM[3], and PM[4].
2)Availability of port pin alternate functions depends on product selection.

**Figure 4. 256-pin BGA configuration**

## 3.1 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[1]

M = Medium[1, 2]

1. See the I/O pad electrical characteristics in the device data sheet for details.
2. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium. For example, Fast/Medium pad will be Medium by default at reset. Similarly, Slow/Medium pad will be Slow by default. Only exception is PC[1] which is in medium configuration by default (refer to PCR.SRC in the reference manual, Pad Configuration Registers (PCR0—PCR198)).

F = Fast[1, 2]

I = Input only with analog feature[1]

A = Analog

## 3.2 System pins

The system pins are listed in Table 3.

**Table 3. System pin descriptions**

| Port pin | Function | I/O direction | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|
| | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| $\overline{\text{RESET}}$ | Bidirectional reset with Schmitt-Trigger characteristics and noise filter. | I/O | M | Input, weak pull-up only after PHASE2 | 29 | 29 | K1 |
| EXTAL | Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used. | I | A[1] | — | 58 | 74 | T8 |
| XTAL | Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode.<br>Analog input for the clock generator when the oscillator is in bypass mode. | I/O | A[1] | — | 56 | 72 | T7 |

NOTES:
1 For analog pads, it is not recommended to enable IBE if APC is enabled to avoid extra current in middle range voltage.

## 3.3 Functional ports

The functional port pins are listed in Table 4.

**Table 4. Functional port pin descriptions**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PA[0] | PCR[0] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[0]<br>E0UC[0]<br>CLKOUT<br>E0UC[13]<br>WKPU[19]<br>CAN1RX | SIUL<br>eMIOS_0<br>MC_CGM<br>eMIOS_0<br>WKPU<br>FlexCAN_1 | I/O<br>I/O<br>O<br>I/O<br>I<br>I | M/S | Tristate | 24 | 24 | G4 |
| PA[1] | PCR[1] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[1]<br>E0UC[1]<br>—<br>—<br>WKPU[2]<br>CAN3RX<br>NMI[0][3] | SIUL<br>eMIOS_0<br>—<br>—<br>WKPU<br>FlexCAN_3<br>WKPU | I/O<br>I/O<br>—<br>—<br>I<br>I<br>I | S | Tristate | 19 | 19 | F3 |
| PA[2] | PCR[2] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[2]<br>E0UC[2]<br>—<br>MA[2]<br>WKPU[3]<br>NMI[1][3] | SIUL<br>eMIOS_0<br>—<br>ADC_0<br>WKPU<br>WKPU | I/O<br>I/O<br>—<br>O<br>I<br>I | S | Tristate | 17 | 17 | F1 |
| PA[3] | PCR[3] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[3]<br>E0UC[3]<br>LIN5TX<br>CS4_1<br>RX_ER_CLK<br>EIRQ[0]<br>ADC1_S[0] | SIUL<br>eMIOS_0<br>LINFlexD_5<br>DSPI_1<br>FEC<br>SIUL<br>ADC_1 | I/O<br>I/O<br>O<br>O<br>I<br>I<br>I | M/S | Tristate | 114 | 138 | G16 |
| PA[4] | PCR[4] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[4]<br>E0UC[4]<br>—<br>CS0_1<br>LIN5RX<br>WKPU[9] | SIUL<br>eMIOS_0<br>—<br>DSPI_1<br>LINFlexD_5<br>WKPU | I/O<br>I/O<br>—<br>I/O<br>I<br>I | S | Tristate | 51 | 61 | T2 |
| PA[5] | PCR[5] | AF0<br>AF1<br>AF2 | GPIO[5]<br>E0UC[5]<br>LIN4TX | SIUL<br>eMIOS_0<br>LINFlexD_4 | I/O<br>I/O<br>O | M/S | Tristate | 146 | 170 | C10 |
| PA[6] | PCR[6] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[6]<br>E0UC[6]<br>—<br>CS1_1<br>LIN4RX<br>EIRQ[1] | SIUL<br>eMIOS_0<br>—<br>DSPI_1<br>LINFlexD_4<br>SIUL | I/O<br>I/O<br>—<br>O<br>I<br>I | S | Tristate | 147 | 171 | D11 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PA[7] | PCR[7] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[7]<br>E0UC[7]<br>LIN3TX<br>—<br>RXD[2]<br>EIRQ[2]<br>ADC1_S[1] | SIUL<br>eMIOS_0<br>LINFlexD_3<br>—<br>FEC<br>SIUL<br>ADC_1 | I/O<br>I/O<br>O<br>—<br>I<br>I<br>I | M/S | Tristate | 128 | 152 | C15 |
| PA[8] | PCR[8] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>—<br>— | GPIO[8]<br>E0UC[8]<br>E0UC[14]<br>—<br>RXD[1]<br>EIRQ[3]<br>ABS[0]<br>LIN3RX | SIUL<br>eMIOS_0<br>eMIOS_0<br>—<br>FEC<br>SIUL<br>MC_RGM<br>LINFlexD_3 | I/O<br>I/O<br>I/O<br>—<br>I<br>I<br>I<br>I | M/S | Input, weak pull-up | 129 | 153 | B16 |
| PA[9] | PCR[9] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[9]<br>E0UC[9]<br>—<br>CS2_1<br>RXD[0]<br>FAB | SIUL<br>eMIOS_0<br>—<br>DSPI1<br>FEC<br>MC_RGM | I/O<br>I/O<br>—<br>O<br>I<br>I | M/S | Pull-down | 130 | 154 | B15 |
| PA[10] | PCR[10] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[10]<br>E0UC[10]<br>SDA<br>LIN2TX<br>COL<br>ADC1_S[2]<br>SIN_1 | SIUL<br>eMIOS_0<br>$I^2C$<br>LINFlexD_2<br>FEC<br>ADC_1<br>DSPI_1 | I/O<br>I/O<br>I/O<br>O<br>I<br>I<br>I | M/S | Tristate | 131 | 155 | A15 |
| PA[11] | PCR[11] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>—<br>— | GPIO[11]<br>E0UC[11]<br>SCL<br>—<br>RX_ER<br>EIRQ[16]<br>LIN2RX<br>ADC1_S[3] | SIUL<br>eMIOS_0<br>$I^2C$<br>—<br>FEC<br>SIUL<br>LINFlexD_2<br>ADC_1 | I/O<br>I/O<br>I/O<br>—<br>I<br>I<br>I<br>I | M/S | Tristate | 132 | 156 | B14 |
| PA[12] | PCR[12] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[12]<br>—<br>E0UC[28]<br>CS3_1<br>EIRQ[17]<br>SIN_0 | SIUL<br>—<br>eMIOS_0<br>DSPI1<br>SIUL<br>DSPI_0 | I/O<br>—<br>I/O<br>O<br>I<br>I | S | Tristate | 53 | 69 | P6 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PA[13] | PCR[13] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[13]<br>SOUT_0<br>E0UC[29]<br>— | SIUL<br>DSPI_0<br>eMIOS_0<br>— | I/O<br>O<br>I/O<br>— | M/S | Tristate | 52 | 66 | R5 |
| PA[14] | PCR[14] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[14]<br>SCK_0<br>CS0_0<br>E0UC[0]<br>EIRQ[4] | SIUL<br>DSPI_0<br>DSPI_0<br>eMIOS_0<br>SIUL | I/O<br>I/O<br>I/O<br>I/O<br>I | M/S | Tristate | 50 | 58 | P4 |
| PA[15] | PCR[15] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[15]<br>CS0_0<br>SCK_0<br>E0UC[1]<br>WKPU[10] | SIUL<br>DSPI_0<br>DSPI_0<br>eMIOS_0<br>WKPU | I/O<br>I/O<br>I/O<br>I/O<br>I | M/S | Tristate | 48 | 56 | R2 |
| PB[0] | PCR[16] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[16]<br>CAN0TX<br>E0UC[30]<br>LIN0TX | SIUL<br>FlexCAN_0<br>eMIOS_0<br>LINFlexD_0 | I/O<br>O<br>I/O<br>I | M/S | Tristate | 39 | 39 | L3 |
| PB[1] | PCR[17] | AF0<br>AF1<br>AF2<br>—<br>—<br>— | GPIO[17]<br>—<br>E0UC[31]<br>LIN0RX<br>WKPU[4]<br>CAN0RX | SIUL<br>—<br>eMIOS_0<br>LINFlexD_0<br>WKPU<br>FlexCAN_0 | I/O<br>—<br>I/O<br>I<br>I<br>I | S | Tristate | 40 | 40 | M2 |
| PB[2] | PCR[18] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[18]<br>LIN0TX<br>SDA<br>E0UC[30] | SIUL<br>LINFlexD_0<br>$I^2C$<br>eMIOS_0 | I/O<br>O<br>I/O<br>I/O | M/S | Tristate | 176 | 208 | A2 |
| PB[3] | PCR[19] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[19]<br>E0UC[31]<br>SCL<br>—<br>WKPU[11]<br>LIN0RX | SIUL<br>eMIOS_0<br>$I^2C$<br>—<br>WKPU<br>LINFlexD_0 | I/O<br>I/O<br>I/O<br>—<br>I<br>I | S | Tristate | 1 | 1 | D4 |
| PB[4] | PCR[20] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[20]<br>—<br>—<br>—<br>ADC0_P[0]<br>ADC1_P[0] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 88 | 104 | T16 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PB[5] | PCR[21] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[21]<br>—<br>—<br>—<br>ADC0_P[1]<br>ADC1_P[1] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 91 | 107 | N13 |
| PB[6] | PCR[22] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[22]<br>—<br>—<br>—<br>ADC0_P[2]<br>ADC1_P[2] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 92 | 108 | N14 |
| PB[7] | PCR[23] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[23]<br>—<br>—<br>—<br>ADC0_P[3]<br>ADC1_P[3] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 93 | 109 | R16 |
| PB[8] | PCR[24] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>—<br>— | GPI[24]<br>—<br>—<br>—<br>ADC0_S[0]<br>ADC1_S[4]<br>WKPU[25]<br>OSC32k_XTAL[4] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1<br>WKPU<br>SXOSC | I<br>—<br>—<br>—<br>I<br>I<br>I<br>I | I | — | 61 | 77 | T11 |
| PB[9][5] | PCR[25] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>—<br>— | GPI[25]<br>—<br>—<br>—<br>ADC0_S[1]<br>ADC1_S[5]<br>WKPU[26]<br>OSC32k_EXTAL[4] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1<br>WKPU<br>SXOSC | I<br>—<br>—<br>—<br>I<br>I<br>I<br>I | I | — | 60 | 76 | T10 |
| PB[10] | PCR[26] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[26]<br>SOUT_1<br>CAN3TX<br>—<br>ADC0_S[2]<br>ADC1_S[6]<br>WKPU[8] | SIUL<br>DSPI_1<br>FlexCAN_3<br>—<br>ADC_0<br>ADC_1<br>WKPU | I/O<br>O<br>—<br>—<br>I<br>I<br>I | S | Tristate | 62 | 78 | N7 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PB[11] | PCR[27] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[27]<br>E0UC[3]<br>—<br>CS0_0<br>ADC0_S[3] | SIUL<br>eMIOS_0<br>—<br>DSPI_0<br>ADC_0 | I/O<br>I/O<br>—<br>I/O<br>I | S | Tristate | 97 | 117 | M13 |
| PB[12] | PCR[28] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[28]<br>E0UC[4]<br>—<br>CS1_0<br>ADC0_X[0] | SIUL<br>eMIOS_0<br>—<br>DSPI_0<br>ADC_0 | I/O<br>I/O<br>—<br>O<br>I | S | Tristate | 101 | 123 | L14 |
| PB[13] | PCR[29] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[29]<br>E0UC[5]<br>—<br>CS2_0<br>ADC0_X[1] | SIUL<br>eMIOS_0<br>—<br>DSPI_0<br>ADC_0 | I/O<br>I/O<br>—<br>O<br>I | S | Tristate | 103 | 125 | L15 |
| PB[14] | PCR[30] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[30]<br>E0UC[6]<br>—<br>CS3_0<br>ADC0_X[2] | SIUL<br>eMIOS_0<br>—<br>DSPI_0<br>ADC_0 | I/O<br>I/O<br>—<br>O<br>I | S | Tristate | 105 | 127 | K15 |
| PB[15] | PCR[31] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[31]<br>E0UC[7]<br>—<br>CS4_0<br>ADC0_X[3] | SIUL<br>eMIOS_0<br>—<br>DSPI_0<br>ADC_0 | I/O<br>I/O<br>—<br>O<br>I | S | Tristate | 107 | 129 | K16 |
| PC[0][6] | PCR[32] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[32]<br>—<br>TDI<br>— | SIUL<br>—<br>JTAGC<br>— | I/O<br>—<br>I<br>— | M/S | Input, weak pull-up | 154 | 178 | B10 |
| PC[1][6] | PCR[33] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[33]<br>—<br>TDO<br>— | SIUL<br>—<br>JTAGC<br>— | I/O<br>—<br>O<br>— | F/M | Tristate | 149 | 173 | D9 |
| PC[2] | PCR[34] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[34]<br>SCK_1<br>CAN4TX<br>—<br>EIRQ[5] | SIUL<br>DSPI_1<br>FlexCAN_4<br>—<br>SIUL | I/O<br>I/O<br>O<br>—<br>I | M/S | Tristate | 145 | 169 | B11 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PC[3] | PCR[35] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[35]<br>CS0_1<br>MA[0]<br>—<br>CAN1RX<br>CAN4RX<br>EIRQ[6] | SIUL<br>DSPI_1<br>ADC_0<br>—<br>FlexCAN_1<br>FlexCAN_4<br>SIUL | I/O<br>I/O<br>O<br><br>I<br>I<br>I | S | Tristate | 144 | 168 | C11 |
| PC[4] | PCR[36] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4<br>—<br>—<br>— | GPIO[36]<br>E1UC[31]<br>—<br><br>FR_B_TX_EN<br>SIN_1<br>CAN3RX<br>EIRQ[18] | SIUL<br>eMIOS_1<br>—<br><br>Flexray<br>DSPI_1<br>FlexCAN_3<br>SIUL | I/O<br>I/O<br>—<br><br>O<br>I<br>I<br>I | M/S | Tristate | 159 | 183 | A9 |
| PC[5] | PCR[37] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4<br>— | GPIO[37]<br>SOUT_1<br>CAN3TX<br>—<br>FR_A_TX<br>EIRQ[7] | SIUL<br>DSPI_1<br>FlexCAN_3<br>—<br>Flexray<br>SIUL | I/O<br>O<br>O<br>—<br>O<br>I | M/S | Tristate | 158 | 182 | B9 |
| PC[6] | PCR[38] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[38]<br>LIN1TX<br>E1UC[28]<br>— | SIUL<br>LINFlexD_1<br>eMIOS_1<br>— | I/O<br>O<br>I/O<br>— | S | Tristate | 44 | 52 | N3 |
| PC[7] | PCR[39] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[39]<br>—<br>E1UC[29]<br>—<br>LIN1RX<br>WKPU[12] | SIUL<br>—<br>eMIOS_1<br>—<br>LINFlexD_1<br>WKPU | I/O<br>—<br>I/O<br>—<br>I<br>I | S | Tristate | 45 | 53 | N4 |
| PC[8] | PCR[40] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[40]<br>LIN2TX<br>E0UC[3]<br>— | SIUL<br>LINFlexD_2<br>eMIOS_0<br>— | I/O<br>O<br>I/O<br>— | S | Tristate | 175 | 207 | B3 |
| PC[9] | PCR[41] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[41]<br>—<br>E0UC[7]<br>—<br>LIN2RX<br>WKPU[13] | SIUL<br>—<br>eMIOS_0<br>—<br>LINFlexD_2<br>WKPU | I/O<br>—<br>I/O<br>—<br>I<br>I | S | Tristate | 2 | 2 | C3 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PC[10] | PCR[42] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[42]<br>CAN1TX<br>CAN4TX<br>MA[1] | SIUL<br>FlexCAN_1<br>FlexCAN_4<br>ADC_0 | I/O<br>O<br>O<br>O | M/S | Tristate | 36 | 36 | L1 |
| PC[11] | PCR[43] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[43]<br>—<br>—<br>MA[2]<br>CAN1RX<br>CAN4RX<br>WKPU[5] | SIUL<br>—<br>—<br>ADC_0<br>FlexCAN_1<br>FlexCAN_4<br>WKPU | I/O<br>—<br>—<br>O<br>I<br>I<br>I | S | Tristate | 35 | 35 | K4 |
| PC[12] | PCR[44] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4<br>—<br>— | GPIO[44]<br>E0UC[12]<br>—<br>—<br>FR_DBG[0]<br>SIN_2<br>EIRQ[19] | SIUL<br>eMIOS_0<br>—<br>—<br>Flexray<br>DSPI_2<br>SIUL | I/O<br>I/O<br>—<br>—<br>O<br>I<br>I | M/S | Tristate | 173 | 205 | B4 |
| PC[13] | PCR[45] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[45]<br>E0UC[13]<br>SOUT_2<br>—<br>FR_DBG[1] | SIUL<br>eMIOS_0<br>DSPI_2<br>—<br>Flexray | I/O<br>I/O<br>O<br>—<br>O | M/S | Tristate | 174 | 206 | A3 |
| PC[14] | PCR[46] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4<br>— | GPIO[46]<br>E0UC[14]<br>SCK_2<br>—<br>FR_DBG[2]<br>EIRQ[8] | SIUL<br>eMIOS_0<br>DSPI_2<br>—<br>Flexray<br>SIUL | I/O<br>I/O<br>I/O<br>—<br>O<br>I | M/S | Tristate | 3 | 3 | B2 |
| PC[15] | PCR[47] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[47]<br>E0UC[15]<br>CS0_2<br>—<br>FR_DBG[3]<br>EIRQ[20] | SIUL<br>eMIOS_0<br>DSPI_2<br>—<br>Flexray<br>SIUL | I/O<br>I/O<br>I/O<br>—<br>O<br>I | M/S | Tristate | 4 | 4 | A1 |
| PD[0] | PCR[48] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPI[48]<br>—<br>—<br>—<br>ADC0_P[4]<br>ADC1_P[4]<br>WKPU[27] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1<br>WKPU | I<br>—<br>—<br>—<br>I<br>I<br>I | I | Tristate | 77 | 93 | R12 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PD[1] | PCR[49] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPI[49]<br>—<br>—<br>—<br>ADC0_P[5]<br>ADC1_P[5]<br>WKPU[28] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1<br>WKPU | I<br>—<br>—<br>—<br>I<br>I<br>I | I | Tristate | 78 | 94 | T13 |
| PD[2] | PCR[50] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[50]<br>—<br>—<br>—<br>ADC0_P[6]<br>ADC1_P[6] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 79 | 95 | N11 |
| PD[3] | PCR[51] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[51]<br>—<br>—<br>—<br>ADC0_P[7]<br>ADC1_P[7] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 80 | 96 | R13 |
| PD[4] | PCR[52] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[52]<br>—<br>—<br>—<br>ADC0_P[8]<br>ADC1_P[8] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 81 | 97 | P12 |
| PD[5] | PCR[53] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[53]<br>—<br>—<br>—<br>ADC0_P[9]<br>ADC1_P[9] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 82 | 98 | T14 |
| PD[6] | PCR[54] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[54]<br>—<br>—<br>—<br>ADC0_P[10]<br>ADC1_P[10] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 83 | 99 | R14 |
| PD[7] | PCR[55] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[55]<br>—<br>—<br>—<br>ADC0_P[11]<br>ADC1_P[11] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 84 | 100 | P13 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PD[8] | PCR[56] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[56]<br>—<br>—<br>—<br>ADC0_P[12]<br>ADC1_P[12] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 87 | 103 | P14 |
| PD[9] | PCR[57] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[57]<br>—<br>—<br>—<br>ADC0_P[13]<br>ADC1_P[13] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 94 | 114 | N16 |
| PD[10] | PCR[58] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[58]<br>—<br>—<br>—<br>ADC0_P[14]<br>ADC1_P[14] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 95 | 115 | M14 |
| PD[11] | PCR[59] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPI[59]<br>—<br>—<br>—<br>ADC0_P[15]<br>ADC1_P[15] | SIUL<br>—<br>—<br>—<br>ADC_0<br>ADC_1 | I<br>—<br>—<br>—<br>I<br>I | I | Tristate | 96 | 116 | M15 |
| PD[12] | PCR[60] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[60]<br>CS5_0<br>E0UC[24]<br>—<br>ADC0_S[4] | SIUL<br>DSPI_0<br>eMIOS_0<br>—<br>ADC_0 | I/O<br>O<br>I/O<br>—<br>I | S | Tristate | 100 | 120 | L13 |
| PD[13] | PCR[61] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[61]<br>CS0_1<br>E0UC[25]<br>—<br>ADC0_S[5] | SIUL<br>DSPI_1<br>eMIOS_0<br>—<br>ADC_0 | I/O<br>I/O<br>I/O<br>—<br>I | S | Tristate | 102 | 124 | K14 |
| PD[14] | PCR[62] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4<br>— | GPIO[62]<br>CS1_1<br>E0UC[26]<br>—<br>FR_DBG[0]<br>ADC0_S[6] | SIUL<br>DSPI_1<br>eMIOS_0<br>—<br>Flexray<br>ADC_0 | I/O<br>O<br>I/O<br>—<br>O<br>I | S | Tristate | 104 | 126 | K13 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PD[15] | PCR[63] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4<br>— | GPIO[63]<br>CS2_1<br>E0UC[27]<br>—<br>FR_DBG[1]<br>ADC0_S[7] | SIUL<br>DSPI_1<br>eMIOS_0<br>—<br>Flexray<br>ADC_0 | I/O<br>O<br>I/O<br>—<br>O<br>I | S | Tristate | 106 | 128 | J13 |
| PE[0] | PCR[64] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[64]<br>E0UC[16]<br>—<br>—<br>CAN5RX<br>WKPU[6] | SIUL<br>eMIOS_0<br>—<br>—<br>FlexCAN_5<br>WKPU | I/O<br>I/O<br>—<br>—<br>I<br>I | S | Tristate | 18 | 18 | G2 |
| PE[1] | PCR[65] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[65]<br>E0UC[17]<br>CAN5TX<br>— | SIUL<br>eMIOS_0<br>FlexCAN_5<br>— | I/O<br>I/O<br>O<br>— | M/S | Tristate | 20 | 20 | F4 |
| PE[2] | PCR[66] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4<br>—<br>— | GPIO[66]<br>E0UC[18]<br>—<br>—<br>FR_A_TX_EN<br>SIN_1<br>EIRQ[21] | SIUL<br>eMIOS_0<br>—<br>—<br>Flexray<br>DSPI_1<br>SIUL | I/O<br>I/O<br>—<br>—<br>O<br>I<br>I | M/S | Tristate | 156 | 180 | A7 |
| PE[3] | PCR[67] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[67]<br>E0UC[19]<br>SOUT_1<br>—<br>FR_A_RX<br>WKPU[29] | SIUL<br>eMIOS_0<br>DSPI_1<br>—<br>Flexray<br>WKPU | I/O<br>I/O<br>O<br>—<br>I<br>I | M/S | Tristate | 157 | 181 | A10 |
| PE[4] | PCR[68] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4<br>— | GPIO[68]<br>E0UC[20]<br>SCK_1<br>—<br>FR_B_TX<br>EIRQ[9] | SIUL<br>eMIOS_0<br>DSPI_1<br>—<br>Flexray<br>SIUL | I/O<br>I/O<br>I/O<br>—<br>O<br>I | M/S | Tristate | 160 | 184 | A8 |
| PE[5] | PCR[69] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[69]<br>E0UC[21]<br>CS0_1<br>MA[2]<br>FR_B_RX<br>WKPU[30] | SIUL<br>eMIOS_0<br>DSPI_1<br>ADC_0<br>Flexray<br>WKPU | I/O<br>I/O<br>I/O<br>O<br>I<br>I | M/S | Tristate | 161 | 185 | B8 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PE[6] | PCR[70] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[70]<br>E0UC[22]<br>CS3_0<br>MA[1]<br>EIRQ[22] | SIUL<br>eMIOS_0<br>DSPI_0<br>ADC_0<br>SIUL | I/O<br>I/O<br>O<br>O<br>I | M/S | Tristate | 167 | 191 | B6 |
| PE[7] | PCR[71] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[71]<br>E0UC[23]<br>CS2_0<br>MA[0]<br>EIRQ[23] | SIUL<br>eMIOS_0<br>DSPI_0<br>ADC_0<br>SIUL | I/O<br>I/O<br>O<br>O<br>I | M/S | Tristate | 168 | 192 | A5 |
| PE[8] | PCR[72] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[72]<br>CAN2TX<br>E0UC[22]<br>CAN3TX | SIUL<br>FlexCAN_2<br>eMIOS_0<br>FlexCAN_3 | I/O<br>O<br>I/O<br>O | M/S | Tristate | 21 | 21 | G1 |
| PE[9] | PCR[73] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[73]<br>—<br>E0UC[23]<br>—<br>WKPU[7]<br>CAN2RX<br>CAN3RX | SIUL<br>—<br>eMIOS_0<br>—<br>WKPU<br>FlexCAN_2<br>FlexCAN_3 | I/O<br>—<br>I/O<br>—<br>I<br>I<br>I | S | Tristate | 22 | 22 | H1 |
| PE[10] | PCR[74] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[74]<br>LIN3TX<br>CS3_1<br>E1UC[30]<br>EIRQ[10] | SIUL<br>LINFlexD_3<br>DSPI_1<br>eMIOS_1<br>SIUL | I/O<br>O<br>O<br>I/O<br>I | S | Tristate | 23 | 23 | G3 |
| PE[11] | PCR[75] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[75]<br>E0UC[24]<br>CS4_1<br>—<br>LIN3RX<br>WKPU[14] | SIUL<br>eMIOS_0<br>DSPI_1<br>—<br>LINFlexD_3<br>WKPU | I/O<br>I/O<br>O<br>—<br>I<br>I | S | Tristate | 25 | 25 | H3 |
| PE[12] | PCR[76] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>—<br>— | GPIO[76]<br>—<br>E1UC[19]<br>—<br>CRS<br>SIN_2<br>EIRQ[11]<br>ADC1_S[7] | SIUL<br>—<br>eMIOS_1<br>—<br>FEC<br>DSPI_2<br>SIUL<br>ADC_1 | I/O<br>—<br>I/O<br>—<br>I<br>I<br>I<br>I | M/S | Tristate | 133 | 157 | C14 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PE[13] | PCR[77] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[77]<br>SOUT_2<br>E1UC[20]<br>—<br>RXD[3] | SIUL<br>DSPI_2<br>eMIOS_1<br>—<br>FEC | I/O<br>O<br>I/O<br>—<br>I | M/S | Tristate | 127 | 151 | C16 |
| PE[14] | PCR[78] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[78]<br>SCK_2<br>E1UC[21]<br>—<br>EIRQ[12] | SIUL<br>DSPI_2<br>eMIOS_1<br>—<br>SIUL | I/O<br>I/O<br>I/O<br>—<br>I | M/S | Tristate | 136 | 160 | A14 |
| PE[15] | PCR[79] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[79]<br>CS0_2<br>E1UC[22]<br>SCK_6 | SIUL<br>DSPI_2<br>eMIOS_1<br>DSPI_6 | I/O<br>I/O<br>I/O<br>I/O | M/S | Tristate | 137 | 161 | C12 |
| PF[0] | PCR[80] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[80]<br>E0UC[10]<br>CS3_1<br>—<br>ADC0_S[8] | SIUL<br>eMIOS_0<br>DSPI_1<br>—<br>ADC_0 | I/O<br>I/O<br>O<br>—<br>I | S | Tristate | 63 | 79 | P7 |
| PF[1] | PCR[81] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[81]<br>E0UC[11]<br>CS4_1<br>—<br>ADC0_S[9] | SIUL<br>eMIOS_0<br>DSPI_1<br>—<br>ADC_0 | I/O<br>I/O<br>O<br>—<br>I | S | Tristate | 64 | 80 | T6 |
| PF[2] | PCR[82] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[82]<br>E0UC[12]<br>CS0_2<br>—<br>ADC0_S[10] | SIUL<br>eMIOS_0<br>DSPI_2<br>—<br>ADC_0 | I/O<br>I/O<br>I/O<br>—<br>I | S | Tristate | 65 | 81 | R6 |
| PF[3] | PCR[83] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[83]<br>E0UC[13]<br>CS1_2<br>—<br>ADC0_S[11] | SIUL<br>eMIOS_0<br>DSPI_2<br>—<br>ADC_0 | I/O<br>I/O<br>O<br>—<br>I | S | Tristate | 66 | 82 | R7 |
| PF[4] | PCR[84] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[84]<br>E0UC[14]<br>CS2_2<br>—<br>ADC0_S[12] | SIUL<br>eMIOS_0<br>DSPI_2<br>—<br>ADC_0 | I/O<br>I/O<br>O<br>—<br>I | S | Tristate | 67 | 83 | R8 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PF[5] | PCR[85] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[85]<br>E0UC[22]<br>CS3_2<br>—<br>ADC0_S[13] | SIUL<br>eMIOS_0<br>DSPI_2<br>—<br>ADC_0 | I/O<br>I/O<br>O<br>—<br>I | S | Tristate | 68 | 84 | P8 |
| PF[6] | PCR[86] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[86]<br>E0UC[23]<br>CS1_1<br>—<br>ADC0_S[14] | SIUL<br>eMIOS_0<br>DSPI_1<br>—<br>ADC_0 | I/O<br>I/O<br>O<br>—<br>I | S | Tristate | 69 | 85 | N8 |
| PF[7] | PCR[87] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[87]<br>—<br>CS2_1<br>—<br>ADC0_S[15] | SIUL<br>—<br>DSPI_1<br>—<br>ADC_0 | I/O<br>—<br>O<br>—<br>I | S | Tristate | 70 | 86 | P9 |
| PF[8] | PCR[88] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[88]<br>CAN3TX<br>CS4_0<br>CAN2TX | SIUL<br>FlexCAN_3<br>DSPI_0<br>FlexCAN_2 | I/O<br>O<br>O<br>O | M/S | Tristate | 42 | 50 | N2 |
| PF[9] | PCR[89] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[89]<br>E1UC[1]<br>CS5_0<br>—<br>CAN2RX<br>CAN3RX<br>WKPU[22] | SIUL<br>eMIOS_1<br>DSPI_0<br>—<br>FlexCAN_2<br>FlexCAN_3<br>WKPU | I/O<br>I/O<br>O<br>—<br>I<br>I<br>I | S | Tristate | 41 | 49 | M4 |
| PF[10] | PCR[90] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[90]<br>CS1_0<br>LIN4TX<br>E1UC[2] | SIUL<br>DSPI_0<br>LINFlexD_4<br>eMIOS_1 | I/O<br>O<br>O<br>I/O | M/S | Tristate | 46 | 54 | P2 |
| PF[11] | PCR[91] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[91]<br>CS2_0<br>E1UC[3]<br>—<br>LIN4RX<br>WKPU[15] | SIUL<br>DSPI_0<br>eMIOS_1<br>—<br>LINFlexD_4<br>WKPU | I/O<br>O<br>I/O<br>—<br>I<br>I | S | Tristate | 47 | 55 | R1 |
| PF[12] | PCR[92] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[92]<br>E1UC[25]<br>LIN5TX<br>— | SIUL<br>eMIOS_1<br>LINFlexD_5<br>— | I/O<br>I/O<br>O<br>— | M/S | Tristate | 43 | 51 | P1 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PF[13] | PCR[93] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[93]<br>E1UC[26]<br>—<br>—<br>LIN5RX<br>WKPU[16] | SIUL<br>eMIOS_1<br>—<br>—<br>LINFlexD_5<br>WKPU | I/O<br>I/O<br>—<br>—<br>I<br>I | S | Tristate | 49 | 57 | P3 |
| PF[14] | PCR[94] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[94]<br>CAN4TX<br>E1UC[27]<br>CAN1TX<br>MDIO | SIUL<br>FlexCAN_4<br>eMIOS_1<br>FlexCAN_1<br>FEC | I/O<br>O<br>I/O<br>O<br>I/O | M/S | Tristate | 126 | 150 | D14 |
| PF[15] | PCR[95] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>—<br>— | GPIO[95]<br>E1UC[4]<br>—<br>—<br>RX_DV<br>CAN1RX<br>CAN4RX<br>EIRQ[13] | SIUL<br>eMIOS_1<br>—<br>—<br>FEC<br>FlexCAN_1<br>FlexCAN_4<br>SIUL | I/O<br>I/O<br>—<br>—<br>I<br>I<br>I<br>I | M/S | Tristate | 125 | 149 | D15 |
| PG[0] | PCR[96] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[96]<br>CAN5TX<br>E1UC[23]<br>—<br>MDC | SIUL<br>FlexCAN_5<br>eMIOS_1<br>—<br>FEC | I/O<br>O<br>I/O<br>—<br>O | F | Tristate | 122 | 146 | E13 |
| PG[1] | PCR[97] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[97]<br>—<br>E1UC[24]<br>—<br>TX_CLK<br>CAN5RX<br>EIRQ[14] | SIUL<br>—<br>eMIOS_1<br>—<br>FEC<br>FlexCAN_5<br>SIUL | I/O<br>—<br>I/O<br>—<br>I<br>I<br>I | M | Tristate | 121 | 145 | E14 |
| PG[2] | PCR[98] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[98]<br>E1UC[11]<br>SOUT_3<br>— | SIUL<br>eMIOS_1<br>DSPI_3<br>— | I/O<br>I/O<br>O<br>— | M/S | Tristate | 16 | 16 | E4 |
| PG[3] | PCR[99] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[99]<br>E1UC[12]<br>CS0_3<br>—<br>WKPU[17] | SIUL<br>eMIOS_1<br>DSPI_3<br>—<br>WKPU | I/O<br>I/O<br>I/O<br>—<br>I | S | Tristate | 15 | 15 | E1 |
| PG[4] | PCR[100] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[100]<br>E1UC[13]<br>SCK_3<br>— | SIUL<br>eMIOS_1<br>DSPI_3<br>— | I/O<br>I/O<br>I/O<br>— | M/S | Tristate | 14 | 14 | F2 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PG[5] | PCR[101] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[101]<br>E1UC[14]<br>—<br>—<br>WKPU[18]<br>SIN_3 | SIUL<br>eMIOS_1<br>—<br>—<br>WKPU<br>DSPI_3 | I/O<br>I/O<br>—<br>—<br>I<br>I | S | Tristate | 13 | 13 | D1 |
| PG[6] | PCR[102] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[102]<br>E1UC[15]<br>LIN6TX<br>— | SIUL<br>eMIOS_1<br>LINFlexD_6<br>— | I/O<br>I/O<br>O<br>— | M/S | Tristate | 38 | 38 | M1 |
| PG[7] | PCR[103] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[103]<br>E1UC[16]<br>E1UC[30]<br>—<br>LIN6RX<br>WKPU[20] | SIUL<br>eMIOS_1<br>eMIOS_1<br>—<br>LINFlexD_6<br>WKPU | I/O<br>I/O<br>I/O<br>—<br>I<br>I | S | Tristate | 37 | 37 | L2 |
| PG[8] | PCR[104] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[104]<br>E1UC[17]<br>LIN7TX<br>CS0_2<br>EIRQ[15] | SIUL<br>eMIOS_1<br>LINFlexD_7<br>DSPI_2<br>SIUL | I/O<br>I/O<br>O<br>I/O<br>I | S | Tristate | 34 | 34 | K3 |
| PG[9] | PCR[105] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[105]<br>E1UC[18]<br>—<br>SCK_2<br>LIN7RX<br>WKPU[21] | SIUL<br>eMIOS_1<br>—<br>DSPI_2<br>LINFlexD_7<br>WKPU | I/O<br>I/O<br>—<br>I/O<br>I<br>I | S | Tristate | 33 | 33 | J4 |
| PG[10] | PCR[106] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[106]<br>E0UC[24]<br>E1UC[31]<br>—<br>SIN_4 | SIUL<br>eMIOS_0<br>eMIOS_1<br>—<br>DSPI_4 | I/O<br>I/O<br>I/O<br>—<br>I | S | Tristate | 138 | 162 | B13 |
| PG[11] | PCR[107] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[107]<br>E0UC[25]<br>CS0_4<br>CS0_6 | SIUL<br>eMIOS_0<br>DSPI_4<br>DSPI_6 | I/O<br>I/O<br>I/O<br>I/O | M/S | Tristate | 139 | 163 | A16 |
| PG[12] | PCR[108] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[108]<br>E0UC[26]<br>SOUT_4<br>—<br>TXD[2] | SIUL<br>eMIOS_0<br>DSPI_4<br>—<br>FEC | I/O<br>I/O<br>O<br>—<br>O | M/S | Tristate | 116 | 140 | F15 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PG[13] | PCR[109] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[109]<br>E0UC[27]<br>SCK_4<br>—<br>TXD[3] | SIUL<br>eMIOS_0<br>DSPI_4<br>—<br>FEC | I/O<br>I/O<br>I/O<br>—<br>O | M/S | Tristate | 115 | 139 | F16 |
| PG[14] | PCR[110] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[110]<br>E1UC[0]<br>LIN8TX<br>—<br>SIN_6 | SIUL<br>eMIOS_1<br>LINFlexD_8<br>—<br>DSPI_6 | I/O<br>I/O<br>O<br>—<br>I | S | Tristate | 134 | 158 | C13 |
| PG[15] | PCR[111] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[111]<br>E1UC[1]<br>SOUT_6<br>—<br>LIN8RX | SIUL<br>eMIOS_1<br>DSPI_6<br>—<br>LINFlexD_8 | I/O<br>I/O<br>O<br>—<br>I | M/S | Tristate | 135 | 159 | D13 |
| PH[0] | PCR[112] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4<br>— | GPIO[112]<br>E1UC[2]<br>—<br>—<br>TXD[1]<br>SIN_1 | SIUL<br>eMIOS_1<br>—<br>—<br>FEC<br>DSPI_1 | I/O<br>I/O<br>—<br>—<br>O<br>I | M/S | Tristate | 117 | 141 | E15 |
| PH[1] | PCR[113] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[113]<br>E1UC[3]<br>SOUT_1<br>—<br>TXD[0] | SIUL<br>eMIOS_1<br>DSPI_1<br>—<br>FEC | I/O<br>I/O<br>O<br>—<br>O | M/S | Tristate | 118 | 142 | F13 |
| PH[2] | PCR[114] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[114]<br>E1UC[4]<br>SCK_1<br>—<br>TX_EN | SIUL<br>eMIOS_1<br>DSPI_1<br>—<br>FEC | I/O<br>I/O<br>I/O<br>—<br>O | M/S | Tristate | 119 | 143 | D16 |
| PH[3] | PCR[115] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[115]<br>E1UC[5]<br>CS0_1<br>—<br>TX_ER | SIUL<br>eMIOS_1<br>DSPI_1<br>—<br>FEC | I/O<br>I/O<br>I/O<br>—<br>O | M/S | Tristate | 120 | 144 | F14 |
| PH[4] | PCR[116] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[116]<br>E1UC[6]<br>SOUT_7<br>— | SIUL<br>eMIOS_1<br>DSPI_7<br>— | I/O<br>I/O<br>O<br>— | M/S | Tristate | 162 | 186 | D7 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PH[5] | PCR[117] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[117]<br>E1UC[7]<br>—<br>—<br>SIN_7 | SIUL<br>eMIOS_1<br>—<br>—<br>DSPI_7 | I/O<br>I/O<br>—<br>—<br>I | S | Tristate | 163 | 187 | B7 |
| PH[6] | PCR[118] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[118]<br>E1UC[8]<br>SCK_7<br>MA[2] | SIUL<br>eMIOS_1<br>DSPI_7<br>ADC_0 | I/O<br>I/O<br>I/O<br>O | M/S | Tristate | 164 | 188 | C7 |
| PH[7] | PCR[119] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[119]<br>E1UC[9]<br>CS3_2<br>MA[1]<br>CS0_7 | SIUL<br>eMIOS_1<br>DSPI_2<br>ADC_0<br>DSPI_7 | I/O<br>I/O<br>O<br>O<br>I/O | M/S | Tristate | 165 | 189 | C6 |
| PH[8] | PCR[120] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[120]<br>E1UC[10]<br>CS2_2<br>MA[0] | SIUL<br>eMIOS_1<br>DSPI_2<br>ADC_0 | I/O<br>I/O<br>O<br>O | M/S | Tristate | 166 | 190 | A6 |
| PH[9][6] | PCR[121] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[121]<br>—<br>—<br>—<br>TCK | SIUL<br>—<br>—<br>—<br>JTAGC | I/O<br>—<br>—<br>—<br>I | S | Input, weak pull-up | 155 | 179 | A11 |
| PH[10][6] | PCR[122] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[122]<br>—<br>—<br>—<br>TMS | SIUL<br>—<br>—<br>—<br>JTAGC | I/O<br>—<br>—<br>—<br>I | M/S | Input, weak pull-up | 148 | 172 | D10 |
| PH[11] | PCR[123] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[123]<br>SOUT_3<br>CS0_4<br>E1UC[5] | SIUL<br>DSPI_3<br>DSPI_4<br>eMIOS_1 | I/O<br>O<br>I/O<br>I/O | M/S | Tristate | 140 | 164 | A13 |
| PH[12] | PCR[124] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[124]<br>SCK_3<br>CS1_4<br>E1UC[25] | SIUL<br>DSPI_3<br>DSPI_4<br>eMIOS_1 | I/O<br>I/O<br>O<br>I/O | M/S | Tristate | 141 | 165 | B12 |
| PH[13] | PCR[125] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[125]<br>SOUT_4<br>CS0_3<br>E1UC[26] | SIUL<br>DSPI_4<br>DSPI_3<br>eMIOS_1 | I/O<br>O<br>I/O<br>I/O | M/S | Tristate | 9 | 9 | B1 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PH[14] | PCR[126] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[126]<br>SCK_4<br>CS1_3<br>E1UC[27] | SIUL<br>DSPI_4<br>DSPI_3<br>eMIOS_1 | I/O<br>I/O<br>O<br>I/O | M/S | Tristate | 10 | 10 | C1 |
| PH[15] | PCR[127] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[127]<br>SOUT_5<br>—<br>E1UC[17] | SIUL<br>DSPI_5<br>—<br>eMIOS_1 | I/O<br>O<br>—<br>I/O | M/S | Tristate | 8 | 8 | E3 |
| PI[0] | PCR[128] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[128]<br>E0UC[28]<br>LIN8TX<br>— | SIUL<br>eMIOS_0<br>LINFlexD_8<br>— | I/O<br>I/O<br>O<br>— | S | Tristate | 172 | 196 | C5 |
| PI[1] | PCR[129] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[129]<br>E0UC[29]<br>—<br>—<br>WKPU[24]<br>LIN8RX | SIUL<br>eMIOS_0<br>—<br>—<br>WKPU<br>LINFlexD_8 | I/O<br>I/O<br>—<br>—<br>I<br>I | S | Tristate | 171 | 195 | A4 |
| PI[2] | PCR[130] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[130]<br>E0UC[30]<br>LIN9TX<br>— | SIUL<br>eMIOS_0<br>LINFlexD_9<br>— | I/O<br>I/O<br>O<br>— | S | Tristate | 170 | 194 | D6 |
| PI[3] | PCR[131] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[131]<br>E0UC[31]<br>—<br>—<br>WKPU[23]<br>LIN9RX | SIUL<br>eMIOS_0<br>—<br>—<br>WKPU<br>LINFlexD_9 | I/O<br>I/O<br>—<br>—<br>I<br>I | S | Tristate | 169 | 193 | B5 |
| PI[4] | PCR[132] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[132]<br>E1UC[28]<br>SOUT_4<br>— | SIUL<br>eMIOS_1<br>DSPI_4<br>— | I/O<br>I/O<br>O<br>— | M/S | Tristate | 143 | 167 | A12 |
| PI[5] | PCR[133] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[133]<br>E1UC[29]<br>SCK_4<br>CS2_5<br>CS2_6 | SIUL<br>eMIOS_1<br>DSPI_4<br>DSPI_5<br>DSPI_6 | I/O<br>I/O<br>I/O<br>O<br>O | M/S | Tristate | 142 | 166 | D12 |
| PI[6] | PCR[134] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[134]<br>E1UC[30]<br>CS0_4<br>CS0_5<br>CS0_6 | SIUL<br>eMIOS_1<br>DSPI_4<br>DSPI_5<br>DSPI_6 | I/O<br>I/O<br>I/O<br>I/O<br>I/O | S | Tristate | 11 | 11 | D2 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PI[7] | PCR[135] | AF0<br>AF1<br>AF2<br>AF3<br>ALT4 | GPIO[135]<br>E1UC[31]<br>CS1_4<br>CS1_5<br>CS1_6 | SIUL<br>eMIOS_1<br>DSPI_4<br>DSPI_5<br>DSPI_6 | I/O<br>I/O<br>O<br>O<br>O | S | Tristate | 12 | 12 | E2 |
| PI[8] | PCR[136] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[136]<br>—<br>—<br>—<br>ADC0_S[16] | SIUL<br>—<br>—<br>—<br>ADC_0 | I/O<br>—<br>—<br>—<br>I | S | Tristate | 108 | 130 | J14 |
| PI[9] | PCR[137] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[137]<br>—<br>—<br>—<br>ADC0_S[17] | SIUL<br>—<br>—<br>—<br>ADC_0 | I/O<br>—<br>—<br>—<br>I | S | Tristate | — | 131 | J15 |
| PI[10] | PCR[138] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[138]<br>—<br>—<br>—<br>ADC0_S[18] | SIUL<br>—<br>—<br>—<br>ADC_0 | I/O<br>—<br>—<br>—<br>I | S | Tristate | — | 134 | J16 |
| PI[11] | PCR[139] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[139]<br>—<br>—<br>—<br>ADC0_S[19]<br>SIN_3 | SIUL<br>—<br>—<br>—<br>ADC_0<br>DSPI_3 | I/O<br>—<br>—<br>—<br>I<br>I | S | Tristate | 111 | 135 | H16 |
| PI[12] | PCR[140] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[140]<br>CS0_3<br>CS0_2<br>—<br>ADC0_S[20] | SIUL<br>DSPI_3<br>DSPI_2<br>—<br>ADC_0 | I/O<br>I/O<br>I/O<br>—<br>I | S | Tristate | 112 | 136 | G15 |
| PI[13] | PCR[141] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[141]<br>CS1_3<br>CS1_2<br>—<br>ADC0_S[21] | SIUL<br>DSPI_3<br>DSPI_2<br>—<br>ADC_0 | I/O<br>O<br>O<br>—<br>I | S | Tristate | 113 | 137 | G14 |
| PI[14] | PCR[142] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[142]<br>—<br>—<br>—<br>ADC0_S[22]<br>SIN_4 | SIUL<br>—<br>—<br>—<br>ADC_0<br>DSPI_4 | I/O<br>—<br>—<br>—<br>I<br>I | S | Tristate | 76 | 92 | T12 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PI[15] | PCR[143] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[143]<br>CS0_4<br>CS2_2<br>—<br>ADC0_S[23] | SIUL<br>DSPI_4<br>DSPI_2<br>—<br>ADC_0 | I/O<br>I/O<br>O<br>—<br>I | S | Tristate | 75 | 91 | P11 |
| PJ[0] | PCR[144] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[144]<br>CS1_4<br>CS3_2<br>—<br>ADC0_S[24] | SIUL<br>DSPI_4<br>DSPI_2<br>—<br>ADC_0 | I/O<br>O<br>O<br>—<br>I | S | Tristate | 74 | 90 | R11 |
| PJ[1] | PCR[145] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[145]<br>—<br>—<br>—<br>ADC0_S[25]<br>SIN_5 | SIUL<br>—<br>—<br>——<br>ADC_0<br>DSPI_5 | I/O<br>—<br>—<br>—<br>I<br>I | S | Tristate | 73 | 89 | N10 |
| PJ[2] | PCR[146] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[146]<br>CS0_5<br>CS0_6<br>CS0_7<br>ADC0_S[26] | SIUL<br>DSPI_5<br>DSPI_6<br>DSPI_7<br>ADC_0 | I/O<br>I/O<br>I/O<br>I/O<br>I | S | Tristate | 72 | 88 | R10 |
| PJ[3] | PCR[147] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[147]<br>CS1_5<br>CS1_6<br>CS1_7<br>ADC0_S[27] | SIUL<br>DSPI_5<br>DSPI_6<br>DSPI_7<br>ADC_0 | I/O<br>O<br>O<br>O<br>I | S | Tristate | 71 | 87 | P10 |
| PJ[4] | PCR[148] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[148]<br>SCK_5<br>E1UC[18]<br>— | SIUL<br>DSPI_5<br>eMIOS_1<br>— | I/O<br>I/O<br>I/O<br>— | M/S | Tristate | 5 | 5 | D3 |
| PJ[5] | PCR[149] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[149]<br>—<br>—<br>—<br>ADC0_S[28] | SIUL<br>—<br>—<br>—<br>ADC_0 | I/O<br>—<br>—<br>—<br>I | S | Tristate | — | 113 | N12 |
| PJ[6] | PCR[150] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[150]<br>—<br>—<br>—<br>ADC0_S[29] | SIUL<br>—<br>—<br>—<br>ADC_0 | I/O<br>—<br>—<br>—<br>I | S | Tristate | — | 112 | N15 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PJ[7] | PCR[151] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[151]<br>—<br>—<br>—<br>ADC0_S[30] | SIUL<br>—<br>—<br>—<br>ADC_0 | I/O<br>—<br>—<br>—<br>I | S | Tristate | — | 111 | P16 |
| PJ[8] | PCR[152] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[152]<br>—<br>—<br>—<br>ADC0_S[31] | SIUL<br>—<br>—<br>—<br>ADC_0 | I/O<br>—<br>—<br>—<br>I | S | Tristate | — | 110 | P15 |
| PJ[9] | PCR[153] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[153]<br>—<br>—<br>—<br>ADC1_S[8] | SIUL<br>—<br>—<br>—<br>ADC_1 | I/O<br>—<br>—<br>—<br>I | S | Tristate | — | 68 | P5 |
| PJ[10] | PCR[154] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[154]<br>—<br>—<br>—<br>ADC1_S[9] | SIUL<br>—<br>—<br>—<br>ADC_1 | I/O<br>—<br>—<br>—<br>I | S | Tristate | — | 67 | T5 |
| PJ[11] | PCR[155] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[155]<br>—<br>—<br>—<br>ADC1_S[10] | SIUL<br>—<br>—<br>—<br>ADC_1 | I/O<br>—<br>—<br>—<br>I | S | Tristate | — | 60 | R3 |
| PJ[12] | PCR[156] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[156]<br>—<br>—<br>—<br>ADC1_S[11] | SIUL<br>—<br>—<br>—<br>ADC_1 | I/O<br>—<br>—<br>—<br>I | S | Tristate | — | 59 | T1 |
| PJ[13] | PCR[157] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>—<br>— | GPIO[157]<br>—<br>CS1_7<br>—<br>CAN4RX<br>ADC1_S[12]<br>CAN1RX<br>WKPU[31] | SIUL<br>—<br>DSPI_7<br>—<br>FlexCAN_4<br>ADC_1<br>FlexCAN_1<br>WKPU | I/O<br>—<br>O<br>—<br>I<br>I<br>I<br>I | S | Tristate | — | 65 | N5 |
| PJ[14] | PCR[158] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[158]<br>CAN1TX<br>CAN4TX<br>CS2_7 | SIUL<br>FlexCAN_1<br>FlexCAN_4<br>DSPI_7 | I/O<br>O<br>O<br>O | M/S | Tristate | — | 64 | T4 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PJ[15] | PCR[159] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[159]<br>—<br>CS1_6<br>—<br>CAN1RX | SIUL<br>—<br>DSPI_6<br>—<br>FlexCAN_1 | I/O<br>—<br>O<br>—<br>I | M/S | Tristate | — | 63 | R4 |
| PK[0] | PCR[160] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[160]<br>CAN1TX<br>CS2_6<br>— | SIUL<br>FlexCAN_1<br>DSPI_6<br>— | I/O<br>O<br>O<br>— | M/S | Tristate | — | 62 | T3 |
| PK[1] | PCR[161] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[161]<br>CS3_6<br>—<br>—<br>CAN4RX | SIUL<br>DSPI_6<br>—<br>—<br>FlexCAN_4 | I/O<br>O<br>—<br>—<br>I | M/S | Tristate | — | 41 | H4 |
| PK[2] | PCR[162] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[162]<br>CAN4TX<br>—<br>— | SIUL<br>FlexCAN_4<br>—<br>— | I/O<br>O<br>—<br>— | M/S | Tristate | — | 42 | L4 |
| PK[3] | PCR[163] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[163]<br>E1UC[0]<br>—<br>—<br>CAN5RX<br>LIN8RX | SIUL<br>eMIOS_1<br>—<br>—<br>FlexCAN_5<br>LINFlexD_8 | I/O<br>I/O<br>—<br>—<br>I<br>I | M/S | Tristate | — | 43 | N1 |
| PK[4] | PCR[164] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[164]<br>LIN8TX<br>CAN5TX<br>E1UC[1] | SIUL<br>LINFlexD_8<br>FlexCAN_5<br>eMIOS_1 | I/O<br>O<br>O<br>I/O | M/S | Tristate | — | 44 | M3 |
| PK[5] | PCR[165] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[165]<br>—<br>—<br>—<br>CAN2RX<br>LIN2RX | SIUL<br>—<br>—<br>—<br>FlexCAN_2<br>LINFlexD_2 | I/O<br>—<br>—<br>—<br>I<br>I | M/S | Tristate | — | 45 | M5 |
| PK[6] | PCR[166] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[166]<br>CAN2TX<br>LIN2TX<br>— | SIUL<br>FlexCAN_2<br>LINFlexD_2<br>— | I/O<br>O<br>O<br>— | M/S | Tristate | — | 46 | M6 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PK[7] | PCR[167] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[167]<br>—<br>—<br>—<br>CAN3RX<br>LIN3RX | SIUL<br>—<br>—<br>—<br>FlexCAN_3<br>LINFlexD_3 | I/O<br>—<br>—<br>—<br>I<br>I | M/S | Tristate | — | 47 | M7 |
| PK[8] | PCR[168] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[168]<br>CAN3TX<br>LIN3TX<br>— | SIUL<br>FlexCAN_3<br>LINFlexD_3<br>— | I/O<br>O<br>O<br>— | M/S | Tristate | — | 48 | M8 |
| PK[9] | PCR[169] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[169]<br>—<br>—<br>—<br>SIN_4 | SIUL<br>—<br>—<br>—<br>DSPI_4 | I/O<br>—<br>—<br>—<br>I | M/S | Tristate | — | 197 | E8 |
| PK[10] | PCR[170] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[170]<br>SOUT_4<br>—<br>— | SIUL<br>DSPI_4<br>—<br>— | I/O<br>O<br>—<br>— | M/S | Tristate | — | 198 | E7 |
| PK[11] | PCR[171] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[171]<br>SCK_4<br>—<br>— | SIUL<br>DSPI_4<br>—<br>— | I/O<br>I/O<br>—<br>— | M/S | Tristate | — | 199 | F8 |
| PK[12] | PCR[172] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[172]<br>CS0_4<br>—<br>— | SIUL<br>DSPI_4<br>—<br>— | I/O<br>I/O<br>—<br>— | M/S | Tristate | — | 200 | G12 |
| PK[13] | PCR[173] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[173]<br>CS3_6<br>CS2_7<br>SCK_1<br>CAN3RX | SIUL<br>DSPI_6<br>DSPI_7<br>DSPI_1<br>FlexCAN_3 | I/O<br>O<br>O<br>I/O<br>I | M/S | Tristate | — | 201 | H12 |
| PK[14] | PCR[174] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[174]<br>CAN3TX<br>CS3_7<br>CS0_1 | SIUL<br>FlexCAN_3<br>DSPI_7<br>DSPI_1 | I/O<br>O<br>O<br>I/O | M/S | Tristate | — | 202 | J12 |
| PK[15] | PCR[175] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[175]<br>—<br>—<br>—<br>SIN_1<br>SIN_7 | SIUL<br>—<br>—<br>—<br>DSPI_1<br>DSPI_7 | I/O<br>—<br>—<br>—<br>I<br>I | M/S | Tristate | — | 203 | D5 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PL[0] | PCR[176] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[176]<br>SOUT_1<br>SOUT_7<br>— | SIUL<br>DSPI_1<br>DSPI_7<br>— | I/O<br>O<br>O<br>— | M/S | Tristate | — | 204 | C4 |
| PL[1] | PCR[177] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[177]<br>—<br>—<br>— | SIUL<br>—<br>—<br>— | I/O<br>—<br>—<br>— | M/S | Tristate | — | — | F7 |
| PL[2] | PCR[178][7] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[178]<br>—<br>MDO0[8]<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | F5 |
| PL[3] | PCR[179] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[179]<br>—<br>MDO1<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | G5 |
| PL[4] | PCR[180] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[180]<br>—<br>MDO2<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | H5 |
| PL[5] | PCR[181] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[181]<br>—<br>MDO3<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | J5 |
| PL[6] | PCR[182] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[182]<br>—<br>MDO4<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | K5 |
| PL[7] | PCR[183] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[183]<br>—<br>MDO5<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | L5 |
| PL[8] | PCR[184] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[184]<br>—<br>—<br>—<br>EVTI | SIUL<br>—<br>—<br>—<br>Nexus | I/O<br>—<br>—<br>—<br>I | S | Pull-up | — | — | M9 |
| PL[9] | PCR[185] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[185]<br>—<br>MSEO<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | M10 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PL[10] | PCR[186] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[186]<br>—<br>MCKO<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | F/S | Tristate | — | — | M11 |
| PL[11] | PCR[187] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[187]<br>—<br>—<br>— | SIUL<br>—<br>—<br>— | I/O<br>—<br>—<br>— | M/S | Tristate | — | — | M12 |
| PL[12] | PCR[188] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[188]<br>—<br>EVTO<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | F11 |
| PL[13] | PCR[189] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[189]<br>—<br>MDO6<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | F10 |
| PL[14] | PCR[190] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[190]<br>—<br>MDO7<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | E12 |
| PL[15] | PCR[191] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[191]<br>—<br>MDO8<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | E11 |
| PM[0] | PCR[192] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[192]<br>—<br>MDO9<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | E10 |
| PM[1] | PCR[193] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[193]<br>—<br>MDO10<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | E9 |
| PM[2] | PCR[194] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[194]<br>—<br>MDO11<br>— | SIUL<br>—<br>Nexus<br>— | I/O<br>—<br>O<br>— | M/S | Tristate | — | — | F12 |
| PM[3] | PCR[195] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[195]<br>—<br>—<br>— | SIUL<br>—<br>—<br>— | I/O<br>—<br>—<br>— | M/S | Tristate | — | — | K12 |

**Table 4. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET config. | Pin number | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 176 LQFP | 208 LQFP | 256 MAPBGA |
| PM[4] | PCR[196] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[196]<br>—<br>—<br>— | SIUL<br>—<br>—<br>— | I/O<br>—<br>—<br>— | M/S | Tristate | — | — | L12 |
| PM[5] | PCR[197] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[197]<br>—<br>—<br>— | SIUL<br>—<br>—<br>— | I/O<br>—<br>—<br>— | M/S | Tristate | — | — | F9 |
| PM[6] | PCR[198] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[198]<br>—<br>—<br>— | SIUL<br>—<br>—<br>— | I/O<br>—<br>—<br>— | M/S | Tristate | — | — | F6 |

NOTES:

1 Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 000 → AF0; PCR.PA = 001 → AF1; PCR.PA = 010 → AF2; PCR.PA = 011 → AF3; PCR.PA = 100 → ALT4. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to ‘1’, regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as “—”.

2 Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

3 NMI[0] and NMI[1] have a higher priority than alternate functions. When NMI is selected, the PCR.PA field is ignored.

4 SXOSC’s OSC32k_XTAL and OSC32k_EXTAL pins are shared with GPIO functionality. When used as crystal pins, other functionality of the pin cannot be used and it should be ensured that application never programs OBE and PUE bit of the corresponding PCR to "1".

5 If you want to use OSC32K functionality through PB[8] and PB[9], you must ensure that PB[10] is static in nature as PB[10] can induce coupling on PB[9] and disturb oscillator frequency.

6 Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
PC[0:1] are available as JTAG pins (TDI and TDO respectively).
PH[9:10] are available as JTAG pins (TCK and TMS respectively).
It is up to the user to configure these pins as GPIO when needed.

7 When MBIST is enabled to run ( STCU Enable = 1), the application must not drive or tie PAD[178) (MDO[0]) to 0 V before the device exits reset (external reset is removed) as the pad is internally driven to 1 to indicate MBIST operation. When MBIST is not enabled (STCU Enable = 0), there are no restriction as the device does not internally drive the pad.

8 These pins can be configured as Nexus pins during reset by the debugger writing to the Nexus Development Interface "Port Control Register" rather than the SIUL. Specifically, the debugger can enable the MDO[7:0], MSEO, and MCKO ports by programming NDI (PCR[MCKO_EN] or PCR[PSTAT_EN]). MDO[8:11] ports can be enabled by programming NDI ((PCR[MCKO_EN] and PCR[FPM]) or PCR[PSTAT_EN]).

# 4 Electrical Characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level ($V_{DD}$ or $V_{SS_HV}$). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

## 4.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 5 are used and the parameters are tagged accordingly in the tables where appropriate.

**Table 5. Parameter classifications**

| Classification tag | Tag description |
|---|---|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

**NOTE**

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

## 4.2 NVUSRO register

Portions of the device configuration, such as high voltage supply is controlled via bit values in the Non-Volatile User Options Register (NVUSRO). For a detailed description of the NVUSRO register, see MPC5646C Reference Manual.

### 4.2.1 NVUSRO [PAD3V5V(0)] field description

Table 6 shows how NVUSRO [PAD3V5V(0)] controls the device configuration for $V_{DD_HV_A}$ domain.

**Table 6. PAD3V5V(0) field description**

| Value[1] | Description |
|---|---|
| 0 | High voltage supply is 5.0 V |
| 1 | High voltage supply is 3.3 V |

NOTES:
1 '1' is delivery value. It is part of shadow flash memory, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V(0,1) bit value.

### 4.2.2 NVUSRO [PAD3V5V(1)] field description

Table 7 shows how NVUSRO [PAD3V5V(1)] controls the device configuration the device configuration for $V_{DD_HV_B}$ domain.

**Table 7. PAD3V5V(1) field description**

| Value[1] | Description |
|---|---|
| 0 | High voltage supply is 5.0 V |
| 1 | High voltage supply is 3.3 V |

NOTES:
1 '1' is delivery value. It is part of shadow flash memory, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V(0,1) bit value.

## 4.3 Absolute maximum ratings

**Table 8. Absolute maximum ratings**

| Symbol | | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{SS_HV}$ | SR | Digital ground on VSS_HV pins | — | 0 | 0 | V |
| $V_{DD_HV_A}$ | SR | Voltage on VDD_HV_A pins with respect to ground ($V_{SS_HV}$) | — | –0.3 | 6.0 | V |
| $V_{DD_HV_B}$[1] | SR | Voltage on VDD_HV_B pins with respect to common ground ($V_{SS_HV}$) | — | –0.3 | 6.0 | V |
| $V_{SS_LV}$ | SR | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground ($V_{SS_HV}$) | — | $V_{SS_HV}$ – 0.1 | $V_{SS_HV}$ + 0.1 | V |

**Table 8. Absolute maximum ratings (continued)**

| Symbol | | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{RC_CTRL}$[2] | | Base control voltage for external BCP68 NPN device | Relative to $V_{DD_LV}$ | 0 | $V_{DD_LV}$ + 1 | V |
| $V_{SS_ADC}$ | SR | Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground ($V_{SS_HV}$) | — | $V_{SS_HV}$ – 0.1 | $V_{SS_HV}$ + 0.1 | V |
| $V_{DD_HV_ADC0}$ | SR | Voltage on VDD_HV_ADC0 with respect to ground ($V_{SS_HV}$) | — | –0.3 | 6.0 | V |
| | | | Relative to $V_{DD_HV_A}$[3] | $V_{DD_HV_A}$ – 0.3 | $V_{DD_HV_A}$+0.3 | |
| $V_{DD_HV_ADC1}$[4] | SR | Voltage on VDD_HV_ADC1 with respect to ground ($V_{SS_HV}$) | — | –0.3 | 6.0 | V |
| | | | Relative to $V_{DD_HV_A}$[2] | $V_{DD_HV_A}$–0.3 | $V_{DD_HV_A}$+0.3 | |
| $V_{IN}$ | SR | Voltage on any GPIO pin with respect to ground ($V_{SS_HV}$) | Relative to $V_{DD_HV_A/HV_B}$ | $V_{DD_HV_A/HV_B}$ –0.3 | $V_{DD_HV_A/HV_B}$ +0.3 | V |
| $I_{INJPAD}$ | SR | Injected input current on any pin during overload condition | — | –10 | 10 | mA |
| $I_{INJSUM}$ | SR | Absolute sum of all injected input currents during overload condition | — | –50 | 50 | |
| $I_{AVGSEG}$[5] | SR | Sum of all the static I/O current within a supply segment ($V_{DD_HV_A}$ or $V_{DD_HV_B}$) | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | | 70 | mA |
| | | | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | | 64 | |
| $T_{STORAGE}$ | SR | Storage temperature | — | –55[6] | 150 | °C |

NOTES:

1. $V_{DD_HV_B}$ can be independently controlled from $V_{DD_HV_A}$. These can ramp up or ramp down in any order. Design is robust against any supply order.
2. This voltage is internally generated by the device and no external voltage should be supplied.
3. Both the relative and the fixed conditions must be met. For instance: If $V_{DD_HV_A}$ is 5.9 V, $V_{DD_HV_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD_HV_A}$ + 0.3 = 6.2 V.
4. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD_HV_B}$ domain hence $V_{DD_HV_ADC1}$ should be within ±300 mV of $V_{DD_HV_B}$ when these channels are used for ADC_1.
5. Any temperature beyond 125 °C should limit the current to 50 mA (max).
6. This is the storage temperature for the flash memory.

**NOTE**

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD_HV_A/HV_B}$ or $V_{IN} < V_{SS_HV}$), the voltage on pins with respect to ground ($V_{SS_HV}$) must not exceed the recommended values.

## 4.4 Recommended operating conditions

**Table 9. Recommended operating conditions (3.3 V)**

| Symbol | | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{SS_HV}$ | SR | Digital ground on VSS_HV pins | — | 0 | 0 | V |
| $V_{DD_HV_A}$[1] | SR | Voltage on $V_{DD_HV_A}$ pins with respect to ground ($V_{SS_HV}$) | — | 3.0 | 3.6 | V |
| $V_{DD_HV_B}$[1] | SR | Voltage on $V_{DD_HV_B}$ pins with respect to ground ($V_{SS_HV}$) | — | 3.0 | 3.6 | V |
| $V_{SS_LV}$[2] | SR | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground ($V_{SS_HV}$) | — | $V_{SS_HV}$ – 0.1 | $V_{SS_HV}$ + 0.1 | V |
| $V_{RC_CTRL}$[3] | | Base control voltage for external BCP68 NPN device | Relative to $V_{DD_LV}$ | 0 | $V_{DD_LV}$ + 1 | V |
| $V_{SS_ADC}$ | SR | Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground ($V_{SS_HV}$) | — | $V_{SS_HV}$ – 0.1 | $V_{SS_HV}$ + 0.1 | V |
| $V_{DD_HV_ADC0}$[4] | SR | Voltage on VDD_HV_ADC0 with respect to ground ($V_{SS_HV}$) | — | 3.0[5] | 3.6 | V |
| | | | Relative to $V_{DD_HV_A}$[6] | $V_{DD_HV_A}$ – 0.1 | $V_{DD_HV_A}$ + 0.1 | |
| $V_{DD_HV_ADC1}$[7] | SR | Voltage on VDD_HV_ADC1 with respect to ground ($V_{SS_HV}$) | — | 3.0 | 3.6 | V |
| | | | Relative to $V_{DD_HV_A}$[6] | $V_{DD_HV_A}$ – 0.1 | $V_{DD_HV_A}$ + 0.1 | |
| $V_{IN}$ | SR | Voltage on any GPIO pin with respect to ground ($V_{SS_HV}$) | — | $V_{SS_HV}$ – 0.1 | — | V |
| | | | Relative to $V_{DD_HV_A/HV_B}$ | — | $V_{DD_HV_A/HV_B}$ + 0.1 | |

**Table 9. Recommended operating conditions (3.3 V) (continued)**

| Symbol | | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $I_{INJPAD}$ | SR | Injected input current on any pin during overload condition | — | –5 | 5 | mA |
| $I_{INJSUM}$ | SR | Absolute sum of all injected input currents during overload condition | — | –50 | 50 | |
| $TV_{DD}$ | SR | $V_{DD_HV_A}$ slope to ensure correct power up[8] | — | — | 0.5 | V/µs |
| | | | — | 0.5 | — | V/min |
| $T_A$ | SR | Ambient temperature under bias | $f_{CPU}$ up to 120 MHz + 2% | –40 | 125 | °C |
| $T_J$ | SR | Junction temperature under bias | — | –40 | 150 | |

NOTES:
1. 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
2. 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 µF bulk capacitance needs to be provided as CREG on each VDD_LV pin. For details refer to the Power Management chapter of the MPC5646C Reference Manual.
3. This voltage is internally generated by the device and no external voltage should be supplied.
4. 100 nF capacitance needs to be provided between $V_{DD_ADC}/V_{SS_ADC}$ pair.
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below $V_{LVDHVL}$, device is reset.
6. Both the relative and the fixed conditions must be met. For instance: If $V_{DD_HV_A}$ is 5.9 V, $V_{DD_HV_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD_HV_A}$ + 0.3 = 6.2 V.
7. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD_HV_B}$ domain hence $V_{DD_HV_ADC1}$ should be within ±100 mV of $V_{DD_HV_B}$ when these channels are used for ADC_1.
8. Guaranteed by the device validation.

**Table 10. Recommended operating conditions (5.0 V)**

| Symbol | | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{SS_HV}$ | SR | Digital ground on VSS_HV pins | — | 0 | 0 | V |
| $V_{DD_HV_A}$[1] | SR | Voltage on VDD_HV_A pins with respect to ground ($V_{SS_HV}$) | — | 4.5 | 5.5 | V |
| | | | Voltage drop[2] | 3.0 | 5.5 | |
| $V_{DD_HV_B}$ | SR | Generic GPIO functionality | — | 3.0 | 5.5 | V |
| | | Ethernet/3.3 V functionality (See the notes in all figures in Section 3, "Package pinouts and signal descriptions" for the list of channels operating in $V_{DD_HV_B}$ domain) | — | 3.0 | 3.6 | V |

**Table 10. Recommended operating conditions (5.0 V) (continued)**

| Symbol | | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{SS_LV}$[3] | SR | Voltage on VSS_LV (Low voltage digital supply) pins with respect to ground ($V_{SS_HV}$) | — | $V_{SS_HV}$ – 0.1 | $V_{SS_HV}$ + 0.1 | V |
| $V_{RC_CTRL}$[4] | | Base control voltage for external BCP68 NPN device | Relative to $V_{DD_LV}$ | 0 | $V_{DD_LV}$ + 1 | V |
| $V_{SS_ADC}$ | SR | Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground ($V_{SS_HV}$) | — | $V_{SS_HV}$ – 0.1 | $V_{SS_HV}$ + 0.1 | V |
| $V_{DD_HV_ADC0}$[5] | SR | Voltage on VDD_HV_ADC0 with respect to ground ($V_{SS_HV}$) | — | 4.5 | 5.5 | V |
| | | | Voltage drop(2) | 3.0 | 5.5 | |
| | | | Relative to $V_{DD_HV_A}$[6] | $V_{DD_HV_A}$ – 0.1 | $V_{DD_HV_A}$ + 0.1 | |
| $V_{DD_HV_ADC1}$[7] | SR | Voltage on VDD_HV_ADC1 with respect to ground ($V_{SS_HV}$) | — | 4.5 | 5.5 | V |
| | | | Voltage drop(2) | 3.0 | 5.5 | |
| | | | Relative to $V_{DD_HV_A}$[6] | $V_{DD_HV_A}$ – 0.1 | $V_{DD_HV_A}$ + 0.1 | |
| $V_{IN}$ | SR | Voltage on any GPIO pin with respect to ground ($V_{SS_HV}$) | — | $V_{SS_HV}$ –0.1 | — | V |
| | | | Relative to $V_{DD_HV_A/HV_B}$ | — | $V_{DD_HV_A/HV_B}$ + 0.1 | |
| $I_{INJPAD}$ | SR | Injected input current on any pin during overload condition | — | –5 | 5 | mA |
| $I_{INJSUM}$ | SR | Absolute sum of all injected input currents during overload condition | — | –50 | 50 | |
| $TV_{DD}$ | SR | $V_{DD_HV_A}$ slope to ensure correct power up[8] | — | — | 0.5 | V/µs |
| | | | — | 0.5 | — | V/min |
| $T_{A}$ C-Grade Part | SR | Ambient temperature under bias | — | –40 | 85 | °C |
| $T_{J}$ C-Grade Part | SR | Junction temperature under bias | — | –40 | 110 | |
| $T_{A}$ V-Grade Part | SR | Ambient temperature under bias | — | –40 | 105 | |
| $T_{J}$ V-Grade Part | SR | Junction temperature under bias | — | –40 | 130 | |
| $T_{A}$ M-Grade Part | SR | Ambient temperature under bias | — | –40 | 125 | |
| $T_{J}$ M-Grade Part | SR | Junction temperature under bias | — | –40 | 150 | |

NOTES:
1. 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
2. Full device operation is guaranteed by design from 3.0 V–5.5 V. OSC functionality is guaranteed from the entire range 3.0V–5.5 V, the parametrics measured are at 3.0V and 5.5V (extreme voltage ranges to cover the range of operation). The parametrics might have some variation in the intermediate voltage range, but there is no impact to functionality.
3. 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 µF bulk capacitance needs to be provided as CREG on each VDD_LV pin.

4 This voltage is internally generated by the device and no external voltage should be supplied.

5 100 nF capacitance needs to be provided between $V_{DD_HV_(ADC0/ADC1)}$/$V_{SS_HV_(ADC0/ADC1)}$ pair.

6 Both the relative and the fixed conditions must be met. For instance: If $V_{DD_HV_A}$ is 5.9 V, $V_{DD_HV_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD_HV_A}$ + 0.3 = 6.2 V.

7 PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD_HV_B}$ domain hence VDD_HV_ADC1 should be within ±100 mV of $V_{DD_HV_B}$ when these channels are used for ADC_1.

8 Guaranteed by device validation.

**NOTE**

SRAM retention guaranteed to LVD levels.

## 4.5 Thermal characteristics

### 4.5.1 Package thermal characteristics

**Table 11. LQFP thermal characteristics[1]**

| Symbol | | C | Parameter | Conditions[2] | Pin count | Value[3] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $R_{\theta JA}$ | CC | D | Thermal resistance, junction-to-ambient natural convection[4] | Single-layer board—1s | 176 | — | — | 38[5] | °C/W |
| | | | | | 208 | — | — | 41[6] | °C/W |
| $R_{\theta JA}$ | CC | D | Thermal resistance, junction-to-ambient natural convection[7] | Four-layer board—2s2p[7] | 176 | — | — | 31 | °C/W |
| | | | | | 208 | — | — | 34 | °C/W |

NOTES:

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C.

3 All values need to be confirmed during device validation.

4 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

5 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6.

6 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-2 and JESD51-6

7 Junction-to-Board thermal resistance determined per JEDEC JESD51-8.

**Table 12. 256 MAPBGA thermal characteristics[1]**

| Symbol | | C | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | CC | — | Thermal resistance, junction-to-ambient natural convection | Single-layer board—1s | 43[2] | °C/W |
| | | | | Four-layer board—2s2p | 26[3] | |

NOTES:

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-ambient thermal resistance determined per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

3 Junction-to-ambient thermal resistance determined per JEDEC JESD51-6 with the board horizontal.

### 4.5.2 Power considerations

The average chip-junction temperature, $T_J$, in degrees Celsius, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \textit{Eqn. 1}$$

Where:

$T_A$ is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

$P_D$ is the sum of $P_{INT}$ and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

$P_{INT}$ is the product of $I_{DD}$ and $V_{DD}$, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2 \quad \textit{Eqn. 3}$$

Where:

K is a constant for the particular part, which may be determined from Equation 3 by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ may be obtained by solving equations 1 and 2 iteratively for any value of $T_A$.

## 4.6 I/O pad electrical characteristics

### 4.6.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—These pads provide maximum speed. These are used for improved Nexus debugging capability.
- Input only pads—These pads are associated to ADC channels and 32 kHz low power external crystal oscillator providing low input leakage.
- Low power pads—These pads are active in standby mode for wakeup source.

Also, medium/slow and fast/medium pads are available in design which can be configured to behave like a slow/medium and medium/fast pads depending upon the slew-rate control.

Medium and fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

## 4.6.2 I/O input DC characteristics

Table 13 provides input DC electrical characteristics as described in Figure 5.

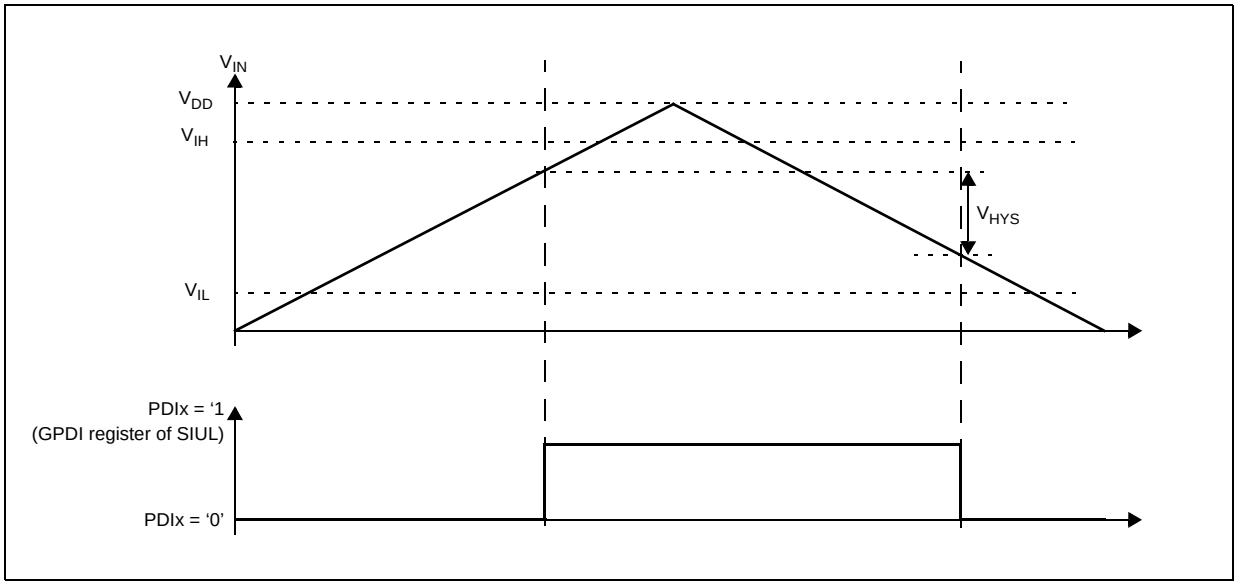



**Figure 5. I/O input DC electrical characteristics definition**

**Table 13. I/O input DC electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $V_{IH}$ | SR | P | Input high level CMOS (Schmitt Trigger) | — | | $0.65V_{DD}$ | — | $V_{DD}$ + 0.4 | V |
| $V_{IL}$ | SR | P | Input low level CMOS (Schmitt Trigger) | — | | –0.3 | — | $0.35V_{DD}$ | |
| $V_{HYS}$ | CC | C | Input hysteresis CMOS (Schmitt Trigger) | — | | $0.1V_{DD}$ | — | — | |
| $I_{LKG}$ | CC | P | Digital input leakage | No injection on adjacent pin | $T_A$ = –40 °C | — | 2 | — | nA |
| | | P | | | $T_A$ = 25 °C | — | 2 | — | |
| | | D | | | $T_A$ = 105 °C | — | 12 | 500 | |
| | | P | | | $T_A$ = 125 °C | — | 70 | 1000 | |
| $W_{FI}$ | SR | P | Width of input pulse rejected by analog filter[3] | — | | — | — | 40[4] | ns |
| $W_{NFI}$ | SR | P | Width of input pulse accepted by analog filter(3) | — | | 1000[4] | — | — | ns |

NOTES:
1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.

2 $V_{DD}$ as mentioned in the table is $V_{DD_HV_A}$/$V_{DD_HV_B}$. All values need to be confirmed during device validation.
3 Analog filters are available on all wakeup lines.
4 The width of input pulse in between 40 ns to 1000 ns is indeterminate. It may pass the noise or may not depending on silicon sample to sample variation.

## 4.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 14 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 15 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 16 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 17 provides output driver characteristics for I/O pads when in FAST configuration.

**Table 14. I/O pull-up/pull-down DC electrical characteristics**

| Symbol | | C | Parameter | Conditions[1,2] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $\|I_{WPU}\|$ | CC | P | Weak pull-up current absolute value | $V_{IN} = V_{IL}$, $V_{DD}$ = 5.0 V ± 10% | PAD3V5V = 0 | 10 | — | 150 | µA |
| | | C | | | PAD3V5V = 1[3] | 10 | — | 250 | |
| | | P | | $V_{IN} = V_{IL}$, $V_{DD}$ = 3.3 V ± 10% | PAD3V5V = 1 | 10 | — | 150 | |
| $\|I_{WPD}\|$ | CC | P | Weak pull-down current absolute value | $V_{IN} = V_{IH}$, $V_{DD}$ = 5.0 V ± 10% | PAD3V5V = 0 | 10 | — | 150 | µA |
| | | C | | | PAD3V5V = 1 | 10 | — | 250 | |
| | | P | | $V_{IN} = V_{IH}$, $V_{DD}$ = 3.3 V ± 10% | PAD3V5V = 1 | 10 | — | 150 | |

NOTES:
1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2 $V_{DD}$ as mentioned in the table is $V_{DD_HV_A}$/$V_{DD_HV_B}$.
3 The configuration PAD3V5 = 1 when $V_{DD}$ = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

**Table 15. SLOW configuration output buffer electrical characteristics**

| Symbol | | C | Parameter | Conditions[1,2] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $V_{OH}$ | CC | P | Output high level SLOW configuration | Push Pull | $I_{OH}$ = –3 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | 0.8$V_{DD}$ | — | — | V |
| | | C | | | $I_{OH}$ = –3 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[3] | 0.8$V_{DD}$ | — | — | |
| | | P | | | $I_{OH}$ = –1.5 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | $V_{DD}$ – 0.8 | — | — | |

**Table 15. SLOW configuration output buffer electrical characteristics (continued)**

| Symbol | | C | Parameter | Conditions[1,2] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $V_{OL}$ | CC | P | Output low level SLOW configuration | Push Pull | $I_{OL}$ = 3 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | $0.1V_{DD}$ | V |
| | | C | | | $I_{OL}$ = 3 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[3] | — | — | $0.1V_{DD}$ | |
| | | P | | | $I_{OL}$ = 1.5 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 0.5 | |

NOTES:
1. $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2. $V_{DD}$ as mentioned in the table is $V_{DD_HV_A}$/$V_{DD_HV_B}$.
3. The configuration PAD3V5 = 1 when $V_{DD}$ = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

**Table 16. MEDIUM configuration output buffer electrical characteristics**

| Symbol | | C | Parameter | Conditions[1,2] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $V_{OH}$ | CC | C | Output high level MEDIUM configuration | Push Pull | $I_{OH}$ = –3 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | $0.8V_{DD}$ | — | — | V |
| | | C | | | $I_{OH}$ = –1.5 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[3] | $0.8V_{DD}$ | — | — | |
| | | C | | | $I_{OH}$ = –2 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | $V_{DD}$ – 0.8 | — | — | |
| $V_{OL}$ | CC | C | Output low level MEDIUM configuration | Push Pull | $I_{OL}$ = 3 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | $0.2V_{DD}$ | V |
| | | C | | | $I_{OL}$ = 1.5 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[3] | — | — | $0.1V_{DD}$ | |
| | | C | | | $I_{OL}$ = 2 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 0.5 | |

NOTES:
1. $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2. $V_{DD}$ as mentioned in the table is $V_{DD_HV_A}$/$V_{DD_HV_B}$.
3. The configuration PAD3V5 = 1 when $V_{DD}$ = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

**Table 17. FAST configuration output buffer electrical characteristics**

| Symbol | | C | Parameter | Conditions[1,2] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $V_{OH}$ | CC | P | Output high level FAST configuration | Push Pull | $I_{OH}$ = –14 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | $0.8V_{DD}$ | — | — | V |
| | | C | | | $I_{OH}$ = –7 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[3] | $0.8V_{DD}$ | — | — | |
| | | C | | | $I_{OH}$ = –11 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | $V_{DD}$ – 0.8 | — | — | |
| $V_{OL}$ | CC | P | Output low level FAST configuration | Push Pull | $I_{OL}$ = 14 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | $0.1V_{DD}$ | V |
| | | C | | | $I_{OL}$ = 7 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1(3) | — | — | $0.1V_{DD}$ | |
| | | C | | | $I_{OL}$ = 11 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 0.5 | |

NOTES:
1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2 $V_{DD}$ as mentioned in the table is $V_{DD_HV_A}$/$V_{DD_HV_B}$.
3 The configuration PAD3V5 = 1 when $V_{DD}$ = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus outputs (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

## 4.6.4 Output pin transition times

**Table 18. Output pin transition times**

| Symbol | | C | Parameter | Conditions[1,2] | | Value[3] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $T_{tr}$ | CC | D | Output transition time output pin[4] SLOW configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 50 | ns |
| | | T | | $C_L$ = 50 pF | | — | — | 100 | |
| | | D | | $C_L$ = 100 pF | | — | — | 125 | |
| | | D | | $C_L$ = 25 pF | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 40 | |
| | | T | | $C_L$ = 50 pF | | — | — | 50 | |
| | | D | | $C_L$ = 100 pF | | — | — | 75 | |

**Table 18. Output pin transition times (continued)**

| Symbol | | C | Parameter | Conditions[1,2] | | Value[3] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $T_{tr}$ | CC | D | Output transition time output pin[4] MEDIUM configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1 | — | — | 10 | ns |
| | | T | | $C_L$ = 50 pF | | — | — | 20 | |
| | | D | | $C_L$ = 100 pF | | — | — | 40 | |
| | | D | | $C_L$ = 25 pF | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1 | — | — | 12 | |
| | | T | | $C_L$ = 50 pF | | — | — | 25 | |
| | | D | | $C_L$ = 100 pF | | — | — | 40 | |
| $T_{tr}$ | CC | D | Output transition time output pin[4] FAST configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 4 | ns |
| | | | | $C_L$ = 50 pF | | — | — | 6 | |
| | | | | $C_L$ = 100 pF | | — | — | 12 | |
| | | | | $C_L$ = 25 pF | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 4 | |
| | | | | $C_L$ = 50 pF | | — | — | 7 | |
| | | | | $C_L$ = 100 pF | | — | — | 12 | |

NOTES:
1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2 $V_{DD}$ as mentioned in the table is $V_{DD_HV_A}$/$V_{DD_HV_B}$.
3 All values need to be confirmed during device validation.
4 $C_L$ includes device and package capacitances ($C_{PKG}$ < 5 pF).

## 4.6.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply is associated to a $V_{DD}$/$V_{SS_HV}$ supply pair as described in Table 19.

Table 20 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the $I_{AVGSEG}$ maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the $I_{DYNSEG}$ maximum value.

**Table 19. I/O supplies**

| Package | I/O Supplies | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 256 MAPBGA | Equivalent to 208-pin LQFP segment pad distribution + G6, G11, H11, J11 | | | | | | | |
| 208 LQFP | pin6 ($V_{DD_HV_A}$) pin7 ($V_{SS_HV}$) | pin27 ($V_{DD_HV_A}$) pin28 ($V_{SS_HV}$) | pin73 ($V_{SS_HV}$) pin75 ($V_{DD_HV_A}$) | pin101 ($V_{DD_HV_A}$) pin102 ($V_{SS_HV}$) | pin132 ($V_{SS_HV}$) pin133 ($V_{DD_HV_A}$) | pin147 ($V_{SS_HV}$) pin148 ($V_{DD_HV_B}$) | pin174 ($V_{SS_HV}$) pin175 ($V_{DD_HV_A}$) | — |

**Table 19. I/O supplies (continued)**

| Package | I/O Supplies | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 176 LQFP | pin6 ($V_{DD_HV_A}$)<br>pin7 ($V_{SS_HV}$) | pin27 ($V_{DD_HV_A}$)<br>pin28 ($V_{SS_HV}$) | pin57 ($V_{SS_HV}$)<br>pin59 ($V_{DD_HV_A}$) | pin85 ($V_{DD_HV_A}$)<br>pin86 ($V_{SS_HV}$) | pin123 ($V_{SS_HV}$)<br>pin124 ($V_{DD_HV_B}$) | pin150 ($V_{SS_HV}$)<br>pin151 ($V_{DD_HV_A}$) | — | — |

**Table 20. I/O consumption**

| Symbol | | C | Parameter | Conditions[1,2] | | Value[3] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $I_{SWTSLW}$[4] | CC | D | Peak I/O current for SLOW configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 19.9 | mA |
| | | | | | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 15.5 | |
| $I_{SWTMED}$(4) | CC | D | Peak I/O current for MEDIUM configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 28.8 | mA |
| | | | | | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 16.3 | |
| $I_{SWTFST}$(4) | CC | D | Peak I/O current for FAST configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 113.5 | mA |
| | | | | | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 52.1 | |
| $I_{RMSSLW}$ | CC | D | Root mean square I/O current for SLOW configuration | $C_L$ = 25 pF, 2 MHz | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 2.22 | mA |
| | | | | $C_L$ = 25 pF, 4 MHz | | — | — | 3.13 | |
| | | | | $C_L$ = 100 pF, 2 MHz | | — | — | 6.54 | |
| | | | | $C_L$ = 25 pF, 2 MHz | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 1.51 | |
| | | | | $C_L$ = 25 pF, 4 MHz | | — | — | 2.14 | |
| | | | | $C_L$ = 100 pF, 2 MHz | | — | — | 4.33 | |
| $I_{RMSMED}$ | CC | D | Root mean square I/O current for MEDIUM configuration | $C_L$ = 25 pF, 13 MHz | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 6.5 | mA |
| | | | | $C_L$ = 25 pF, 40 MHz | | — | — | 13.32 | |
| | | | | $C_L$ = 100 pF, 13 MHz | | — | — | 18.26 | |
| | | | | $C_L$ = 25 pF, 13 MHz | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 4.91 | |
| | | | | $C_L$ = 25 pF, 40 MHz | | — | — | 8.47 | |
| | | | | $C_L$ = 100 pF, 13 MHz | | — | — | 10.94 | |
| $I_{RMSFST}$ | CC | D | Root mean square I/O current for FAST configuration | $C_L$ = 25 pF, 40 MHz | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 21.05 | mA |
| | | | | $C_L$ = 25 pF, 64 MHz | | — | — | 33 | |
| | | | | $C_L$ = 100 pF, 40 MHz | | — | — | 55.77 | |
| | | | | $C_L$ = 25 pF, 40 MHz | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 14 | |
| | | | | $C_L$ = 25 pF, 64 MHz | | — | — | 20 | |
| | | | | $C_L$ = 100 pF, 40 MHz | | — | — | 34.89 | |

**Table 20. I/O consumption (continued)**

| Symbol | | C | Parameter | Conditions[1,2] | Value[3] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $I_{AVGSEG}$ | SR | D | Sum of all the static I/O current within a supply segment | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 70 | mA |
| | | | | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 65[4] | |

NOTES:
1. $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2. $V_{DD}$ as mentioned in the table is $V_{DD_HV_A}$/$V_{DD_HV_B}$.
3. All values need to be confirmed during device validation.
4. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

## 4.7 RESET electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

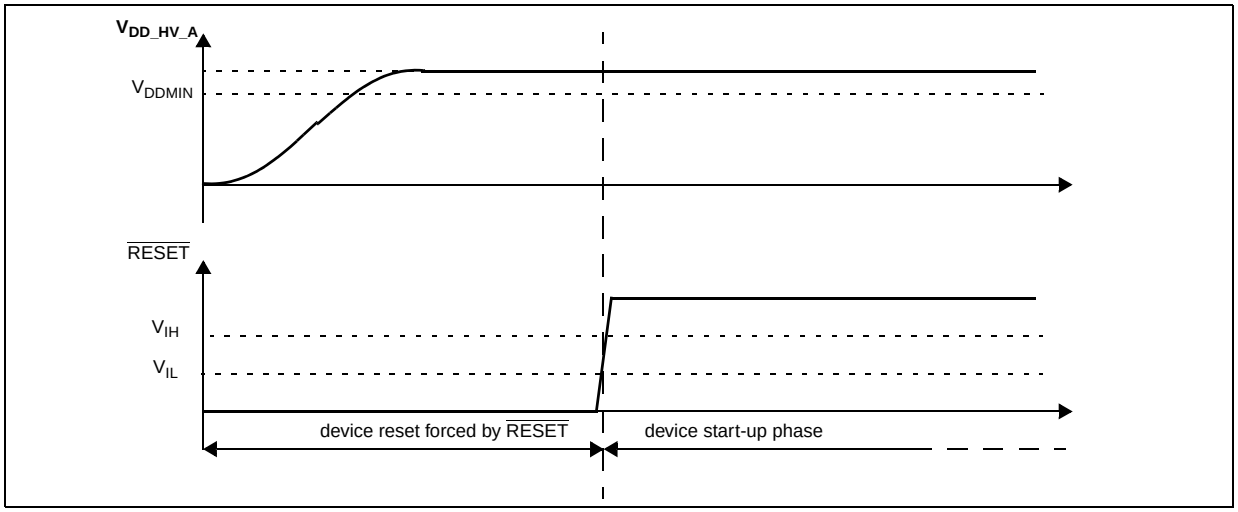



**Figure 6. Start-up reset requirements**

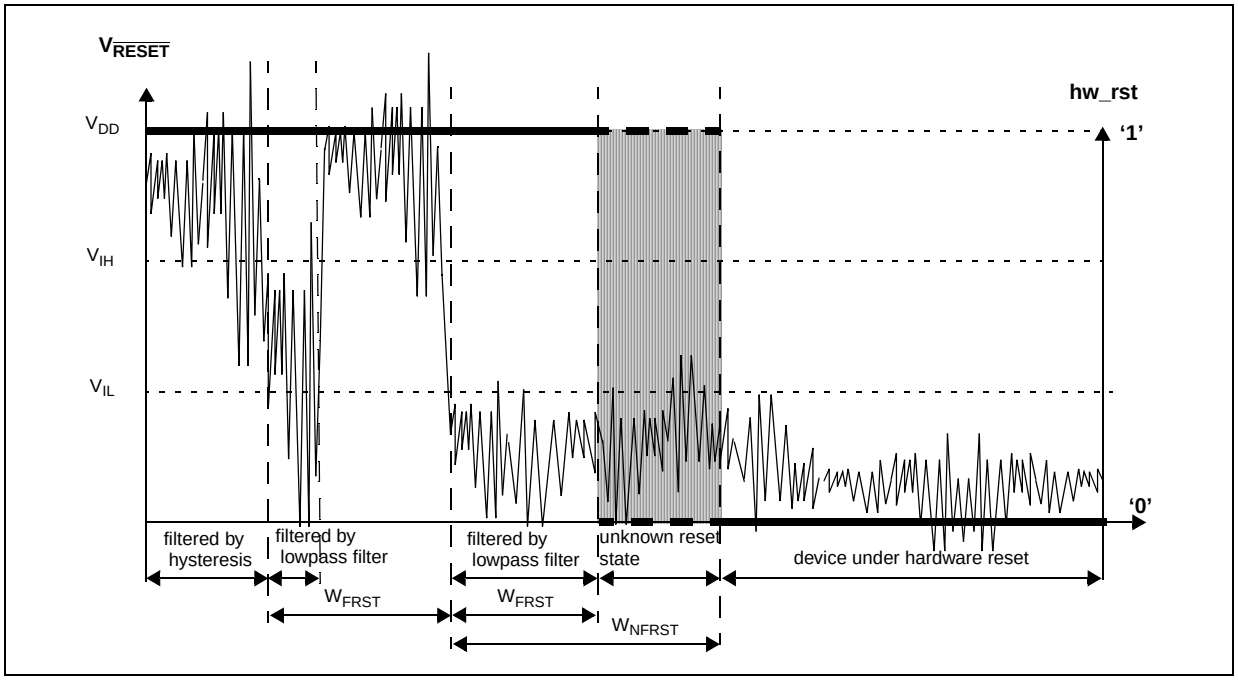



**Figure 7. Noise filtering on reset signal**

**Table 21. Reset electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{IH}$ | SR | P | Input High Level CMOS (Schmitt Trigger) | — | $0.65V_{DD}$ | — | $V_{DD}$ + 0.4 | V |
| $V_{IL}$ | SR | P | Input low Level CMOS (Schmitt Trigger) | — | –0.3 | — | $0.35V_{DD}$ | V |
| $V_{HYS}$ | CC | C | Input hysteresis CMOS (Schmitt Trigger) | — | $0.1V_{DD}$ | — | — | V |
| $V_{OL}$ | CC | P | Output low level | Push Pull, $I_{OL}$ = 2 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | $0.1V_{DD}$ | V |
| | | | | Push Pull, $I_{OL}$ = 1 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[3] | — | — | $0.1V_{DD}$ | |
| | | | | Push Pull, $I_{OL}$ = 1 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |

**Table 21. Reset electrical characteristics (continued)**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $T_{tr}$ | CC | D | Output transition time output pin[4] MEDIUM configuration | $C_L$ = 25 pF, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 10 | ns |
| | | | | $C_L$ = 50 pF, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 20 | |
| | | | | $C_L$ = 100 pF, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 40 | |
| | | | | $C_L$ = 25 pF, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 12 | |
| | | | | $C_L$ = 50 pF, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 25 | |
| | | | | $C_L$ = 100 pF, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 40 | |
| $W_{FRST}$ | SR | P | Reset input filtered pulse | — | — | — | 40 | ns |
| $W_{NFRST}$ | SR | P | Reset input not filtered pulse | — | 1000 | — | — | ns |
| $\|I_{WPU}\|$ | CC | P | Weak pull-up current absolute value | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | 10 | — | 150 | µA |
| | | | | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | 10 | — | 150 | |
| | | | | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[5] | 10 | — | 250 | |

NOTES:
1. $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2. $V_{DD}$ as mentioned in the table is $V_{DD_HV_A}$/$V_{DD_HV_B}$. All values need to be confirmed during device validation.
3. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to the RGM module section of the device Reference Manual).
4. $C_L$ includes device and package capacitance ($C_{PKG}$ < 5 pF).
5. The configuration PAD3V5 = 1 when $V_{DD}$ = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

## 4.8 Power management electrical characteristics

### 4.8.1 Voltage regulator electrical characteristics

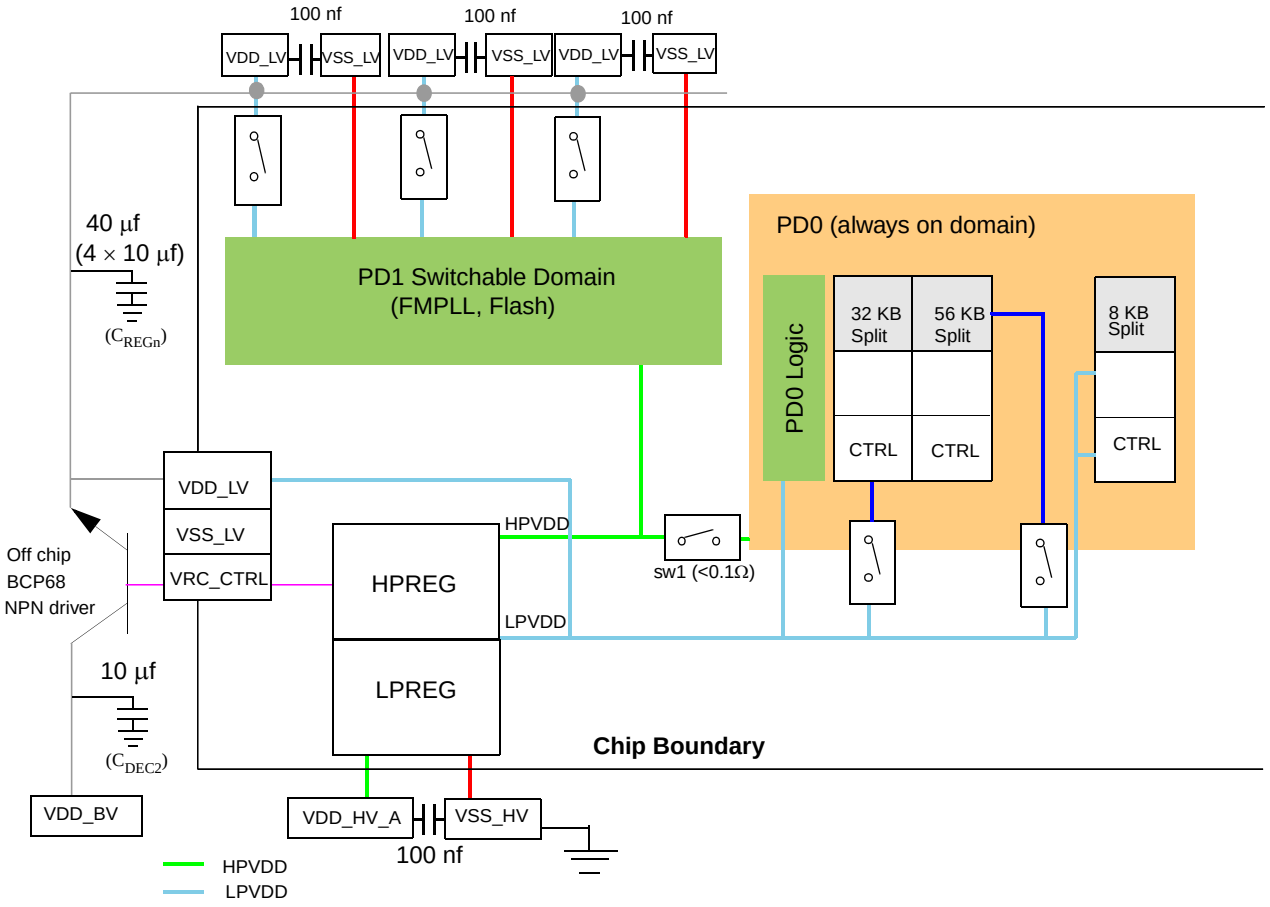
The device implements an internal voltage regulator to generate the low voltage core supply $V_{DD_LV}$ from the high voltage supply $V_{DD_HV_A}$. The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through $V_{DD_HV_A}$ power pin.
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the on-chip VREG with an external ballast (BCP68 NPN device). It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.

— LV_CFLA0/CFLA1: Low voltage supply for the two code Flash modules. It is shorted with LV_COR through double bonding.

— LV_DFLA: Low voltage supply for data Flash module. It is shorted with LV_COR through double bonding.

— LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.




1) All VSS_LV pins must be grounded, as shown for VSS_HV pin.

**Figure 8. Voltage regulator capacitance connection**

The internal voltage regulator requires external bulk capacitance ($C_{REGn}$) to be connected to the device to provide a stable low voltage digital supply to the device. Also required for stability is the $C_{DEC2}$ capacitor at ballast collector. This is needed to minimize sharp injection current when ballast is turning ON. Apart from the bulk capacitance, user should connect EMI/decoupling cap ($C_{REGP}$) at each $V_{DD_LV}/V_{SS_LV}$ pin pair.

### 4.8.1.1 Recommendations

- The external NPN driver must be BCP68 type.
- $V_{DD_LV}$ should be implemented as a power plane from the emitter of the ballast transistor.

- 10 µF capacitors should be connected to the 4 pins closest to the outside of the package and should be evenly distributed around the package. For BGA packages, the balls should be used are D8, H14, R9, J3–one cap on each side of package.
  - There should be a track direct from the capacitor to this pin (pin also connects to $V_{DD_LV}$ plane). The tracks ESR should be less than 100 mΩ.
  - The remaining $V_{DD_LV}$ pins (exact number will vary with package) should be decoupled with 0.1 µF caps, connected to the pin as per 10 µF.

(see Section 4.4, "Recommended operating conditions").

### 4.8.2 $V_{DD_BV}$ options

- Option 1: $V_{DD_BV}$ shared with $V_{DD_HV_A}$

  $V_{DD_BV}$ must be star routed from $V_{DD_HV_A}$ from the common source. This is to eliminate ballast noise injection on the MCU.
- Option 2: $V_{DD_BV}$ independent of the MCU supply

  $V_{DD_BV}$ > 2.6 V for correct functionality. The device is not monitoring this supply hence the external component must meet the 2.6 V criteria through external monitoring if required.

**Table 22. Voltage regulator electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $C_{REGn}$ | SR | — | External ballast stability capacitance | — | 40 | — | 60 | µF |
| $R_{REG}$ | SR | — | Stability capacitor equivalent serial resistance | — | — | — | 0.2 | Ω |
| $C_{REGP}$ | SR | — | Decoupling capacitance (Close to the pin) | $V_{DD_HV_A/HV_B}/V_{SS_HV}$ pair | | 100 | — | nF |
| | | | | $V_{DD_LV}/V_{SS_LV}$ pair | | 100 | — | nF |
| $C_{DEC2}$ | SR | — | Stability capacitance regulator supply (Close to the ballast collector) | $V_{DD_BV}/V_{SS_HV}$ | 10 | — | 40 | µF |
| $V_{MREG}$ | CC | P | Main regulator output voltage | Before trimming | — | 1.32 | — | V |
| | | | | After trimming<br>$T_A$ = 25 °C | 1.20 | 1.28 | — | |
| $I_{MREG}$ | SR | — | Main regulator current provided to $V_{DD_LV}$ domain | — | — | — | 350 | mA |
| $I_{MREGINT}$ | CC | D | Main regulator module current consumption | $I_{MREG}$ = 200 mA | — | — | 2 | mA |
| | | | | $I_{MREG}$ = 0 mA | — | — | 1 | |
| $V_{LPREG}$ | CC | P | Low power regulator output voltage | After trimming<br>$T_A$ = 25 °C | 1.21 | 1.27 | — | V |
| $I_{LPREG}$ | SR | — | Low power regulator current provided to $V_{DD_LV}$ domain | — | — | — | 50 | mA |

**Table 22. Voltage regulator electrical characteristics (continued)**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $I_{LPREGINT}$ | CC | D | Low power regulator module current consumption | $I_{LPREG}$ = 15 mA; $T_A$ = 55 °C | — | — | 600 | µA |
| | | — | | $I_{LPREG}$ = 0 mA; $T_A$ = 55 °C | — | 20 | — | |
| $I_{VREGREF}$ | CC | D | Main LVDs and reference current consumption (low power and main regulator switched off) | $T_A$ = 55 °C | — | 2 | — | µA |
| $I_{VREDLVD12}$ | CC | D | Main LVD current consumption (switch-off during standby) | $T_A$ = 55 °C | — | 1 | — | µA |
| $I_{DD_HV_A}$ | CC | D | In-rush current on $V_{DD_BV}$ during power-up | — | — | — | 600[3] | mA |

NOTES:
1. $V_{DD_HV_A}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Inrush current is seen more like steps of 600 mA peak. The startup of the regulator happens in steps of 50 mV in ~25 steps to reach ~1.2 V $V_{DD_LV}$. Each step peak current is within 600 mA

## 4.8.3 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the $V_{DD_HV_A}$ and the $V_{DD_LV}$ voltage while device is supplied:

- POR monitors $V_{DD_HV_A}$ during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors $V_{DD_HV_A}$ to ensure device is reset below minimum functional supply
- LVDHV5 monitors $V_{DD_HV_A}$ when application uses device in the 5.0 V±10% range
- LVDLVCOR monitors power domain No. 1 (PD1)
- LVDLVBKP monitors power domain No. 0 (PD0). VDD_LV is same as PD0 supply.

**NOTE**

When enabled, PD2 (RAM retention) is monitored through LVD_DIGBKP.

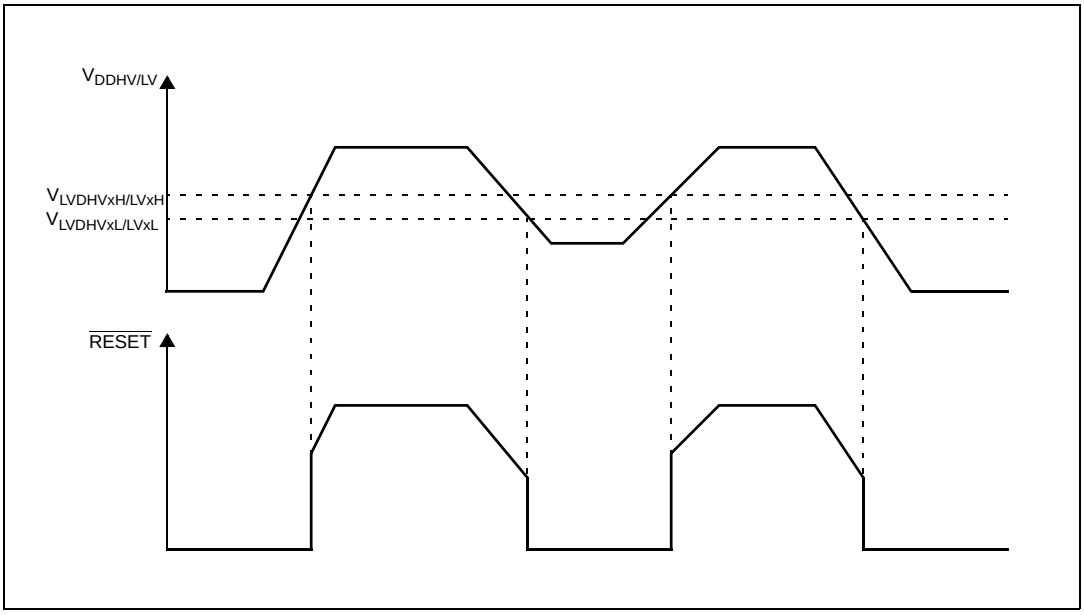



**Figure 9. Low voltage monitor vs. Reset**

**Table 23. Low voltage monitor electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{PORUP}$ | SR | P | Supply for functional POR module | — | 1.0 | — | 5.5 | V |
| $V_{PORH}$ | CC | P | Power-on reset threshold | — | 1.5 | — | 2.6 | |
| $V_{LVDHV3H}$ | CC | T | LVDHV3 low voltage detector high threshold | — | 2.7 | — | 2.85 | |
| $V_{LVDHV3L}$ | CC | T | LVDHV3 low voltage detector low threshold | — | 2.6 | — | 2.74 | |
| $V_{LVDHV5H}$ | CC | T | LVDHV5 low voltage detector high threshold | — | 4.3 | — | 4.5 | |
| $V_{LVDHV5L}$ | CC | T | LVDHV5 low voltage detector low threshold | — | 4.2 | — | 4.4 | |
| $V_{LVDLVCORL}$ | CC | P | LVDLVCOR low voltage detector low threshold | $T_A$ = 25 °C, after trimming | 1.12 | 1.145 | 1.17 | |
| $V_{LVDLVBKPL}$ | CC | P | LVDLVBKP low voltage detector low threshold | | 1.12 | 1.145 | 1.17 | |

NOTES:
1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2 All values need to be confirmed during device validation.

## 4.9 Low voltage domain power consumption

Table 24 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

**Table 24. Low voltage power domain electrical characteristics[1]**

| Symbol | | C | Parameter | Conditions[2] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ[3] | Max[4] | |
| $I_{DDMAX}$[5] | CC | D | RUN mode maximum average current | — | | — | 210 | 300[6,7] | mA |
| $I_{DDRUN}$ | CC | P | RUN mode typical average current[8] | at 120 MHz | $T_A$ = 25 °C | — | 150 | 200[9] | mA |
| | | D | | at 80 MHz | $T_A$ = 25 °C | — | 110[8] | 150[10] | mA |
| | | C | | at 120 MHz | $T_A$ = 125 °C | — | 180 | 270 | mA |
| $I_{DDHALT}$ | CC | P | HALT mode current[11] | at 120 MHz | $T_A$ = 25 °C | — | 20 | 27 | mA |
| | | C | | at 120 MHz | $T_A$ = 125 °C | — | 35 | 113 | mA |
| $I_{DDSTOP}$ | CC | P | STOP mode current[12] | No clocks active | $T_A$ = 25 °C | — | 0.4 | 3 | mA |
| | | C | | | $T_A$ = 125 °C | — | 16 | 95 | mA |
| $I_{DDSTDBY3}$ (96 KB RAM retained) | CC | P | STANDBY3 mode current[13] | No clocks active | $T_A$ = 25 °C | — | 50 | 99 | µA |
| | | C | | | $T_A$ = 125 °C | — | 630 | 3200 | µA |
| $I_{DDSTDBY2}$ (64 KB RAM retained) | CC | C | STANDBY2 mode current[14] | No clocks active | $T_A$ = 25 °C | — | 40 | 94 | µA |
| | | C | | | $T_A$ = 125 °C | — | 500 | 2500 | µA |
| $I_{DDSTDBY1}$ (8 KB RAM retained) | CC | C | STANDBY1 mode current[15] | No clocks active | $T_A$ = 25 °C | — | 25 | 87 | µA |
| | | C | | | $T_A$ = 125 °C | — | 230 | 1250 | µA |
| Adders in LP mode | CC | T | 32 KHz OSC | — | $T_A$ = 25 °C | — | — | 5 | µA |
| | | | 4–40 MHz OSC | — | $T_A$ = 25 °C | — | — | 3 | mA |
| | | | 16 MHz IRC | — | $T_A$ = 25 °C | — | — | 500 | µA |
| | | | 128 KHz IRC | — | $T_A$ = 25 °C | — | — | 5 | µA |

NOTES:
1. Except for $I_{DDMAX}$, all the current values are total current drawn from $V_{DD_HV_A}$.
2. $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified All temperatures are based on an ambient temperature.
3. Target typical current consumption for the following typical operating conditions and configuration. Process = typical, Voltage = 1.2 V.
4. Target maximum current consumption for mode observed under typical operating conditions. Process = Fast, Voltage = 1.32 V.
5. Running consumption is given on voltage regulator supply ($V_{DDREG}$). It does not include consumption linked to I/Os toggling. This value is highly dependent on the application. The given value is thought to be a worst case value with all cores and peripherals running, and code fetched from code flash while modify operation on-going on data flash. It is to be noticed that this value can be significantly reduced by application: switch-off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.
6. Higher current may sunk by device during power-up and standby exit. Please refer to in rush current in Table 22.
7. Maximum “allowed” current is package dependent.
8. Only for the “P” classification: Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled. RUN current measured with typical application with accesses on both code flash and RAM.

[9] Subject to change, Configuration: 1 × e200z4d + 4 kbit/s Cache, 1 × e200z0h (1/2 system frequency), CSE, 1 × eDMA (10 ch.), 6 × FlexCAN (4 × 500 kbit/s, 2 × 125 kbit/s), 4 × LINFlexD (20 kbit/s), 6 × DSPI (2 × 2 Mbit/s, 3 × 4 Mbit/s, 1 × 10 Mbit/s), 16 × Timed I/O, 16 × ADC Input, 1 × FlexRay (2 ch., 10 Mbit/s), 1 × FEC (100 Mbit/s), 1 × RTC, 4 PIT channels, 1 × SWT, 1 × STM. For lower pin count packages reduce the amount of timed I/O's and ADC channels. RUN current measured with typical application with accesses on both code flash and RAM.

[10] This value is obtained from limited sample set.

[11] Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz ON. 16 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but no reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but no reception or transmission), instance: 3-9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]-PA[11] and PC[12]-PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication, instance: 1-7 clocks gated). RTC/API ON. PIT ON. STM ON. ADC ON but no conversion except 2 analog watchdogs.

[12] Only for the "P" classification: No clock, FIRC 16 MHz OFF, SIRC128 kHz ON, PLL OFF, HPvreg OFF, LPVreg ON. All possible peripherals off and clock gated. Flash in power down mode.

[13] Only for the "P" classification: LPreg ON, HPVreg OFF, 96 KB RAM ON, device configured for minimum consumption, all possible modules switched-off.

[14] Only for the "P" classification: LPreg ON, HPVreg OFF, 64 KB RAM ON, device configured for minimum consumption, all possible modules switched-off.

[15] LPreg ON, HPVreg OFF, 8 KB RAM ON, device configured for minimum consumption, all possible modules switched OFF.

# 4.10 Flash memory electrical characteristics

## 4.10.1 Program/Erase characteristics

Table 25 shows the code flash memory program and erase characteristics.

**Table 25. Code flash memory—Program and erase specifications**

| Symbol | | C | Parameter | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Initial max[2] | Max[3] | |
| $T_{dwprogram}$ | CC | C | Double word (64 bits) program time[4] | — | 18 | 50 | 500 | µs |
| $T_{16Kpperase}$ | | | 16 KB block pre-program and erase time | — | 200 | 500 | 5000 | ms |
| $T_{32Kpperase}$ | | | 32 KB block pre-program and erase time | — | 300 | 600 | 5000 | ms |
| $T_{128Kpperase}$ | | | 128 KB block pre-program and erase time | — | 600 | 1300 | 5000 | ms |
| $T_{eslat}$ | | D | Erase Suspend Latency | — | — | 30 | 30 | µs |
| $t_{ESRT}$[5] | | C | Erase Suspend Request Rate | 20 | — | — | — | ms |
| $t_{PABT}$ | | D | Program Abort Latency | — | — | 10 | 10 | µs |
| $t_{EAPT}$ | | D | Erase Abort Latency | — | — | 30 | 30 | µs |

NOTES:

[1] Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

[2] Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

[3] The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

[4] Actual hardware programming times. This does not include software overhead.

[5] It is Time between erase suspend resume and the next erase suspend request.

Table 26 shows the data flash memory program and erase characteristics.

**Table 26. Data flash memory—Program and erase specifications**

| Symbol | | C | Parameter | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Initial max[2] | Max[3] | |
| $T_{wprogram}$ | CC | C | Word (32 bits) program time[4] | — | 30 | 70 | 500 | µs |
| $T_{16Kpperase}$ | | | 16 KB block pre-program and erase time | — | 700 | 800 | 5000 | ms |
| $T_{eslat}$ | | D | Erase Suspend Latency | — | — | 30 | 30 | µs |
| $t_{ESRT}$[5] | | C | Erase Suspend Request Rate | 10 | — | — | — | ms |
| $t_{PABT}$ | | D | Program Abort Latency | — | — | 12 | 12 | µs |
| $t_{EAPT}$ | | D | Erase Abort Latency | — | — | 30 | 30 | µs |

NOTES:
1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4 Actual hardware programming times. This does not include software overhead.
5 It is time between erase suspend resume and next erase suspend.

**Table 27. Flash memory module life**

| Symbol | | C | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | |
| P/E | CC | C | Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range ($T_J$) | — | 100,000 | 100,000 | cycles |
| | | | Number of program/erase cycles per block for 32 Kbyte blocks over the operating temperature range ($T_J$) | — | 10,000 | 100,000 | cycles |
| | | | Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range ($T_J$) | — | 1,000 | 100,000 | cycles |
| Retention | CC | C | Minimum data retention at 85 °C average ambient temperature[1] | Blocks with 0–1,000 P/E cycles | 20 | — | years |
| | | | | Blocks with 10,000 P/E cycles | 10 | — | years |
| | | | | Blocks with 100,000 P/E cycles | 5 | — | years |

NOTES:
1 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

**Table 28. Flash memory read access timing[1]**

| Symbol | | C | Parameter | Conditions[2] | | Frequency range | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Code flash memory | Data flash memory | | |
| $f_{READ}$ | CC | P | Maximum frequency for Flash reading | 5 wait states | 13 wait states | 120 —100 | MHz |
| | | C | | 4 wait states | 11 wait states | 100—80 | |
| | | D | | 3 wait states | 9 wait states | 80—64 | |
| | | C | | 2 wait states | 7 wait states | 64—40 | |
| | | C | | 1 wait states | 4 wait states | 40—20 | |
| | | C | | 0 wait states | 2 wait states | 20—0 | |

NOTES:
1 Max speed is the maximum speed allowed including PLL frequency modulation (FM).
2 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.

## 4.10.2 Flash memory power supply DC characteristics

Table 29 shows the flash memory power supply DC characteristics on external supply.

**Table 29. Flash memory power supply DC electrical characteristics**

| Symbol | | Parameter | Conditions[1] | | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $I_{CFREAD}$[3] | CC | Sum of the current consumption on $V_{DD_HV_A}$ on read access | Flash memory module read $f_{CPU}$ = 120 MHz + 2%[4] | Code flash memory | | | 33 | mA |
| $I_{DFREAD}$[(3)] | | | | Data flash memory | | | 13 | |
| $I_{CFMOD}$[(3)] | CC | Sum of the current consumption on $V_{DD_HV_A}$ (program/erase) | Program/Erase on-going while reading flash memory registers $f_{CPU}$ = 120 MHz + 2% [(4)] | Code flash memory | | | 52 | mA |
| $I_{DFMOD}$[(3)] | | | | Data flash memory | | | 13 | |
| $I_{CFLPW}$[(3)] | CC | Sum of the current consumption on $V_{DD_HV_A}$ during flash memory low power mode | | Code flash memory | | | 1.1 | mA |
| $I_{CFPWD}$[(3)] | CC | Sum of the current consumption on $V_{DD_HV_A}$ during flash memory power down mode | | Code flash memory | | | 150 | µA |
| $I_{DFPWD}$[(3)] | | | | Data flash memory | | | 150 | |

NOTES:
1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2 All values need to be confirmed during device validation.

3 Data based on characterization results, not tested in production.

4 $f_{CPU}$ 120 MHz + 2% can be achieved over full temperature 125 °C ambient, 150 °C junction temperature.

### 4.10.3 Flash memory start-up/switch-off timings

**Table 30. Start-up time/Switch-off time**

| Symbol | | C | Parameter | | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $T_{FLARSTEXIT}$ | CC | D | Delay for flash memory module to exit reset mode | Code flash memory | — | — | — | 125 | µs |
| | | | | Data flash memory | | — | — | | |
| $T_{FLALPEXIT}$ | CC | T | Delay for flash memory module to exit low-power mode | Code flash memory | — | — | — | 0.5 | |
| $T_{FLAPDEXIT}$ | CC | T | Delay for flash memory module to exit power-down mode | Code flash memory | — | — | — | 30 | |
| | | | | Data flash memory | | — | — | | |
| $T_{FLALPENTRY}$ | CC | T | Delay for flash memory module to enter low-power mode | Code flash memory | — | — | — | 0.5 | |

NOTES:
1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.

## 4.11 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

### 4.11.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and pre-qualification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers)
- Pre-qualification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

## 4.11.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

**Table 31. EMI radiated emission measurement[1,2]**

| Symbol | | C | Parameter | Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| — | SR | — | Scan range | — | | 0.150 | | 1000 | MHz |
| $f_{CPU}$ | SR | — | Operating frequency | — | | — | 120 | — | MHz |
| $V_{DD_LV}$ | SR | — | LV operating voltages | — | | — | 1.28 | — | V |
| $S_{EMI}$ | CC | T | Peak level | $V_{DD}$ = 5 V, $T_A$ = 25 °C, LQFP176 package Test conforming to IEC 61967-2, $f_{OSC}$ = 40 MHz/$f_{CPU}$ = 120 MHz | No PLL frequency modulation | — | — | 18 | dBµV |
| | | | | | ± 2% PLL frequency modulation | — | — | 14[3] | dBµV |

NOTES:
1. EMI testing and I/O port waveforms per IEC 61967-1, -2, -4.
2. For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.
3. All values need to be confirmed during device validation.

## 4.11.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

### 4.11.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

**Table 32. ESD absolute maximum ratings[1,2]**

| Symbol | Ratings | Conditions | Class | Max value[3] | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (Human Body Model) | $T_A$ = 25 °C conforming to AEC-Q100-002 | H1C | 2000 | V |
| $V_{ESD(MM)}$ | Electrostatic discharge voltage (Machine Model) | $T_A$ = 25 °C conforming to AEC-Q100-003 | M2 | 200 | |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (Charged Device Model) | $T_A$ = 25 °C conforming to AEC-Q100-011 | C3A | 500 | |
| | | | | 750 (corners) | |

NOTES:
1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3. Data based on characterization results, not tested in production.

#### 4.11.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply over-voltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

**Table 33. Latch-up results**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = 125 °C conforming to JESD 78 | II level A |

## 4.12 Fast external crystal oscillator (4–40 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 10 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 34 provides the parameter description of 4 MHz to 40 MHz crystals used for the design simulations.

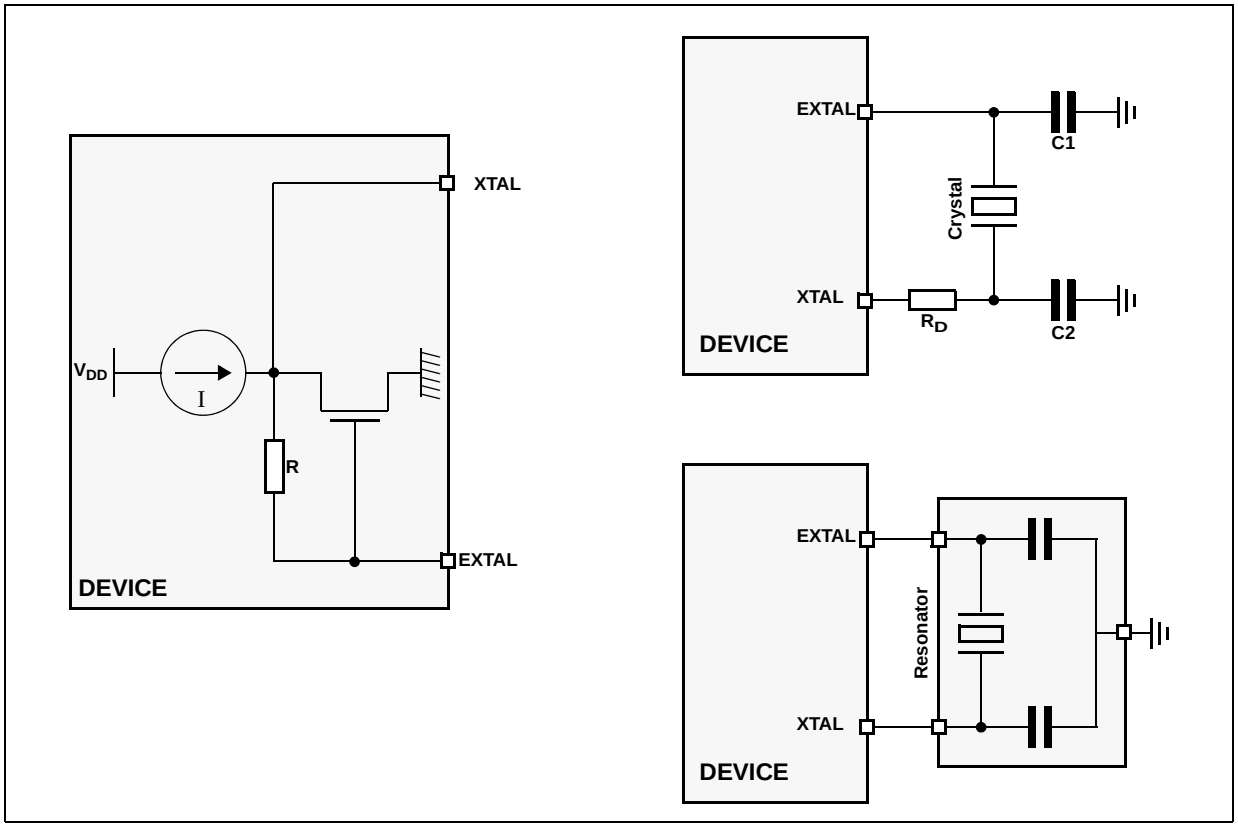



**Figure 10. Crystal oscillator and resonator connection scheme**

## NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

**Table 34. Crystal description**

| Nominal frequency (MHz) | NDK crystal reference | Crystal equivalent series resistance ESR Ω | Crystal motional capacitance ($C_m$) fF | Crystal motional inductance ($L_m$) mH | Load on xtalin/xtalout C1 = C2 (pF)[1] | Shunt capacitance between xtalout and xtalin C0[2] (pF) |
|---|---|---|---|---|---|---|
| 4 | NX8045GB | 300 | 2.68 | 591.0 | 21 | 2.93 |
| 8 | NX5032GA | 300 | 2.46 | 160.7 | 17 | 3.01 |
| 10 | | 150 | 2.93 | 86.6 | 15 | 2.91 |
| 12 | | 120 | 3.11 | 56.5 | 15 | 2.93 |
| 16 | | 120 | 3.90 | 25.3 | 10 | 3.00 |
| 40 | NX5032GA | 50 | 6.18 | 2.56 | 8 | 3.49 |

NOTES:
1 The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.
2 The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

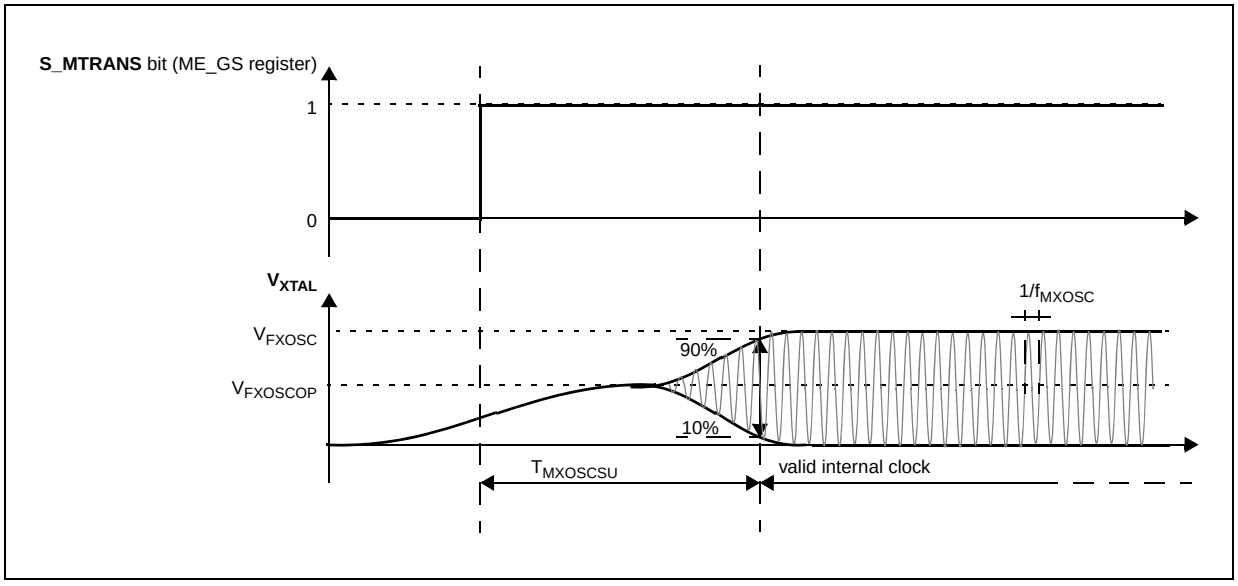



**Figure 11. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics**

**Table 35. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $f_{FXOSC}$ | SR | — | Fast external crystal oscillator frequency | — | 4.0 | — | 40.0 | MHz |
| $g_{mFXOSC}$ | CC | C | Fast external crystal oscillator transconductance | $V_{DD}$ = 3.3 V ± 10% | 4[3] | — | 20[3] | mA/V |
| | | | | $V_{DD}$ = 5.0 V ± 10% | 4[3] | — | 20[3] | |
| $V_{FXOSC}$ | CC | T | Oscillation amplitude at EXTAL | $f_{OSC}$ = 40 MHz For both $V_{DD}$ = 3.3 V ± 10%, $V_{DD}$ = 5.0 V ± 10% | — | 0.95 | — | V |
| $V_{FXOSCOP}$ | CC | P | Oscillation operating point | — | — | 1.8 | | V |
| $I_{FXOSC}$,[4] | CC | T | Fast external crystal oscillator consumption | $V_{DD}$ = 3.3 V ± 10%, $f_{OSC}$ = 40 MHz | — | 2 | 2.2 | mA |
| | | | | $V_{DD}$ = 5.0 V ± 10%, $f_{OSC}$ = 40 MHz | — | 2.3 | 2.5 | |
| | | | | $V_{DD}$ = 3.3 V ± 10%, $f_{OSC}$ = 16 MHz | — | 1.3 | 1.5 | |
| | | | | $V_{DD}$ = 5.0 V ± 10%, $f_{OSC}$ = 16 MHz | — | 1.6 | 1.8 | |
| $T_{FXOSCSU}$ | CC | T | Fast external crystal oscillator start-up time | $f_{OSC}$ = 40 MHz For both $V_{DD}$ = 3.3 V ± 10%, $V_{DD}$ = 5.0 V ± 10% | — | — | 5 | ms |

**Table 35. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{IH}$ | SR | P | Input high level CMOS (Schmitt Trigger) | Oscillator bypass mode | $0.65V_{DD_HV_A}$ | — | $V_{DD_HV_A}$ + 0.4 | V |
| $V_{IL}$ | SR | P | Input low level CMOS (Schmitt Trigger) | Oscillator bypass mode | –0.3 | — | $0.35V_{DD_HV_A}$ | V |

NOTES:
1. $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Based on ATE Cz
4. Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

## 4.13 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

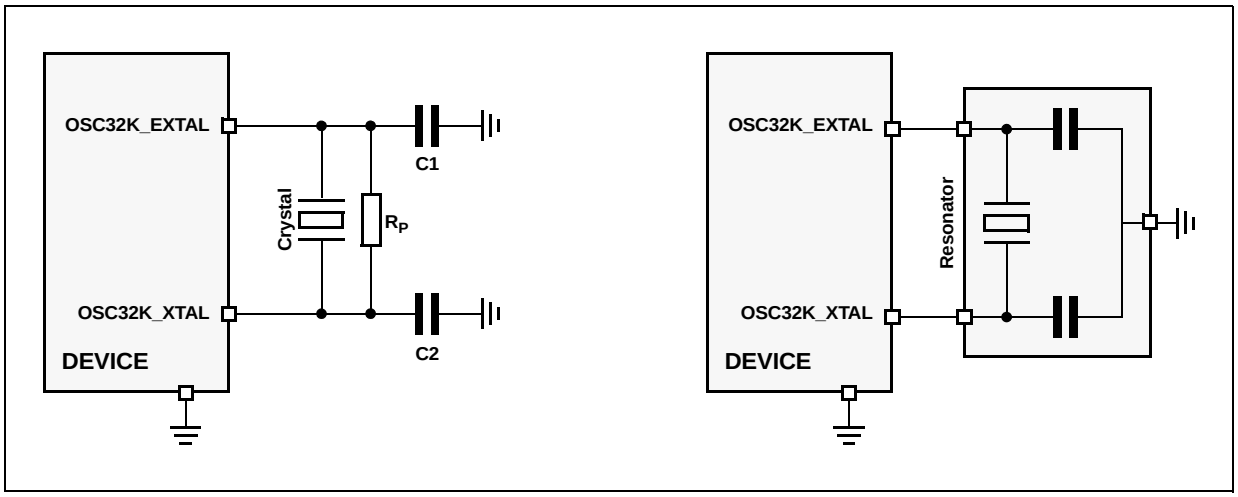



**Figure 12. Crystal oscillator and resonator connection scheme**

**NOTE**

OSC32K_XTAL/OSC32K_EXTAL must not be directly used to drive external circuits.

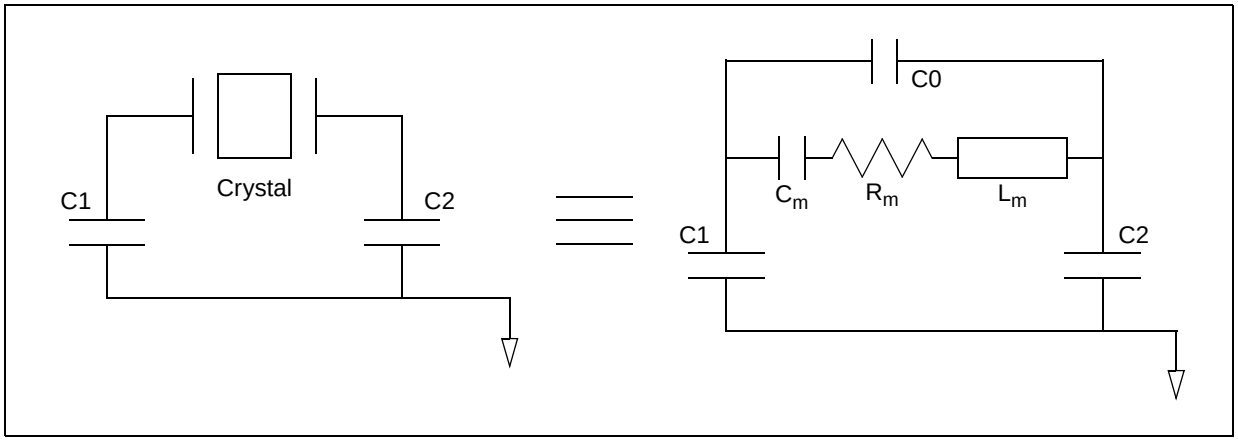



**Figure 13. Equivalent circuit of a quartz crystal**

**Table 36. Crystal motional characteristics[1]**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $L_m$ | Motional inductance | — | — | 11.796 | — | KH |
| $C_m$ | Motional capacitance | — | — | 2 | — | fF |
| C1/C2 | Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground[2] | — | 18 | — | 28 | pF |
| $R_m$[3] | Motional resistance | AC coupled @ C0 = 2.85 pF[4] | — | — | 65 | kΩ |
| | | AC coupled @ C0 = 4.9 pF[(4)] | — | — | 50 | |
| | | AC coupled @ C0 = 7.0 pF[(4)] | — | — | 35 | |
| | | AC coupled @ C0 = 9.0 pF[(4)] | — | — | 30 | |

NOTES:
1 The crystal used is Epson Toyocom MC306.
2 This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.
3 Maximum ESR ($R_m$) of the crystal is 50 kΩ.
4 C0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins.

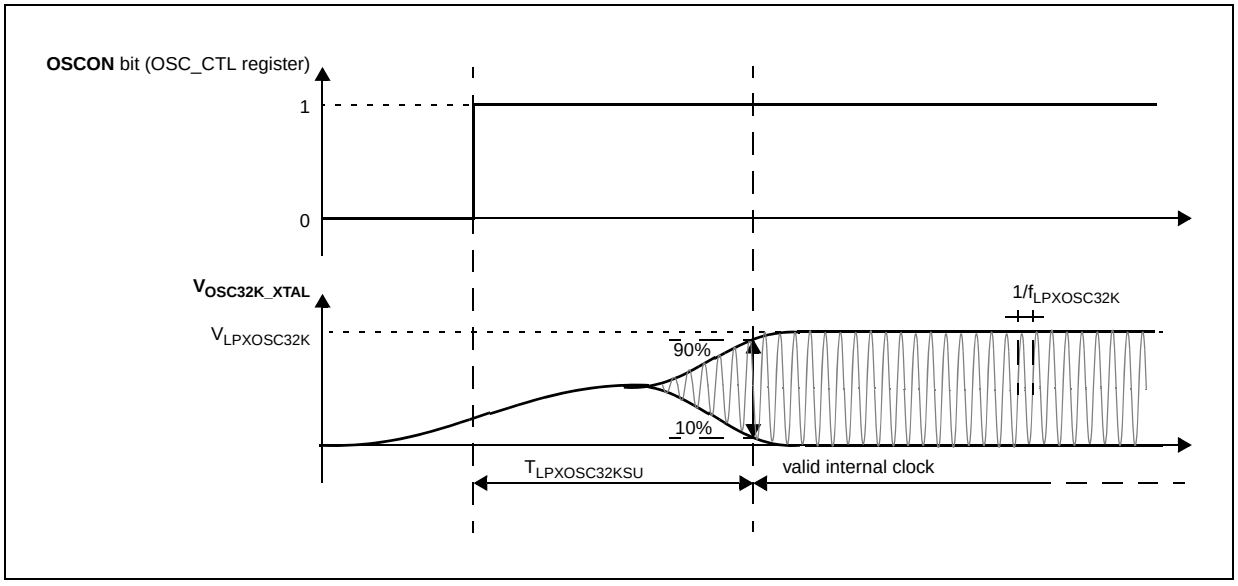



**Figure 14. Slow external crystal oscillator (32 kHz) electrical characteristics**

**Table 37. Slow external crystal oscillator (32 kHz) electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $f_{SXOSC}$ | SR | — | Slow external crystal oscillator frequency | — | 32 | 32.768 | 40 | kHz |
| $g_{mSXOSC}$ | CC | — | Slow external crystal oscillator transconductance | $V_{DD}$ = 3.3 V ± 10%, | 13[3] | — | 33[3] | µA/V |
| | | | | $V_{DD}$ = 5.0 V ± 10% | 15[3] | — | 35[3] | |
| $V_{SXOSC}$ | CC | T | Oscillation amplitude | — | 1.2 | 1.4 | 1.7 | V |
| $I_{SXOSCBIAS}$ | CC | T | Oscillation bias current | — | 1.2 | — | 4.4 | µA |
| $I_{SXOSC}$ | CC | T | Slow external crystal oscillator consumption | — | — | — | 7 | µA |
| $T_{SXOSCSU}$ | CC | T | Slow external crystal oscillator start-up time | — | — | — | 2[4] | s |

NOTES:
1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2 All values need to be confirmed during device validation.
3 Based on ATE CZ
4 Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

## 4.14 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

**Table 38. FMPLL electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $f_{PLLIN}$ | SR | — | FMPLL reference clock[3] | — | 4 | — | 64 | MHz |
| $\Delta_{PLLIN}$ | SR | — | FMPLL reference clock duty cycle(3) | — | 40 | — | 60 | % |
| $f_{PLLOUT}$ | CC | P | FMPLL output clock frequency | — | 16 | — | 120 | MHz |
| $f_{CPU}$ | SR | — | System clock frequency | — | — | — | 120 + 2%[4] | MHz |
| $f_{FREE}$ | CC | P | Free-running frequency | — | 20 | — | 150 | MHz |
| $t_{LOCK}$ | CC | P | FMPLL lock time | Stable oscillator ($f_{PLLIN}$ = 16 MHz) | | 40 | 100 | µs |
| $\Delta t_{LTJIT}$ | CC | — | FMPLL long term jitter | $f_{PLLIN}$ = 40 MHz (resonator), $f_{PLLCLK}$ @ 120 MHz, 4000 cycles | — | — | 6 (for < 1ppm) | ns |
| $I_{PLL}$ | CC | C | FMPLL consumption | $T_A$ = 25 °C | — | — | 3 | mA |

NOTES:
1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2 All values need to be confirmed during device validation.
3 PLLIN clock retrieved directly from 4-40 MHz XOSC or 16 MIRC. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify $f_{PLLIN}$ and $\Delta_{PLLIN}$.
4 $f_{CPU}$ 120 + 2% MHz can be achieved at 125 °C.

## 4.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device and can also be used as input to PLL.

**Table 39. Fast internal RC oscillator (16 MHz) electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $f_{FIRC}$ | CC | P | Fast internal RC oscillator high frequency | $T_A$ = 25 °C, trimmed | — | 16 | — | MHz |
| | SR | — | | — | 12 | | 20 | |
| $I_{FIRCRUN}$[3], | CC | T | Fast internal RC oscillator high frequency current in running mode | $T_A$ = 25 °C, trimmed | — | — | 200 | µA |
| $I_{FIRCPWD}$ | CC | D | Fast internal RC oscillator high frequency current in power down mode | $T_A$ = 25 °C | — | — | 100 | nA |
| | | D | | $T_A$ = 55 °C | — | — | 200 | nA |
| | | D | | $T_A$ = 125 °C | — | — | 1 | µA |

**Table 39. Fast internal RC oscillator (16 MHz) electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $I_{FIRCSTOP}$ | CC | T | Fast internal RC oscillator high frequency and system clock current in stop mode | $T_A$ = 25 °C | sysclk = off | — | 500 | — | µA |
| | | | | | sysclk = 2 MHz | — | 600 | — | |
| | | | | | sysclk = 4 MHz | — | 700 | — | |
| | | | | | sysclk = 8 MHz | — | 900 | — | |
| | | | | | sysclk = 16 MHz | — | 1250 | — | |
| $T_{FIRCSU}$ | CC | C | Fast internal RC oscillator start-up time | $T_A$ = 55 °C | $V_{DD}$ = 5.0 V ± 10% | — | — | 2.0 | µs |
| | | — | | | $V_{DD}$ = 3.3 V ± 10% | — | — | 5 | |
| | | — | | $T_A$ = 125 °C | $V_{DD}$ = 5.0 V ± 10% | — | — | 2.0 | |
| | | — | | | $V_{DD}$ = 3.3 V ± 10% | — | — | 5 | |
| $\Delta_{FIRCPRE}$ | CC | C | Fast internal RC oscillator precision after software trimming of $f_{FIRC}$ | $T_A$ = 25 °C | | –1 | — | +1 | % |
| $\Delta_{FIRCTRIM}$ | CC | C | Fast internal RC oscillator trimming step | $T_A$ = 25 °C | | — | 1.6 | | % |
| $\Delta_{FIRCVAR}$ | CC | C | Fast internal RC oscillator variation over temperature and supply with respect to $f_{FIRC}$ at $T_A$ = 25 °C in high-frequency configuration | — | | –5 | — | +5 | % |

NOTES:
1. $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

## 4.16 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz low power internal RC oscillator. This can be used as the reference clock for the RTC module.

**Table 40. Slow internal RC oscillator (128 kHz) electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $f_{SIRC}$ | CC | P | Slow internal RC oscillator low frequency | $T_A$ = 25 °C, trimmed | — | 128 | — | kHz |
| | SR | — | | untrimmed, across temperatures | 84 | — | 205 | |
| $I_{SIRC}$[3], | CC | C | Slow internal RC oscillator low frequency current | $T_A$ = 25 °C, trimmed | — | — | 5 | µA |

**Table 40. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $T_{SIRCSU}$ | CC | P | Slow internal RC oscillator start-up time | $T_A$ = 25 °C, $V_{DD}$ = 5.0 V ± 10% | — | 8 | 12 | µs |
| $\Delta_{SIRCPRE}$ | CC | C | Slow internal RC oscillator precision after software trimming of $f_{SIRC}$ | $T_A$ = 25 °C | –2 | — | +2 | % |
| $\Delta_{SIRCTRIM}$ | CC | C | Slow internal RC oscillator trimming step | — | — | 2.7 | — | |
| $\Delta_{SIRCVAR}$ | CC | C | Variation in $f_{SIRC}$ across temperature and fluctuation in supply voltage, post trimming | — | –10 | — | +10 | % |

NOTES:
1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2 All values need to be confirmed during device validation.
3 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

## 4.17 ADC electrical characteristics

### 4.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

**NOTE**

Due to ADC limitations, the two ADCs cannot sample a shared channel at the same time i.e., their sampling windows cannot overlap if a shared channel is selected. If this is done, neither of the ADCs can guarantee their conversion accuracies.

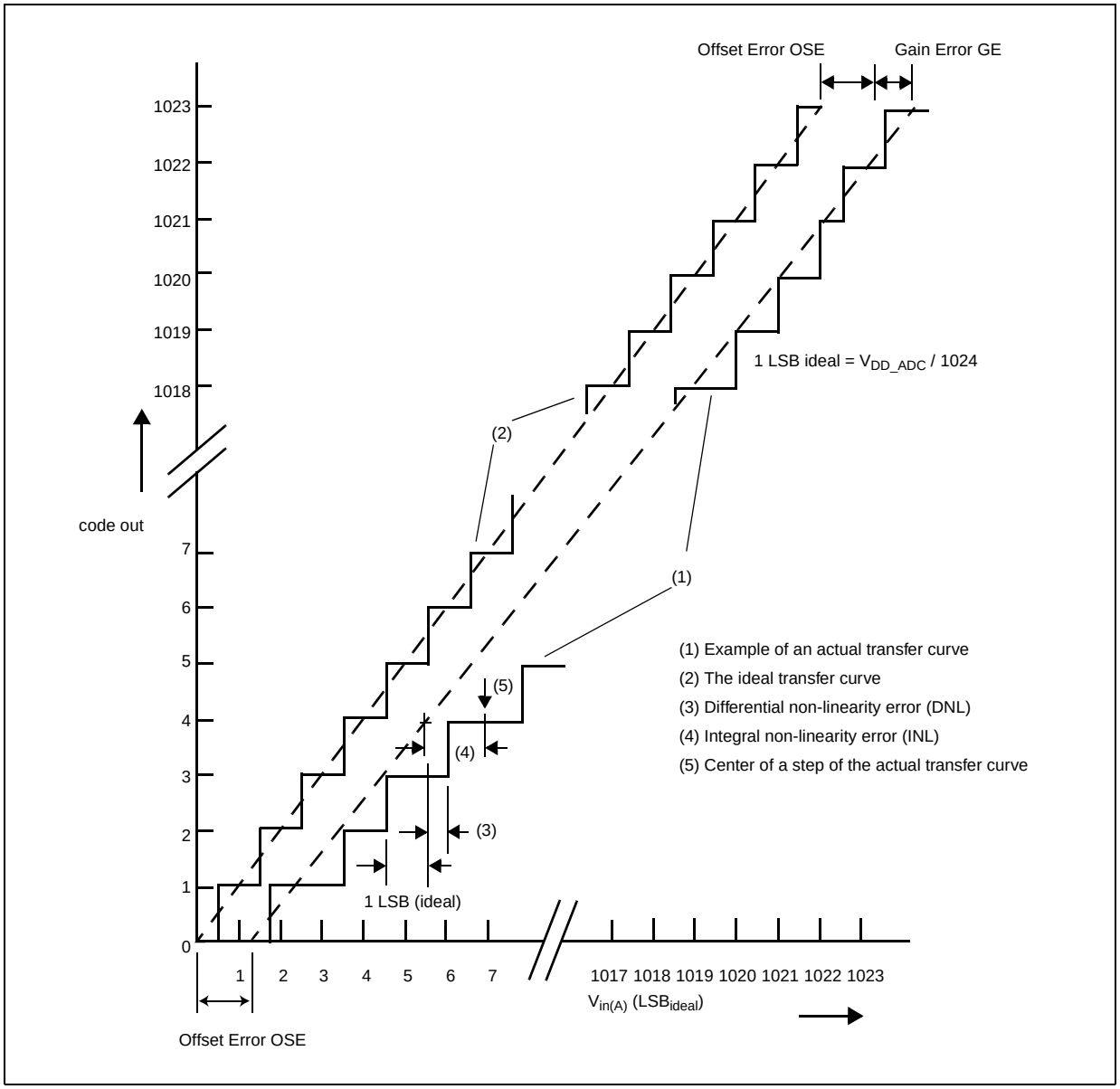



**Figure 15. ADC_0 characteristic and error definitions**

### 4.17.1.1 Input impedance and ADC accuracy

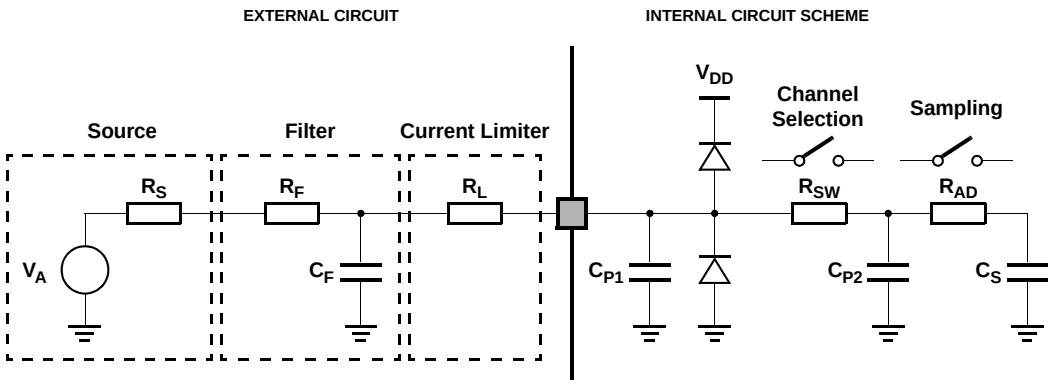
To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device, can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source. A real filter, can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC Filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being CS and $Cp_2$ substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1MHz, with $CS+Cp_2$ equal to 3pF, a resistance of 330KΩ is obtained (Reqiv = 1 / (fc*($CS+Cp_2$)), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $CS+Cp_2$) and the sum of $R_S + R_F$, the external circuit must be designed to respect the following relation

***Eqn. 4***

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

The formula above provides a constraint for external network design, in particular on resistive path.




| | |
|---|---|
| $R_S$ | Source Impedance |
| $R_F$ | Filter Resistance |
| $C_F$ | Filter Capacitance |
| $R_L$ | Current Limiter Resistance |
| $R_{SW}$ | Channel Selection Switch Impedance |
| $R_{AD}$ | Sampling Switch Impedance |
| $C_P$ | Pin Capacitance (two contributions, $C_{P1}$ and $C_{P2}$) |
| $C_S$ | Sampling Capacitance |

**Figure 16. Input equivalent circuit (precise channels)**

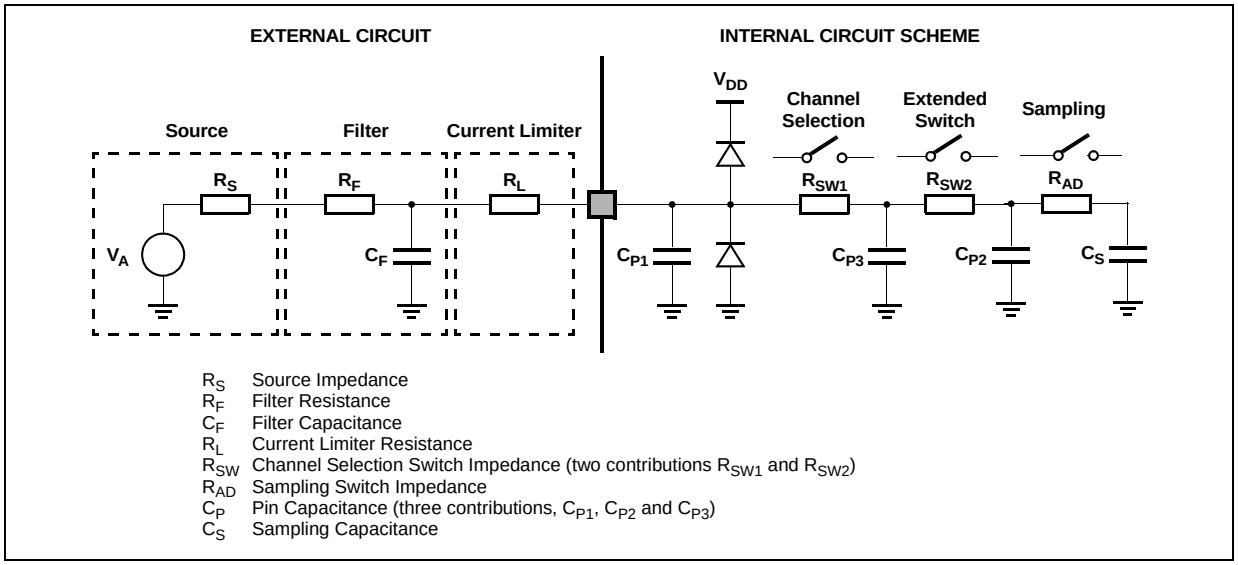



**Figure 17. Input equivalent circuit (extended channels)**

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances $C_F$, $C_{P1}$ and $C_{P2}$ initially charged at the source voltage $V_A$ (refer to the equivalent circuit reported in Figure 16): when the sampling phase is started (A/D switch close), a charge sharing phenomena is installed.

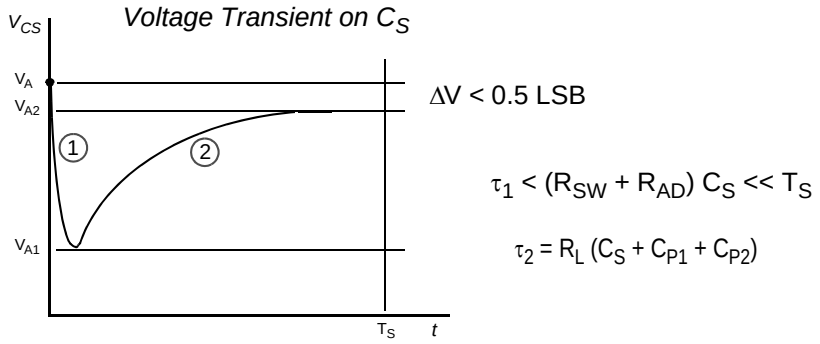



**Figure 18. Transient behavior during sampling phase**

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance $C_{P1}$ and $C_{P2}$ to the sampling capacitance $C_S$ occurs ($C_S$ is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which $C_{P2}$ is reported in parallel to $C_{P1}$ (call $C_P = C_{P1} + C_{P2}$), the two capacitances $C_P$ and $C_S$ are in series, and the time constant is

***Eqn. 5***

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

This relation can again be simplified considering $C_S$ as an additional worst condition. In reality, transient is faster, but the A/D converter circuitry has been designed to be robust also in very worst case: the sampling time $T_s$ is always much longer than the internal time constant.

***Eqn. 6***

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of $C_{P1}$ and $C_{P2}$ is redistributed on $C_S$,determining a new value of the voltage $V_{A1}$ on the capacitance according to the following equation

***Eqn. 7***

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also $C_F$ (that is typically bigger than the on-chip capacitance) through the resistance RL: again considering the worst case in which $C_{P2}$ and $C_S$ were in parallel to $C_{P1}$ (since the time constant in reality would be faster), the time constant is:

***Eqn. 8***

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time $T_S$, a constraints on $R_L$ sizing is obtained:

***Eqn. 9***

$$8.5 \bullet \tau_2 = 8.5 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, $R_L$ shall be sized also according to the current limitation constraints, in combination with $R_S$ (source impedance) and $R_F$ (filter resistance). Being $C_F$ definitively bigger than $C_{P1}$, $C_{P2}$ and $C_S$, then the final voltage $V_{A2}$ (at the end of the charge transfer transient) will be much higher than $V_{A1}$. The following equation must be respected (charge balance assuming now $C_S$ already charged at $V_{A1}$):

***Eqn. 10***

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on $C_S$ with respect to the ideal source $V_A$; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time ($T_S$). The filter is typically designed to act as anti-aliasing

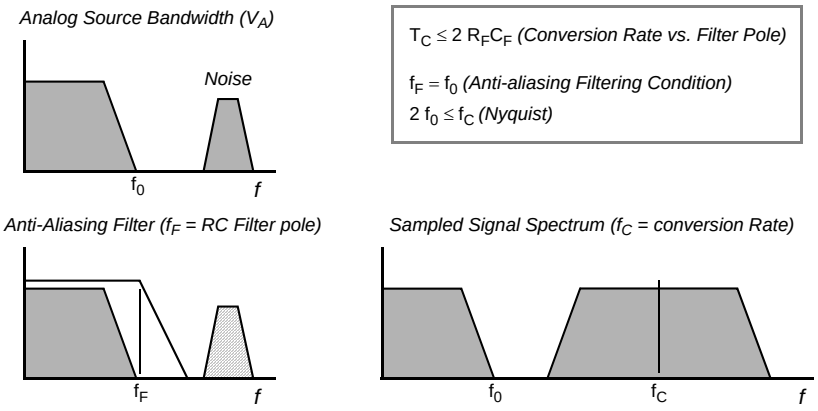



**Figure 19. Spectral representation of input signal**

Calling $f_0$ the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, $f_F$), according to the Nyquist theorem the conversion rate $f_C$ must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period ($T_C$). Again the conversion period $T_C$ is longer than the sampling time $T_S$, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time $T_S$, so the charge level on $C_S$ cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on $C_S$; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on $C_S$:

***Eqn. 11***

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when $V_A$ is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on $C_F$ value:

**ADC_0 (10-bit)** ***Eqn. 12***

$$C_F > 2048 \bullet C_S$$

**ADC_1 (12-bit)** ***Eqn. 13***

$$C_F > 8192 \bullet C_S$$

### 4.17.1.2 ADC electrical characteristics

**Table 41. ADC input leakage current**

| Symbol | | C | Parameter | Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $I_{LKG}$ | CC | C | Input leakage current | $T_A$ = –40 °C | No current injection on adjacent pin | — | 1 | — | nA |
| | | C | | $T_A$ = 25 °C | | — | 1 | — | |
| | | C | | $T_A$ = 105 °C | | — | 8 | 200 | |
| | | P | | $T_A$ = 125 °C | | — | 45 | 400 | |

**Table 42. ADC conversion characteristics (10-bit ADC_0)**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{SS_ADC0}$ | SR | — | Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground ($V_{SS_HV}$)[2] | — | –0.1 | — | 0.1 | V |
| $V_{DD_ADC0}$ | SR | — | Voltage on VDD_HV_ADC0 pin (ADC_0 reference) with respect to ground ($V_{SS_HV}$) | — | $V_{DD_HV_A}$ – 0.1 | — | $V_{DD_HV_A}$ + 0.1 | V |
| $V_{AINx}$ | SR | — | Analog input voltage[3] | — | $V_{SS_ADC0}$ – 0.1 | — | $V_{DD_ADC0}$ + 0.1 | V |
| $f_{ADC0}$ | SR | — | ADC_0 analog frequency | — | 6 | — | 32 + 2% | MHz |
| $t_{ADC0_PU}$ | SR | — | ADC_0 power up delay | — | — | — | 1.5 | µs |
| $t_{ADC0_S}$ | CC | T | Sample time[4] | $f_{ADC}$ = 32 MHz | 500 | — | | ns |
| $t_{ADC0_C}$ | CC | P | Conversion time[5,6] | $f_{ADC}$ = 32 MHz | 0.625 | — | | µs |
| | | | | $f_{ADC}$ = 30 MHz | 0.700 | — | | |
| $C_S$ | CC | D | ADC_0 input sampling capacitance | — | — | — | 3 | pF |
| $C_{P1}$ | CC | D | ADC_0 input pin capacitance 1 | — | — | — | 3 | pF |
| $C_{P2}$ | CC | D | ADC_0 input pin capacitance 2 | — | — | — | 1 | pF |
| $C_{P3}$ | CC | D | ADC_0 input pin capacitance 3 | — | — | — | 1 | pF |
| $R_{SW1}$ | CC | D | Internal resistance of analog source | — | — | — | 3 | kΩ |

**Table 42. ADC conversion characteristics (10-bit ADC_0) (continued)**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $R_{SW2}$ | CC | D | Internal resistance of analog source | — | | — | — | 2 | kΩ |
| $R_{AD}$ | CC | D | Internal resistance of analog source | — | | — | — | 2 | kΩ |
| $I_{INJ}$[7] | SR | — | Input current Injection | Current injection on one ADC_0 input, different from the converted one | $V_{DD}$ = 3.3 V ± 10% | –5 | — | 5 | mA |
| | | | | | $V_{DD}$ = 5.0 V ± 10% | –5 | — | 5 | |
| \| INL \| | CC | T | Absolute value for integral non-linearity | No overload | | — | 0.5 | 1.5 | LSB |
| \| DNL \| | CC | T | Absolute differential non-linearity | No overload | | — | 0.5 | 1.0 | LSB |
| \| OFS \| | CC | T | Absolute offset error | — | | — | 0.5 | — | LSB |
| \| GNE \| | CC | T | Absolute gain error | — | | — | 0.6 | — | LSB |
| TUEP | CC | P | Total unadjusted error[8] for precise channels, input only pins | Without current injection | | –2 | 0.6 | 2 | LSB |
| | | T | | With current injection | | –3 | | 3 | |
| TUEX | CC | T | Total unadjusted error[(8)] for extended channel | Without current injection | | –3 | 1 | 3 | LSB |
| | | T | | With current injection | | –4 | | 4 | |

NOTES:

1. $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2. Analog and digital $V_{SS_HV}$ must be common (to be tied together externally).
3. $V_{AINx}$ may exceed $V_{SS_ADC0}$ and $V_{DD_ADC0}$ limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
4. During the sample time the input capacitance $C_S$ can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_{ADC0_S}$. After the end of the sample time $t_{ADC0_S}$, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock $t_{ADC0_S}$ depend on programming.
5. This parameter does not include the sample time $t_{ADC0_S,}$ but only the time for determining the digital result and the time to load the result's register with the conversion result
6. Refer to ADC conversion table for detailed calculations.
7. PB10 should not have any current injected. It can disturb accuracy on other ADC_0 pins.
8. Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

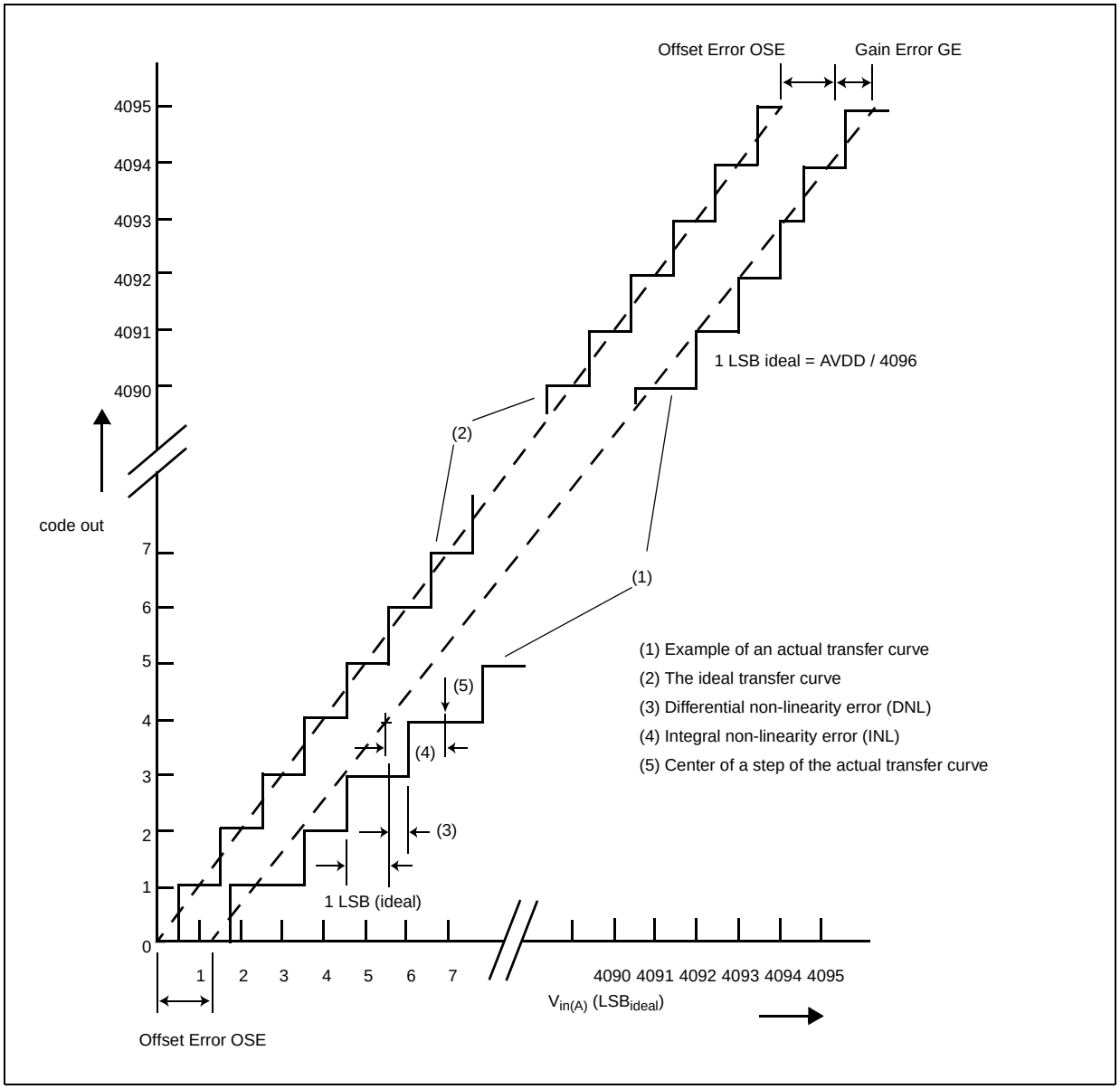



**Figure 20. ADC_1 characteristic and error definitions**

**Table 43. Conversion characteristics (12-bit ADC_1)**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{SS_ADC1}$ | SR | — | Voltage on VSS_HV_ADC1 (ADC_1 reference) pin with respect to ground ($V_{SS_HV}$)[2] | — | –0.1 | | 0.1 | V |
| $V_{DD_ADC1}$[3] | SR | — | Voltage on VDD_HV_ADC1 pin (ADC_1 reference) with respect to ground ($V_{SS_HV}$) | — | $V_{DD_HV_A}$ – 0.1 | | $V_{DD_HV_A}$ + 0.1 | V |
| $V_{AINx}$[3,4] | SR | — | Analog input voltage[5] | — | $V_{SS_ADC1}$ – 0.1 | | $V_{DD_ADC1}$ + 0.1 | V |
| $f_{ADC1}$ | SR | — | ADC_1 analog frequency | — | 8 + 2% | | 32 + 2% | MHz |
| $t_{ADC1_PU}$ | SR | — | ADC_1 power up delay | — | 1.5 | | | µs |
| $t_{ADC1_S}$ | CC | T | Sample time[6] VDD=5.0 V | — | 440 | | | ns |
| | | | Sample time(6) VDD=3.3 V | — | 530 | | | |
| $t_{ADC1_C}$ | CC | P | Conversion time[7, 8] VDD=5.0 V | $f_{ADC1}$ = 32 MHz | 2 | | | µs |
| | | | Conversion time(7), (6) VDD =5.0 V | $f_{ADC\ 1}$= 30 MHz | 2.1 | | | |
| | | | Conversion time(7), (6) VDD=3.3 V | $f_{ADC\ 1}$= 20 MHz | 3 | | | |
| | | | Conversion time(7), (6) VDD =3.3 V | $f_{ADC1}$ = 15 MHz | 3.01 | | | |
| $C_S$ | CC | D | ADC_1 input sampling capacitance | — | 5 | | | pF |
| $C_{P1}$ | CC | D | ADC_1 input pin capacitance 1 | — | 3 | | | pF |
| $C_{P2}$ | CC | D | ADC_1 input pin capacitance 2 | — | 1 | | | pF |
| $C_{P3}$ | CC | D | ADC_1 input pin capacitance 3 | — | 1.5 | | | pF |
| $R_{SW1}$ | CC | D | Internal resistance of analog source | — | | | 1 | kΩ |

**Table 43. Conversion characteristics (12-bit ADC_1) (continued)**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $R_{SW2}$ | CC | D | Internal resistance of analog source | — | | | | 2 | kΩ |
| $R_{AD}$ | CC | D | Internal resistance of analog source | — | | | | 0.3 | kΩ |
| $I_{INJ}$ | SR | — | Input current Injection | Current injection on one ADC_1 input, different from the converted one | $V_{DD}$ = 3.3 V ± 10% | −5 | — | 5 | mA |
| | | | | | $V_{DD}$ = 5.0 V ± 10% | −5 | — | 5 | |
| INLP | CC | T | Absolute Integral non-linearity-Precise channels | No overload | | | 1 | 3 | LSB |
| INLS | CC | T | Absolute Integral non-linearity-Standard channels | No overload | | | 1.5 | 5 | LSB |
| DNL | CC | T | Absolute Differential non-linearity | No overload | | | 0.5 | 1 | LSB |
| OFS | CC | T | Absolute Offset error | — | | | 2 | | LSB |
| GNE | CC | T | Absolute Gain error | — | | | 2 | | LSB |
| TUEP[9] | CC | P | Total Unadjusted Error for precise channels, input only pins | Without current injection | | −6 | | 6 | LSB |
| | | T | | With current injection | | −8 | | 8 | LSB |
| TUES[(9)] | CC | T | Total Unadjusted Error for standard channel | Without current injection | | −10 | | 10 | LSB |
| | | T | | With current injection | | −12 | | 12 | LSB |

NOTES:

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = −40 to 125 °C, unless otherwise specified.

2 Analog and digital $V_{SS_HV}$ **must** be common (to be tied together externally).

3 PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD_HV_B}$ domain hence VDD_HV_ADC1 should be within ±100 mV of VDD_HV_B when these channels are used for ADC_1.

4 VDD_HV_ADC1 can operate at 5V condition while $V_{DD_HV_B}$ can operate at 3.3V provided that ADC_1 channels coming from $V_{DD_HV_B}$ domain are limited in max swing as $V_{DD_HV_B}$.

5 $V_{AINx}$ may exceed $V_{SS_ADC1}$ and $V_{DD_ADC1}$ limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.

6 During the sample time the input capacitance $C_S$ can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_{ADC1_S}$. After the end of the sample time $t_{ADC1_S}$, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock $t_{ADC1_S}$ depend on programming.

7 Conversion time = Bit evaluation time + Sampling time + 1 Clock cycle delay.

8 Refer to ADC conversion table for detailed calculations.

9 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

## 4.18 Fast Ethernet Controller

MII signals use CMOS signal levels compatible with devices operating at 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

### 4.18.1 MII Receive Signal Timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency in 2:1 mode and two times the RX_CLK frequency in 1:1 mode.

**Table 44. MII Receive Signal Timing**

| Spec | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M1 | RXD[3:0], RX_DV, RX_ER to RX_CLK setup | 5 | — | ns |
| M2 | RX_CLK to RXD[3:0], RX_DV, RX_ER hold | 5 | — | ns |
| M3 | RX_CLK pulse width high | 35% | 65% | RX_CLK period |
| M4 | RX_CLK pulse width low | 35% | 65% | RX_CLK period |

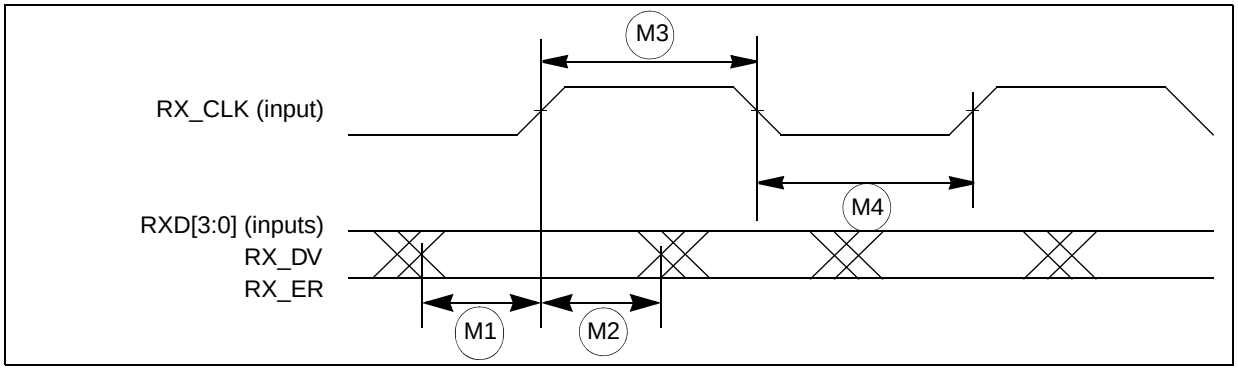



**Figure 21. MII receive signal timing diagram**

### 4.18.2 MII Transmit Signal Timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency in 2:1 mode and two times the TX_CLK frequency in 1:1 mode.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Fast Ethernet Controller (FEC) chapter of the MPC5646C Reference Manual for details of this option and how to enable it.

**Table 45. MII transmit signal timing[1]**

| Spec | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M5 | TX_CLK to TXD[3:0], TX_EN, TX_ER invalid | 5 | — | ns |
| M6 | TX_CLK to TXD[3:0], TX_EN, TX_ER valid | — | 25 | ns |
| M7 | TX_CLK pulse width high | 35% | 65% | TX_CLK period |
| M8 | TX_CLK pulse width low | 35% | 65% | TX_CLK period |

NOTES:
1 Output pads configured with SRE = 0b11.

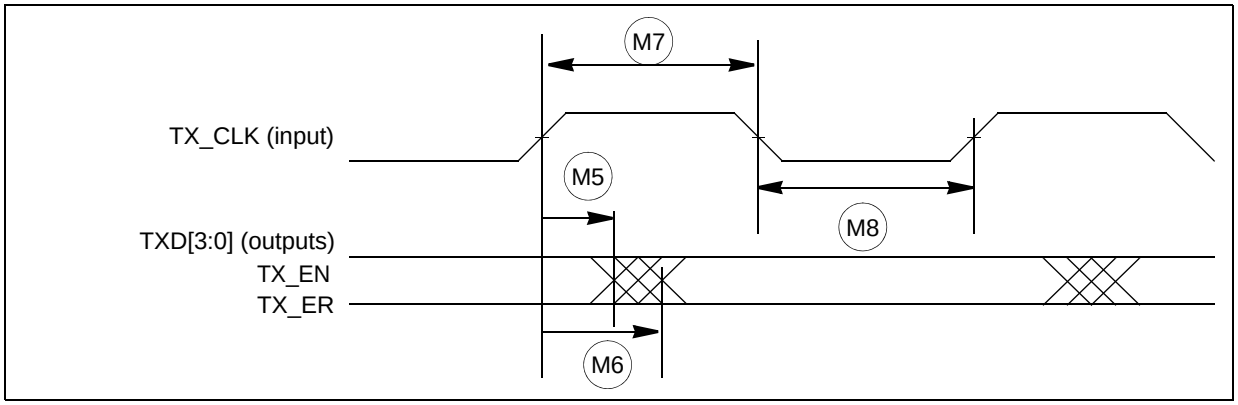



**Figure 22. MII transmit signal timing diagram**

## 4.18.3 MII Async Inputs Signal Timing (CRS and COL)

**Table 46. MII Async Inputs Signal Timing[1]**

| Spec | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M9 | CRS, COL minimum pulse width | 1.5 | — | TX_CLK period |

NOTES:
1 Output pads configured with SRE = 0b11.

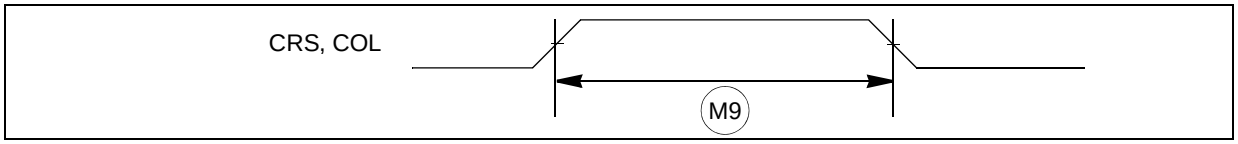



**Figure 23. MII async inputs timing diagram**

## 4.18.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

**Table 47. MII serial management channel timing[1]**

| Spec | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M10 | MDC falling edge to MDIO output invalid (minimum propagation delay) | 0 | — | ns |
| M11 | MDC falling edge to MDIO output valid (max prop delay) | — | 25 | ns |
| M12 | MDIO (input) to MDC rising edge setup | 28 | — | ns |
| M13 | MDIO (input) to MDC rising edge hold | 0 | — | ns |
| M14 | MDC pulse width high | 40% | 60% | MDC period |
| M15 | MDC pulse width low | 40% | 60% | MDC period |

NOTES:
1 Output pads configured with SRE = 0b11.

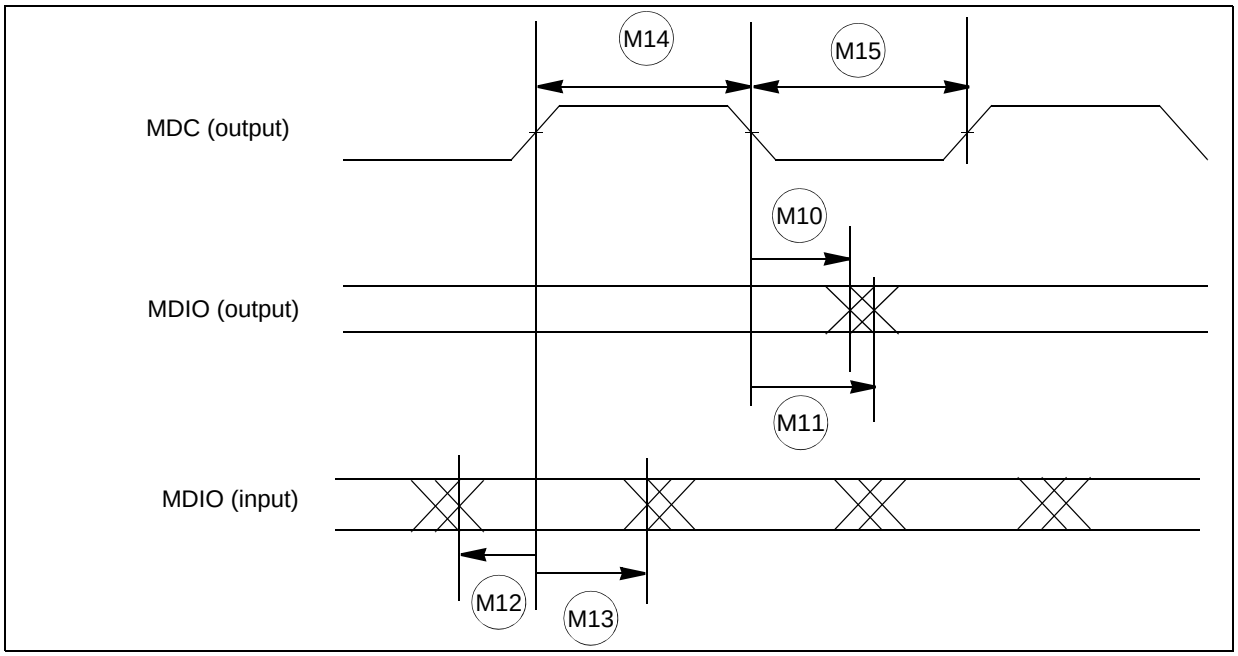



**Figure 24. MII serial management channel timing diagram**

# 4.19 On-chip peripherals

## 4.19.1 Current consumption

**Table 48. On-chip peripherals current consumption[1]**

| Symbol | | C | Parameter | Conditions | | Value[2] Typ | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD_HV_A(CAN)}$ | CC | D | CAN (FlexCAN) supply current on $V_{DD_HV_A}$ | 500 Kbps | Total (static + dynamic) consumption: FlexCAN in loop-back mode XTAL@8 MHz used as CAN engine clock source Message sending period is 580 µs | $7.652 \times f_{periph} + 84.73$ | µA |
| | | | | 125 Kbps | | $8.0743 \times f_{periph} + 26.757$ | |
| $I_{DD_HV_A(eMIOS)}$ | CC | D | eMIOS supply current on $V_{DD_HV_A}$ | Static consumption: eMIOS channel OFF Global prescaler enabled | | $28.7 \times f_{periph}$ | |
| | | | | Dynamic consumption: It does not change varying the frequency (0.003 mA) | | 3 | |
| $I_{DD_HV_A(SCI)}$ | CC | D | SCI (LINFlex) supply current on $V_{DD_HV_A}$ | Total (static + dynamic) consumption: LIN mode Baudrate: 20 Kbps | | $4.7804 \times f_{periph} + 30.946$ | |
| $I_{DD_HV_A(SPI)}$ | CC | D | SPI (DSPI) supply current on $V_{DD_HV_A}$ | Ballast static consumption (only clocked) | | 1 | |
| | | | | Ballast dynamic consumption (continuous communication): Baudrate: 2 Mbit Transmission every 8 µs Frame: 16 bits | | $16.3 \times f_{periph}$ | |
| $I_{DD_HV_A(ADC)}$ | CC | D | ADC supply current on $V_{DD_HV_A}$ | $V_{DD}$ = 5.5 V | Ballast static consumption (no conversion) | $0.0409 \times f_{periph}$ | mA |
| | | | | $V_{DD}$ = 5.5 V | Ballast dynamic consumption (continuous conversion) | $0.0049 \times f_{periph}$ | |
| IDD_HV_ADC0 | CC | D | ADC_0 supply current on $V_{DD_HV_ADC0}$ | $V_{DD}$ = 5.5 V | Analog static consumption (no conversion) | 200 | µA |
| | | | | | Analog dynamic consumption (continuous conversion) | 4 | mA |

**Table 48. On-chip peripherals current consumption[1]**

| Symbol | | C | Parameter | Conditions | | Value[2] | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | | Typ | |
| IDD_HV_ADC1 | CC | D | ADC_1 supply current on $V_{DD_HV_ADC1}$ | $V_{DD}$ = 5.5 V | Analog static consumption (no conversion) | 300 × $f_{periph}$ | µA |
| | | | | $V_{DD}$ = 5.5 V | Analog dynamic consumption (continuous conversion) | 6 | mA |
| $I_{DD_HV(FLASH)}$ | CC | D | CFlash + DFlash supply current on $V_{DD_HV_ADC}$ | $V_{DD}$ = 5.5 V | — | 13.25 | mA |
| $I_{DD_HV(PLL)}$ | CC | D | PLL supply current on $V_{DD_HV}$ | $V_{DD}$ = 5.5 V | — | 0.0031 × $f_{periph}$ | |

NOTES:
1 Operating conditions: $T_A$ = 25 °C, $f_{periph}$ = 8 MHz to 120 MHz.
2 $f_{periph}$ is in absolute value.

## 4.19.2 DSPI characteristics

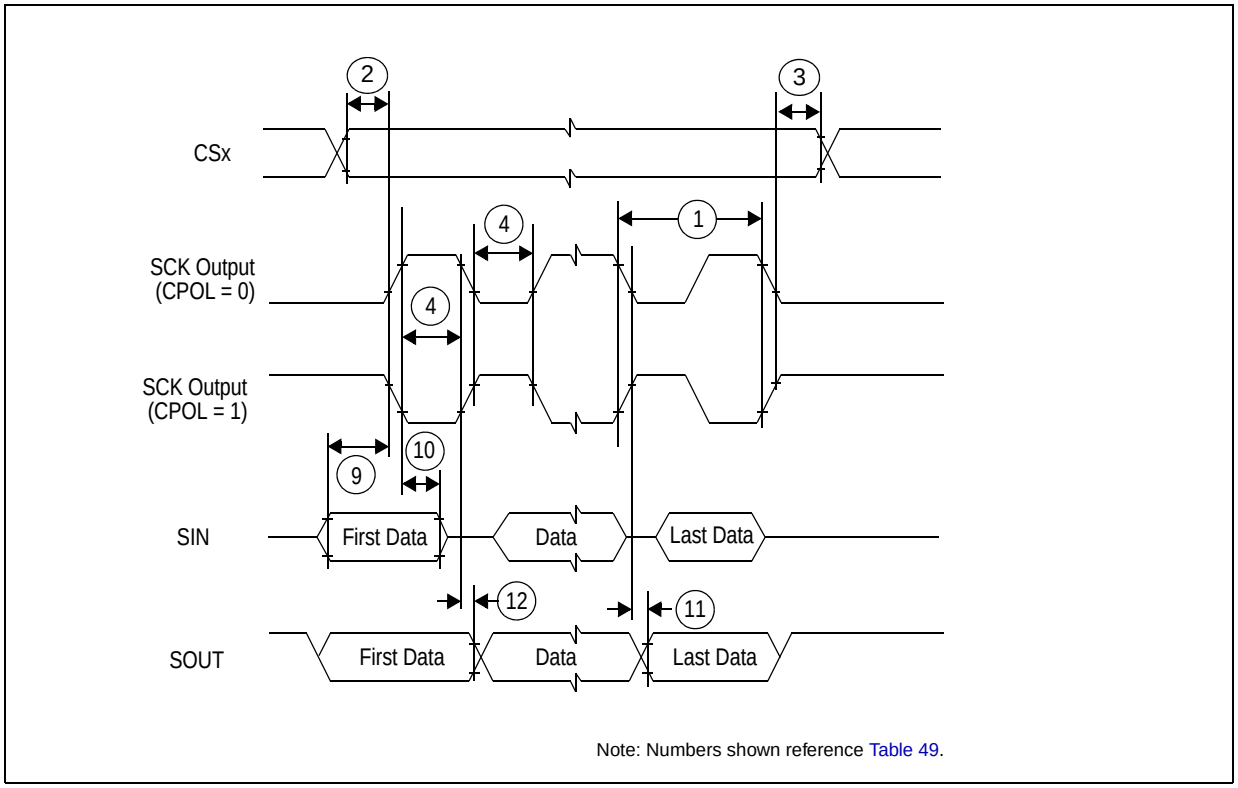
**Table 49. DSPI timing**

| Spec | Characteristic | Symbol | | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | DSPI Cycle Time | $t_{SCK}$ | Refer note[1] | — | ns |
| — | Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0 | $\Delta t_{CSC}$ | — | 115 | ns |
| — | Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1 | $\Delta t_{ASC}$ | 15 | — | ns |
| 2 | CS to SCK Delay[2] | $t_{CSC}$ | 7 | — | ns |
| 3 | After SCK Delay[3] | $t_{ASC}$ | 15 | — | ns |
| 4 | SCK Duty Cycle | $t_{SDC}$ | $0.4 \times t_{SCK}$ | $0.6 \times t_{SCK}$ | ns |
| — | Slave Setup Time ($\overline{SS}$ active to SCK setup time) | $t_{SUSS}$ | 5 | — | ns |
| — | Slave Hold Time ($\overline{SS}$ active to SCK hold time) | $t_{HSS}$ | 10 | — | ns |
| 5 | Slave Access Time ($\overline{SS}$ active to SOUT valid)[4] | $t_A$ | — | 42 | ns |
| 6 | Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid) | $t_{DIS}$ | — | 25 | ns |
| 7 | CSx to $\overline{PCSS}$ time | $t_{PCSC}$ | 0 | — | ns |
| 8 | $\overline{PCSS}$ to PCSx time | $t_{PASC}$ | 0 | — | ns |

**Table 49. DSPI timing (continued)**

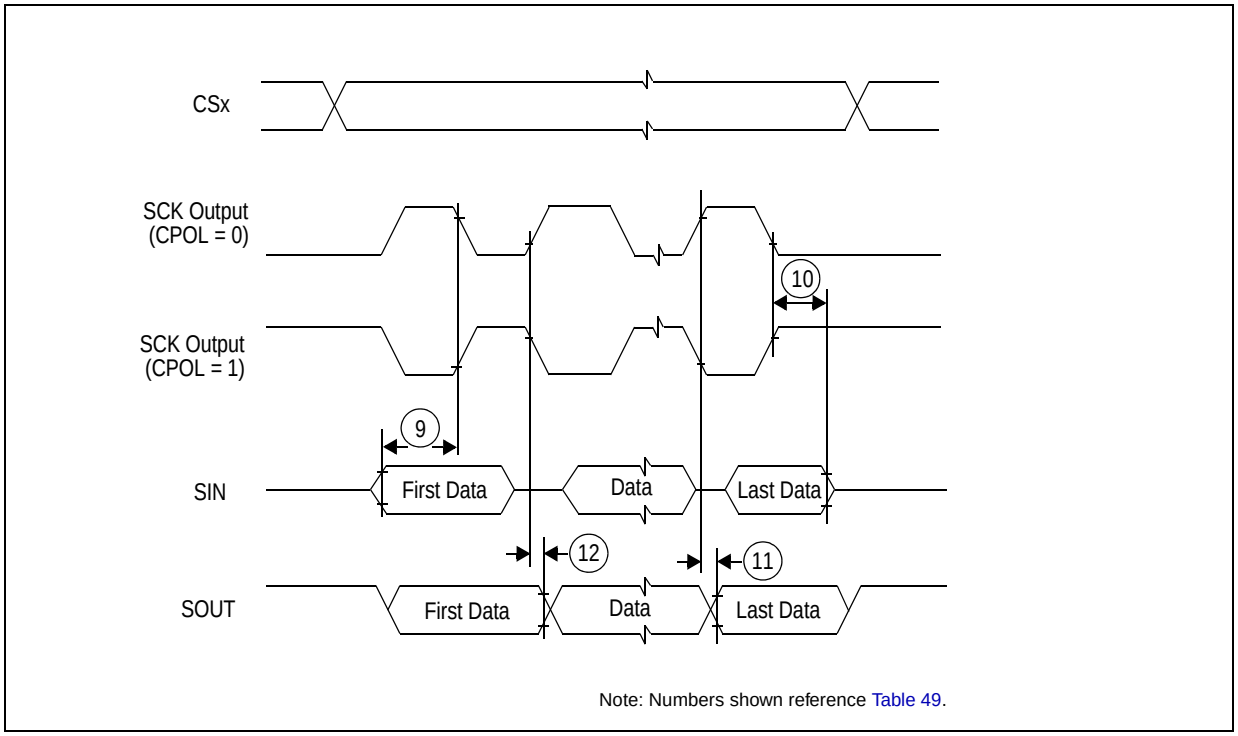
| Spec | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 9 | Data Setup Time for Inputs | $t_{SUI}$ | | | |
| | Master (MTFE = 0) | | 36 | — | ns |
| | Slave | | 5 | — | ns |
| | Master (MTFE = 1, CPHA = 0)[5] | | 36 | — | ns |
| | Master (MTFE = 1, CPHA = 1) | | 36 | — | ns |
| 10 | Data Hold Time for Inputs | $t_{HI}$ | | | |
| | Master (MTFE = 0) | | 0 | — | ns |
| | Slave | | 4 | — | ns |
| | Master (MTFE = 1, CPHA = 0)[5] | | 0 | — | ns |
| | Master (MTFE = 1, CPHA = 1) | | 0 | — | ns |
| 11 | Data Valid (after SCK edge) | $t_{SUO}$ | | | |
| | Master (MTFE = 0) | | — | 12 | ns |
| | Slave | | — | 37 | ns |
| | Master (MTFE = 1, CPHA = 0) | | — | 12 | ns |
| | Master (MTFE = 1, CPHA = 1) | | — | 12 | ns |
| 12 | Data Hold Time for Outputs | $t_{HO}$ | | | |
| | Master (MTFE = 0) | | 0[6] | — | ns |
| | Slave | | 9.5 | — | ns |
| | Master (MTFE = 1, CPHA = 0) | | 0[7] | — | ns |
| | Master (MTFE = 1, CPHA = 1) | | 0[8] | — | ns |

NOTES:
1. This value of this parameter is dependent upon the external device delays and the other parameters mentioned in this table.
2. The maximum value is programmable in DSPI_CTAR*n* [PSSCK] and DSPI_CTAR*n* [CSSCK]. For MPC5646C, the spec value of $t_{CSC}$ will be attained only if $T_{DSPI}$ x PSSCK x CSSCK > $\Delta t_{CSC}$.
3. The maximum value is programmable in DSPI_CTAR*n* [PASC] and DSPI_CTAR*n* [ASC]. For MPC5646C, the spec value of $t_{ASC}$ will be attained only if $T_{DSPI}$ x PASC x ASC > $\Delta t_{ASC.}$
4. The parameter value is obtained from $t_{SUSS}$ and $t_{SUO}$ for slave.
5. This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b00.
6. For DSPI1, the Data Hold Time for Outputs in Master (MTFE = 0) is –2 ns.
7. For DSPI1, the Data Hold Time for Outputs in Master (MTFE = 1, CPHA = 0) is –2 n.
8. For DSPI1, the Data Hold Time for Outputs in Master (MTFE = 1, CPHA = 1) is –2 ns.




Note: Numbers shown reference Table 49.

**Figure 25. DSPI classic SPI timing–master, CPHA = 0**




Note: Numbers shown reference Table 49.

**Figure 26. DSPI classic SPI timing–master, CPHA = 1**

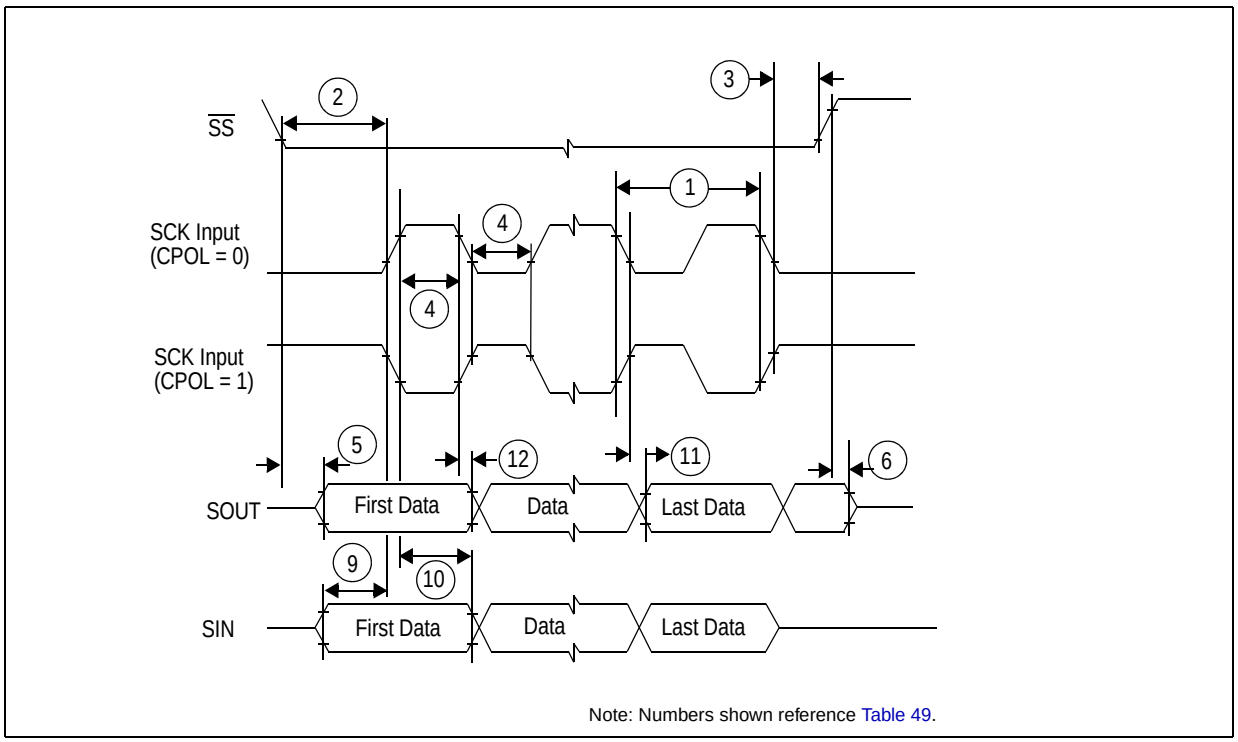



**Figure 27. DSPI classic SPI timing–slave, CPHA = 0**

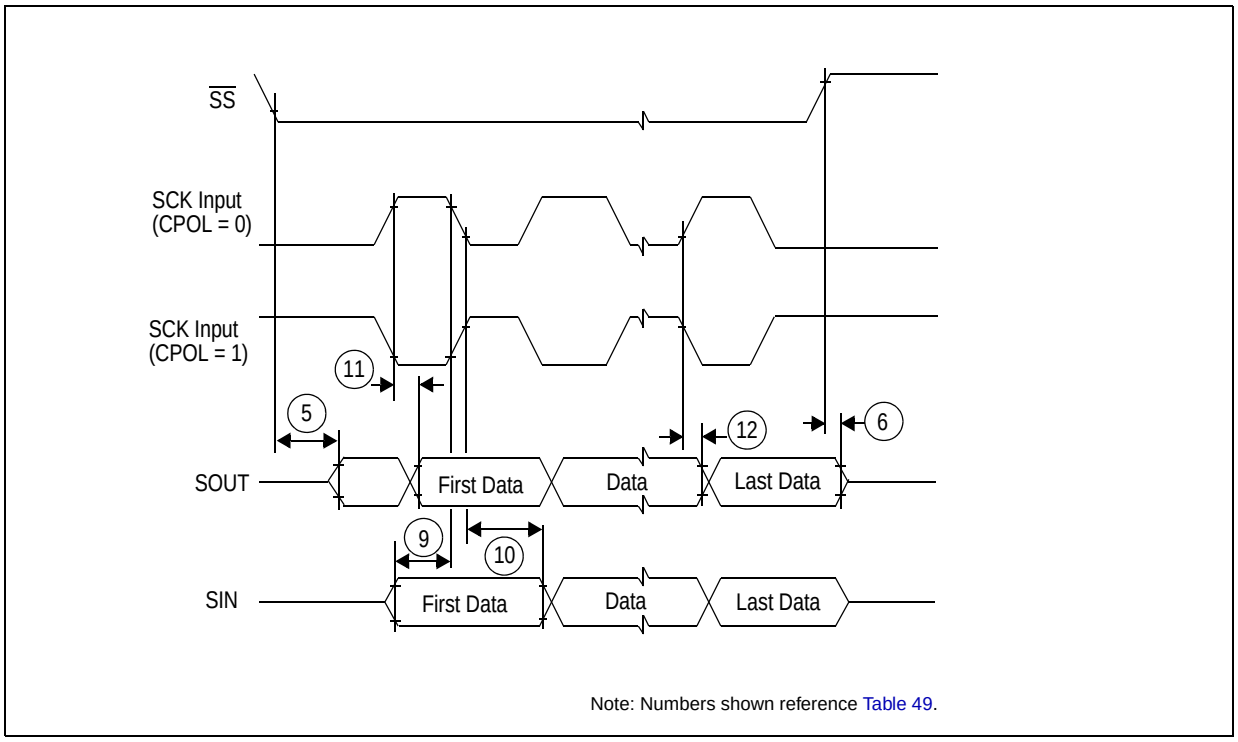



**Figure 28. DSPI classic SPI timing–slave, CPHA = 1**

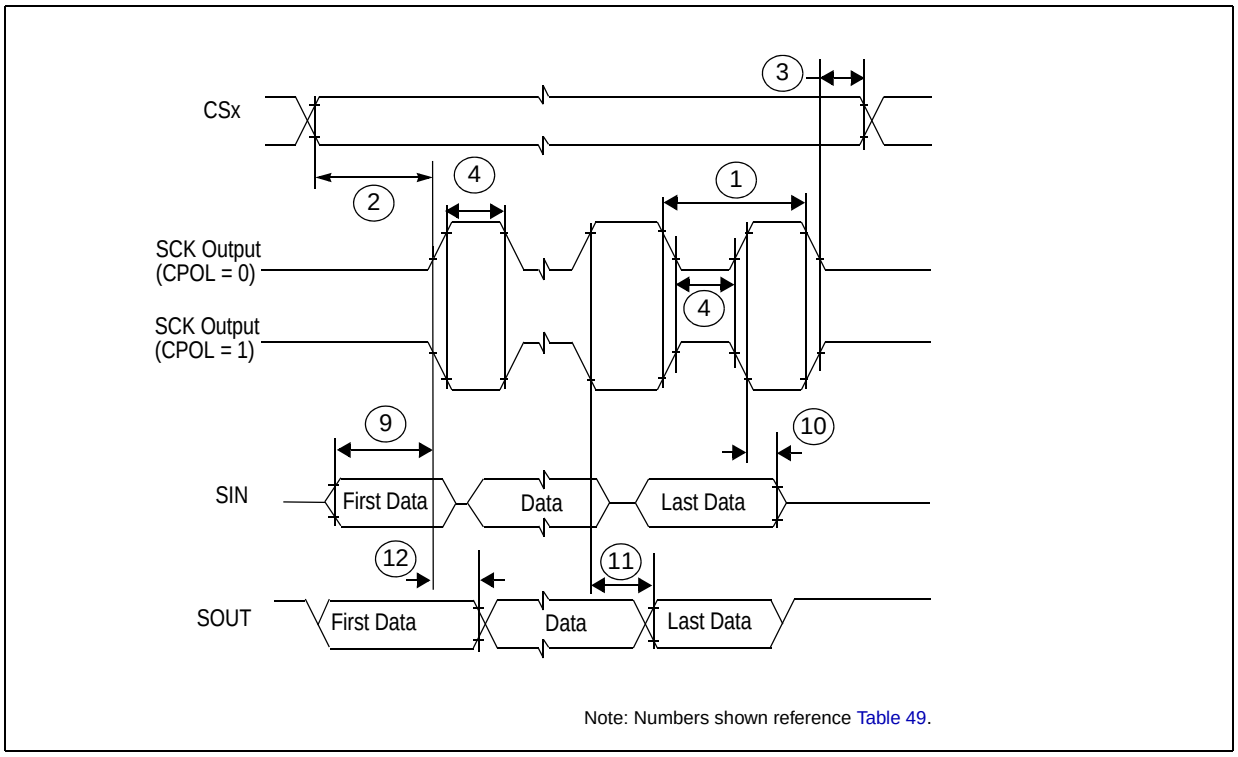



**Figure 29. DSPI modified transfer format timing–master, CPHA = 0**

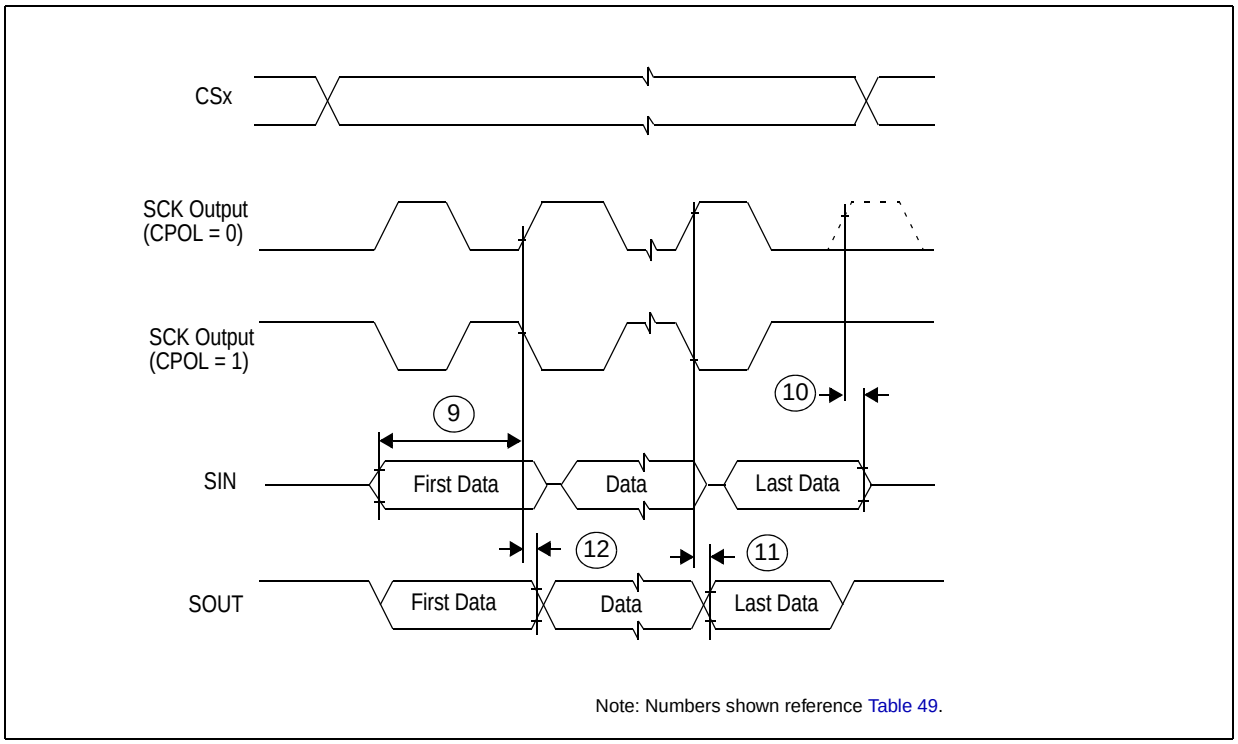



**Figure 30. DSPI modified transfer format timing–master, CPHA = 1**

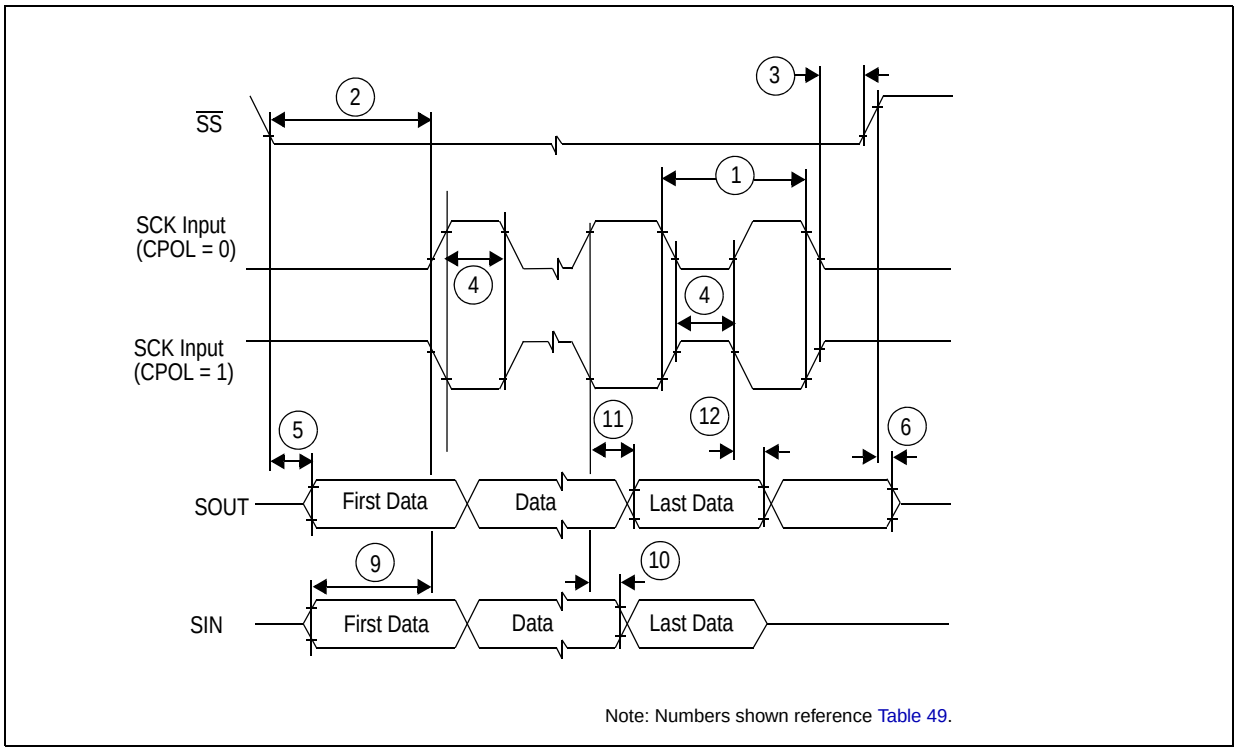



**Figure 31. DSPI modified transfer format timing–slave, CPHA = 0**

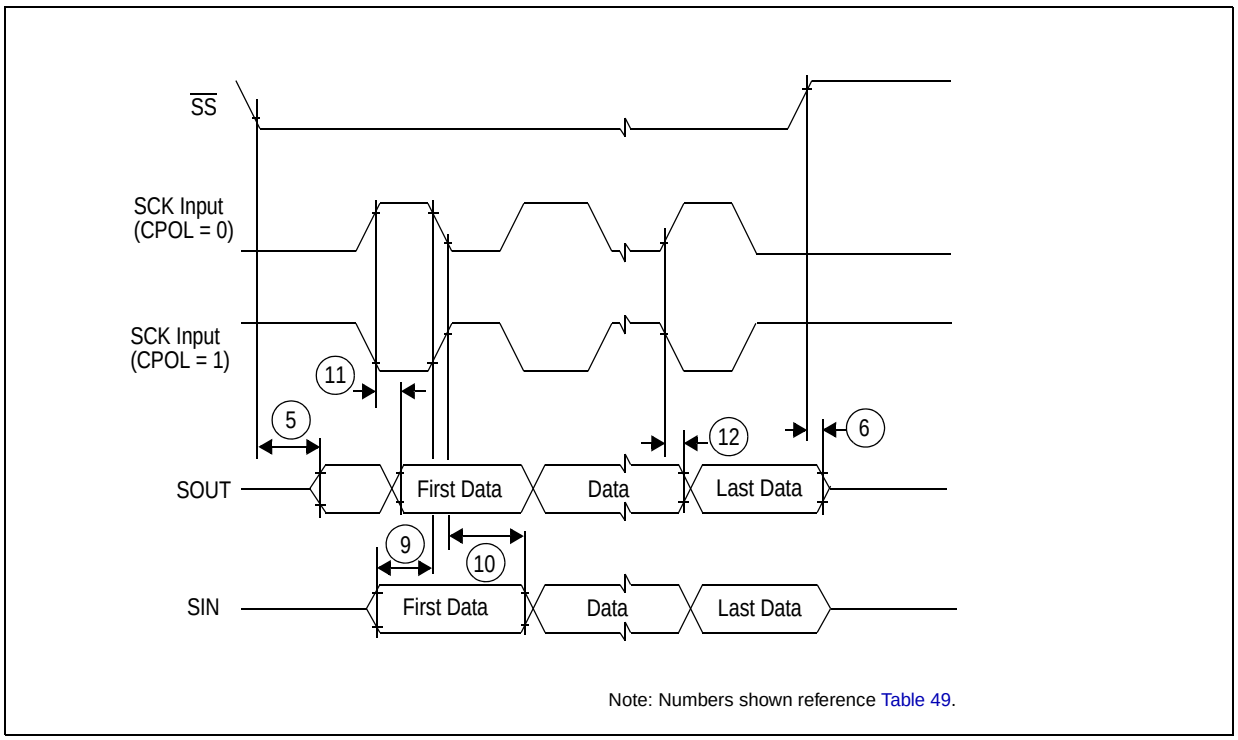
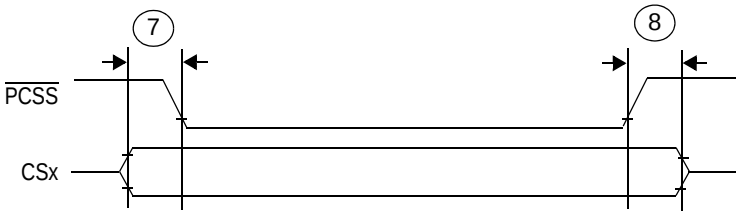



**Figure 32. DSPI modified transfer format timing–slave, CPHA = 1**




Note: Numbers shown reference Table 49.

**Figure 33. DSPI PCS strobe (PCSS) timing**

## 4.19.3 Nexus characteristics

**Table 50. Nexus debug port timing[1]**

| Spec | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | MCKO Cycle Time[2] | $t_{MCYC}$ | 16.3 | — | ns |
| 2 | MCKO Duty Cycle | $t_{MDC}$ | 40 | 60 | % |
| 3 | MCKO Low to MDO, MSEO, EVTO Data Valid[3] | $t_{MDOV}$ | –0.1 | 0.25 | $t_{MCYC}$ |
| 4 | EVTI Pulse Width | $t_{EVTIPW}$ | 4.0 | — | $t_{TCYC}$ |
| 5 | EVTO Pulse Width | $t_{EVTOPW}$ | 1 | | $t_{MCYC}$ |
| 6 | TCK Cycle Time[4] | $t_{TCYC}$ | 40 | — | ns |
| 7 | TCK Duty Cycle | $t_{TDC}$ | 40 | 60 | % |
| 8 | TDI, TMS Data Setup Time | $t_{NTDIS}$, $t_{NTMSS}$ | 8 | — | ns |
| 9 | TDI, TMS Data Hold Time | $t_{NTDIH}$, $t_{NTMSH}$ | 5 | — | ns |
| 10 | TCK Low to TDO Data Valid | $t_{JOV}$ | 0 | 25 | ns |

NOTES:
1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at $V_{DDE}$ = 4.0 – 5.5 V, $T_A = T_L$ to $T_H$, and $C_L$ = 30 pF with SRC = 0b11.
2. MCKO can run up to 1/2 of full system frequency. It can also run at system frequency when it is <60 MHz.
3. MDO, MSEO, and EVTO data is held valid until next MCKO low cycle.
4. The system clock frequency needs to be three times faster than the TCK frequency.

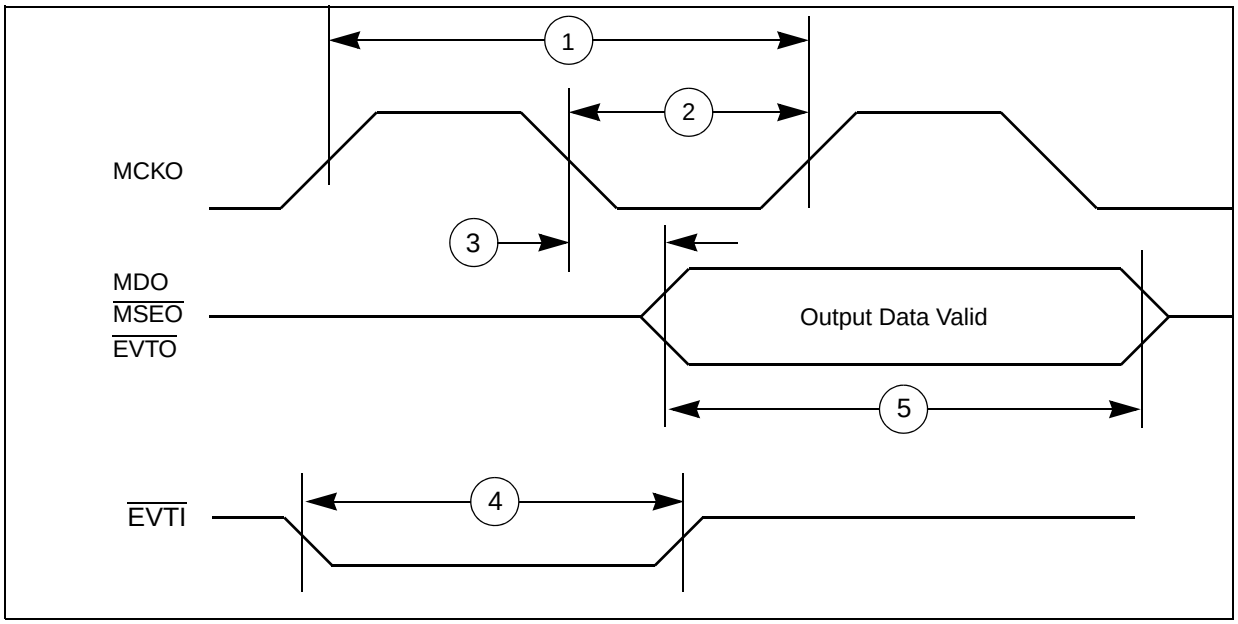



**Figure 34. Nexus output timing**

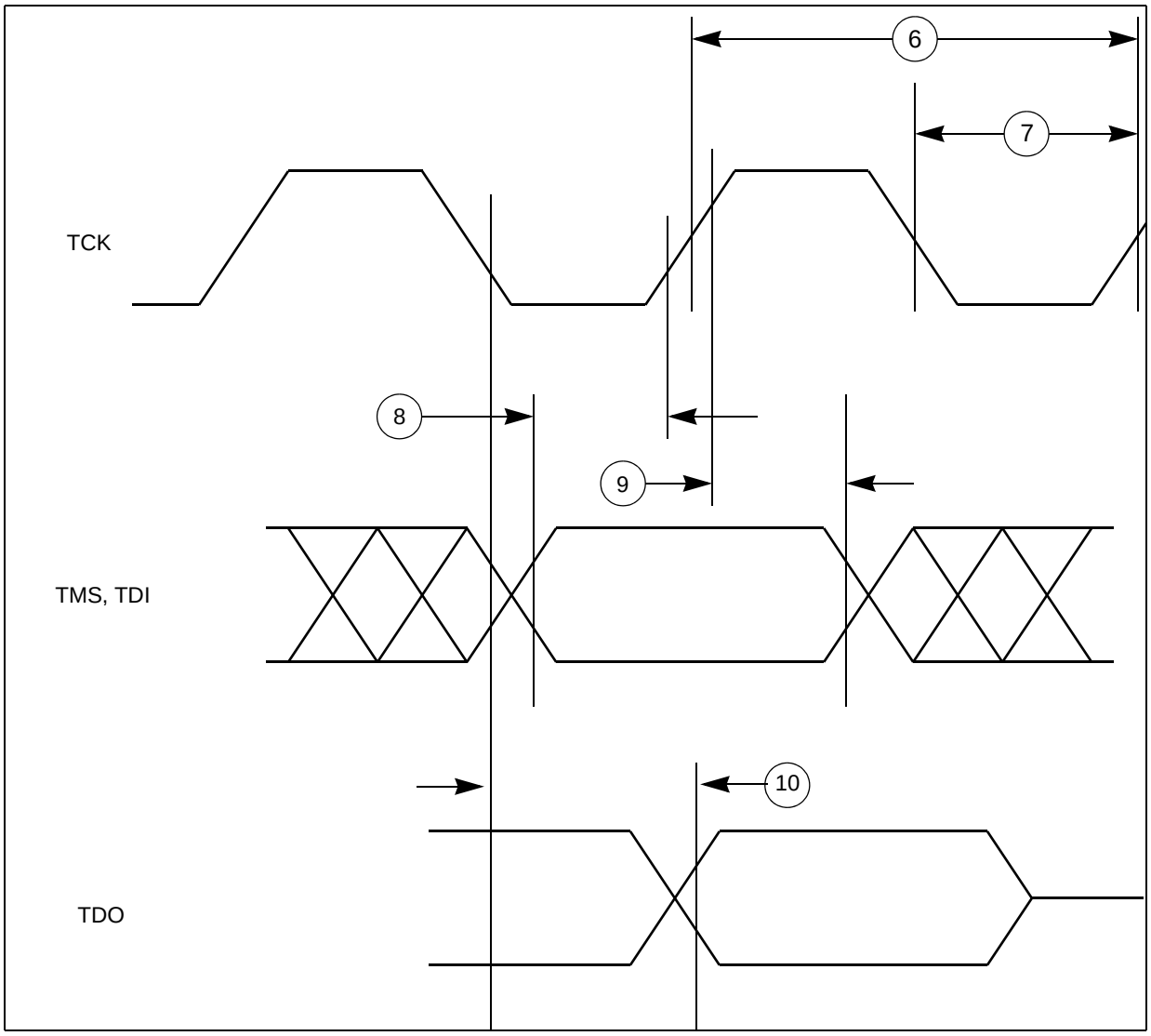



**Figure 35. Nexus TDI, TMS, TDO timing**

## 4.19.4 JTAG characteristics

**Table 51. JTAG characteristics**

| No. | Symbol | | C | Parameter | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| 1 | $t_{JCYC}$ | CC | D | TCK cycle time | 64 | — | — | ns |
| 2 | $t_{TDIS}$ | CC | D | TDI setup time | 10 | — | — | ns |
| 3 | $t_{TDIH}$ | CC | D | TDI hold time | 5 | — | — | ns |
| 4 | $t_{TMSS}$ | CC | D | TMS setup time | 10 | — | — | ns |
| 5 | $t_{TMSH}$ | CC | D | TMS hold time | 5 | — | — | ns |

**Table 51. JTAG characteristics (continued)**

| No. | Symbol | | C | Parameter | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| 6 | $t_{TDOV}$ | CC | D | TCK low to TDO valid | — | — | 33 | ns |
| 7 | $t_{TDOI}$ | CC | D | TCK low to TDO invalid | 6 | — | — | ns |
| — | $t_{TDC}$ | CC | D | TCK Duty Cycle | 40 | — | 60 | % |
| — | $t_{TCKRISE}$ | CC | D | TCK Rise and Fall Times | — | — | 3 | ns |

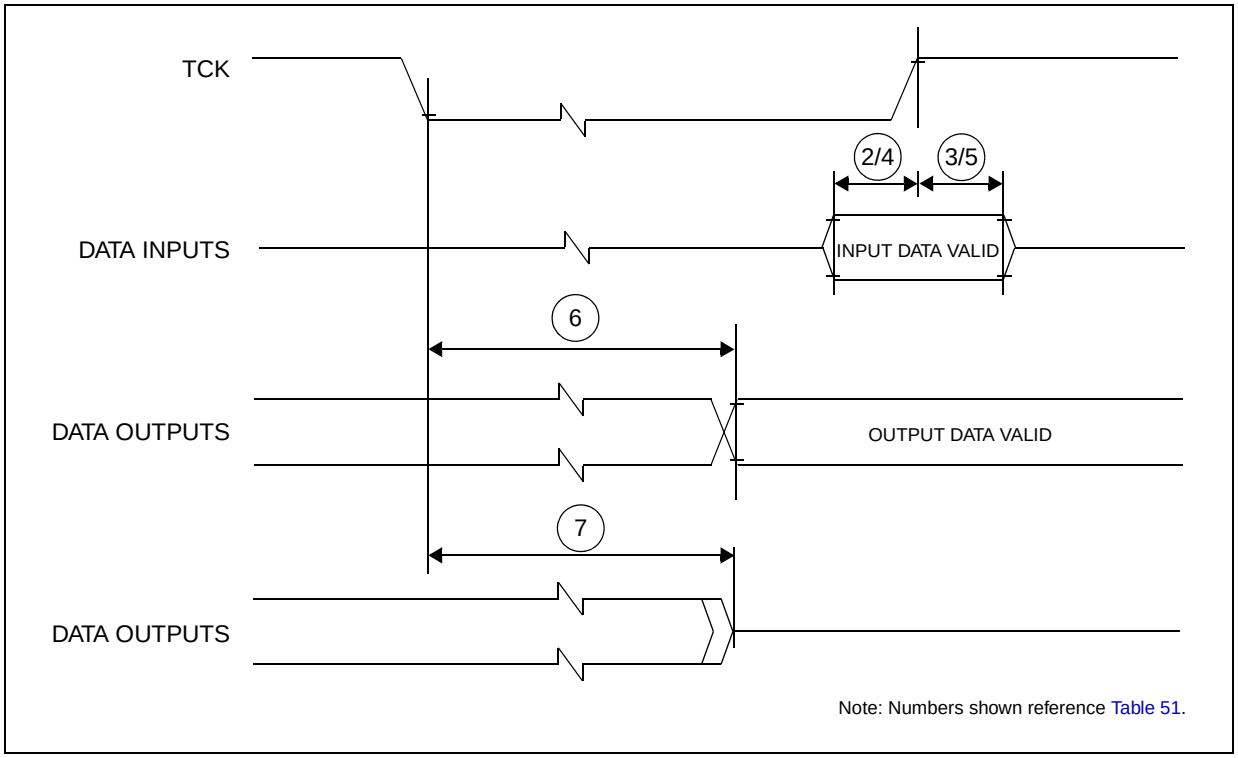



**Figure 36. Timing diagram - JTAG boundary scan**

# 5 Package characteristics

## 5.1 Package mechanical data

### 5.1.1 176 LQFP package mechanical drawing

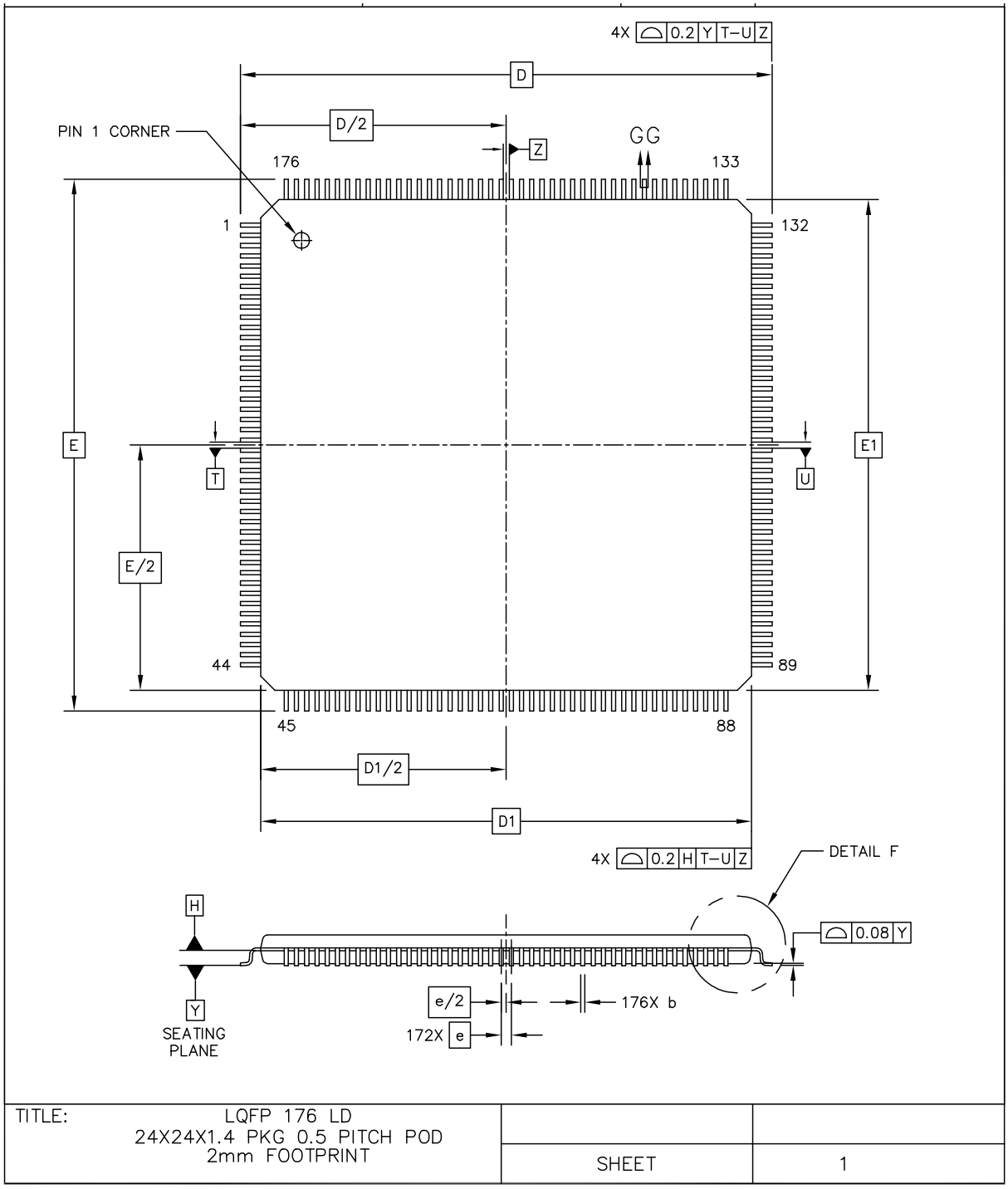



**Figure 37. 176 LQFP mechanical drawing (Part 1 of 3)**

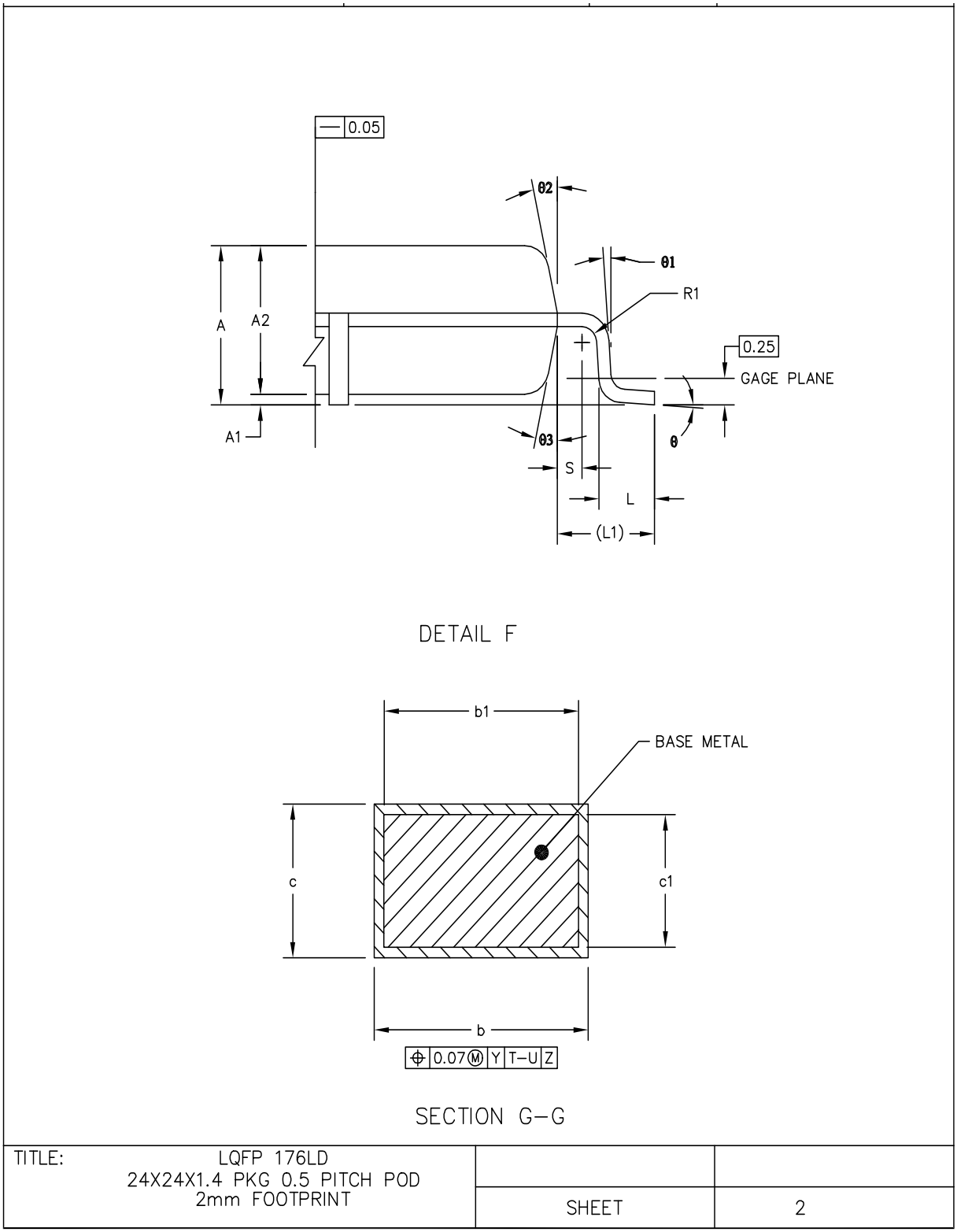



**Figure 38. 176 LQFP mechanical drawing (Part 2 of 3)**

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | --- | | 1.6 | L1 | | 1 REF | | | | | |
| A1 | 0.05 | | 0.15 | R1 | 0.08 | | --- | | | | |
| A2 | 1.35 | 1.4 | 1.45 | R2 | 0.08 | | 0.2 | | | | |
| b | 0.17 | 0.22 | 0.27 | S | | 0.2 REF | | | | | |
| b1 | 0.17 | 0.2 | 0.23 | θ | 0° | 3.5° | 7° | | | | |
| c | 0.09 | | 0.2 | θ1 | 0° | | --- | | | | |
| c1 | 0.09 | | 0.16 | θ2 | 11° | 12° | 13° | | | | |
| D | | 26 BSC | | θ3 | 11° | 12° | 13° | | | | |
| D1 | | 24 BSC | | | | | | | | | |
| e | | 0.5 BSC | | | | | | | | | |
| E | | 26 BSC | | | | | | | | | |
| E1 | | 24 BSC | | | | | | | | | |
| L | 0.45 | 0.6 | 0.75 | | | | | | | | |

| UNIT | DIMENSION AND TOLERANCES | REFERENCE DOCUMENT |
|---|---|---|
| MM | ASME Y14.5M | 64-06-280-1392 |

| TITLE: | | |
|---|---|---|
| LQFP 176LD<br>24X24X1.4 PKG 0.5 PITCH POD<br>2mm FOOTPRINT | | |
| | SHEET | 3 |

**Figure 39. 176 LQFP mechanical drawing (Part 3 of 3)**

## 5.1.2 208 LQFP package mechanical drawing

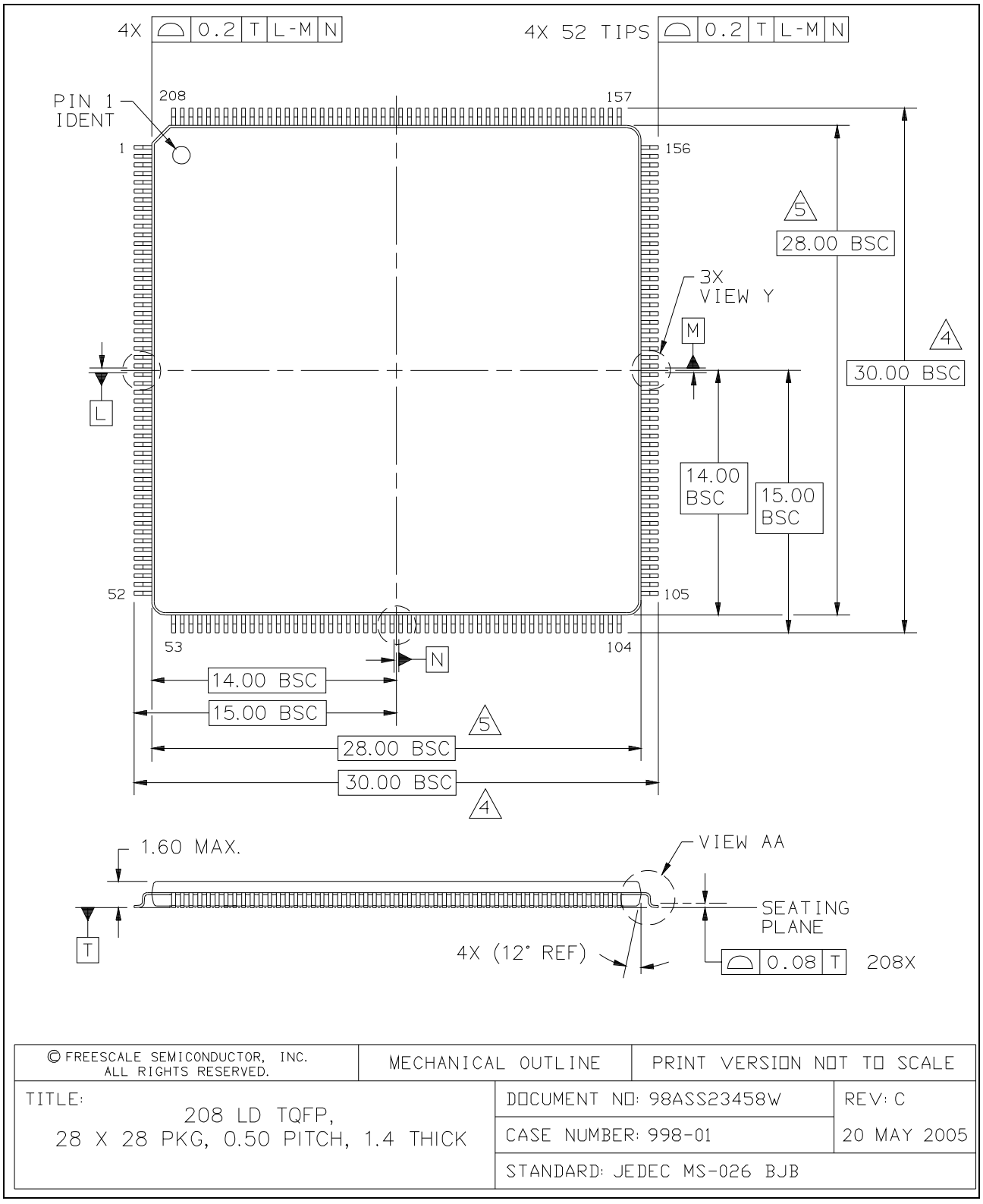



**Figure 40. 208 LQFP mechanical drawing (Part 1 of 3)**

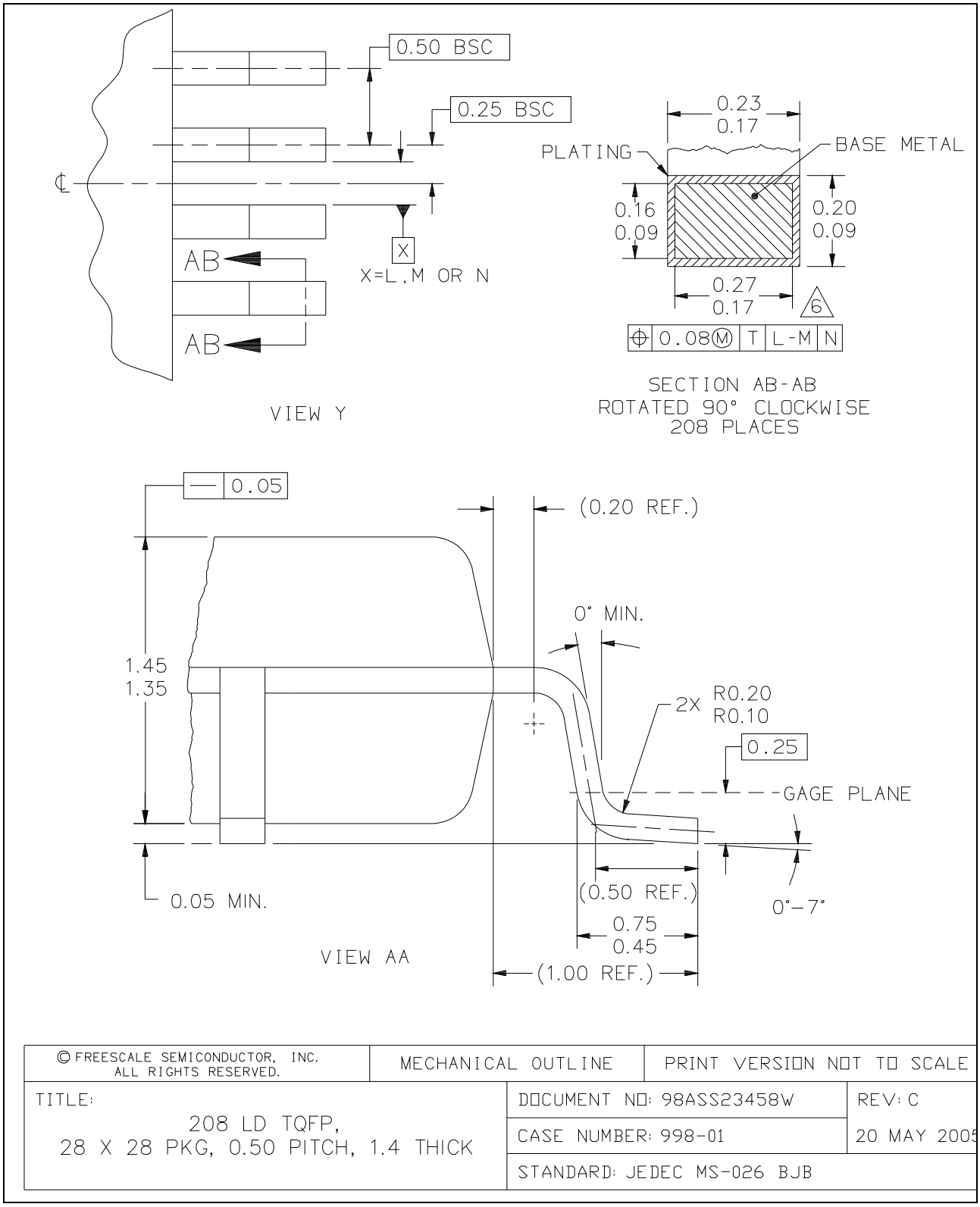



**Figure 41. 208 LQFP mechanical drawing (Part 2 of 3)**

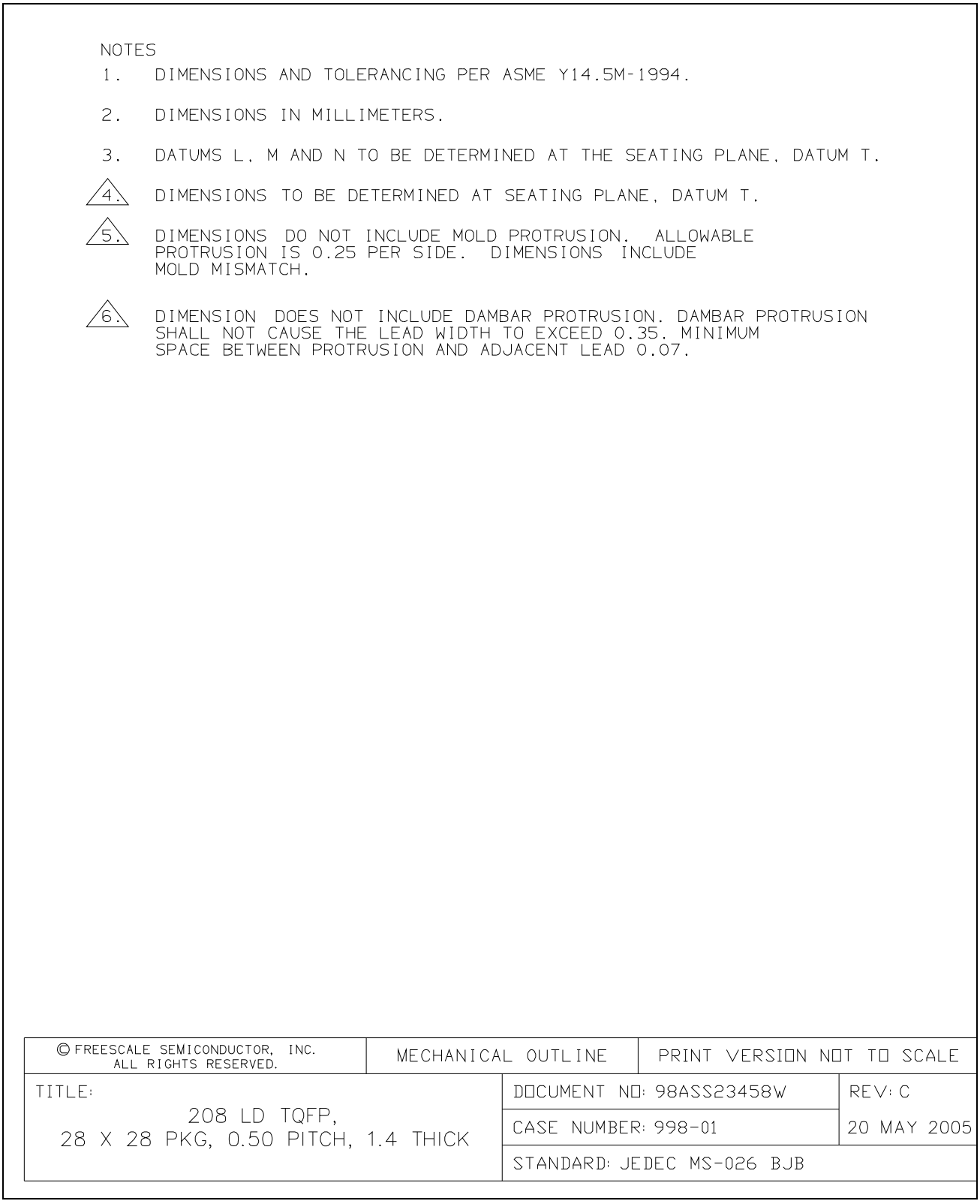



**Figure 42. 208 LQFP mechanical drawing (Part 3 of 3)**

### 5.1.3 256 MAPBGA package mechanical drawing

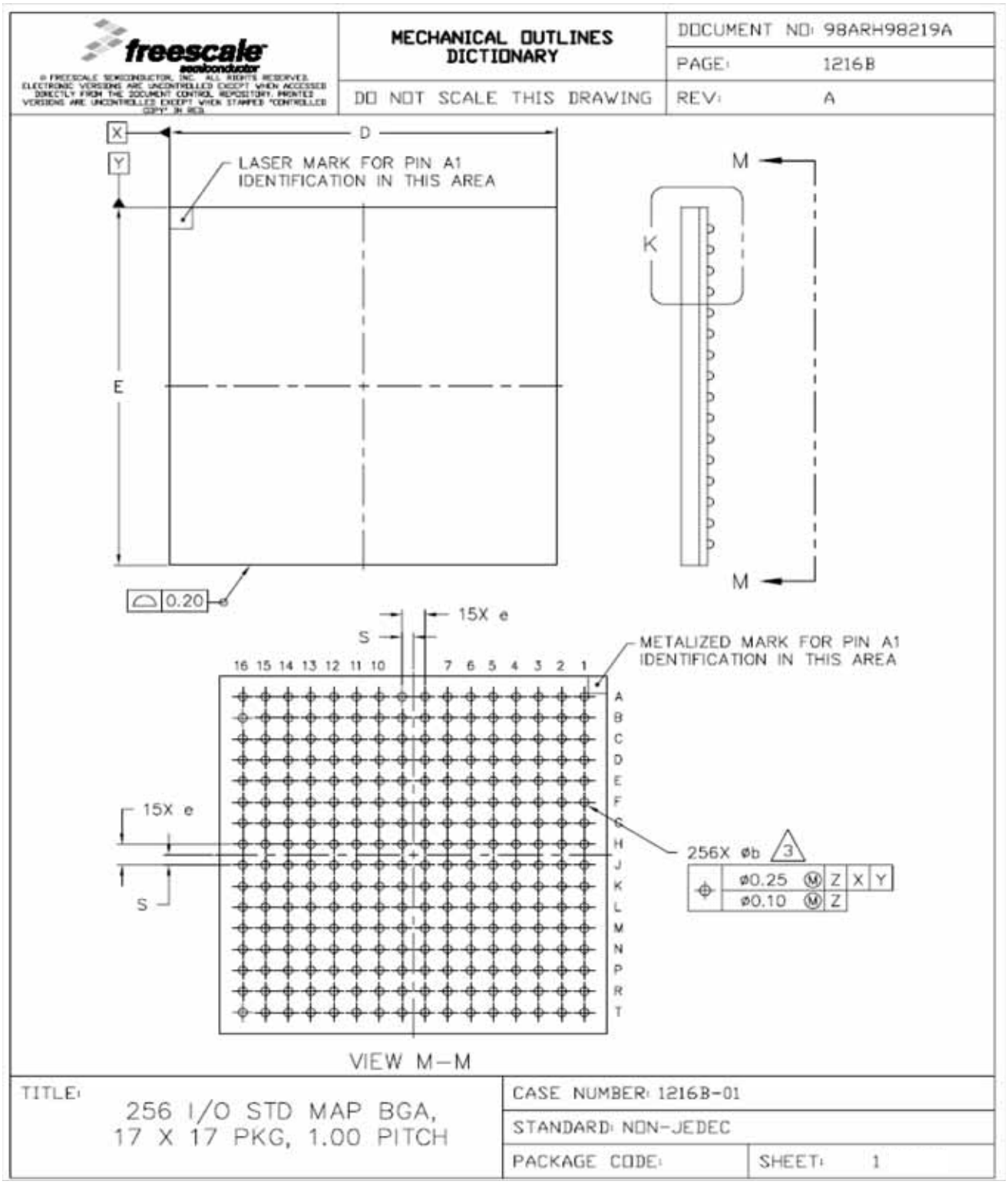



**Figure 43. 256 MAPBGA mechanical drawing (Part 1 of 2)**

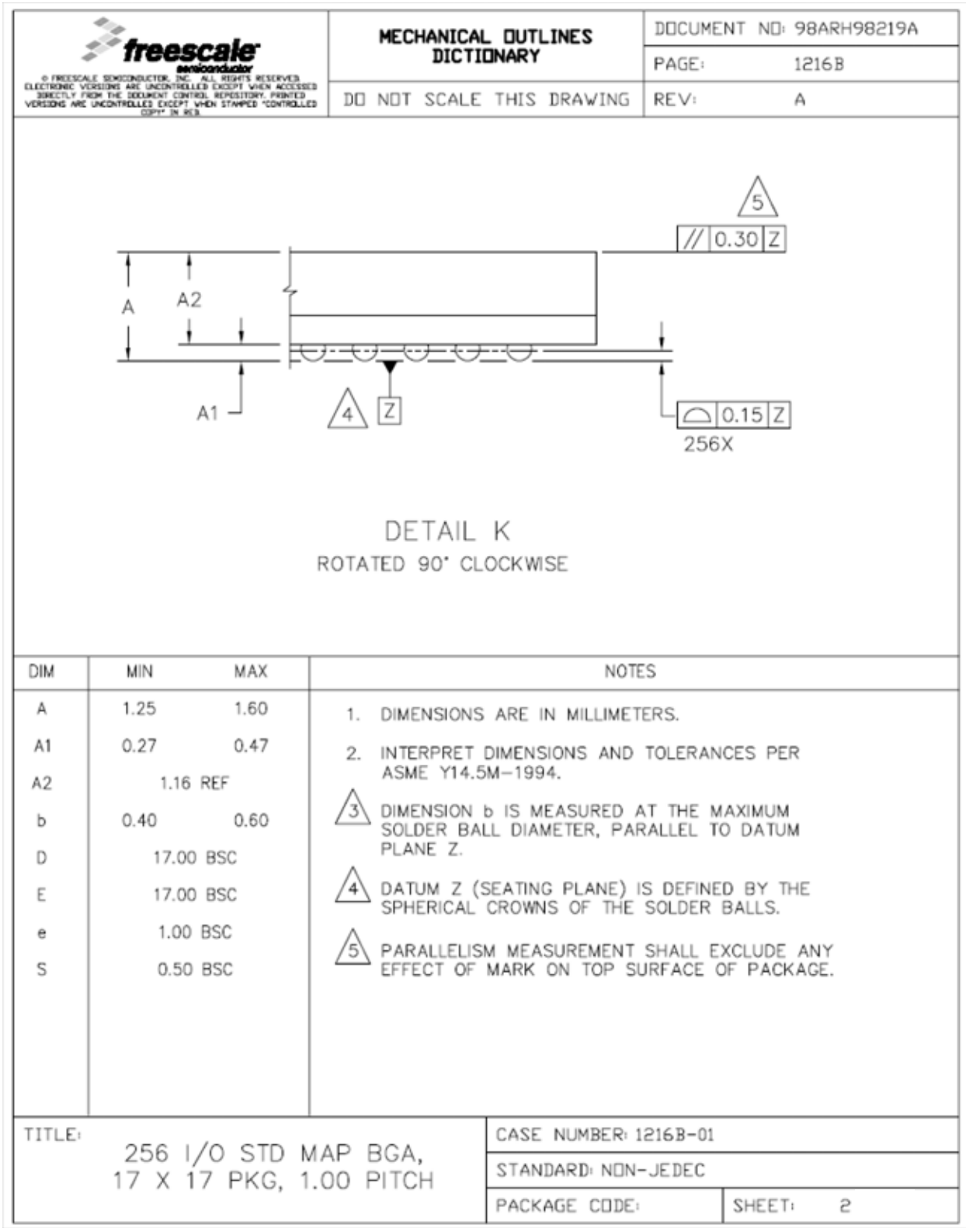
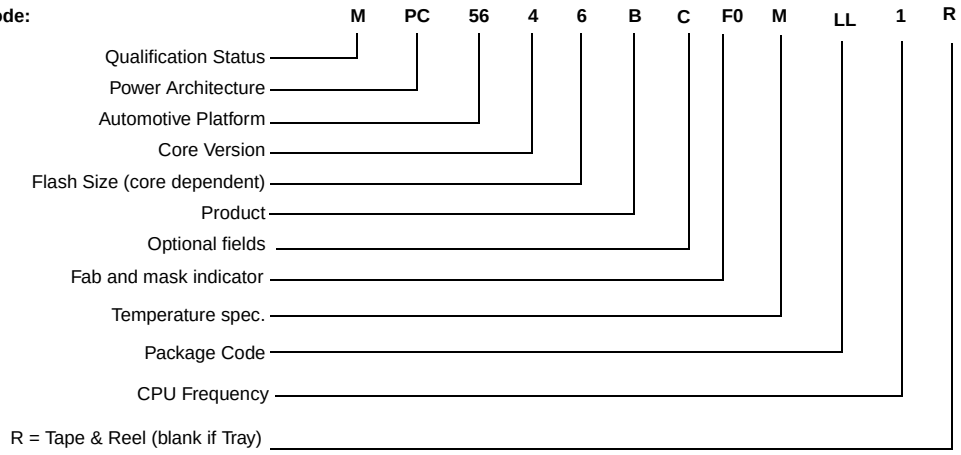



**Figure 44. 256 MAPBGA mechanical drawing (Part 2 of 2)**

# 6 Ordering information




**Qualification Status**
M = MC status
S = Auto qualified
P = PC status

**PC = Power Architecture**

**Automotive Platform**
56 = Power Architecture in 90 nm

**Core Version**
4 = e200z4d core version (highest core version in the case of multiple cores)

**Flash Memory Size**
4 = 1.5 MB
5 = 2 MB
6 = 3 MB

**Product Version**
B = Body
C = Gateway

**Optional fields**
C = CSE module available
Blank = none of these options available

**Fab and mask version indicator**
F = ATMC
0 = First version of the mask

**Temperature spec.**
C = –40 °C to 85 °C
V = –40 °C to 105 °C
M = –40 °C to 125 °C

**Package Code**
LU = 176 LQFP
LT = 208 LQFP
MJ = 256 MAPBGA

**CPU Frequency**
1 = e200z4d operates up to 120 MHz
8 = e200z4d operates up to 80 MHz

**Shipping Method**
R = Tape and reel
Blank = Tray

Note: Not all options are available on all devices. Refer to Table 1, which shows the orderable part numbers for MPC564xx.

**Figure 45. Orderable parts**

# 7 Revision history

Table 52 summarizes revisions to this document.

**Table 52. Revision history**

| Revision | Date | Changes |
|---|---|---|
| 1 | 15 April 2010 | Initial Release |
| 2 | 17 August 2010 | • Editing and formatting updates throughout the document.<br>• Updated Voltage regulator capacitance connection figure.<br>• Added a new sub-section "$V_{DD_BV}$ Options"<br>• Program and erase specifications:<br>-Updated Tdwprogram TYP to 22 us<br>-Updated T128Kpperase Max to 5000 ms<br>-Added $t_{ESUS}$ parameter<br>• Added 208 MAPBGA thermal characteristics<br>• Added recommendation in the Voltage regulator electrical characteristics section.<br>• Added Crystal description table in Fast external crystal oscillator (4 to 140 MHz) electrical characteristics section and corrected the cross-reference to the same.<br>• Added new sections - Pad types, System pins and functional ports<br>• Updated TYP numbers in the Flash program and erase specifications table<br>• Added a new table: Program and erase specifications (Data Flash)<br>• Flash read access timing table: Added Data flash memory numbers<br>• Flash power supply DC electrical characteristics table: Updated IDFREAD and IDFMOD values for Data flash, Removed IDFLPW parameter<br>• Updated feature list.<br>• MPC5646C 3M family comparison table: Updated ADC channels and added ADC footnotes.<br>• MPC5646C 3M block diagram: Updated ADC channels and added legends.<br>• MPC5646C 3M series block summary: Added new blocks.<br>• Functional Port Pin Descriptions table: Added OSC32k_XTAL and OSC32k_EXTAL function at PB8 and PB9 port pins.<br>• Electrical Characteristics: Replaced VSS with VSS_HV throughout the section.<br>• Absolute maximum ratings, Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V) tables: VRC_CTRL min is updated to "0".<br>• Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V) tables: Clarified VIN parameter, clarified footnote 2 in both tables.<br>• LQFP thermal characteristics section: Updated numbers for LQFP packages.<br>• Low voltage power domain electrical characteristics table: Clarified footnotes based upon review comments.<br>• Code flash memory—Program and erase specifications: Updated tESRT to 20 ms.<br>• ADC electrical characteristics section: Replace ADC0 with ADC_0 and ADC1 with ADC_1 throughout the document.<br>• DSPI characteristics section: Replaced PCSx with CSx in all figures and tables. |

**Table 52. Revision history (continued)**

| Revision | Date | Changes |
|---|---|---|
| 3 | 28 April 2011 | • Replaced VIL min from –0.4 V to –0.3 V in the following tables:<br>- I/O input DC electrical characteristics<br>- Reset electrical characteristics<br>- Fast external crystal oscillator (4 to 40 MHz) electrical characteristics<br>• Updated Crystal oscillator and resonator connection scheme figure<br>• Specified NPN transistor as the recommended BCP68 transistor throughout the document<br>• Code and Data flash memory—Program and erase specifications tables: Renamed the parameter $t_{ESUS\ to}$ $T_{eslat}$<br>• Revised the footnotes in the “Functional port pin descriptions” table.<br>• In the “System pin descriptions” table, added a footnote to the A pads regarding not using IBE.<br>For ports PB[12–15], changed ANX to ADC0_X.<br>• Revised the presentation of the ADC functions on the following ports:<br>PB[4–7]<br>PD[0–11]<br>• ADC conversion characteristics (10-bit ADC_0) table and Conversion characteristics (12-bit ADC_1) table- Updated footnote 5 and 7 respectively for the definition of the conversion time.<br>• Data flash memory—Program and erase specifications: Updated $T_{wprogram}$ to 500 µs and $T_{16Kpperase}$ to 500 µs. Corrected Teslat classification from “C” to “D”.<br>• Code flash memory—Program and erase specifications: Corrected Teslat classification from “C” to “D”.<br>• Flash Start-up time/Switch-off time: Changed $T_{FLARSTEXIT}$ classification from “C” to “D”.<br>• Functional port pin description: Added a footnote at the PB [9] port pin.<br>• Absolute maximum ratings table: Added footnote 1.<br>• Low voltage power domain electrical characteristics table: Updated IDDHALT, IDDSTOP, IDDSTBY3, IDDSTDBY2, IDDSTDBY1.<br>• Slow external crystal oscillator (32 kHz) electrical characteristics table: Updated $g_{mSXOSC}$, $V_{SXOSC}$, $I_{SXOSCBIAS}$ and $I_{SXOSC}$.<br>• FMPLL electrical characteristics table: Updated $\Delta t_{LTJIT}$.<br>• Fast internal RC oscillator (16 MHz) electrical characteristics table: Updated TFIRCSU and IFIRCPWD.<br>• MII serial management channel timing table: Updated M12<br>• JTAG characteristics table: Updated $t_{TDOV}$.<br>• Low voltage monitor electrical characteristics table: Updated VLVDHV3H, VLVDHV3L, VLVDHV5H, VLVDHV5L.<br>• DSPI electricals table: Updated spec 1, 5, 6. Updated footnote 2 and 3. Added $\Delta t_{CSC}$, $\Delta t_{ASC}$, $t_{SUSS}$, $t_{HSS}$.<br>• IO consumption table: Updated all parameter values.<br>• DSPI electricals: Updated $\Delta t_{CSC}$ max to 115 ns.<br>• Low voltage power domain electrical characteristics table: Added footnote 9.<br>• ADC electrical characteristics: Added 2 notes above 10-bit and 12-bit conversion tables. |

**Table 52. Revision history (continued)**

| Revision | Date | Changes |
|---|---|---|
| 4 | 23 June 2011 | • Interchanged the denominator with numerator in Equation 11 of Input impedance and ADC accuracy section<br>• Removed the note (All ADC conversion characteristics described in the table below are applicable only for the precision channels. The data for semi-precision and extended channels is awaited and same will be subsequently updated in later revs.) in the ADC electrical characteristics section.<br>• In On-chip peripherals current consumption table, replaced IDD_HV_ADC with IDD_HV_ADC0 and IDD_HV_ADC1 values as per ADC specs<br>• In ADC conversion characteristics (10-bit ADC_0) table, the minimum sample time of ADC0 changed to 500 at 32 MHz<br>• In ADC conversion characteristics (10-bit ADC_0) table, removed the entry for sample time at 30 MHz<br>• In Conversion characteristics (12-bit ADC_1)table, changed TUEX to TUES and INLX to INLS (Extended channels are not supported by the device. So, changed to standard channel.) |

**Table 52. Revision history (continued)**

| Revision | Date | Changes |
|---|---|---|
| 5 | 21 June 2012 | • Updated the pins 23 and 24 of Figure 2.176-pin LQFP configuration<br>• Updated unit of measure in Table 43 Conversion characteristics (12-bit ADC_1)<br>• Modified the value to typical value in Table 48 On-chip peripherals current consumption<br>• Added footnote to $t_{ESRT}$ parameter in Table 25 Code flash memory—Program and erase specifications<br>• Added footnote to $t_{ESRT}$ parameter in Table 26 Data flash memory—Program and erase specifications<br>• Updated Table 28 Flash memory read access timing.<br>• Updated Notes 2 and Notes 3 of Table 9 Recommended operating conditions (3.3 V) and Table 10 Recommended operating conditions (5.0 V) respectively.<br>• Updated the footnote1 of Table 9 Recommended operating conditions (3.3 V) and Table 10 Recommended operating conditions (5.0 V)<br>• Updated $V_{DD_HV_A}$ to $V_{DD_BV}$ for $C_{DEC2}$ and $I_{DD_HV_A}$ in Table 22 Voltage regulator electrical characteristics and deleted footnote3<br>• Updated the dedicated number of channels for 12-bit ADC in family comparison tables<br>• Updated the values of $f_{SIRC,}$ parameters and conditions of $\Delta_{SIRCVAR}$ in Table 40 Slow internal RC oscillator (128 kHz) electrical characteristics<br>• Updated second footnote in Table 10, Recommended operating conditions (5.0 V)<br>• Updated the value of $t_{ADC0_PU}$ in Table 42, ADC conversion characteristics (10-bit ADC_0)<br>• Updated the IDD values in Table 24, Low voltage power domain electrical characteristics<br>• Added footnote to Table 24, Low voltage power domain electrical characteristics related to current drawn from $V_{DD_HV_A}$ and $V_{DD_HV_B}$<br>• Updated entire Section 4.17.1.1, ”Input impedance and ADC accuracy”- Updated the values of VLPREG in Table 22, Voltage regulator electrical characteristics.<br>• Updated the values of $V_{LPREG}$ in Table 22, Voltage regulator electrical characteristics.<br>• Added $T_A$ = 25 °C, min and max values of $V_{MREG}$ in Table 22, Voltage regulator electrical characteristics<br>• Added $T_A$ = 25 °C, min and max values of $V_{LPREG}$ in Table 22, Voltage regulator electrical characteristics<br>• Updated the min, max and typical values of $V_{LVDLVCORL}$ and $V_{LVDLVBKPL}$ in Table 23, Low voltage monitor electrical characteristics<br>• Updated values of gmFXOSC in Table 35, Fast external crystal oscillator (4 to 40 MHz) electrical characteristicsUpdated values of gmSXOSC in Table 37, Slow external crystal oscillator (32 kHz) electrical characteristics<br>• Updated the footnote 5 for $T_{ADC0_C}$ in Table 42, ADC conversion characteristics (10-bit ADC_0)<br>• Updated the footnotes of Table 24, Low voltage power domain electrical characteristics |
| 5.1 | 15 Aug 2012 | • Removed Footer: Preliminary tag |

**Table 52. Revision history (continued)**

| Revision | Date | Changes |
|---|---|---|
| 6 | 12 Feb 2014 | • Removed occurrences of 208BGA from Table 3 System pin descriptions.<br>• Added PM[3] and PM[4] in the figure note 1 of Figure 4, 256-pin BGA configuration.<br>• Added a table note in Table 19 I/O supplies.<br>• Updated Figure 8, Voltage regulator capacitance connection and added a note in this figure.<br>• Removed max values of $V_{LPREG}$ and $V_{MREG}$, changed min value of $V_{LPREG}$ to 1.21 V, and updated $V_{MREG}$ and $V_{LPREG}$ after trimming values in Table 22 Voltage regulator electrical characteristics.<br>• Updated 1st footnote and updated max values for $I_{DDRUN}$, $I_{DDHALT}$, $I_{DDSTOP}$, $I_{DDSTDBY3}$, $I_{DDSTDBY2}$, $I_{DDSTDBY1}$ and removed values at 85°C and 105°C in Table 24 Low voltage power domain electrical characteristics.<br>• Added a footnote below Table 28 Flash memory read access timing.<br>• Updated the formula in Eq. 11 in Section 4.17.1.1, "Input impedance and ADC accuracy.<br>• Added Figure 17, Input equivalent circuit (extended channels).<br>• Updated $t_{ADC0_PU}$ value to 1.5 as max and added footnote for $I_{INJ}$ in Table 42 ADC conversion characteristics (10-bit ADC_0).<br>• Added Category column in Table 43 Conversion characteristics (12-bit ADC_1).<br>• Added the IDD_HV_ADC0 values in Table 48 On-chip peripherals current consumption.<br>• Added a note in Figure 45, Orderable parts. |

**NOTE**

This revision history uses clickable cross-references for ease of navigation. The numbers and titles in each cross-reference are relative to the latest published release.

# Appendix A
# Abbreviations

Table 53 lists abbreviations used but not defined elsewhere in this document.

**Table 53. Abbreviations**

| Abbreviation | Meaning |
|---|---|
| CS | Chip select |
| EVTO | Event out |
| MCKO | Message clock out |
| MDO | Message data out |
| MSEO | Message start/end out |
| MTFE | Modified timing format enable |
| SCK | Serial communications clock |
| SOUT | Serial data out |
| TBD | To be defined |
| TCK | Test clock input |
| TDI | Test data input |
| TDO | Test data output |
| TMS | Test mode select |

***How to Reach Us:***

***Home Page:***
www.freescale.com

***Web Support:***
http://www.freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer’s technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: http://www.reg.net/v2/webservices/Freescale/Docs/TermsandConditions.html.

Freescale, the Freescale logo, is trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.
© 2009-2014 Freescale Semiconductor, Inc.

MPC5646C
Rev.6
02/2014

LifeElectronics
Живое партнерство

**ООО «ЛайфЭлектроникс»** **“LifeElectronics” LLC**

*ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703*

*Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.*

*С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров*

*Мы предлагаем:*

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

*В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.*

*Конструкторский отдел помогает осуществить:*

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

*Тел: +7 (812) 336 43 04 (многоканальный)*
*Email: org@lifeelectronics.ru*

***www.lifeelectronics.ru***