# 2M x 36, 2M x 32, 4M x 18
# 72 Mb SYNCHRONOUS PIPELINED, SINg LE CYCLE DESELECT STATIC RAM

**APRIL 2015**

## FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- JTAG Boundary Scan for PBGA package
- Power Supply

  LPS: $V_{DD}$ 3.3V (± 5%), $V_{DDQ}$ 3.3V/2.5V (± 5%)

  VPS: $V_{DD}$ 2.5V (± 5%), $V_{DDQ}$ 2.5V (± 5%)

  VVPS: $V_{DD}$ 1.8V (± 5%), $V_{DDQ}$ 1.8V (± 5%)
- JEDEC 100-Pin TQFP, 119-ball PBGA, and 165-ball PBGA packages
- Lead-free available

## DESCRIPTION

The 72Mb product family features high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61LPS/VPS204836B and IS64LPS204836B are organized as 2,096,952 words by 36 bits. The IS61LPS204832B is organized as 2,096,952 words by 32 bits. The IS61LPS/VPS409618B is organized as 4,193,904 words by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. The byte write operation is performed by using the byte write enable ($\overline{BWE}$) input combined with one or more individual byte write signals ($\overline{BWx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{ADV}$ (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

## FAST ACCESS TIME

| Symbol | Parameter | 250 | 200 | 166 | Units |
|---|---|---|---|---|---|
| $t_{KQ}$ | Clock Access Time | 2.8 | 3.1 | 3.8 | ns |
| $t_{KC}$ | Cycle Time | 4 | 5 | 6 | ns |
| | Frequency | 250 | 200 | 166 | MHz |

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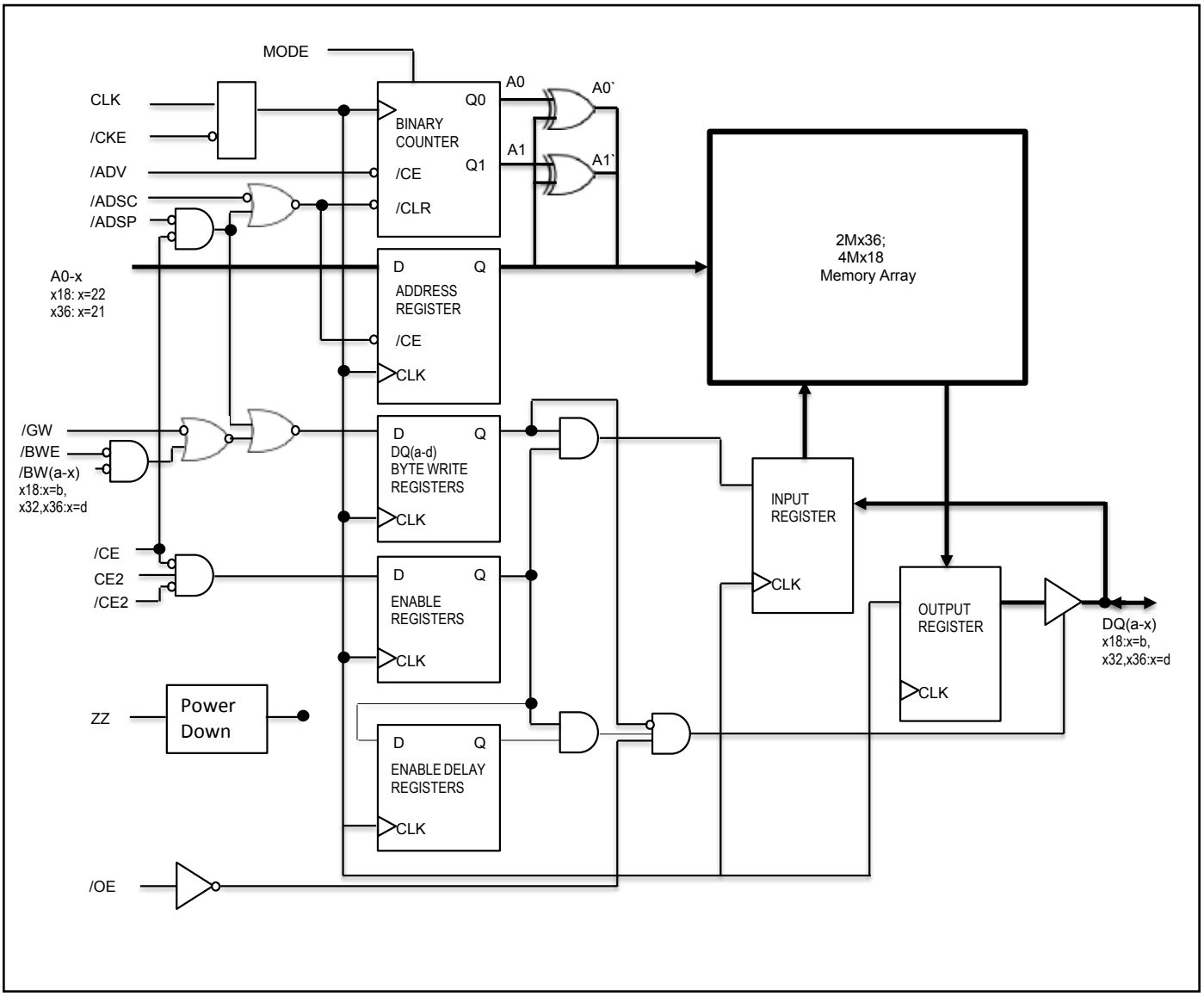
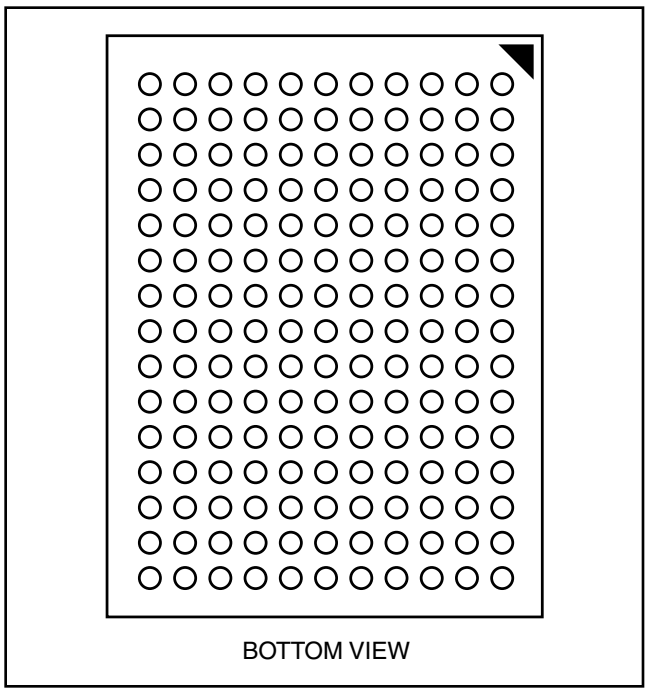
a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

## BLOCK DIAGRAM



## 165-PIN Bg A

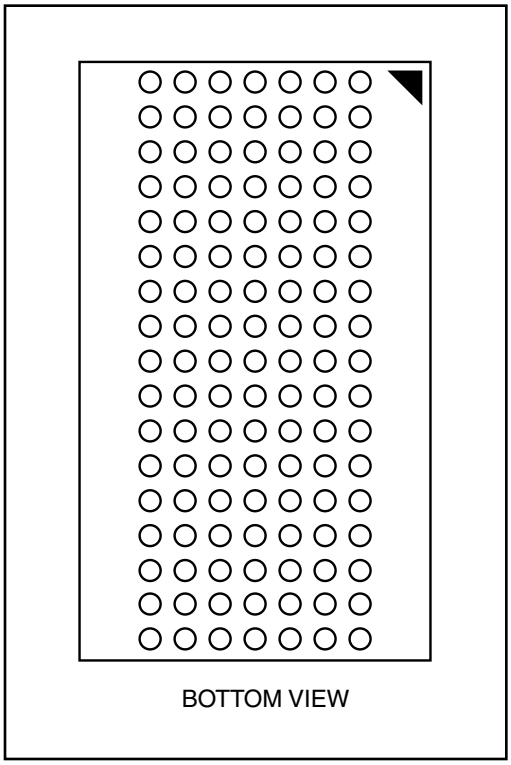
165-Ball, 13x15 mm BGA
165-Ball, 15x17 mm BGA
1mm Ball Pitch, 11x15 Ball Array



BOTTOM VIEW

## 119-PIN Bg A

119-Ball, 14x22 mm BGA
1.27mm Ball Pitch, 7x17 Ball Array



BOTTOM VIEW

## 119 BGA PACKAGE PIN CONFIGURATION-2M x 36 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | A | A | $\overline{ADSP}$ | A | A | $V_{DDQ}$ |
| **B** | NC | A | A | $\overline{ADSC}$ | A | A | NC |
| **C** | NC | A | A | $V_{DD}$ | A | A | NC |
| **D** | DQc | DQPc | Vss | NC | Vss | DQPb | DQb |
| **E** | DQc | DQc | Vss | $\overline{CE}$ | Vss | DQb | DQb |
| **F** | $V_{DDQ}$ | DQc | Vss | $\overline{OE}$ | Vss | DQb | $V_{DDQ}$ |
| **g** | DQc | DQc | $\overline{BWc}$ | $\overline{ADV}$ | $\overline{BWb}$ | DQb | DQb |
| **H** | DQc | DQc | Vss | $\overline{GW}$ | Vss | DQb | DQb |
| **J** | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| **K** | DQd | DQd | Vss | CLK | Vss | DQa | DQa |
| **L** | DQd | DQd | $\overline{BWd}$ | NC | $\overline{BWa}$ | DQa | DQa |
| **M** | $V_{DDQ}$ | DQd | Vss | $\overline{BWE}$ | Vss | DQa | $V_{DDQ}$ |
| **N** | DQd | DQd | Vss | $A_1$* | Vss | DQa | DQa |
| **P** | DQd | DQPd | Vss | $A_0$* | Vss | DQPa | DQa |
| **R** | NC | A | MODE | $V_{DD}$ | NC | A | NC |
| **T** | NC | A | A | A | A | A | ZZ |
| **U** | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

**Note:** * $A_0$ and $A_1$ are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

## PIN DESCRIPTIONS

| Symbol | Pin Name |
|---|---|
| A | Synchronous Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| $\overline{ADV}$ | Synchronous Burst Address Advance |
| $\overline{ADSP}$ | Synchronous Address Status Processor |
| $\overline{ADSC}$ | Synchronous Address Status Controller |
| $\overline{GW}$ | Synchronous Global Write Enable |
| CLK | Synchronous Clock |
| $\overline{CE}$, CE2 | Synchronous Chip Select |
| $\overline{BWa}$-$\overline{BWd}$ | Synchronous Byte Write Controls |
| $\overline{BWE}$ | Synchronous Byte Write Enable |

| Symbol | Pin Name |
|---|---|
| $\overline{OE}$ | Asynchronous Output Enable |
| ZZ | Asynchronous Power Sleep Mode |
| MODE | Burst Sequence Selection |
| TCK, TDO<br>TMS, TDI | JTAG Pins |
| NC | No Connect |
| DQa-DQd | Synchronous Data Inputs/Outputs |
| DQPa-DQPd | Synchronous Parity Data Inputs/Outputs |
| $V_{DD}$ | Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| Vss | Ground |

## 119 BGA PACKAGE PIN CONFIGURATION

4Mx18 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | A | A | $\overline{ADSP}$ | A | A | $V_{DDQ}$ |
| **B** | NC | A | A | $\overline{ADSC}$ | A | A | NC |
| **C** | NC | A | A | $V_{DD}$ | A | A | NC |
| **D** | DQb | NC | Vss | NC | Vss | DQPa | NC |
| **E** | NC | DQb | Vss | $\overline{CE}$ | Vss | NC | DQa |
| **F** | $V_{DDQ}$ | NC | Vss | $\overline{OE}$ | Vss | DQa | $V_{DDQ}$ |
| **g** | NC | DQb | $\overline{BWb}$ | $\overline{ADV}$ | Vss | NC | DQa |
| **H** | DQb | NC | Vss | $\overline{GW}$ | Vss | DQa | NC |
| **J** | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| **K** | NC | DQb | Vss | CLK | Vss | NC | DQa |
| **L** | DQb | NC | Vss | NC | $\overline{BWa}$ | DQa | NC |
| **M** | $V_{DDQ}$ | DQb | Vss | $\overline{BWE}$ | Vss | NC | $V_{DDQ}$ |
| **N** | DQb | NC | Vss | $A_1$* | Vss | DQa | NC |
| **P** | NC | DQPb | Vss | $A_0$* | Vss | NC | DQa |
| **R** | NC | A | MODE | $V_{DD}$ | NC | A | NC |
| **T** | A | A | A | A | A | A | ZZ |
| **U** | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

**Note:** * $A_0$ and $A_1$ are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

## PIN DESCRIPTIONS

| Symbol | Pin Name |
|---|---|
| A | Synchronous Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| $\overline{ADV}$ | Synchronous Burst Address Advance |
| $\overline{ADSP}$ | Synchronous Address Status Processor |
| $\overline{ADSC}$ | Synchronous Address Status Controller |
| $\overline{GW}$ | Synchronous Global Write Enable |
| CLK | Synchronous Clock |
| $\overline{CE}$, CE2 | Synchronous Chip Select |
| $\overline{BWa}$-$\overline{BWb}$ | Synchronous Byte Write Controls |
| $\overline{BWE}$ | Synchronous Byte Write Enable |

| Symbol | Pin Name |
|---|---|
| $\overline{OE}$ | Asynchronous Output Enable |
| ZZ | Asynchronous Power Sleep Mode |
| MODE | Burst Sequence Selection |
| TCK, TDO<br>TMS, TDI | JTAG Pins |
| NC | No Connect |
| DQa-DQb | Synchronous Data Inputs/Outputs |
| DQPa-DQPb | Synchronous Parity Data Inputs/Outputs |
| $V_{DD}$ | Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| Vss | Ground |

## 165 PBGA PACKAGE PIN CONFIGURATION

2M x 36 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | NC | A | $\overline{CE}$ | $\overline{BWc}$ | $\overline{BWb}$ | $\overline{CE2}$ | $\overline{BWE}$ | $\overline{ADSC}$ | $\overline{ADV}$ | A | NC |
| **B** | NC | A | CE2 | $\overline{BWd}$ | $\overline{BWa}$ | CLK | $\overline{GW}$ | $\overline{OE}$ | $\overline{ADSP}$ | A | NC |
| **C** | DQPc | NC | $V_{DDQ}$ | Vss | Vss | Vss | Vss | Vss | $V_{DDQ}$ | NC | DQPb |
| **D** | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| **E** | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| **F** | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| **g** | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| **H** | NC | NC | NC | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | NC | NC | ZZ |
| **J** | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| **K** | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| **L** | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| **M** | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| **N** | DQPd | NC | $V_{DDQ}$ | Vss | NC | A | NC | Vss | $V_{DDQ}$ | NC | DQPa |
| **P** | NC | A | A | A | TDI | A1* | TDO | A | A | A | A |
| **R** | MODE | A | A | A | TMS | A0* | TCK | A | A | A | A |

**Note:** * $A_0$ and $A_1$ are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

## PIN DESCRIPTIONS

| Symbol | Pin Name |
|---|---|
| A | Synchronous Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
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| $\overline{ADSP}$ | Synchronous Address Status Processor |
| $\overline{ADSC}$ | Synchronous Address Status Controller |
| $\overline{GW}$ | Synchronous Global Write Enable |
| CLK | Synchronous Clock |
| $\overline{CE}$, $\overline{CE2}$, CE2 | Synchronous Chip Select |
| $\overline{BWa}$-$\overline{BWd}$ | Synchronous Byte Write Controls |

| Symbol | Pin Name |
|---|---|
| $\overline{BWE}$ | Synchronous Byte Write Enable |
| $\overline{OE}$ | Asynchronous Output Enable |
| ZZ | Asynchronous Power Sleep Mode |
| MODE | Burst Sequence Selection |
| TCK, TDO TMS, TDI | JTAG Pins |
| NC | No Connect |
| DQa-DQd | Synchronous Data Inputs/Outputs |
| DQPa-DQPd | Synchronous Parity Data Inputs/Outputs |
| $V_{DD}$ | Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| Vss | Ground |

## 165 PBGA PACKAGE PIN CONFIGURATION

4M x 18 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | NC | A | $\overline{CE}$ | $\overline{BWb}$ | NC | $\overline{CE2}$ | $\overline{BWE}$ | $\overline{ADSC}$ | $\overline{ADV}$ | A | A |
| **B** | NC | A | CE2 | NC | $\overline{BWa}$ | CLK | $\overline{GW}$ | $\overline{OE}$ | $\overline{ADSP}$ | A | NC |
| **C** | NC | NC | $V_{DDQ}$ | Vss | Vss | Vss | Vss | Vss | $V_{DDQ}$ | NC | DQPa |
| **D** | NC | DQb | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | NC | DQa |
| **E** | NC | DQb | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | NC | DQa |
| **F** | NC | DQb | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | NC | DQa |
| **g** | NC | DQb | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | NC | DQa |
| **H** | NC | NC | NC | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | NC | NC | ZZ |
| **J** | DQb | NC | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | DQa | NC |
| **K** | DQb | NC | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | DQa | NC |
| **L** | DQb | NC | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | DQa | NC |
| **M** | DQb | NC | $V_{DDQ}$ | $V_{DD}$ | Vss | Vss | Vss | $V_{DD}$ | $V_{DDQ}$ | DQa | NC |
| **N** | DQPb | NC | $V_{DDQ}$ | Vss | NC | A | NC | Vss | $V_{DDQ}$ | NC | NC |
| **P** | NC | A | A | A | TDI | $A_1$* | TDO | A | A | A | A |
| **R** | MODE | A | A | A | TMS | $A_0$* | TCK | A | A | A | A |

**Note:** * $A_0$ and $A_1$ are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

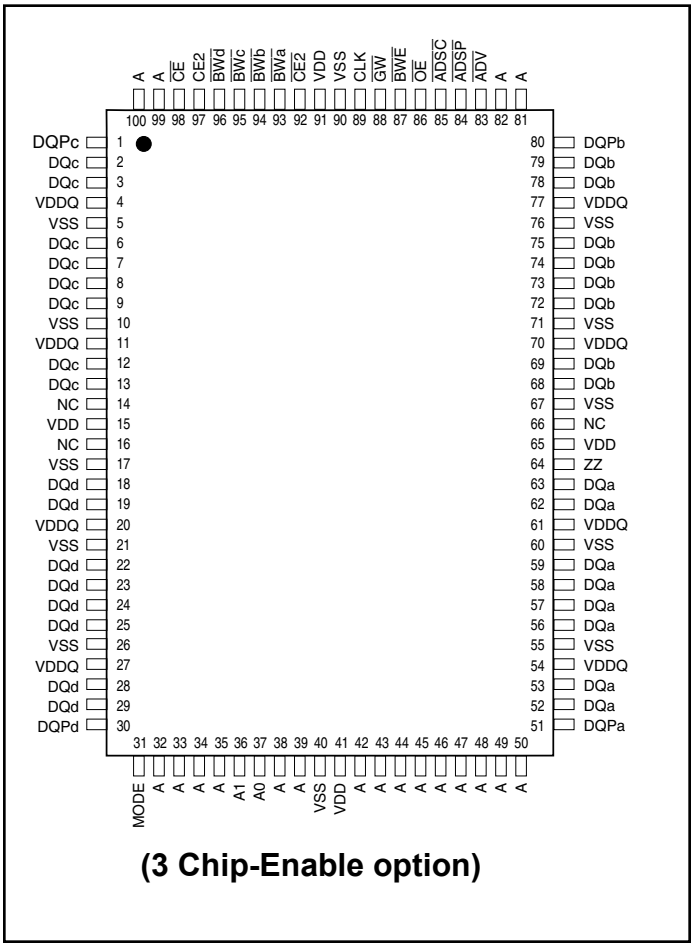
## PIN DESCRIPTIONS

| Symbol | Pin Name |
|---|---|
| A | Synchronous Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| $\overline{ADV}$ | Synchronous Burst Address Advance |
| $\overline{ADSP}$ | Synchronous Address Status Processor |
| $\overline{ADSC}$ | Synchronous Address Status Controller |
| $\overline{GW}$ | Synchronous Global Write Enable |
| CLK | Synchronous Clock |
| $\overline{CE}$, $\overline{CE2}$, CE2 | Synchronous Chip Select |
| $\overline{BWa}$-$\overline{BWb}$ | Synchronous Byte Write Controls |

| Symbol | Pin Name |
|---|---|
| $\overline{BWE}$ | Synchronous Byte Write Enable |
| $\overline{OE}$ | Asynchronous Output Enable |
| ZZ | Asynchronous Power Sleep Mode |
| MODE | Burst Sequence Selection |
| TCK, TDO TMS, TDI | JTAG Pins |
| NC | No Connect |
| DQa-DQb | Synchronous Data Inputs/Outputs |
| DQPa-DQPb | Synchronous Parity Data Inputs/Outputs |
| $V_{DD}$ | 3.3V/2.5V Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| Vss | Ground |

## PIN CONFIGURATION

### 100-PIN TQFP (2M x 36)




**(3 Chip-Enable option)**

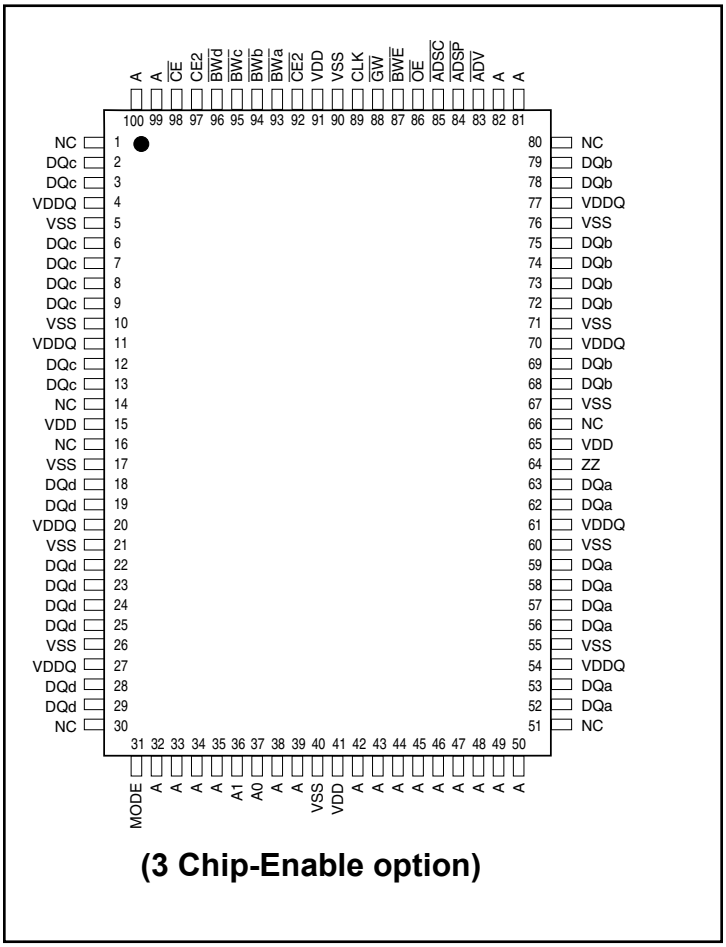
## PIN DESCRIPTIONS

| | |
|---|---|
| A0, A1 | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A | Synchronous Address Inputs |
| $\overline{ADSC}$ | Synchronous Controller Address Status |
| $\overline{ADSP}$ | Synchronous Processor Address Status |
| $\overline{ADV}$ | Synchronous Burst Address Advance |
| $\overline{BWa}$-$\overline{BWd}$ | Synchronous Byte Write Enable |
| $\overline{BWE}$ | Synchronous Byte Write Enable |
| $\overline{CE}$, $\overline{CE2}$, CE2 | Synchronous Chip Enable |
| CLK | Synchronous Clock |

| | |
|---|---|
| DQa-DQd | Synchronous Data Inputs/Outputs |
| DQPa-DQPd | Synchronous Parity Data Inputs/Outputs |
| $\overline{GW}$ | Synchronous Global Write Enable |
| MODE | Burst Sequence Mode Selection |
| $\overline{OE}$ | Asynchronous Output Enable |
| $V_{DD}$ | Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| Vss | Ground |
| ZZ | Asynchronous Snooze Enable |

## PIN CONFIGURATION

### 100-PIN TQFP (2M x 32)




**(3 Chip-Enable option)**

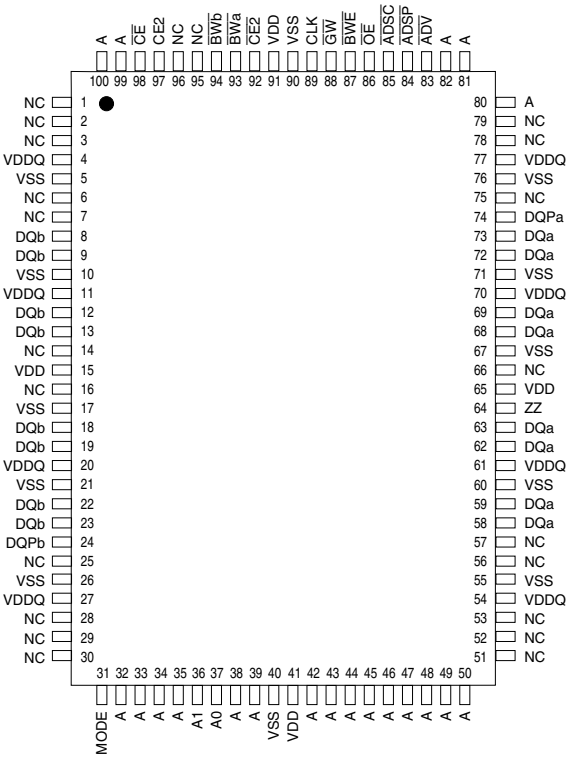
## PIN DESCRIPTIONS

| | |
|---|---|
| A0, A1 | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A | Synchronous Address Inputs |
| $\overline{ADSC}$ | Synchronous Controller Address Status |
| $\overline{ADSP}$ | Synchronous Processor Address Status |
| $\overline{ADV}$ | Synchronous Burst Address Advance |
| $\overline{BWa}$-$\overline{BWd}$ | Synchronous Byte Write Enable |
| $\overline{BWE}$ | Synchronous Byte Write Enable |
| $\overline{CE}$, $\overline{CE2}$, CE2 | Synchronous Chip Enable |
| CLK | Synchronous Clock |

| | |
|---|---|
| DQa-DQd | Synchronous Data Inputs/Outputs |
| $\overline{GW}$ | Synchronous Global Write Enable |
| MODE | Burst Sequence Mode Selection |
| $\overline{OE}$ | Asynchronous Output Enable |
| $V_{DD}$ | Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| Vss | Ground |
| ZZ | Asynchronous Snooze Enable |

## PIN CONFIGURATION

### 100-PIN TQFP (4M x 18)




### (3 Chip-Enable Option)

## PIN DESCRIPTIONS

| | |
|---|---|
| A0, A1 | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A | Synchronous Address Inputs |
| $\overline{ADSC}$ | Synchronous Controller Address Status |
| $\overline{ADSP}$ | Synchronous Processor Address Status |
| $\overline{ADV}$ | Synchronous Burst Address Advance |
| $\overline{BWa}$-$\overline{BWb}$ | Synchronous Byte Write Enable |
| $\overline{BWE}$ | Synchronous Byte Write Enable |
| $\overline{CE}$, CE2, $\overline{CE2}$ | Synchronous Chip Enable |
| CLK | Synchronous Clock |
| DQa-DQb | Synchronous Data Inputs/Outputs |

| | |
|---|---|
| DQPa-DQPb | Synchronous Parity Data Inputs/Outputs |
| $\overline{GW}$ | Synchronous Global Write Enable |
| MODE | Burst Sequence Mode Selection |
| $\overline{OE}$ | Asynchronous Output Enable |
| $V_{DD}$ | Power Supply |
| $V_{DDQ}$ | I/O Power Supply |
| Vss | Ground |
| ZZ | Asynchronous Snooze Enable |

## TRUTH TABLE[1-8]

| OPERATION | ADDRESS | $\overline{CE}$ | $\overline{CE2}$ | CE2 | ZZ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{WRITE}$ | $\overline{OE}$ | CLK | DQ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Deselect Cycle, Power-Down | None | H | X | X | L | X | L | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | X | L | L | L | X | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | H | X | L | L | X | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | X | L | L | H | L | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | H | X | L | H | L | X | X | X | L-H | High-Z |
| Snooze Mode, Power-Down | None | X | X | X | H | X | X | X | X | X | X | High-Z |
| Read Cycle, Begin Burst | External | L | L | H | L | L | X | X | X | L | L-H | Q |
| Read Cycle, Begin Burst | External | L | L | H | L | L | X | X | X | H | L-H | High-Z |
| Write Cycle, Begin Burst | External | L | L | H | L | H | L | X | L | X | L-H | D |
| Read Cycle, Begin Burst | External | L | L | H | L | H | L | X | H | L | L-H | Q |
| Read Cycle, Begin Burst | External | L | L | H | L | H | L | X | H | H | L-H | High-Z |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | L | L-H | Q |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | H | L-H | High-Z |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | L | L-H | Q |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | H | L-H | High-Z |
| Write Cycle, Continue Burst | Next | X | X | X | L | H | H | L | L | X | L-H | D |
| Write Cycle, Continue Burst | Next | H | X | X | L | X | H | L | L | X | L-H | D |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | L | L-H | Q |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | H | L-H | High-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | L | L-H | Q |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | H | L-H | High-Z |
| Write Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | L | X | L-H | D |
| Write Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | L | X | L-H | D |

**NOTE:**

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For $\overline{WRITE}$, L means one or more byte write enable signals ($\overline{BWa-d}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$ = H for all $\overline{BWx}$, $\overline{BWE}$, $\overline{GW}$ HIGH.
3. $\overline{BWa}$ enables WRITEs to DQa's and DQPa. $\overline{BWb}$ enables WRITEs to DQb's and DQPb. $\overline{BWc}$ enables WRITEs to DQc's and DQPc. $\overline{BWd}$ enables WRITEs to DQd's and DQPd. DQPa and DQPb are available on the x18 version. DQPa-DQPd are available on the x36 version.
4. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

## PARTIAL TRUTH TABLE

| Function | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BWa}$ | $\overline{BWb}$ | $\overline{BWc}$ | $\overline{BWd}$ |
|---|---|---|---|---|---|---|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write Byte 1 | H | L | L | H | H | H |
| Write All Bytes | H | L | L | L | L | L |
| Write All Bytes | L | X | X | X | X | X |

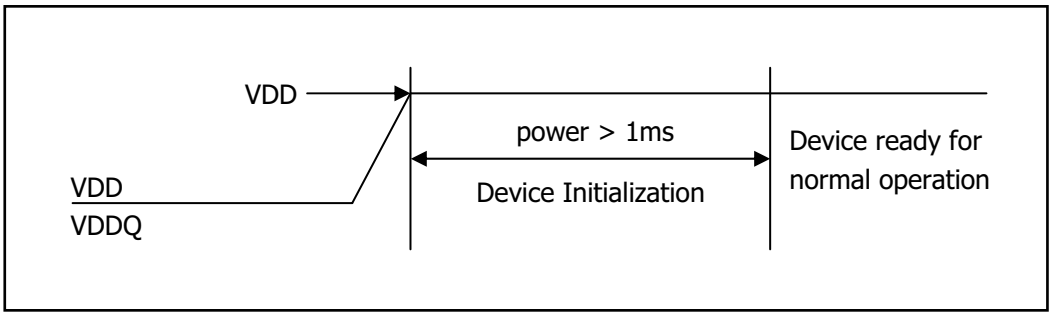
## POWER UP SEQUENCE

$V_{DDQ} \rightarrow V_{DD}$[1] $\rightarrow$ I/O Pins[2]

**Notes:**

1. $V_{DD}$ can be applied at the same time as $V_{DDQ}$
2. Applying I/O inputs is recommended after $V_{DDQ}$ is ready. The inputs of the I/O pins can be applied at the same time as $V_{DDQ}$ provided $V_{IH}$ (level of I/O pins) is lower than $V_{DDQ}$.

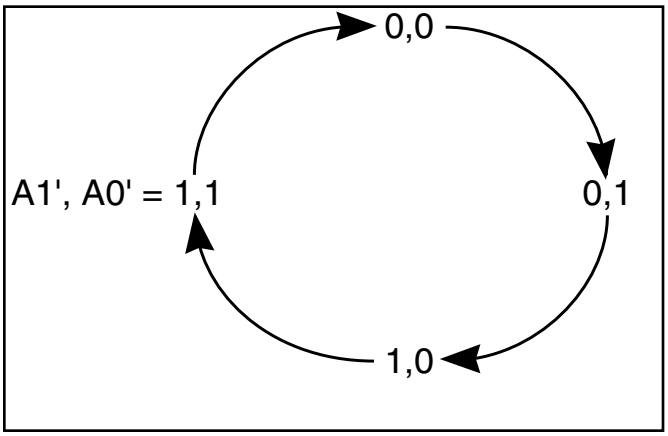
## POWER-UP INITIALIZATION TIMING




## INTERLEAVED BURST ADDRESS TABLE (MODE = $V_{DD}$ or No Connect)

| External Address A1 A0 | 1st Burst Address A1 A0 | 2nd Burst Address A1 A0 | 3rd Burst Address A1 A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

## LINEAR BURST ADDRESS TABLE (MODE = VSS)



## ABSOLUTE MAXIMUM RATINg S[1]

| Symbol | Parameter | LPS Value | VPS/VVPS Value | Unit |
|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | –55 to +150 | –55 to +150 | °C |
| $P_D$ | Power Dissipation | 1.6 | 1.6 | W |
| $I_{OUT}$ | Output Current (per I/O) | 100 | 100 | mA |
| $V_{IN}$, $V_{OUT}$ | Voltage Relative to Vss for I/O Pins | –0.5 to $V_{DDQ}$ + 0.5 | –0.5 to $V_{DDQ}$ + 0.3 | V |
| $V_{IN}$ | Voltage Relative to Vss for for Address and Control Inputs | –0.5 to $V_{DD}$ + 0.5 | –0.5 to $V_{DD}$ + 0.3 | V |
| $V_{DD}$ | Voltage on $V_{DD}$ Supply Relative to Vss | –0.5 to $V_{DDQ}$ + 0.5 | –0.3 to $V_{DDQ}$ + 0.3 | V |

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

## OPERATINg RANg E (IS61LPSXXXXX)

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |
| Industrial | –40°C to +85°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |

## OPERATINg RANg E (IS61VPSXXXXX)

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 2.5V ± 5% | 2.5V ± 5% |
| Industrial | –40°C to +85°C | 2.5V ± 5% | 2.5V ± 5% |

## OPERATINg RANg E (IS61VVPSXXXXX)

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 1.8V ± 5% | 1.8V ± 5% |
| Industrial | –40°C to +85°C | 1.8V ± 5% | 1.8V ± 5% |

## OPERATINg RANg E (IS64LPSXXXXX)

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Automotive | –40°C to +125°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range) [1, 2, 3]

| | | | 3.3V | | 2.5V | | 1.8V | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test Conditions** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Unit** |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –4.0 mA (3.3V)<br>$I_{OH}$ = –1.0 mA (2.5V, 1.8V) | 2.4 | — | 2.0 | — | $V_{DDQ}$ - 0.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 8.0 mA (3.3V)<br>$I_{OL}$ = 1.0 mA (2.5V, 1.8V) | — | 0.4 | — | 0.4 | — | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{DD}$ + 0.3 | 1.7 | $V_{DD}$ + 0.3 | 0.6$V_{DD}$ | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | -0.3 | 0.8 | -0.3 | 0.7 | -0.3 | 0.3$V_{DD}$ | V |
| $I_{LI}$ | Input Leakage Current | $V_{SS} \le V_{IN} \le V_{DD}$ [1,4] | -5 | 5 | -5 | 5 | -5 | 5 | µA |
| | Input Current of MODE | $V_{SS} \le V_{IN} \le V_{DD}$ [5] | -30 | 5 | -30 | 5 | -30 | 5 | |
| | Input Current of ZZ | $V_{SS} \le V_{IN} \le V_{DD}$ [6] | -5 | 30 | -5 | 30 | -5 | 30 | |
| $I_{LO}$ | Output Leakage Current | $V_{SS} \le V_{OUT} \le V_{DDQ}$, $\overline{OE}$ = $V_{IH}$ | -5 | 5 | -5 | 5 | -5 | 5 | µA |

**Notes:**
1. All voltages referenced to ground.
2. Overshoot:
   3.3V and 2.5V: $V_{IH}$ (AC) ≤ $V_{DD}$ + 1.5V (Pulse width less than $t_{KC}$ /2)
   1.8V: $V_{IH}$ (AC) ≤ $V_{DD}$ + 0.5V (Pulse width less than $t_{KC}$ /2)
3. Undershoot:
   3.3V and 2.5V: $V_{IL}$ (AC) ≥ -1.5V (Pulse width less than $t_{KC}$ /2)
   1.8V: $V_{IL}$ (AC) ≥ -0.5V (Pulse width less than $t_{KC}$ /2)
4. Except MODE and ZZ
5. MODE is connected to pull-up resister internally.
6. ZZ is connected to pull-down resister internally.

## POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

| | | | | -250 MAX | | -200 MAX | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test Conditions** | **Temp. range** | **x18** | **x36** | **x18** | **x36** | **Unit** |
| $I_{CC}$ | AC Operating Supply Current | Device Selected, $\overline{OE}$ = $V_{IH}$, ZZ ≤ $V_{IL}$, All Inputs ≤ 0.2V or ≥ $V_{DD}$ – 0.2V, Cycle Time ≥ $t_{KC}$ min. | Com. | 450 | 450 | 400 | 400 | mA |
| | | | Ind. | 500 | 500 | 450 | 450 | |
| | | | Auto. | - | - | 550 | 550 | |
| $I_{SB}$ | Standby Current TTL Input | Device Deselected, $V_{DD}$ = Max., All Inputs ≤ $V_{IL}$ or ≥ $V_{IH}$, ZZ ≤ $V_{IL}$, f = Max. | Com. | 200 | 200 | 200 | 200 | mA |
| | | | Ind. | 220 | 220 | 220 | 220 | |
| | | | Auto. | - | - | 350 | 350 | |
| $I_{SBI}$ | Standby Current CMOS Input | Device Deselected, $V_{DD}$ = Max., $V_{IN}$ ≤ $V_{SS}$ + 0.2V or ≥$V_{DD}$ – 0.2V f = 0 | Com. | 180 | 180 | 180 | 180 | mA |
| | | | Ind. | 200 | 200 | 200 | 200 | |
| | | | Auto. | - | - | 320 | 320 | |

## CAPACITANCE[1,2]

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{OUT}$ | Input/Output Capacitance | $V_{OUT}$ = 0V | 8 | pF |

**Notes:**
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A$ = 25°C, f = 1 MHz, $V_{DD}$ = 3.3V.

## 3.3V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Refe rence Level | 1.5V |
| Output Load | See Figures 1 and 2 |

## AC TEST LOADS

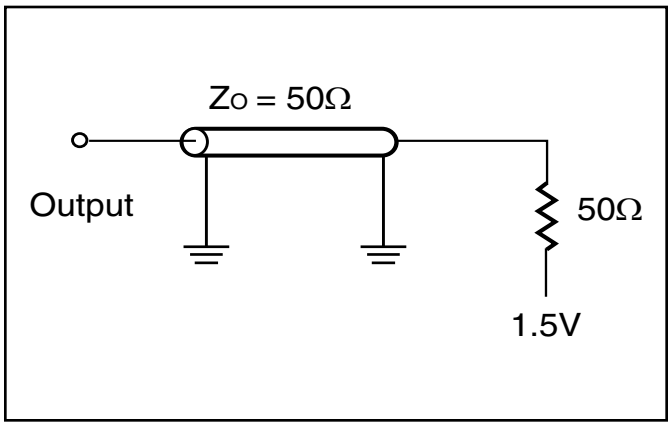



**Figure 1**

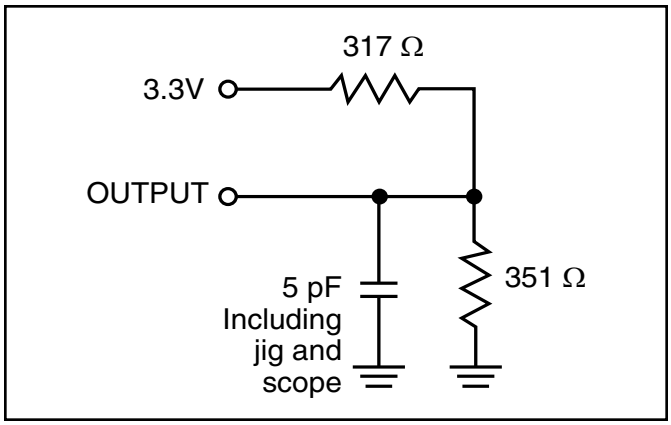



**Figure 2**

## 2.5V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---|
| Input Pulse Level | 0V to 2.5V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.25V |
| Output Load | See Figures 3 and 4 |

## 2.5 I/O OUTPUT LOAD EQUIVALENT

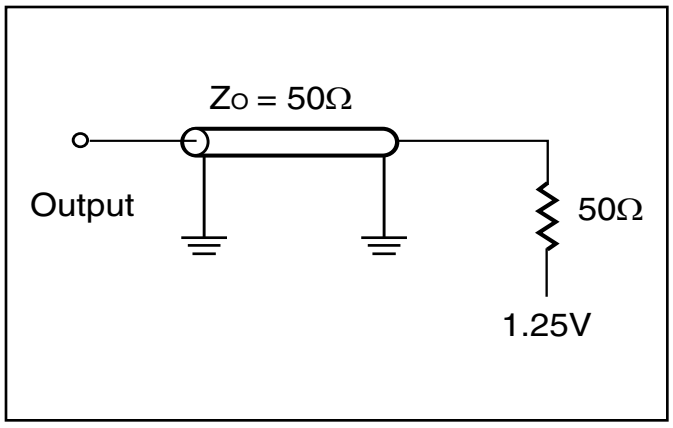



Figure 3

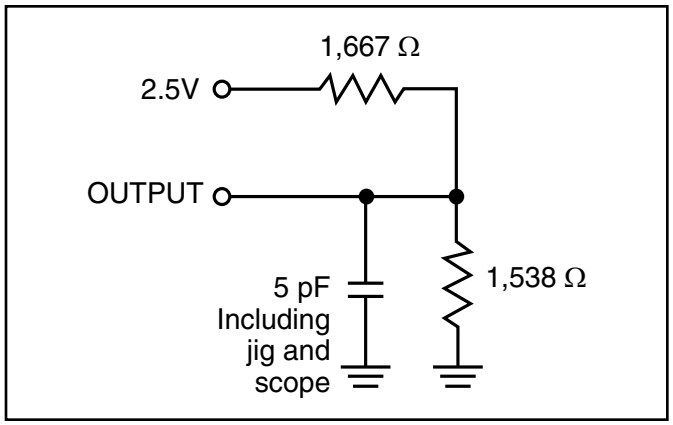



Figure 4

## 1.8V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---|
| Input Pulse Level | 0V to 1.8V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 0.9V |
| Output Load | See Figures 5 and 6 |

## 1.8 I/O OUTPUT LOAD EQUIVALENT

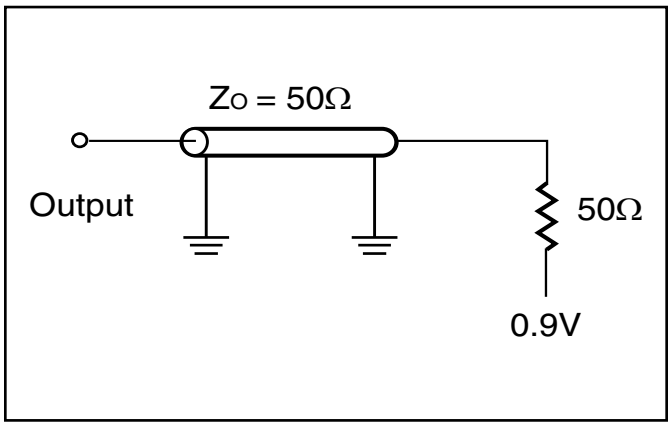



Figure 5

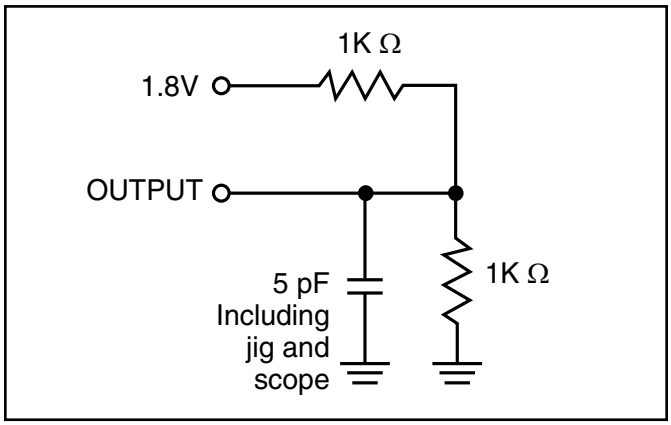


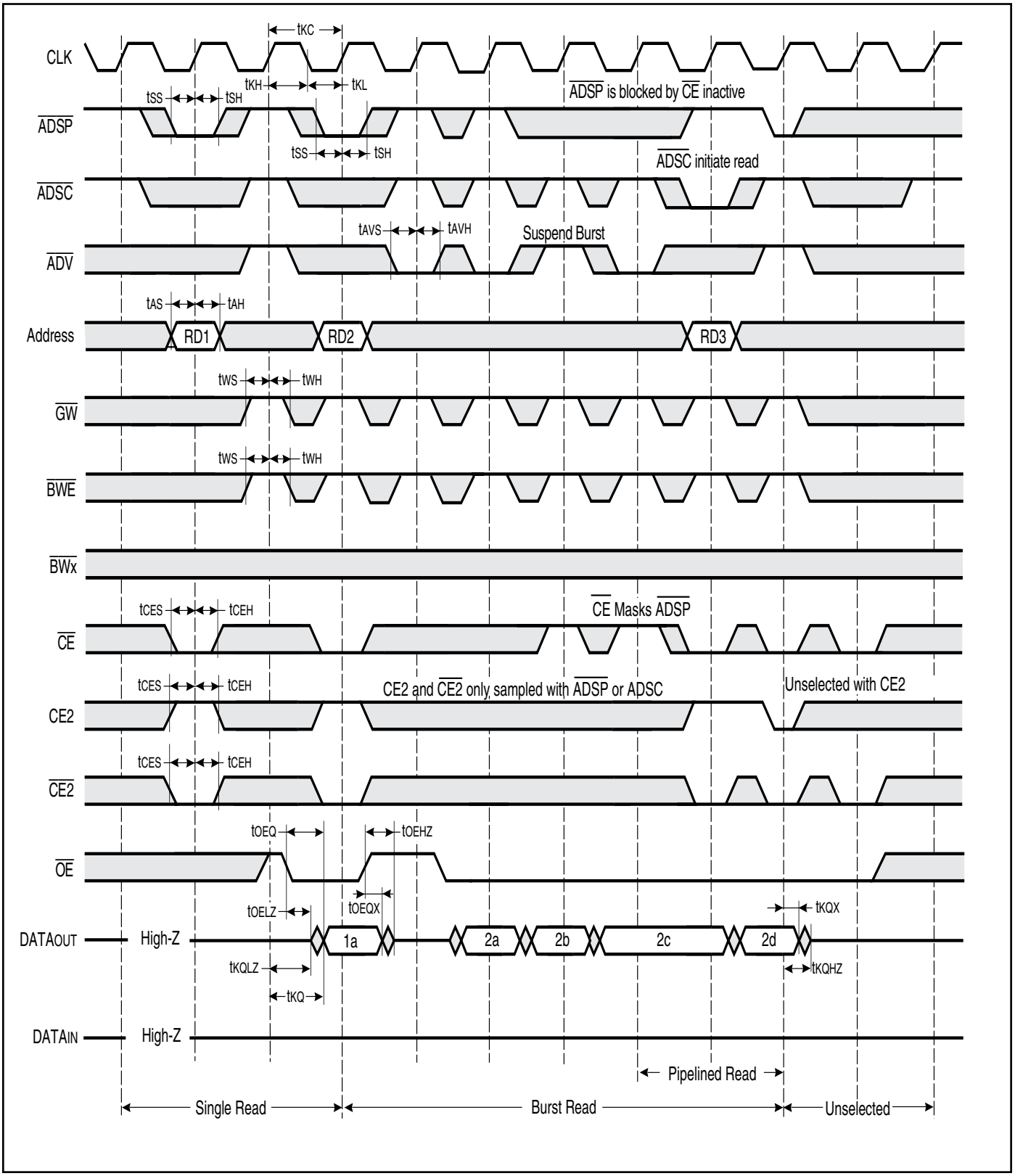

Figure 6

## READ/wRITE CYCLE SwITCHINg CHARACTERISTICS (Over Operating Range)

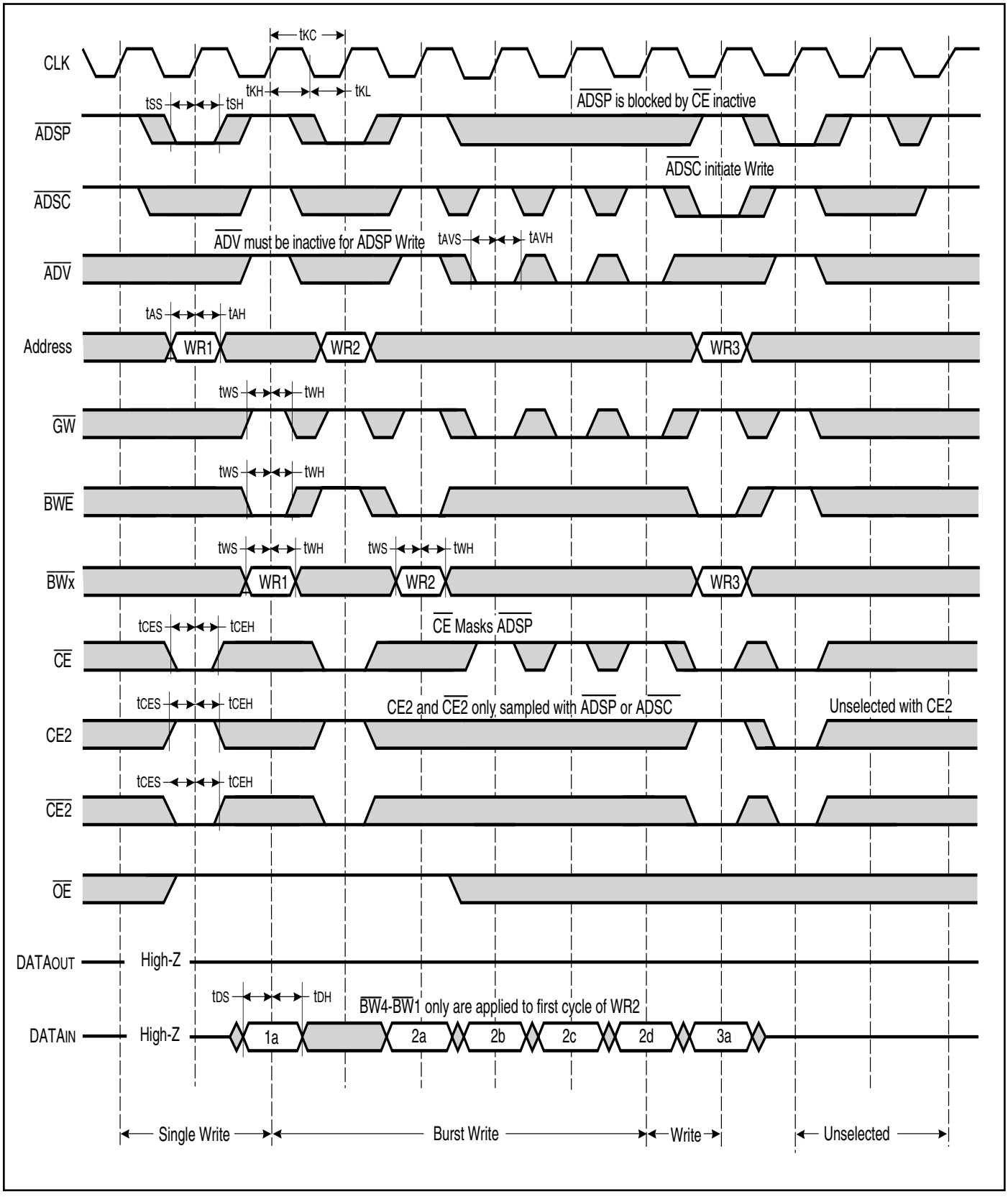
| | | -250 | | -200 | | -166 | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Unit** |
| $f_{MAX}$ | Clock Frequency | — | 250 | — | 200 | — | 166 | MHz |
| $t_{KC}$ | Cycle Time | 4.0 | — | 5 | — | 6 | — | ns |
| $t_{KH}$ | Clock High Time | 1.7 | — | 2 | — | 2.4 | — | ns |
| $t_{KL}$ | Clock Low Time | 1.7 | — | 2 | — | 2.3 | — | ns |
| $t_{KQ}$ | Clock Access Time | — | 2.8 | — | 3.1 | — | 3.8 | ns |
| $t_{KQX}$(2) | Clock High to Output Invalid | 0.8 | — | 1.5 | — | 1.5 | — | ns |
| $t_{KQLZ}$(2,3) | Clock High to Output Low-Z | 0.8 | — | 1 | — | 1.5 | — | ns |
| $t_{KQHZ}$(2,3) | Clock High to Output High-Z | — | 2.8 | — | 3.1 | 3.8 | — | ns |
| $t_{OEQ}$ | Output Enable to Output Valid | — | 2.8 | — | 3.1 | 3.8 | — | ns |
| $t_{OELZ}$(2,3) | Output Enable to Output Low-Z | 0 | — | 0 | — | 0 | — | ns |
| $t_{OEHZ}$(2,3) | Output Disable to Output High-Z | — | 2.8 | — | 3.1 | 3.8 | — | ns |
| $t_{AS}$ | Address Setup Time | 1.4 | — | 1.4 | — | 1.5 | — | ns |
| $t_{WS}$ | Read/Write Setup Time | 1.4 | — | 1.4 | — | 1.5 | — | ns |
| $t_{CES}$ | Chip Enable Setup Time | 1.4 | — | 1.4 | — | 1.5 | — | ns |
| $t_{AVS}$ | Address Advance Setup Time | 1.4 | — | 1.4 | — | 1.5 | — | ns |
| $t_{DS}$ | Data Setup Time | 1.4 | — | 1.4 | — | 1.5 | — | ns |
| $t_{AH}$ | Address Hold Time | 0.4 | — | 0.4 | — | 0.5 | — | ns |
| $t_{WH}$ | Write Hold Time | 0.4 | — | 0.4 | — | 0.5 | — | ns |
| $t_{CEH}$ | Chip Enable Hold Time | 0.4 | — | 0.4 | — | 0.5 | — | ns |
| $t_{AVH}$ | Address Advance Hold Time | 0.4 | — | 0.4 | — | 0.5 | — | ns |
| $t_{DH}$ | Data Hold Time | 0.4 | — | 0.4 | — | 0.5 | — | ns |
| $t_{POWER}$(4) | $V_{DD}$ (typical) to First Access | 1 | — | 1 | — | 1 | — | ms |

**Note:**
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.
4. $t_{POWER}$ is the time that the power needs to be supplied above $V_{DD}$ (min) initially before READ or WRITE operation can be initiated.

## READ/w RITE CYCLE TIMINg



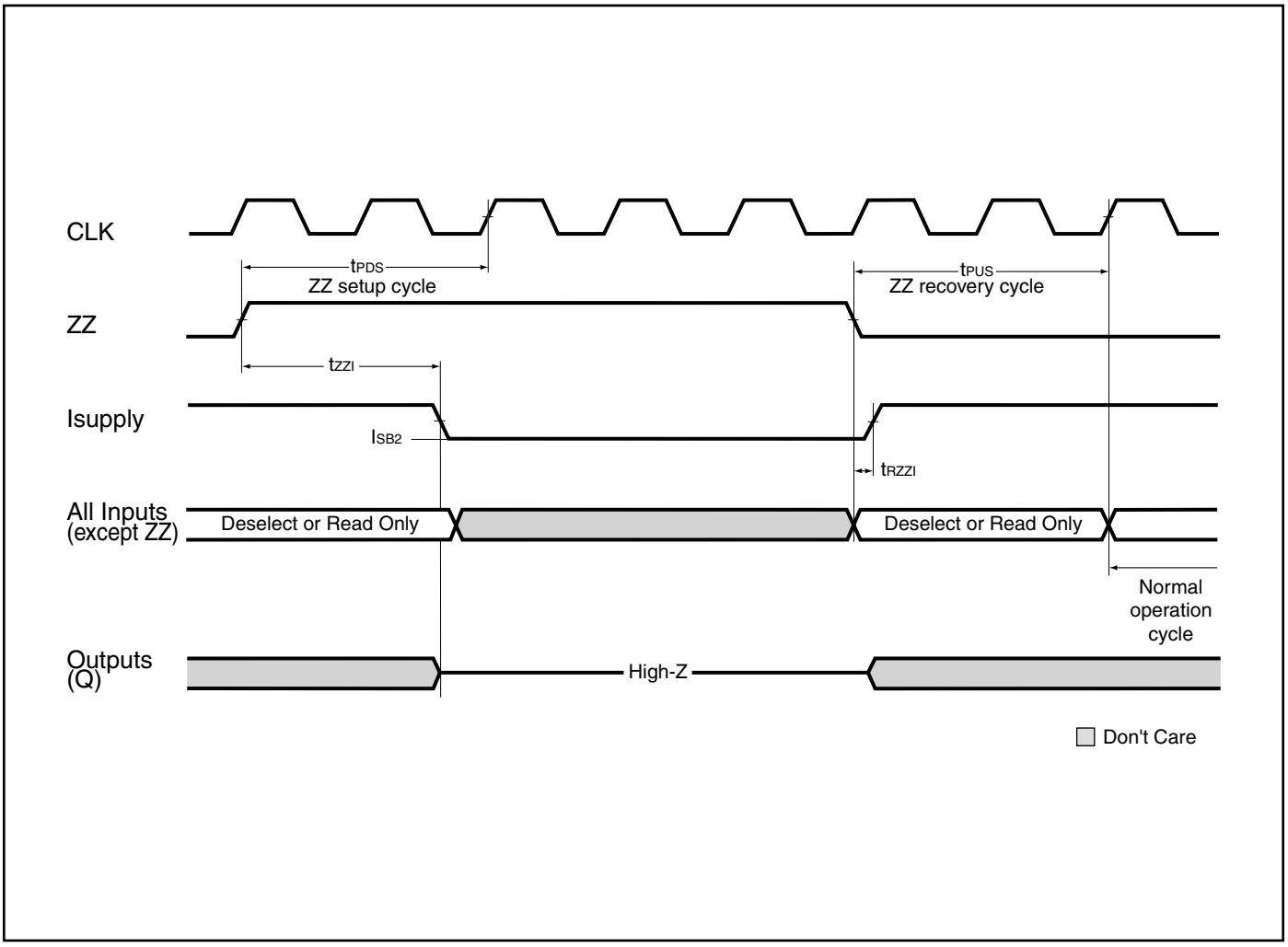
## w RITE CYCLE TIMINg



## SNOOZE MODE ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Temperature Range | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SB2}$ | Current during SNOOZE MODE | ZZ ≥ $V_{DD}$ - 0.2V | Com. | — | 120 | mA |
| | | | Ind. | — | 130 | |
| | | | Auto. | — | 250 | |
| $t_{PDS}$ | ZZ active to input ignored | | | — | 2 | cycle |
| $t_{PUS}$ | ZZ inactive to input sampled | | | 2 | — | cycle |
| $t_{ZZI}$ | ZZ active to SNOOZE current | | | — | 2 | cycle |
| $t_{RZZI}$ | ZZ inactive to exit SNOOZE current | | | 0 | — | ns |

## SNOOZE MODE TIMINg



## IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAg )

The serial boundary scan Test Access Port (TAP) is only available in the PBGA package. (The TQFP package not available.) This port operates in accordance with IEEE Standard 1149.1-1900, but does not include all functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because they place added delay in the critical speed path of the SRAM. The TAP controller operates in a manner that does not conflict with the performance of other devices using 1149.1 fully compliant TAPs.

## DISABLINg THE JTAg FEATURE

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (Vss) to prevent clocking of the device. TDI and TMS are internally pulled up and may be disconnected. They may alternately be connected to $V_{DD}$ through a pull-up resistor. TDO should be left disconnected. On power-up, the device will start in a reset state which will not interfere with the device operation.

## TEST ACCESS PORT (TAP) - TEST CLOCK

The test clock is only used with the TAP controller. All inputs are captured on the rising edge of TCK and outputs are driven from the falling edge of TCK.

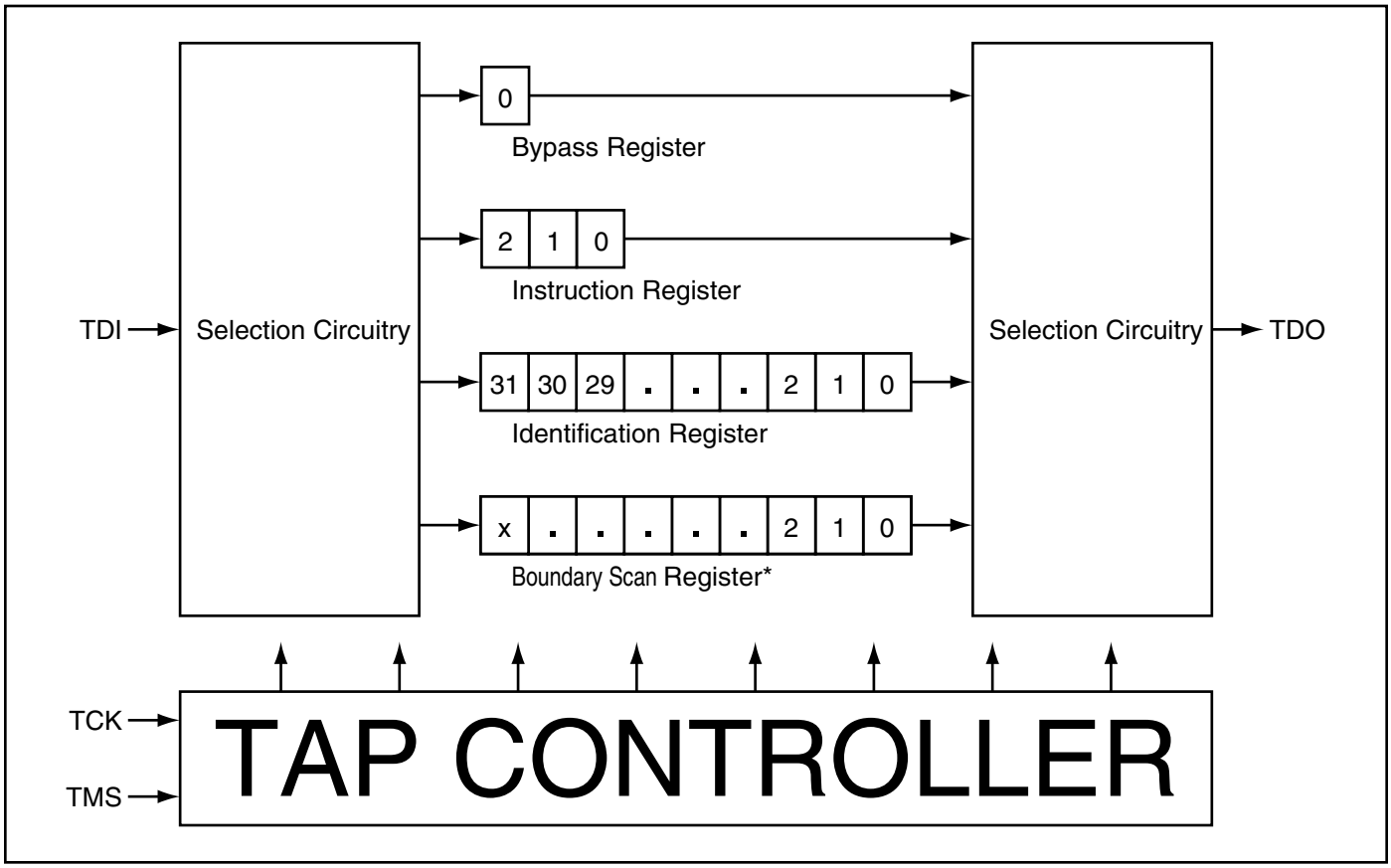
## TEST MODE SELECT (TMS)

The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left disconnected if the TAP is not used. The pin is internally pulled up, resulting in a logic HIGH level.

## TEST DATA-IN (TDI)

The TDI pin is used to serially input information to the registers and can be connected to the input of any register. The register between TDI and TDO is chosen by the instruction loaded into the TAP instruction register. For information on instruction register loading, see the TAP Controller State Diagram. TDI is internally pulled up and can be disconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

## TAP CONTROLLER BLOCK DIAg RAM



## TEST DATA OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending on the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK and TDO is connected to the Least Significant Bit (LSB) of any register.

## PERFORMINg A TAP RESET

A Reset is performed by forcing TMS HIGH ($V_{DD}$) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

## TAP REg ISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry**.** Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

### Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins. (See TAP Controller Block Diagram) At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as previously described.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

### Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ($V_{SS}$) when the BYPASS instruction is executed.

### Boundary Scan Register

The boundary scan register is connected to all input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a 75-bit-long register and the x18 configuration also has a 75-bit-long register. The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE-Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

### Scan Register Sizes

| Register Name | Bit Size (x18) | Bit Size (x36) |
|---|---|---|
| Instruction | 3 | 3 |
| Bypass | 1 | 1 |
| ID | 32 | 32 |
| Boundary Scan | 90 | 90 |

### Identification (ID) Registe

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded to the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has vendor code and other information described in the Identification Register Definitions table.

## IDENTIFICATION REg ISTER DEFINITIONS

| Instruction Field | Description | 2M x 36 | 4M x 18 |
|---|---|---|---|
| Revision Number (31:28) | Reserved for version number. | xxxx | xxxx |
| Device Depth (27:23) | Defines depth of SRAM. 2M or 4M | 01010 | 01011 |
| Device Width (22:18) | Defines width of the SRAM. x36 or x18 | 00100 | 00011 |
| ISSI Device ID (17:12) | Reserved for future use. | xxxxx | xxxxx |
| ISSI JEDEC ID (11:1) | Allows unique identification of SRAM vendor. | 00001010101 | 00001010101 |
| ID Register Presence (0) | Indicate the presence of an ID register. | 1 | 1 |

## TAP INSTRUCTION SET

Eight instructions are possible with the three-bit instruction register and all combinations are listed in the Instruction Code table. Three instructions are listed as RESERVED and should not be used and the other five instructions are described below. The TAP controller used in this SRAM is not fully compliant with the 1149.1 convention because some mandatory instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; instead it performs a capture of the Inputs and Output ring when these instructions are executed. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

## EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. Because EXTEST is not implemented in the TAP controller, this device is not 1149.1 standard compliant. The TAP controller recognizes an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is a difference between the instructions, unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

## IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

## SAMPLE-Z

The SAMPLE-Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

## SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant. When the SAMPLE/PRELOAD instruction is loaded to the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

It is important to realize that the TAP controller clock operates at a frequency up to 10 MHz, while the SRAM clock runs more than an order of magnitude faster. Because of the clock frequency differences, it is possible that during the Capture-DR state, an input or output will under-go a transition. The TAP may attempt a signal capture while in transition (metastable state). The device will not be harmed, but there is no guarantee of the value that will be captured or repeatable results.

To guarantee that the boundary scan register will capture the correct signal value, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times ($t_{CS}$ and $t_{CH}$). To insure that the SRAM clock input is captured correctly, designs need a way to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is not an issue, it is possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

## BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

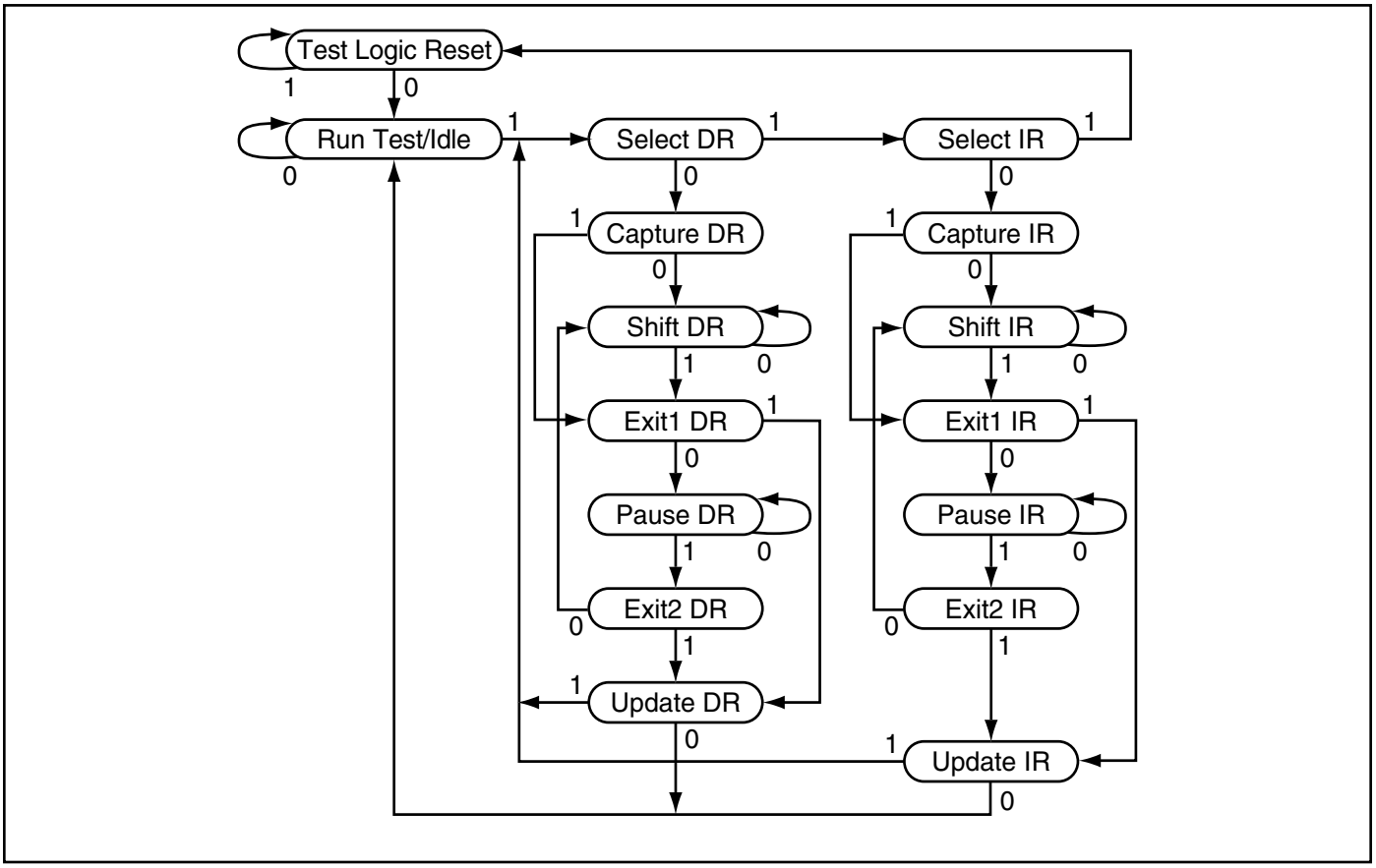
## RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.

## INSTRUCTION CODES

| Code | Instruction | Description |
|---|---|---|
| 000 | EXTEST | Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1 compliant. |
| 001 | IDCODE | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation. |
| 010 | SAMPLE-Z | Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state. |
| 011 | RESERVED | Do Not Use: This instruction is reserved for future use. |
| 100 | SAMPLE/PRELOAD | Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant. |
| 101 | RESERVED | Do Not Use: This instruction is reserved for future use. |
| 110 | RESERVED | Do Not Use: This instruction is reserved for future use. |
| 111 | BYPASS | Places the bypass register between TDI and TDO. This operation does not affect SRAM operation. |

## TAP CONTROLLER STATE DIAg RAM



## TAP Electrical Characteristics ($V_{DDQ}$ = 3.3V Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{OH1}$ | Output HIGH Voltage | $I_{OH}$ = -4 mA | 2.4 | — | V |
| $V_{OH2}$ | Output HIGH Voltage | $I_{OH}$ = -100 µA | 2.9 | — | V |
| $V_{OL1}$ | Output LOW Voltage | $I_{OL}$ = 8 mA | — | 0.4 | V |
| $V_{OL2}$ | Output LOW Voltage | $I_{OL}$ = 100 µA | — | 0.2 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | –0.3 | 0.8 | V |
| $I_X$ | Input Load Current | $V_{SS} \le V_{IN} \le V_{DDQ}$ | –30 | 30 | µA |

## TAP Electrical Characteristics ($V_{DDQ}$ = 2.5V Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{OH1}$ | Output HIGH Voltage | $I_{OH}$ = -1 mA | 2.0 | — | V |
| $V_{OH2}$ | Output HIGH Voltage | $I_{OH}$ = -100 µA | 2.1 | — | V |
| $V_{OL1}$ | Output LOW Voltage | $I_{OL}$ = 1 mA | — | 0.4 | V |
| $V_{OL2}$ | Output LOW Voltage | $I_{OL}$ = 100 µA | — | 0.2 | V |
| $V_{IH}$ | Input HIGH Voltage | | 1.7 | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | -0.3 | 0.7 | V |
| $I_X$ | Input Load Current | $V_{SS} \le V_{IN} \le V_{DDQ}$ | –30 | 30 | µA |

## TAP Electrical Characteristics ($V_{DDQ}$ = 1.8V Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{OH1}$ | Output HIGH Voltage | $I_{OH}$ = -1 mA | $V_{DD}$ -0.4 | — | V |
| $V_{OL1}$ | Output LOW Voltage | $I_{OL}$ = 1 mA | — | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | | 1.3 | $V_{DD}$ +0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | -0.3 | 0.7 | V |
| $I_X$ | Input Load Current | $V_{SS} \le V\ I \le V_{DDQ}$ | -30 | 30 | µA |

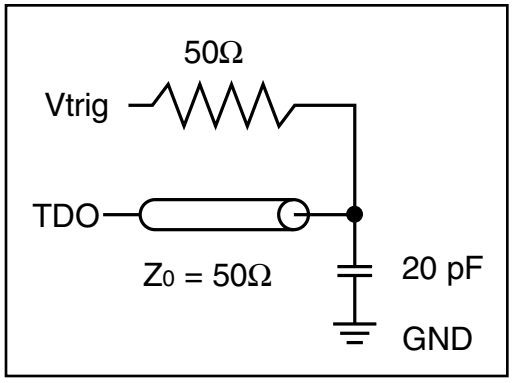
## TAP AC ELECTRICAL CHARACTERISTICS (OVER OPERATING RANGE)

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| TCK cycle time | $t_{THTH}$ | 100 | – | ns |
| TCK high pulse width | $t_{THTL}$ | 40 | – | ns |
| TCK low pulse width | $t_{TLTH}$ | 40 | – | ns |
| TMS Setup | $t_{MVTH}$ | 10 | – | ns |
| TMS Hold | $t_{THMX}$ | 10 | – | ns |
| TDI Setup | $t_{DVTH}$ | 10 | – | ns |
| TDI Hold | $t_{THDX}$ | 10 | – | ns |
| TCK Low to Valid Data | $t_{TLOV}$ | – | 20 | ns |

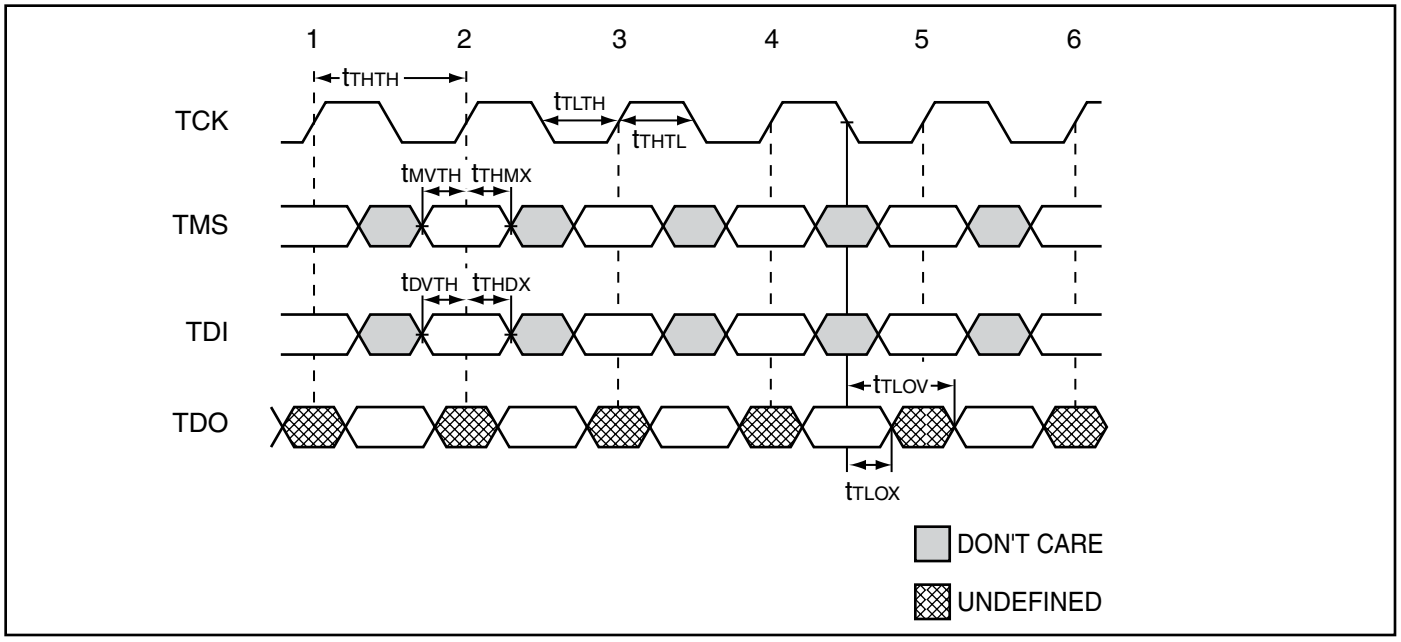
## TAP AC TEST CONDITIONS (1.8V/2.5V/3.3V)

| | |
|---|---|
| Input pulse levels | 0 to 1.8V/0 to 2.5V/0 to 3.0V |
| Input rise and fall times | 1.5ns |
| Input timing reference levels | 0.9V/1.25V/1.5V |
| Output reference levels | 0.9V/1.25V/1.5V |
| Test load termination supply voltage | 0.9V/1.25V/1.5V |
| Vtrig | 0.9V/1.25V/1.5V |

### TAP Output Load Equivalent




### TAP TIMING



## BOUNDARY SCAN ORDER

| 165 BgA | | | | | 119 BgA | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | X36 | | X18 | | | X36 | | X18 | |
| Bit # | Bump ID | Signal | Bump ID | Signal | Bit # | Bump ID | Signal | Bump ID | Signal |
| 1 | N6 | A9 | N6 | A9 | 1 | C7 | NC | C7 | NC |
| 2 | N7 | NC | N7 | NC | 2 | R5 | NC | R5 | NC |
| 3 | N10 | NC | N10 | NC | 3 | R7 | NC | R7 | NC |
| 4 | P11 | A8 | P11 | A8 | 4 | U6 | NC | U6 | NC |
| 5 | P8 | A18 | P8 | A18 | 5 | B5 | A18 | B5 | A18 |
| 6 | R8 | A17 | R8 | A17 | 6 | C6 | A17 | C6 | A17 |
| 7 | R9 | A16 | R9 | A16 | 7 | T3 | A16 | T3 | A16 |
| 8 | P9 | A15 | P9 | A15 | 8 | T4 | A15 | T4 | A15 |
| 9 | P10 | A14 | P10 | A14 | 9 | T5 | A14 | T5 | A14 |
| 10 | R10 | A13 | R10 | A13 | 10 | T6 | A13 | T6 | A13 |
| 11 | R11 | A12 | R11 | A12 | 11 | R6 | A12 | R6 | A12 |
| 12 | H11 | ZZ | H11 | ZZ | 12 | T7 | ZZ | T7 | ZZ |
| 13 | N11 | DQa0 | N11 | NC | 13 | P6 | DQa0 | P6 | NC |
| 14 | M11 | DQa1 | M11 | NC | 14 | N7 | DQa1 | N7 | NC |
| 15 | L11 | DQa2 | L11 | NC | 15 | M6 | DQa2 | M6 | NC |
| 16 | K11 | DQa6 | K11 | NC | 16 | L7 | DQa6 | L7 | NC |
| 17 | J11 | DQa7 | J11 | NC | 17 | K6 | DQa7 | K6 | NC |
| 18 | M10 | DQa3 | M10 | DQa8 | 18 | P7 | DQa3 | P7 | DQa8 |
| 19 | L10 | DQa4 | L10 | DQa7 | 19 | N6 | DQa4 | N6 | DQa7 |
| 20 | K10 | DQa5 | K10 | DQa6 | 20 | L6 | DQa5 | L6 | DQa6 |
| 21 | J10 | DQa8 | J10 | DQa5 | 21 | K7 | DQa8 | K7 | DQa5 |
| 22 | H9 | NC | H9 | NC | 22 | - | NC | - | NC |
| 23 | H10 | NC | H10 | NC | 23 | - | NC | - | NC |
| 24 | G11 | DQb8 | G11 | DQa4 | 24 | H6 | DQb8 | H6 | DQa4 |
| 25 | F11 | DQb7 | F11 | DQa3 | 25 | G7 | DQb7 | G7 | DQa3 |
| 26 | E11 | DQb5 | E11 | DQa2 | 26 | F6 | DQb5 | F6 | DQa2 |
| 27 | D11 | DQb4 | D11 | DQa1 | 27 | E7 | DQb4 | E7 | DQa1 |
| 28 | G10 | DQb6 | G10 | NC | 28 | H7 | DQb6 | H7 | NC |
| 29 | F10 | DQb3 | F10 | NC | 29 | G6 | DQb3 | G6 | NC |
| 30 | E10 | DQb2 | E10 | NC | 30 | E6 | DQb2 | E6 | NC |
| 31 | D10 | DQb1 | D10 | NC | 31 | D7 | DQb1 | D7 | NC |
| 32 | C11 | DQb0 | C11 | DQa0 | 32 | D6 | DQb0 | D6 | DQa0 |
| 33 | A11 | NC | A11 | A21 | 33 | T1 | NC | T1 | A21 |
| 34 | B11 | NC | B11 | NC | 34 | R1 | NC | R1 | NC |
| 35 | A10 | A11 | A10 | A11 | 35 | A6 | A11 | A6 | A11 |
| 36 | B10 | A10 | B10 | A10 | 36 | A5 | A10 | A5 | A10 |
| 37 | A9 | /ADV | A9 | /ADV | 37 | G4 | /ADV | G4 | /ADV |
| 38 | B9 | /ADSP | B9 | /ADSP | 38 | A4 | /ADSP | A4 | /ADSP |
| 39 | C10 | NC | C10 | NC | 39 | B7 | NC | B7 | NC |
| 40 | A8 | /ADSC | A8 | /ADSC | 40 | B4 | /ADSC | B4 | /ADSC |
| 41 | B8 | /OE | B8 | /OE | 41 | F4 | /OE | F4 | /OE |
| 42 | A7 | /BWE | A7 | /BWE | 42 | M4 | /BWE | M4 | /BWE |
| 43 | B7 | /GW | B7 | /GW | 43 | H4 | /GW | H4 | /GW |
| 44 | B6 | CLK | B6 | CLK | 44 | K4 | CLK | K4 | CLK |

NOT RECOMMENDED FOR NEW DESIGN

| 165 BgA | | | | | 119 BgA | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | X36 | | X18 | | | X36 | | X18 | |
| Bit # | Bump ID | Signal | Bump ID | Signal | Bit # | Bump ID | Signal | Bump ID | Signal |
| 45 | A6 | /CE2 | A6 | /CE2 | 45 | B6 | A9 | B6 | A9 |
| 46 | B5 | /Bwa | B5 | /Bwa | 46 | L5 | /Bwa | L5 | /Bwa |
| 47 | A5 | /Bwb | A5 | NC | 47 | G5 | /Bwb | G5 | NC |
| 48 | A4 | /Bwc | A4 | /Bwb | 48 | G3 | /Bwc | G3 | /Bwb |
| 49 | B4 | /Bwd | B4 | NC | 49 | L3 | /Bwd | L3 | NC |
| 50 | B3 | CE2 | B3 | CE2 | 50 | B2 | A8 | B2 | A8 |
| 51 | A3 | /CE1 | A3 | /CE1 | 51 | E4 | /CE1 | E4 | /CE1 |
| 52 | A2 | A7 | A2 | A7 | 52 | A3 | A7 | A3 | A7 |
| 53 | B2 | A6 | B2 | A6 | 53 | A2 | A6 | A2 | A6 |
| 54 | C2 | NC | C2 | NC | 54 | B1 | NC | B1 | NC |
| 55 | B1 | NC | B1 | NC | 55 | C1 | NC | C1 | NC |
| 56 | A1 | NC | A1 | NC | 56 | D4 | NC | D4 | NC |
| 57 | C1 | DQc0 | C1 | NC | 57 | D2 | DQc0 | D2 | NC |
| 58 | D1 | DQc1 | D1 | NC | 58 | E1 | DQc1 | E1 | NC |
| 59 | E1 | DQc2 | E1 | NC | 59 | F2 | DQc2 | F2 | NC |
| 60 | F1 | DQc6 | F1 | NC | 60 | G1 | DQc6 | G1 | NC |
| 61 | G1 | DQc7 | G1 | NC | 61 | H2 | DQc7 | H2 | NC |
| 62 | D2 | DQc3 | D2 | DQb8 | 62 | D1 | DQc3 | D1 | DQb8 |
| 63 | E2 | DQc4 | E2 | DQb7 | 63 | E2 | DQc4 | E2 | DQb7 |
| 64 | F2 | DQc5 | F2 | DQb6 | 64 | G2 | DQc5 | G2 | DQb6 |
| 65 | G2 | DQc8 | G2 | DQb5 | 65 | H1 | DQc8 | H1 | DQb5 |
| 66 | H1 | NC | H1 | NC | 66 | - | NC | - | NC |
| 67 | H2 | NC | H2 | NC | 67 | - | NC | - | NC |
| 68 | H3 | NC | H3 | NC | 68 | - | NC | - | NC |
| 69 | J1 | DQd8 | J1 | DQb4 | 69 | K2 | DQd8 | K2 | DQb4 |
| 70 | K1 | DQd7 | K1 | DQb3 | 70 | L1 | DQd7 | L1 | DQb3 |
| 71 | L1 | DQd5 | L1 | DQb2 | 71 | M2 | DQd5 | M2 | DQb2 |
| 72 | M1 | DQd4 | M1 | DQb1 | 72 | N1 | DQd4 | N1 | DQb1 |
| 73 | J2 | DQd6 | J2 | NC | 73 | K1 | DQd6 | K1 | NC |
| 74 | K2 | DQd3 | K2 | NC | 74 | L2 | DQd3 | L2 | NC |
| 75 | L2 | DQd2 | L2 | NC | 75 | N2 | DQd2 | N2 | NC |
| 76 | M2 | DQd1 | M2 | NC | 76 | P1 | DQd1 | P1 | NC |
| 77 | N1 | DQd0 | N1 | DQb0 | 77 | P2 | DQd0 | P2 | DQb0 |
| 78 | N2 | NC | N2 | NC | 78 | L4 | NC | L4 | NC |
| 79 | P1 | NC | P1 | NC | 79 | J5 | NC | J5 | NC |
| 80 | R1 | MODE | R1 | MODE | 80 | R3 | MODE | R3 | MODE |
| 81 | R2 | A4 | R2 | A4 | 81 | C2 | A4 | C2 | A4 |
| 82 | P3 | A3 | P3 | A3 | 82 | B3 | A3 | B3 | A3 |
| 83 | R3 | A2 | R3 | A2 | 83 | C3 | A2 | C3 | A2 |
| 84 | P2 | A5 | P2 | A5 | 84 | R2 | A5 | R2 | A5 |
| 85 | R4 | A19 | R4 | A19 | 85 | C5 | A19 | C5 | A19 |
| 86 | P4 | A20 | P4 | A20 | 86 | T2 | A20 | T2 | A20 |
| 87 | N5 | NC | N5 | NC | 87 | J3 | NC | J3 | NC |
| 88 | P6 | A1 | P6 | A1 | 88 | N4 | A1 | N4 | A1 |
| 89 | R6 | A0 | R6 | A0 | 89 | P4 | A0 | P4 | A0 |
| 90 | * | Int | * | Int | 90 | * | Int | * | Int |

PRELIMINARY NOT RECOMMENDED FOR NEW DESIGN

## ORDERINg INFORMATION

**Commercial Range: 0°C to 70°C(vDD = 3.3v / vDDQ = 2.5v/3.3v)**

| Speed | x32 | Package |
|---|---|---|
| 200MHz | IS61LPS204832B-200TQ | 100 TQFP, 3CE |
| | IS61LPS204832B-200TQL | 100 TQFP, 3CE, Lead-free |
| | IS61LPS204832B-200TQ2 | 100 TQFP, 2CE |
| | IS61LPS204832B-200TQ2L | 100 TQFP, 2CE, Lead-free |

| Speed | x36 | x18 | Package |
|---|---|---|---|
| 250MHz | IS61LPS204836B-250TQ | IS61LPS409618B-250TQ | 100 TQFP, 3CE |
| | IS61LPS204836B-250TQ2 | IS61LPS409618B-250TQ2 | 100 TQFP, 2CE |
| | IS61LPS204836B-250B3 | IS61LPS409618B-250B3 | 165 PBGA,13x15mm |
| | IS61LPS204836B-250M3 | IS61LPS409618B-250M3 | 165 PBGA,15x17mm |
| | IS61LPS204836B-250B2 | IS61LPS409618B-250B2 | 119 PBGA |
| | IS61LPS204836B-250TQL | IS61LPS409618B-250TQL | 100 TQFP, 3CE, Lead-free |
| | IS61LPS204836B-250TQ2L | IS61LPS409618B-250TQ2L | 100 TQFP, 2CE, Lead-free |
| | IS61LPS204836B-250B3L | IS61LPS409618B-250B3L | 165 PBGA,13x15mm, Lead-free |
| | IS61LPS204836B-250M3L | IS61LPS409618B-250M3L | 165 PBGA,15x17mm, Lead-free |
| | IS61LPS204836B-250B2L | IS61LPS409618B-250B2L | 119 PBGA, Lead-free |
| 200MHz | IS61LPS204836B-200TQ | IS61LPS409618B-200TQ | 100 TQFP, 3CE |
| | IS61LPS204836B-200TQ2 | IS61LPS409618B-200TQ2 | 100 TQFP, 2CE |
| | IS61LPS204836B-200B3 | IS61LPS409618B-200B3 | 165 PBGA,13x15mm |
| | IS61LPS204836B-200M3 | IS61LPS409618B-200M3 | 165 PBGA,15x17mm |
| | IS61LPS204836B-200B2 | IS61LPS409618B-200B2 | 119 PBGA |
| | IS61LPS204836B-200TQL | IS61LPS409618B-200TQL | 100 TQFP, 3CE, Lead-free |
| | IS61LPS204836B-200TQ2L | IS61LPS409618B-200TQ2L | 100 TQFP, 2CE, Lead-free |
| | IS61LPS204836B-200B3L | IS61LPS409618B-200B3L | 165 PBGA,13x15mm, Lead-free |
| | IS61LPS204836B-200M3L | IS61LPS409618B-200M3L | 165 PBGA,15x17mm, Lead-free |
| | IS61LPS204836B-200B2L | IS61LPS409618B-200B2L | 119 PBGA, Lead-free |
| 166MHz | IS61LPS204836B-166TQ | IS61LPS409618B-166TQ | 100 TQFP, 2CE |
| | IS61LPS204836B-166TQ2 | IS61LPS409618B-166TQ2 | 100 TQFP, 3CE |
| | IS61LPS204836B-166B3 | IS61LPS409618B-166B3 | 165 PBGA,13x15mm |
| | IS61LPS204836B-166M3 | IS61LPS409618B-166M3 | 165 PBGA,15x17mm |
| | IS61LPS204836B-166B2 | IS61LPS409618B-166B2 | 119 PBGA |
| | IS61LPS204836B-166TQL | IS61LPS409618B-166TQL | 100 TQFP, 3CE, Lead-free |
| | IS61LPS204836B-166TQ2L | IS61LPS409618B-166TQ2L | 100 TQFP, 2CE, Lead-free |
| | IS61LPS204836B-166B3L | IS61LPS409618B-166B3L | 165 PBGA,13x15mm, Lead-free |
| | IS61LPS204836B-166M3L | IS61LPS409618B-166M3L | 165 PBGA,15x17mm, Lead-free |
| | IS61LPS204836B-166B2L | IS61LPS409618B-166B2L | 119 PBGA, Lead-free |

**Commercial Range: 0°C to 70°C ($V_{DD}$ = 2.5v / $V_{DDQ}$ = 2.5v)**

| Speed | x36 | x18 | Package |
|---|---|---|---|
| 250MHz | IS61VPS204836B-250TQ | IS61VPS409618B-250TQ | 100 TQFP, 3CE |
| | IS61VPS204836B-250TQ2 | IS61VPS409618B-250TQ2 | 100 TQFP, 2CE |
| | IS61VPS204836B-250B3 | IS61VPS409618B-250B3 | 165 PBGA,13x15mm |
| | IS61VPS204836B-250M3 | IS61VPS409618B-250M3 | 165 PBGA,15x17mm |
| | IS61VPS204836B-250B2 | IS61VPS409618B-250B2 | 119 PBGA |
| | IS61VPS204836B-250TQL | IS61VPS409618B-250TQL | 100 TQFP, 3CE, Lead-free |
| | IS61VPS204836B-250TQ2L | IS61VPS409618B-250TQ2L | 100 TQFP, 2CE, Lead-free |
| | IS61VPS204836B-250B3L | IS61VPS409618B-250B3L | 165 PBGA,13x15mm, Lead-free |
| | IS61VPS204836B-250M3L | IS61VPS409618B-250M3L | 165 PBGA,15x17mm, Lead-free |
| | IS61VPS204836B-250B2L | IS61VPS409618B-250B2L | 119 PBGA, Lead-free |
| 200MHz | IS61VPS204836B-200TQ | IS61VPS409618B-200TQ | 100 TQFP, 3CE |
| | IS61VPS204836B-200TQ2 | IS61VPS409618B-200TQ2 | 100 TQFP, 2CE |
| | IS61VPS204836B-200B3 | IS61VPS409618B-200B3 | 165 PBGA,13x15mm |
| | IS61VPS204836B-200M3 | IS61VPS409618B-200M3 | 165 PBGA,15x17mm |
| | IS61VPS204836B-200B2 | IS61VPS409618B-200B2 | 119 PBGA |
| | IS61VPS204836B-200TQL | IS61VPS409618B-200TQL | 100 TQFP, 3CE, Lead-free |
| | IS61VPS204836B-200TQ2L | IS61VPS409618B-200TQ2L | 100 TQFP, 2CE, Lead-free |
| | IS61VPS204836B-200B3L | IS61VPS409618B-200B3L | 165 PBGA,13x15mm, Lead-free |
| | IS61VPS204836B-200M3L | IS61VPS409618B-200M3L | 165 PBGA,15x17mm, Lead-free |
| | IS61VPS204836B-200B2L | IS61VPS409618B-200B2L | 119 PBGA, Lead-free |
| 166MHz | IS61VPS204836B-166TQ | IS61VPS409618B-166TQ | 100 TQFP, 3CE |
| | IS61VPS204836B-166TQ2 | IS61VPS409618B-166TQ2 | 100 TQFP, 2CE |
| | IS61VPS204836B-166B3 | IS61VPS409618B-166B3 | 165 PBGA,13x15mm |
| | IS61VPS204836B-166M3 | IS61VPS409618B-166M3 | 165 PBGA,15x17mm |
| | IS61VPS204836B-166B2 | IS61VPS409618B-166B2 | 119 PBGA |
| | IS61VPS204836B-166TQL | IS61VPS409618B-166TQL | 100 TQFP, 3CE, Lead-free |
| | IS61VPS204836B-166TQ2L | IS61VPS409618B-166TQ2L | 100 TQFP, 2CE, Lead-free |
| | IS61VPS204836B-166B3L | IS61VPS409618B-166B3L | 165 PBGA,13x15mm, Lead-free |
| | IS61VPS204836B-166M3L | IS61VPS409618B-166M3L | 165 PBGA,15x17mm, Lead-free |
| | IS61VPS204836B-166B2L | IS61VPS409618B-166B2L | 119 PBGA, Lead-free |

**Commercial Range: 0°C to 70°C(vDD = 1.8v / vDDQ = 1.8v)**

| Speed | x36 | x18 | Package |
|---|---|---|---|
| 200MHz | Please contact ISSI SRAM@issi.com | | |
| 166MHz | IS61VVPS204836B-166TQ | IS61VVPS409618B-166TQ | 100 TQFP, 3CE |
| | IS61VVPS204836B-166TQ2 | IS61VVPS409618B-166TQ2 | 100 TQFP, 2CE |
| | IS61VVPS204836B-166B3 | IS61VVPS409618B-166B3 | 165 PBGA,13x15mm |
| | IS61VVPS204836B-166M3 | IS61VVPS409618B-166M3 | 165 PBGA,15x17mm |
| | IS61VVPS204836B-166B2 | IS61VVPS409618B-166B2 | 119 PBGA |
| | IS61VVPS204836B-166TQL | IS61VVPS409618B-166TQL | 100 TQFP, 3CE, Lead-free |
| | IS61VVPS204836B-166TQ2L | IS61VVPS409618B-166TQ2L | 100 TQFP, 2CE, Lead-free |
| | IS61VVPS204836B-166B3L | IS61VVPS409618B-166B3L | 165 PBGA,13x15mm, Lead-free |
| | IS61VVPS204836B-166M3L | IS61VVPS409618B-166M3L | 165 PBGA,15x17mm, Lead-free |
| | IS61VVPS204836B-166B2L | IS61VVPS409618B-166B2L | 119 PBGA, Lead-free |

**Industrial Range: -40°C to +85°C (vDD = 3.3v / vDDQ = 2.5v/3.3v)**

| Speed | x32 | Package |
|---|---|---|
| 200MHz | IS61LPS204832B-200TQI | 100 TQFP, 3CE |
| | IS61LPS204832B-200TQLI | 100 TQFP, 3CE, Lead-free |
| | IS61LPS204832B-200TQ2I | 100 TQFP, 2CE |
| | IS61LPS204832B-200TQ2LI | 100 TQFP, 2CE, Lead-free |

| Speed | x36 | x18 | Package |
|---|---|---|---|
| 250MHz | IS61LPS204836B-250TQI | IS61LPS409618B-250TQI | 100 TQFP, 3CE |
| | IS61LPS204836B-250TQ2I | IS61LPS409618B-250TQ2I | 100 TQFP, 2CE |
| | IS61LPS204836B-250B3I | IS61LPS409618B-250B3I | 165 PBGA,13x15mm |
| | IS61LPS204836B-250M3I | IS61LPS409618B-250M3I | 165 PBGA,15x17mm |
| | IS61LPS204836B-250B2I | IS61LPS409618B-250B2I | 119 PBGA |
| | IS61LPS204836B-250TQLI | IS61LPS409618B-250TQLI | 100 TQFP, 3CE, Lead-free |
| | IS61LPS204836B-250TQ2LI | IS61LPS409618B-250TQ2LI | 100 TQFP, 2CE, Lead-free |
| | IS61LPS204836B-250B3LI | IS61LPS409618B-250B3LI | 165 PBGA,13x15mm, Lead-free |
| | IS61LPS204836B-250M3LI | IS61LPS409618B-250M3LI | 165 PBGA,15x17mm, Lead-free |
| | IS61LPS204836B-250B2LI | IS61LPS409618B-250B2LI | 119 PBGA, Lead-free |

| Speed | x36 | x18 | Package |
|---|---|---|---|
| 200MHz | IS61LPS204836B-200TQI | IS61LPS409618B-200TQI | 100 TQFP, 3CE |
| | IS61LPS204836B-200TQ2I | IS61LPS409618B-200TQ2I | 100 TQFP, 2CE |
| | IS61LPS204836B-200B3I | IS61LPS409618B-200B3I | 165 PBGA,13x15mm |
| | IS61LPS204836B-200M3I | IS61LPS409618B-200M3I | 165 PBGA,15x17mm |
| | IS61LPS204836B-200B2I | IS61LPS409618B-200B2I | 119 PBGA |
| | IS61LPS204836B-200TQLI | IS61LPS409618B-200TQLI | 100 TQFP, 3CE, Lead-free |
| | IS61LPS204836B-200TQ2LI | IS61LPS409618B-200TQ2LI | 100 TQFP, 2CE, Lead-free |
| | IS61LPS204836B-200B3LI | IS61LPS409618B-200B3LI | 165 PBGA,13x15mm, Lead-free |
| | IS61LPS204836B-200M3LI | IS61LPS409618B-200M3LI | 165 PBGA,15x17mm, Lead-free |
| | IS61LPS204836B-200B2LI | IS61LPS409618B-200B2LI | 119 PBGA, Lead-free |
| 166MHz | IS61LPS204836B-166TQI | IS61LPS409618B-166TQI | 100 TQFP, 2CE |
| | IS61LPS204836B-166TQ2I | IS61LPS409618B-166TQ2I | 100 TQFP, 3CE |
| | IS61LPS204836B-166B3I | IS61LPS409618B-166B3I | 165 PBGA,13x15mm |
| | IS61LPS204836B-166M3I | IS61LPS409618B-166M3I | 165 PBGA,15x17mm |
| | IS61LPS204836B-166B2I | IS61LPS409618B-166B2I | 119 PBGA |
| | IS61LPS204836B-166TQLI | IS61LPS409618B-166TQLI | 100 TQFP, 3CE, Lead-free |
| | IS61LPS204836B-166TQ2LI | IS61LPS409618B-166TQ2LI | 100 TQFP, 2CE, Lead-free |
| | IS61LPS204836B-166B3LI | IS61LPS409618B-166B3LI | 165 PBGA,13x15mm, Lead-free |
| | IS61LPS204836B-166M3LI | IS61LPS409618B-166M3LI | 165 PBGA,15x17mm, Lead-free |
| | IS61LPS204836B-166B2LI | IS61LPS409618B-166B2LI | 119 PBGA, Lead-free |

**Industrial Range: -40°C to +85°C (vDD = 2.5v / vDDQ = 2.5v)**

| Speed | x36 | x18 | Package |
|---|---|---|---|
| 250MHz | IS61VPS204836B-250TQI | IS61VPS409618B-250TQI | 100 TQFP, 3CE |
| | IS61VPS204836B-250TQ2I | IS61VPS409618B-250TQ2I | 100 TQFP, 2CE |
| | IS61VPS204836B-250B3I | IS61VPS409618B-250B3I | 165 PBGA,13x15mm |
| | IS61VPS204836B-250M3I | IS61VPS409618B-250M3I | 165 PBGA,15x17mm |
| | IS61VPS204836B-250B2I | IS61VPS409618B-250B2I | 119 PBGA |
| | IS61VPS204836B-250TQLI | IS61VPS409618B-250TQLI | 100 TQFP, 3CE, Lead-free |
| | IS61VPS204836B-250TQ2LI | IS61VPS409618B-250TQ2LI | 100 TQFP, 2CE, Lead-free |
| | IS61VPS204836B-250B3LI | IS61VPS409618B-250B3LI | 165 PBGA,13x15mm, Lead-free |
| | IS61VPS204836B-250M3LI | IS61VPS409618B-250M3LI | 165 PBGA,15x17mm, Lead-free |
| | IS61VPS204836B-250B2LI | IS61VPS409618B-250B2LI | 119 PBGA, Lead-free |
| 200MHz | IS61VPS204836B-200TQI | IS61VPS409618B-200TQI | 100 TQFP, 3CE |
| | IS61VPS204836B-200TQ2I | IS61VPS409618B-200TQ2I | 100 TQFP, 2CE |
| | IS61VPS204836B-200B3I | IS61VPS409618B-200B3I | 165 PBGA,13x15mm |
| | IS61VPS204836B-200M3I | IS61VPS409618B-200M3I | 165 PBGA,15x17mm |
| | IS61VPS204836B-200B2I | IS61VPS409618B-200B2I | 119 PBGA |
| | IS61VPS204836B-200TQLI | IS61VPS409618B-200TQLI | 100 TQFP, 3CE, Lead-free |
| | IS61VPS204836B-200TQ2LI | IS61VPS409618B-200TQ2LI | 100 TQFP, 2CE, Lead-free |
| | IS61VPS204836B-200B3LI | IS61VPS409618B-200B3LI | 165 PBGA,13x15mm, Lead-free |
| | IS61VPS204836B-200M3LI | IS61VPS409618B-200M3LI | 165 PBGA,15x17mm, Lead-free |
| | IS61VPS204836B-200B2LI | IS61VPS409618B-200B2LI | 119 PBGA, Lead-free |

| Speed | x36 | x18 | Package |
|---|---|---|---|
| 166MHz | IS61VPS204836B-166TQI | IS61VPS409618B-166TQI | 100 TQFP, 3CE |
| | IS61VPS204836B-166TQ2I | IS61VPS409618B-166TQ2I | 100 TQFP, 2CE |
| | IS61VPS204836B-166B3I | IS61VPS409618B-166B3I | 165 PBGA,13x15mm |
| | IS61VPS204836B-166M3I | IS61VPS409618B-166M3I | 165 PBGA,15x17mm |
| | IS61VPS204836B-166B2I | IS61VPS409618B-166B2I | 119 PBGA |
| | IS61VPS204836B-166TQLI | IS61VPS409618B-166TQLI | 100 TQFP, 3CE, Lead-free |
| | IS61VPS204836B-166TQ2LI | IS61VPS409618B-166TQ2LI | 100 TQFP, 2CE, Lead-free |
| | IS61VPS204836B-166B3LI | IS61VPS409618B-166B3LI | 165 PBGA,13x15mm, Lead-free |
| | IS61VPS204836B-166M3LI | IS61VPS409618B-166M3LI | 165 PBGA,15x17mm, Lead-free |
| | IS61VPS204836B-166B2LI | IS61VPS409618B-166B2LI | 119 PBGA, Lead-free |

**Industrial Range: -40°C to +85°C ($V_{DD}$ = 1.8v / $V_{DDQ}$ = 1.8v)**

| Speed | x36 | x18 | Package |
|---|---|---|---|
| 200MHz | IS61VVPS204836B-200TQI | IS61VVPS409618B-200TQI | 100 TQFP, 3CE |
| | IS61VVPS204836B-200TQ2I | IS61VVPS409618B-200TQ2I | 100 TQFP, 2CE |
| | IS61VVPS204836B-200B3I | IS61VVPS409618B-200B3I | 165 PBGA,13x15mm |
| | IS61VVPS204836B-200M3I | IS61VVPS409618B-200M3I | 165 PBGA,15x17mm |
| | IS61VVPS204836B-200B2I | IS61VVPS409618B-200B2I | 119 PBGA |
| | IS61VVPS204836B-200TQLI | IS61VVPS409618B-200TQLI | 100 TQFP, 3CE, Lead-free |
| | IS61VVPS204836B-200TQ2LI | IS61VVPS409618B-200TQ2LI | 100 TQFP, 2CE, Lead-free |
| | IS61VVPS204836B-200B3LI | IS61VVPS409618B-200B3LI | 165 PBGA,13x15mm, Lead-free |
| | IS61VVPS204836B-200M3LI | IS61VVPS409618B-200M3LI | 165 PBGA,15x17mm, Lead-free |
| | IS61VVPS204836B-200B2LI | IS61VVPS409618B-200B2LI | 119 PBGA, Lead-free |
| 166MHz | IS61VVPS204836B-166TQI | IS61VVPS409618B-166TQI | 100 TQFP, 3CE |
| | IS61VVPS204836B-166TQ2I | IS61VVPS409618B-166TQ2I | 100 TQFP, 2CE |
| | IS61VVPS204836B-166B3I | IS61VVPS409618B-166B3I | 165 PBGA,13x15mm |
| | IS61VVPS204836B-166M3I | IS61VVPS409618B-166M3I | 165 PBGA,15x17mm |
| | IS61VVPS204836B-166B2I | IS61VVPS409618B-166B2I | 119 PBGA |
| | IS61VVPS204836B-166TQLI | IS61VVPS409618B-166TQLI | 100 TQFP, 3CE, Lead-free |
| | IS61VVPS204836B-166TQ2LI | IS61VVPS409618B-166TQ2LI | 100 TQFP, 2CE, Lead-free |
| | IS61VVPS204836B-166B3LI | IS61VVPS409618B-166B3LI | 165 PBGA,13x15mm, Lead-free |
| | IS61VVPS204836B-166M3LI | IS61VVPS409618B-166M3LI | 165 PBGA,15x17mm, Lead-free |
| | IS61VVPS204836B-166B2LI | IS61VVPS409618B-166B2LI | 119 PBGA, Lead-free |

**Automotive(A3) Range: -40°C to +125°C (vDD = 3.3v / vDDQ = 2.5v/3.3v)**

| Speed | X32 | Package |
|---|---|---|
| | Please contact ISSI SRAM@issi.com | |

| Speed | x36 | x18 | Package |
|---|---|---|---|
| 200MHz | Please contact ISSI SRAM@issi.com | | |
| 166MHz | IS64LPS204836B-166TQA3 | IS64LPS409618B-166TQA3 | 100 TQFP, 2CE |
| | IS64LPS204836B-166TQ2A3 | IS64LPS409618B-166TQ2A3 | 100 TQFP, 3CE |
| | IS64LPS204836B-166B3A3 | IS64LPS409618B-166B3A3 | 165 PBGA,13x15mm |
| | IS64LPS204836B-166M3A3 | IS64LPS409618B-166M3A3 | 165 PBGA,15x17mm |
| | IS64LPS204836B-166B2A3 | IS64LPS409618B-166B2A3 | 119 PBGA |
| | IS64LPS204836B-166TQLA3 | IS64LPS409618B-166TQLA3 | 100 TQFP, 3CE, Lead-free |
| | IS64LPS204836B-166TQ2LA3 | IS64LPS409618B-166TQ2LA3 | 100 TQFP, 2CE, Lead-free |
| | IS64LPS204836B-166B3LA3 | IS64LPS409618B-166B3LA3 | 165 PBGA,13x15mm, Lead-free |
| | IS64LPS204836B-166M3LA3 | IS64LPS409618B-166M3LA3 | 165 PBGA,15x17mm, Lead-free |
| | IS64LPS204836B-166B2LA3 | IS64LPS409618B-166B2LA3 | 119 PBGA, Lead-free |

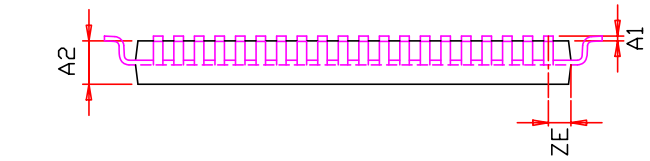
**Automotive(A3) Range: -40°C to +125°C (vDD = 2.5v / vDDQ = 2.5v)**

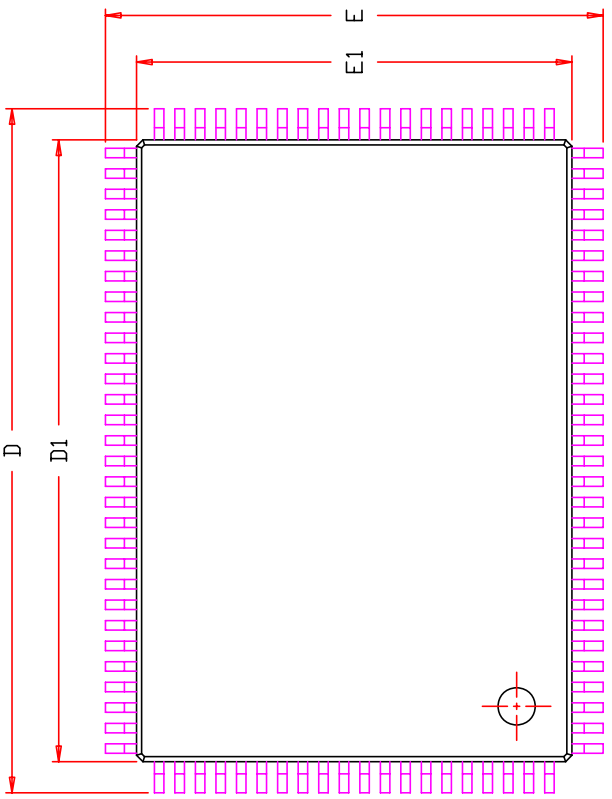
| Speed | x36 | x18 | Package |
|---|---|---|---|
| 200MHz | IS64VPS204836B-200TQA3 | IS64VPS409618B-200TQA3 | 100 TQFP, 3CE |
| | IS64VPS204836B-200TQ2A3 | IS64VPS409618B-200TQ2A3 | 100 TQFP, 2CE |
| | IS64VPS204836B-200B3A3 | IS64VPS409618B-200B3A3 | 165 PBGA,13x15mm |
| | IS64VPS204836B-200M3A3 | IS64VPS409618B-200M3A3 | 165 PBGA,15x17mm |
| | IS64VPS204836B-200B2A3 | IS64VPS409618B-200B2A3 | 119 PBGA |
| | IS64VPS204836B-200TQLA3 | IS64VPS409618B-200TQLA3 | 100 TQFP, 3CE, Lead-free |
| | IS64VPS204836B-200TQ2LA3 | IS64VPS409618B-200TQ2LA3 | 100 TQFP, 2CE, Lead-free |
| | IS64VPS204836B-200B3LA3 | IS64VPS409618B-200B3LA3 | 165 PBGA,13x15mm, Lead-free |
| | IS64VPS204836B-200M3LA3 | IS64VPS409618B-200M3LA3 | 165 PBGA,15x17mm, Lead-free |
| | IS64VPS204836B-200B2LA3 | IS64VPS409618B-200B2LA3 | 119 PBGA, Lead-free |
| 166MHz | IS64VPS204836B-166TQA3 | IS64VPS409618B-166TQA3 | 100 TQFP, 3CE |
| | IS64VPS204836B-166TQ2A3 | IS64VPS409618B-166TQ2A3 | 100 TQFP, 2CE |
| | IS64VPS204836B-166B3A3 | IS64VPS409618B-166B3A3 | 165 PBGA,13x15mm |
| | IS64VPS204836B-166M3A3 | IS64VPS409618B-166M3A3 | 165 PBGA,15x17mm |
| | IS64VPS204836B-166B2A3 | IS64VPS409618B-166B2A3 | 119 PBGA |
| | IS64VPS204836B-166TQLA3 | IS64VPS409618B-166TQLA3 | 100 TQFP, 3CE, Lead-free |
| | IS64VPS204836B-166TQ2LA3 | IS64VPS409618B-166TQ2LA3 | 100 TQFP, 2CE, Lead-free |
| | IS64VPS204836B-166B3LA3 | IS64VPS409618B-166B3LA3 | 165 PBGA,13x15mm, Lead-free |
| | IS64VPS204836B-166M3LA3 | IS64VPS409618B-166M3LA3 | 165 PBGA,15x17mm, Lead-free |
| | IS64VPS204836B-166B2LA3 | IS64VPS409618B-166B2LA3 | 119 PBGA, Lead-free |

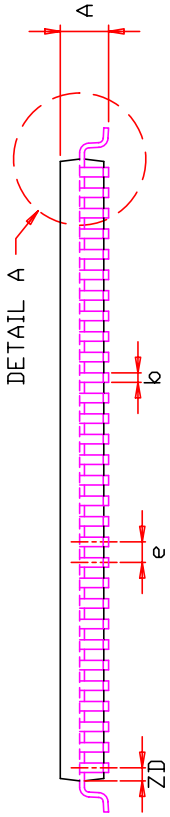
**Automotive(A3) Range: -40°C to +125°C ($V_{DD}$ = 1.8v / $V_{DDQ}$ = 1.8v)**

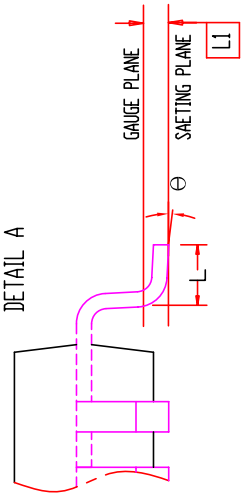
| Speed | x36 | x18 | Package |
|---|---|---|---|
| 200MHz | IS64VVPS204836B-200TQA3 | IS64VVPS409618B-200TQA3 | 100 TQFP, 3CE |
| | IS64VVPS204836B-200TQ2A3 | IS64VVPS409618B-200TQ2A3 | 100 TQFP, 2CE |
| | IS64VVPS204836B-200B3A3 | IS64VVPS409618B-200B3A3 | 165 PBGA,13x15mm |
| | IS64VVPS204836B-200M3A3 | IS64VVPS409618B-200M3A3 | 165 PBGA,15x17mm |
| | IS64VVPS204836B-200B2A3 | IS64VVPS409618B-200B2A3 | 119 PBGA |
| | IS64VVPS204836B-200TQLA3 | IS64VVPS409618B-200TQLA3 | 100 TQFP, 3CE, Lead-free |
| | IS64VVPS204836B-200TQ2LA3 | IS64VVPS409618B-200TQ2LA3 | 100 TQFP, 2CE, Lead-free |
| | IS64VVPS204836B-200B3LA3 | IS64VVPS409618B-200B3LA3 | 165 PBGA,13x15mm, Lead-free |
| | IS64VVPS204836B-200M3LA3 | IS64VVPS409618B-200M3LA3 | 165 PBGA,15x17mm, Lead-free |
| | IS64VVPS204836B-200B2LA3 | IS64VVPS409618B-200B2LA3 | 119 PBGA, Lead-free |
| 166MHz | IS64VVPS204836B-166TQA3 | IS64VVPS409618B-166TQA3 | 100 TQFP, 3CE |
| | IS64VVPS204836B-166TQ2A3 | IS64VVPS409618B-166TQ2A3 | 100 TQFP, 2CE |
| | IS64VVPS204836B-166B3A3 | IS64VVPS409618B-166B3A3 | 165 PBGA,13x15mm |
| | IS64VVPS204836B-166M3A3 | IS64VVPS409618B-166M3A3 | 165 PBGA,15x17mm |
| | IS64VVPS204836B-166B2A3 | IS64VVPS409618B-166B2A3 | 119 PBGA |
| | IS64VVPS204836B-166TQLA3 | IS64VVPS409618B-166TQLA3 | 100 TQFP, 3CE, Lead-free |
| | IS64VVPS204836B-166TQ2LA3 | IS64VVPS409618B-166TQ2LA3 | 100 TQFP, 2CE, Lead-free |
| | IS64VVPS204836B-166B3LA3 | IS64VVPS409618B-166B3LA3 | 165 PBGA,13x15mm, Lead-free |
| | IS64VVPS204836B-166M3LA3 | IS64VVPS409618B-166M3LA3 | 165 PBGA,15x17mm, Lead-free |
| | IS64VVPS204836B-166B2LA3 | IS64VVPS409618B-166B2LA3 | 119 PBGA, Lead-free |

| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.40 | —— | 1.60 | 0.055 | —— | 0.063 |
| A1 | 0.05 | —— | 0.15 | 0.002 | —— | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.22 | 0.30 | 0.38 | 0.009 | 0.012 | 0.015 |
| D | 21.90 | 22.00 | 22.10 | 0.862 | 0.866 | 0.870 |
| D1 | 19.90 | 20.00 | 20.10 | 0.783 | 0.787 | 0.791 |
| E | 15.90 | 16.00 | 16.10 | 0.626 | 0.630 | 0.634 |
| E1 | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| e | | 0.65 BSC. | | | 0.026 BSC. | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 0.25 BSC. | | | 0.010 BSC. | |
| ZD | | 0.575 REF. | | | 0.023 REF. | |
| ZE | | 0.825 REF. | | | 0.032 REF. | |
| θ | 0 | 3.5° | 7° | 0 | 3.5° | 7° |



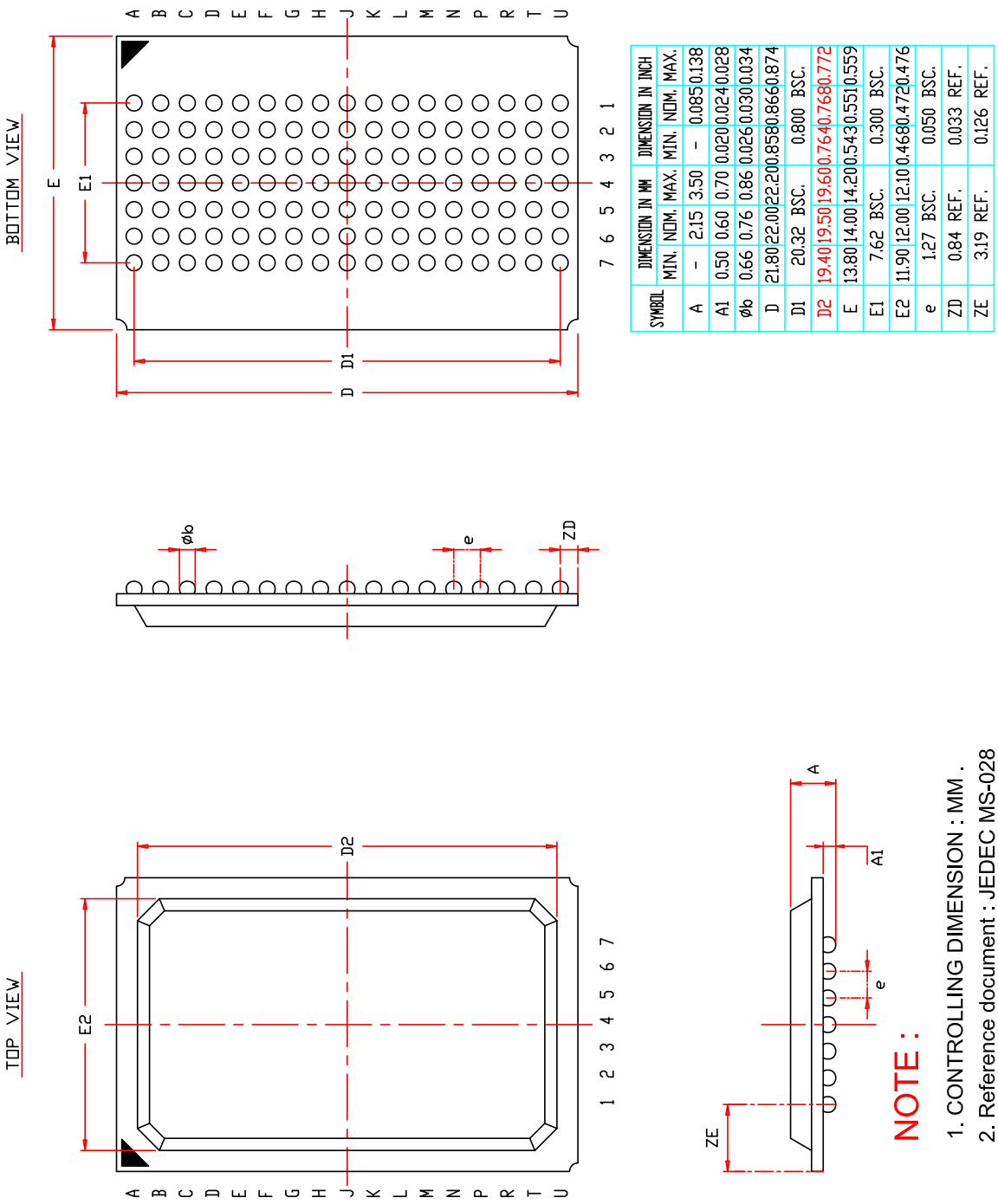




NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

| | TITLE | REV. | DATE |
|---|---|---|---|
| ISSI | 100L 14x20x1.4mm LQFP (Footprint : 2.0 mm) Package Outline | F | 09/01/2009 |

280-600-011 REV. A

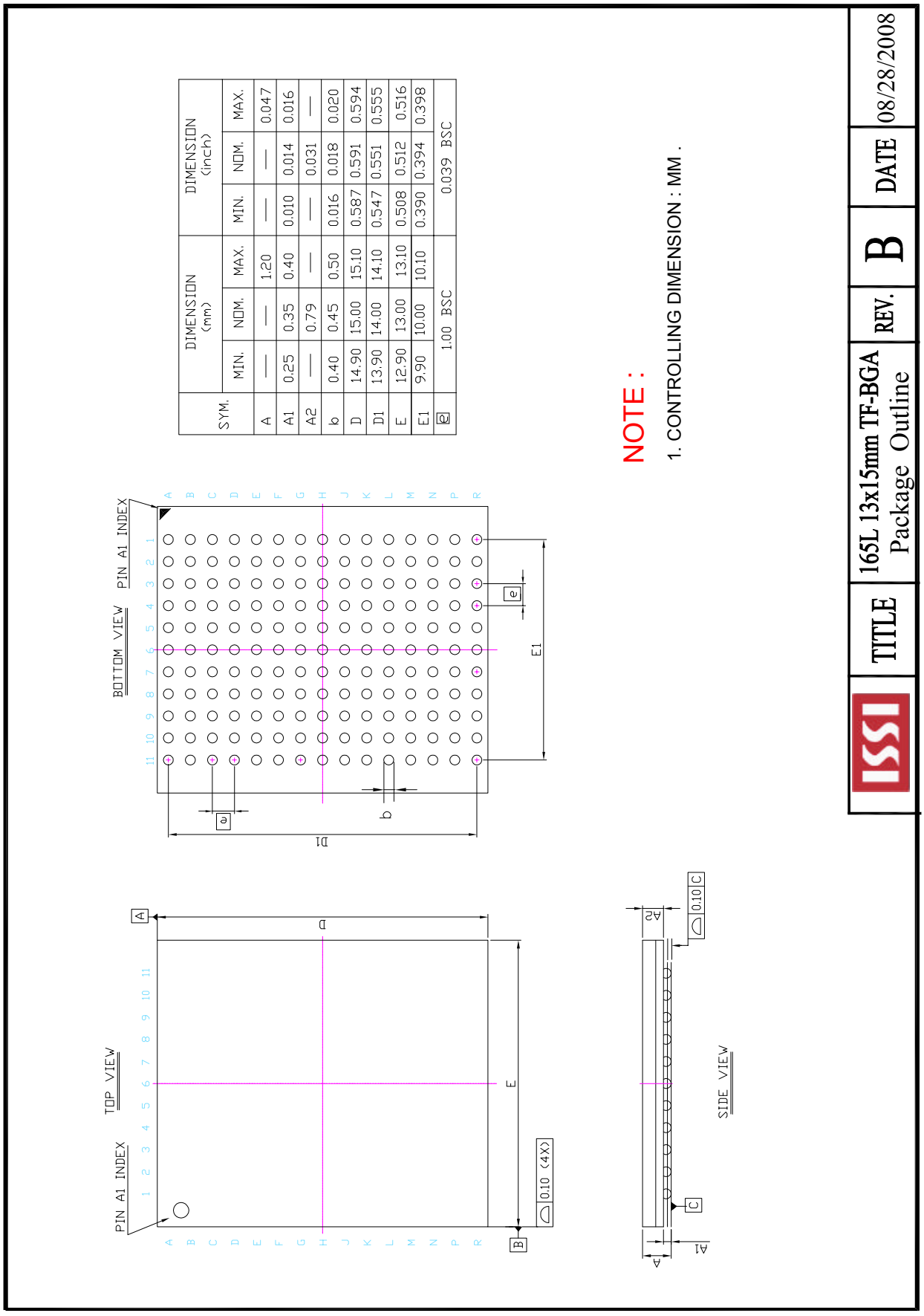


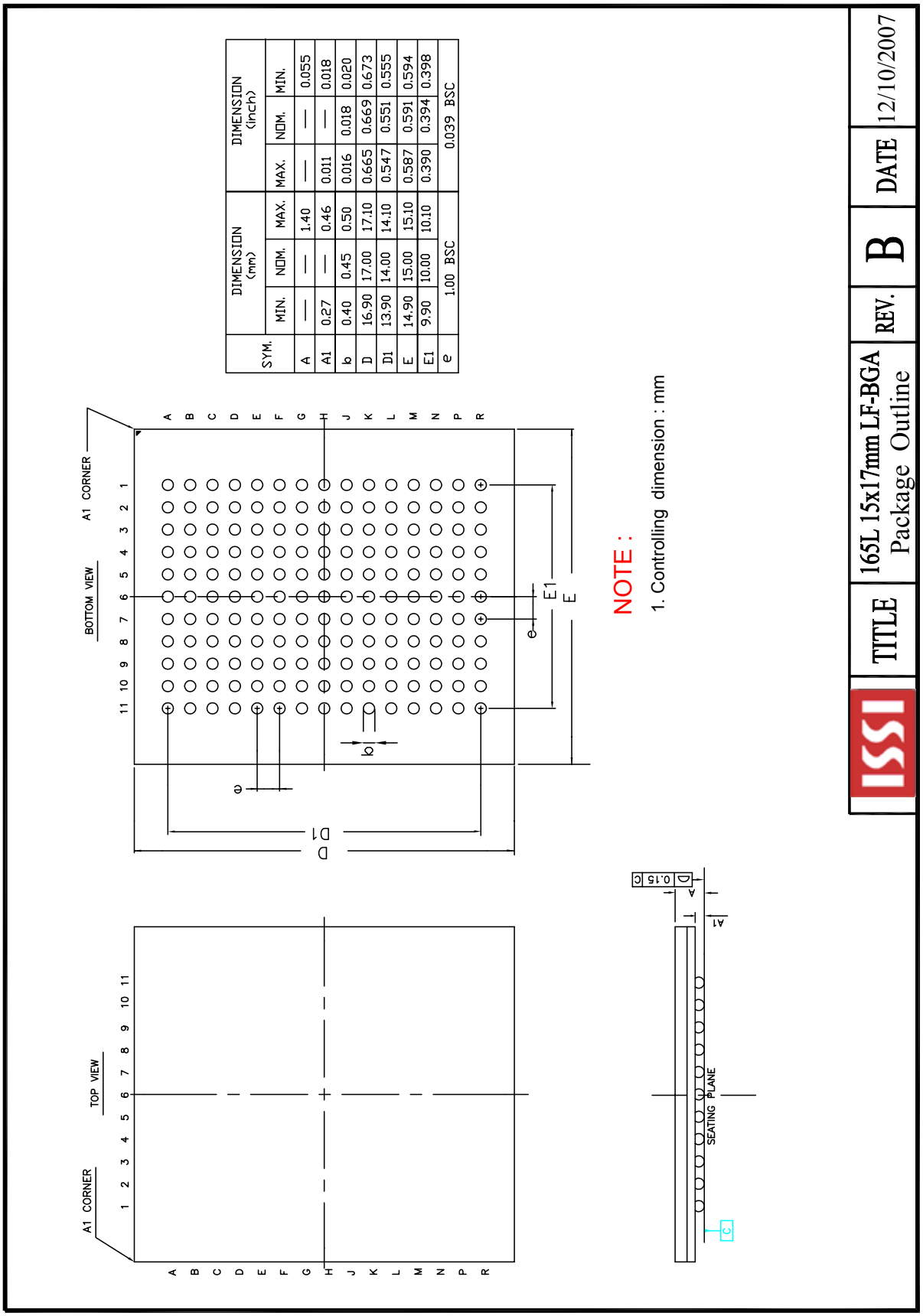

| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | – | 2.15 | 3.50 | – | 0.085 | 0.138 |
| A1 | 0.50 | 0.60 | 0.70 | 0.020 | 0.024 | 0.028 |
| øb | 0.66 | 0.76 | 0.86 | 0.026 | 0.030 | 0.034 |
| D | 21.80 | 22.00 | 22.20 | 0.858 | 0.866 | 0.874 |
| D1 | | 20.32 BSC. | | | 0.800 BSC. | |
| D2 | 19.40 | 19.50 | 19.60 | 0.764 | 0.768 | 0.772 |
| E | 13.80 | 14.00 | 14.20 | 0.543 | 0.551 | 0.559 |
| E1 | | 7.62 BSC. | | | 0.300 BSC. | |
| E2 | 11.90 | 12.00 | 12.10 | 0.468 | 0.472 | 0.476 |
| e | | 1.27 BSC. | | | 0.050 BSC. | |
| ZD | | 0.84 REF. | | | 0.033 REF. | |
| ZE | | 3.19 REF. | | | 0.126 REF. | |

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MS-028

| | | | | |
|---|---|---|---|---|
| ISSI | TITLE | 119L 14x22mm PBGA Package Outline | REV. E | DATE 10/13/2010 |


ISSI
TITLE
165L 13x15mm TF-BGA Package Outline
REV.
B
DATE
08/28/2008
NOTE :
1. CONTROLLING DIMENSION : MM .
SYM.
DIMENSION (mm)
MIN. NOM. MAX.
DIMENSION (inch)
MIN. NOM. MAX.
A — — 1.20 — — 0.047
A1 0.25 0.35 0.40 0.010 0.014 0.016
A2 — 0.79 — — 0.031 —
b 0.40 0.45 0.50 0.016 0.018 0.020
D 14.90 15.00 15.10 0.587 0.591 0.594
D1 13.90 14.00 14.10 0.547 0.551 0.555
E 12.90 13.00 13.10 0.508 0.512 0.516
E1 9.90 10.00 10.10 0.390 0.394 0.398
e 1.00 BSC 0.039 BSC
BOTTOM VIEW
PIN A1 INDEX
TOP VIEW
PIN A1 INDEX
SIDE VIEW
0.10 C
0.10 (4X)




| SYM. | DIMENSION (mm) | | | DIMENSION (inch) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.40 | 0.055 | — | — |
| A1 | 0.27 | — | 0.46 | 0.018 | — | 0.011 |
| b | 0.40 | 0.45 | 0.50 | 0.020 | 0.018 | 0.016 |
| D | 16.90 | 17.00 | 17.10 | 0.673 | 0.669 | 0.665 |
| D1 | 13.90 | 14.00 | 14.10 | 0.555 | 0.551 | 0.547 |
| E | 14.90 | 15.00 | 15.10 | 0.594 | 0.591 | 0.587 |
| E1 | 9.90 | 10.00 | 10.10 | 0.398 | 0.394 | 0.390 |
| e | 1.00 BSC | | | 0.039 BSC | | |

LifeElectronics
Живое партнерство

**ООО «ЛайфЭлектроникс»** **“LifeElectronics” LLC**

*ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703*

*Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.*

*С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров*

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- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
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- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

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- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

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*Конструкторский отдел помогает осуществить:*

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- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
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*Тел: +7 (812) 336 43 04 (многоканальный)*
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