

PROTECTION PRODUCTS - MicroClamp™

Description

The μClamp™ series of TVS arrays are designed to protect sensitive electronics from damage or latch-up due to ESD. They are designed for use in applications where board space is at a premium. Each device requires less than 2.9mm² of PCB area and will protect up to four lines. They are unidirectional devices and may be used on lines with positive signal polarities.

The μclamp™3304A is constructed using Semtech's proprietary EPD process technology. The EPD process provides low standoff voltages with significant reductions in leakage currents and capacitance over silicon-avalanche diode processes. They feature a true operating voltage of 3.3 volts for superior protection when compared to traditional pn junction devices.

These devices may be used to meet the immunity requirements of IEC 61000-4-2, level 4. They offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation. The small SC89 package makes them ideal for use in portable electronics such as cell phones, PDAs, notebook computers, and digital cameras.

Features

- ◆ Transient protection for data lines to **IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact) IEC 61000-4-4 (EFT) 40A (5/50ns)**
- ◆ Protects four unidirectional I/O lines
- ◆ Ultra-small SC-89 package (**1.7 x 1.7 x 0.6mm**) requires less than 2.9mm² of PCB area
- ◆ Working voltage: 3.3V
- ◆ Low leakage current
- ◆ Low operating and clamping voltages
- ◆ Solid-state silicon-avalanche technology

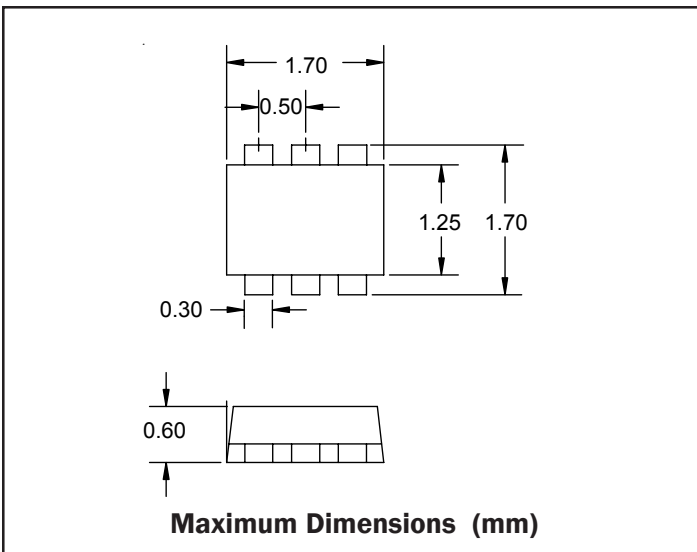
Mechanical Characteristics

- ◆ SC-89 (SOT-666) package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking: Marking Code
- ◆ Lead Finish: Matte Tin
- ◆ RoHS Compliant
- ◆ Weight: 2.9mg (typical)
- ◆ Packaging: Tape and Reel

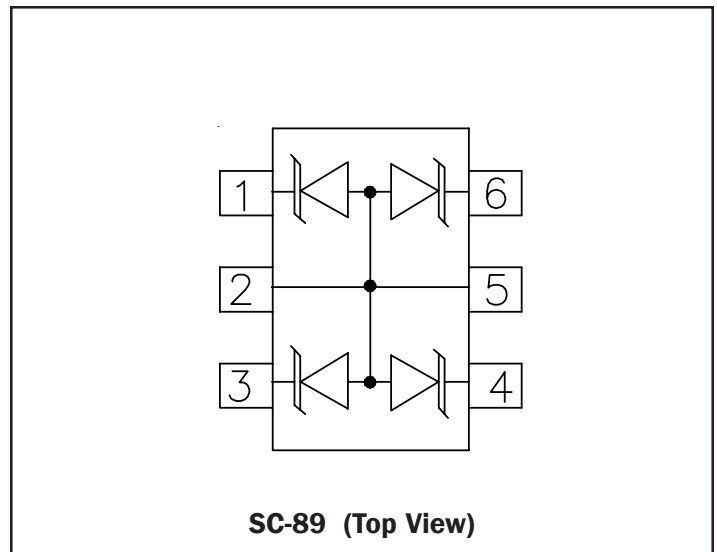
Applications

- ◆ Cellular Handsets and Accessories
- ◆ Cordless Phones
- ◆ Notebooks and Handhelds
- ◆ Portable Instrumentation
- ◆ Digital Cameras
- ◆ Peripherals
- ◆ MP3 Players

Dimensions



Schematic & PIN Configuration



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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P_{pk}	40	Watts
Maximum Peak Pulse Current (tp = 8/20μs)	I_{pp}	5	Amps
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{PP}	+/- 20 +/- 15	kV
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

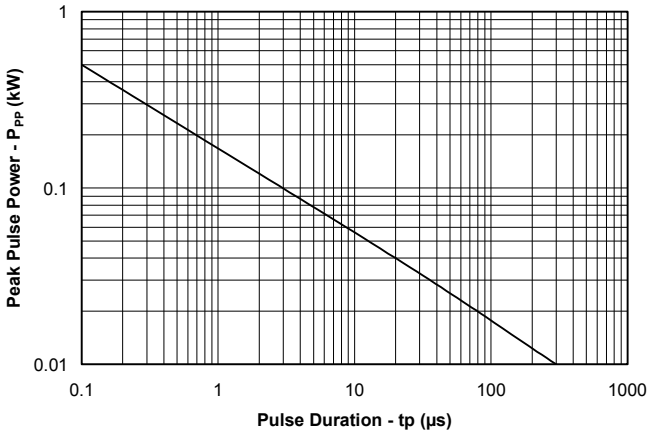
Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				3.3	V
Punch-Through Voltage	V_{PT}	$I_{PT} = 2\mu A$	3.5			V
Snap-Back Voltage	V_{SB}	$I_{SB} = 50mA$	2.8			V
Reverse Leakage Current	I_R	$V_{RWM} = 3.3V$		0.05	0.5	μA
Clamping Voltage	V_C	$I_{PP} = 1A, tp = 8/20\mu s$			5.5	V
Clamping Voltage	V_C	$I_{PP} = 5A, tp = 8/20\mu s$			8.0	V
Forward Clamping Voltage	V_F	$I_{PP} = 1A, tp = 8/20\mu s$			2.4	V
Junction Capacitance	C_j	I/O pin to Gnd $V_R = 0V, f = 1MHz$		22	30	pF
		I/O pin to Gnd $V_R = 3.3V, f = 1MHz$		14		pF

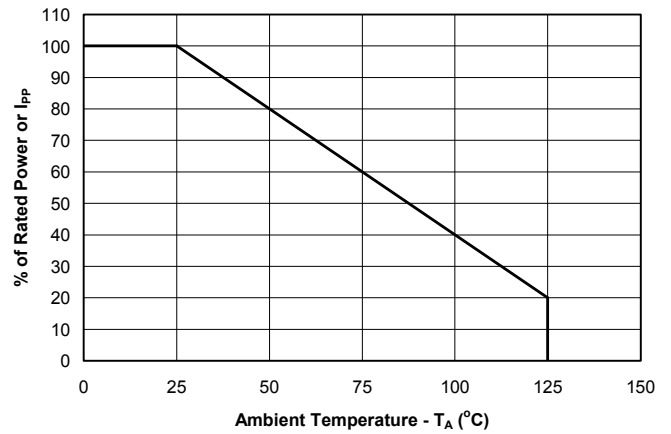
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Typical Characteristics

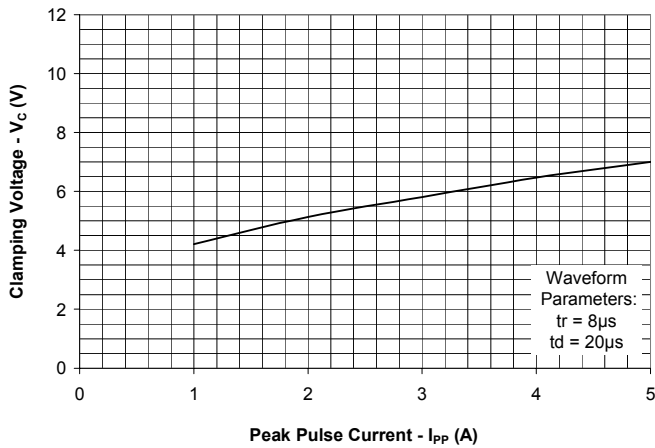
Non-Repetitive Peak Pulse Power vs. Pulse Time



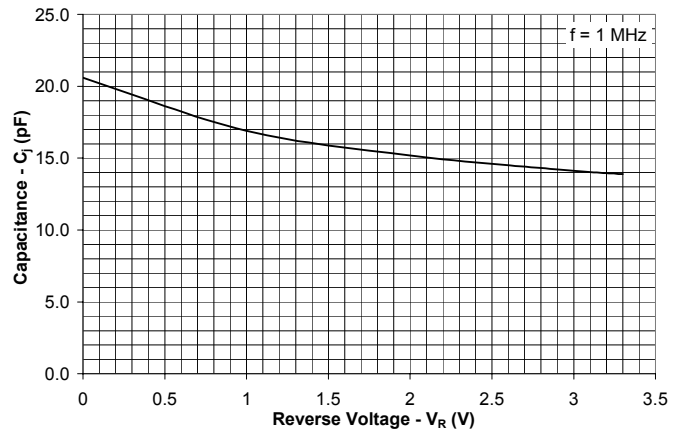
Power Derating Curve



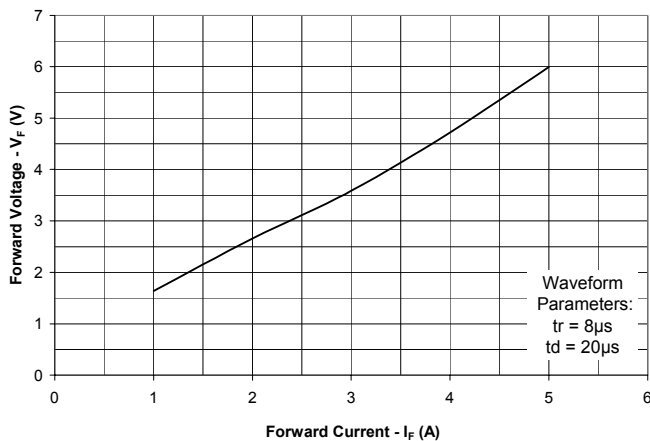
Clamping Voltage vs. Peak Pulse Current



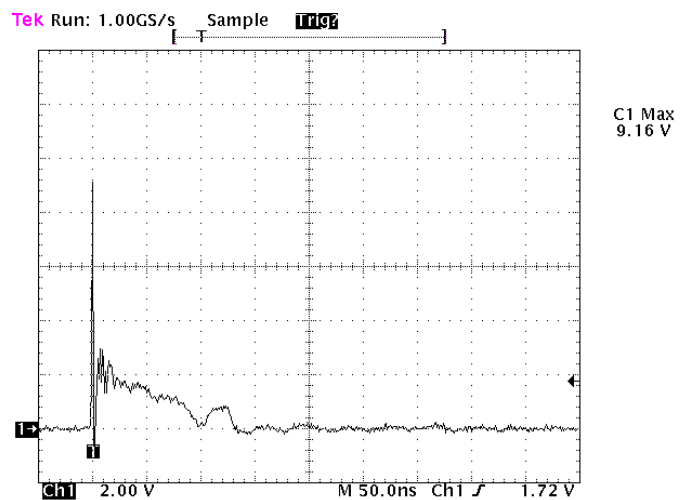
Junction Capacitance vs. Reverse Voltage



Forward Voltage vs Forward Current



ESD Clamping (8kV Contact per IEC 61000-4-2)



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Applications Information

Device Connection for Protection of Four Data Lines

These devices are designed to protect up to four unidirectional data lines. The device is connected as follows:

1. Unidirectional protection of four I/O lines is achieved by connecting pins 1, 3, 4, and 6 to the data lines. Pins 2 and 5 are connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.

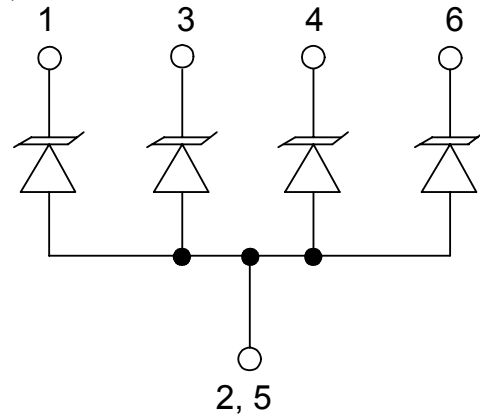
Due to the “snap-back” characteristics of the low voltage TVS, it is not recommended that any of the I/O lines be directly connected to a DC source greater than snap-back voltage (V_{SB}) as the device can latch on as described below.

EPD TVS Characteristics

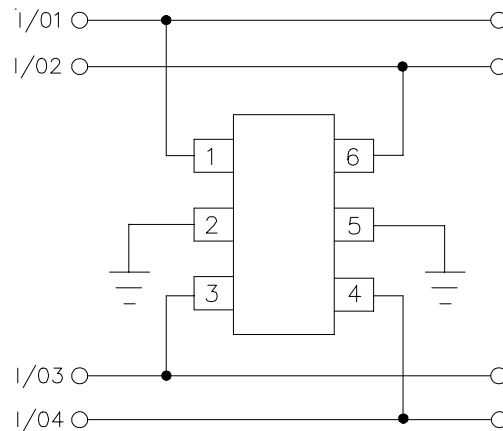
The SMF3.3 is constructed using Semtech’s proprietary EPD technology. The structure of the EPD TVS is vastly different from the traditional pn-junction devices. At voltages below 5V, high leakage current and junction capacitance render conventional avalanche technology impractical for most applications. However, by utilizing the EPD technology, the SMF3.3 can effectively operate at 3.3V while maintaining excellent electrical characteristics.

The EPD TVS employs a complex npnp structure in contrast to the pn structure normally found in traditional silicon-avalanche TVS diodes. Since the EPD TVS devices use a 4-layer structure, they exhibit a slightly different IV characteristic curve when compared to conventional devices. During normal operation, the device represents a high-impedance to the circuit up to the device working voltage (V_{RWM}). During an ESD event, the device will begin to conduct and will enter a low impedance state when the punch through voltage (V_{PT}) is exceeded. Unlike a conventional device, the low voltage TVS will exhibit a slight negative resistance characteristic as it conducts current. This characteristic aids in lowering the clamping voltage of the device, but must be considered in applications where DC voltages are present.

Circuit Diagram



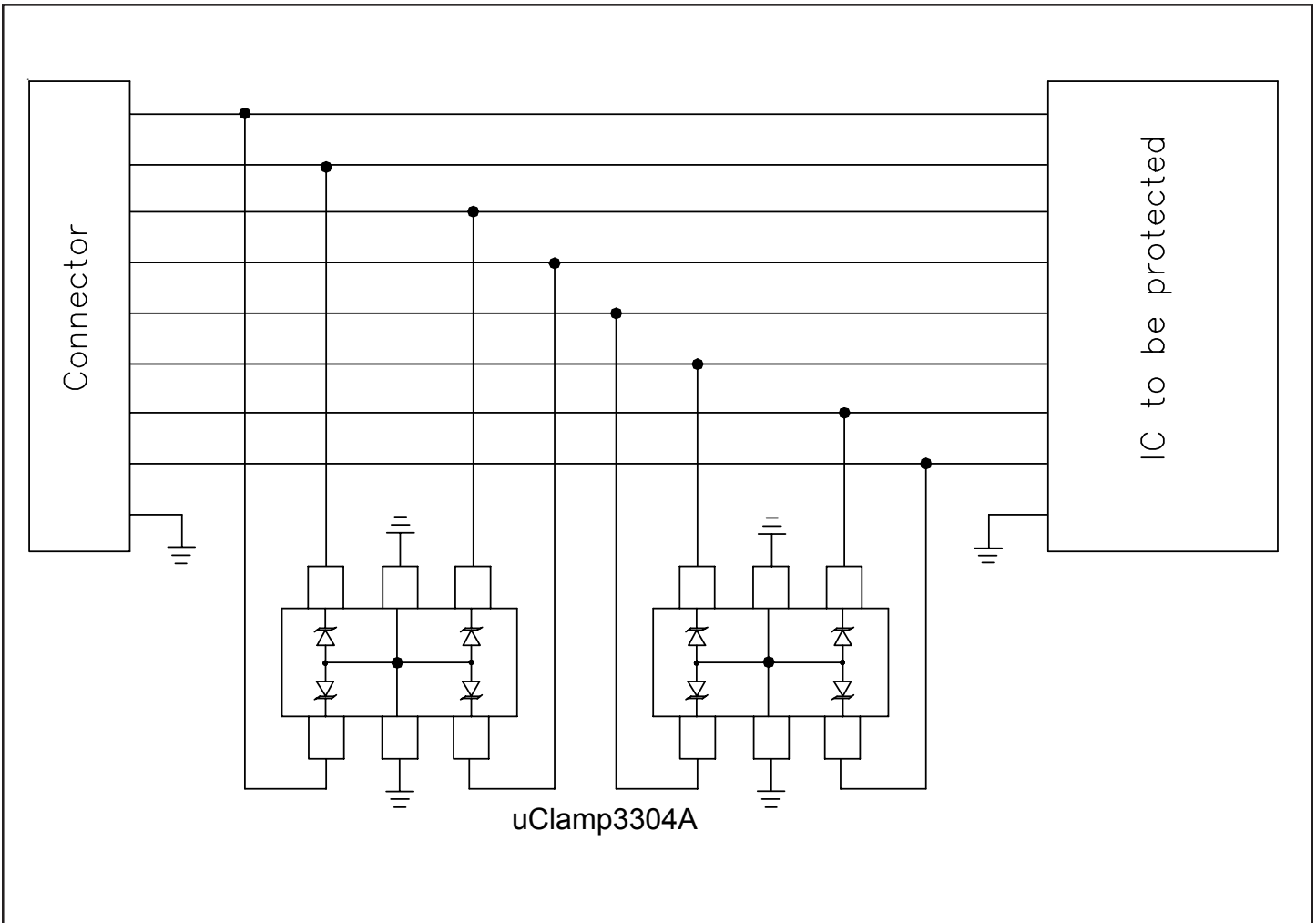
Protection of Four Unidirectional Lines



When the TVS is conducting current, it will exhibit a slight “snap-back” or negative resistance characteristics due to its structures. This point is defined on the curve by the snap-back voltage (V_{SB}) and snap-back current (I_{SB}). To return to a non-conducting state, the current through the device must fall below the I_{SB} (approximately <50mA) and the voltage must fall below the V_{SB} (normally 2.8 volts for a 3.3V device). If a 3.3V TVS is connected to 3.3V DC source, it will never fall below the snap-back voltage of 2.8V and will therefore stay in a conducting state.

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Typical Applications



Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

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Applications Information - Spice Model

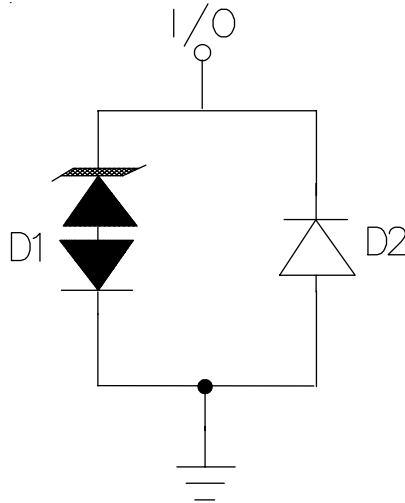
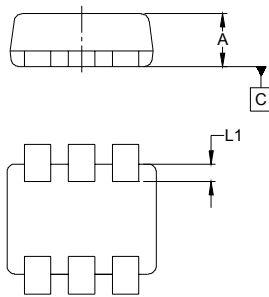
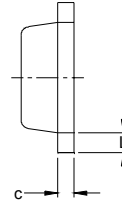
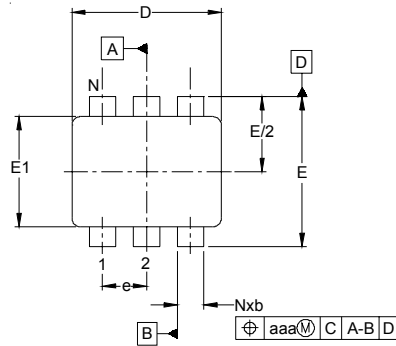


Figure 1 - μClamp3304A Spice Model

Table 1 - μClamp3304A Spice Parameters			
Parameter	Unit	D1 (TVS)	D2 (LCRD)
IS	Amp	1.00E-20	1.00E-20
BV	Volt	3.47	8
VJ	Volt	14	0.70
RS	Ohm	0.737	0.795
IBV	Amp	1.0E-3	1.0E-3
CJO	Farad	14.53E-12	6E-12
TT	sec	2.541E-9	2.541E-9
M	-	0.152	0.152
N	-	1.1	1.1
EG	eV	1.11	1.11

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Outline Drawing - SC-89 (SOT-666)

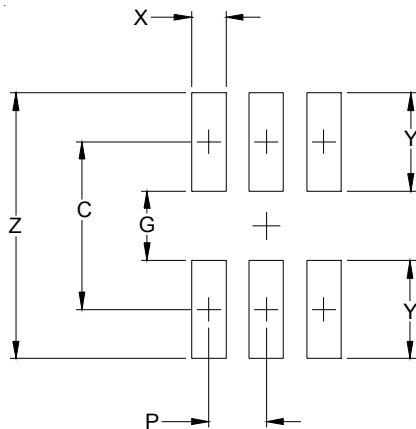


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.019	-	.024	0.50	-	0.60
b	.005	-	.012	0.15	-	0.30
c	.003	-	.007	0.10	-	0.18
D	.059	.063	.067	1.50	1.60	1.70
E	.061	.063	.067	1.55	1.60	1.70
E1	.043	.047	.049	1.10	1.20	1.25
e	.020 BSC			0.50 BSC		
L	.003	.008	.012	0.10	0.20	0.30
L1	.003	.006	.008	0.10	0.15	0.20
N	6			6		
aaa	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern - SC-89 (SOT-666)



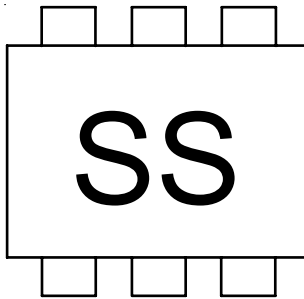
DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.057)	(1.45)
P	.020	0.50
G	.024	0.60
X	.012	0.30
Y	.033	0.85
Z	.090	2.30

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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Marking Code



Ordering Information

Part Number	Working Voltage	Device Marking	Qty per Reel	Reel Size
uClamp3304A.TCT	3.3V	SS	3,000	7 Inch

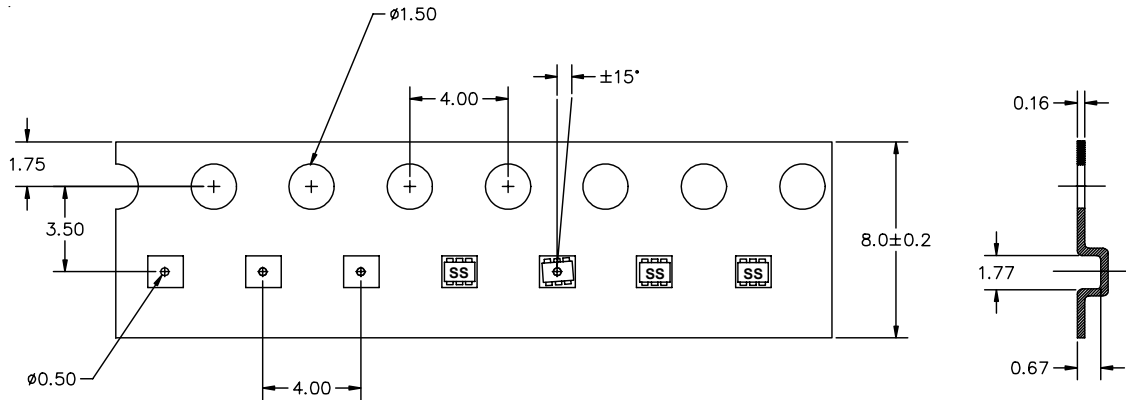
Note: Lead finish is lead-free matte tin

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Note:

(1) Device is symmetrical so there is no pin 1 identifier

Tape and Reel Specification



- DIMENSIONS ARE IN MILLIMETERS.
- SAME AS 3M US046041.

Tape Specifications and Device Orientation

Contact Information

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 Protection Products Division
 200 Flynn Rd., Camarillo, CA 93012
 Phone: (805)498-2111 FAX (805)498-3804

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