

CBTL04083A; CBTL04083B

3.3 V, 4 differential channel, 2 : 1 multiplexer/demultiplexer switch for PCI Express Gen3

Rev. 4 — 25 June 2012

Product data sheet

1. General description

CBTL04083A/B is a 4 differential channel, 2-to-1 multiplexer/demultiplexer switch for PCI Express Generation 3 (Gen3) applications. The CBTL04083A/B can switch four differential signals to one of two locations. Using a unique design technique, NXP has minimized the impedance of the switch such that the attenuation observed through the switch is negligible, and also minimized the channel-to-channel skew as well as channel-to-channel crosstalk, as required by the high-speed serial interface. CBTL04083A/B allows expansion of existing high speed ports for extremely low power.

The device's pin out are optimized to match different application layouts. CBTL04083A has input and output pins on the opposite of the package, and is suitable for edge connector(s) with different signal sources on the motherboard. CBTL04083B has outputs on both sides of the package, and the device can be placed between two connectors to multiplex differential signals from a controller. Please refer to [Section 8](#) for layout examples.

2. Features and benefits

- 4 differential channel, 2 : 1 multiplexer/demultiplexer
- High-speed signal switching for 8.0 Gbit/s PCIe Gen3 speed
- Low intra-pair skew: 5 ps typical
- Low inter-pair skew: 35 ps maximum
- High bandwidth:
 - ◆ –3 dB at 8.3 GHz for CBTL04083A
 - ◆ –3 dB at 8.0 GHz for CBTL04083B
- Low crosstalk: –29 dB at 4 GHz
- Low insertion loss
 - ◆ –0.5 dB at 100 MHz
 - ◆ –1.3 dB at 4 GHz
- Low off-state isolation: –20 dB at 4 GHz
- Low return loss: –14 dB at 4 GHz
- V_{DD} operating range: 3.3 V \pm 10 %
- Dual shutdown pins for channel 0/1 and 2/3 independently to minimize power consumption
- ESD tolerance:
 - ◆ 2000 V HBM
 - ◆ 1000 V CDM
- HVQFN42 package



3. Applications

- Routing of high-speed differential signals with low signal attenuation
 - ◆ PCIe Gen3
 - ◆ DisplayPort 1.2
 - ◆ USB 3.0
 - ◆ SATA 6 Gbit/s

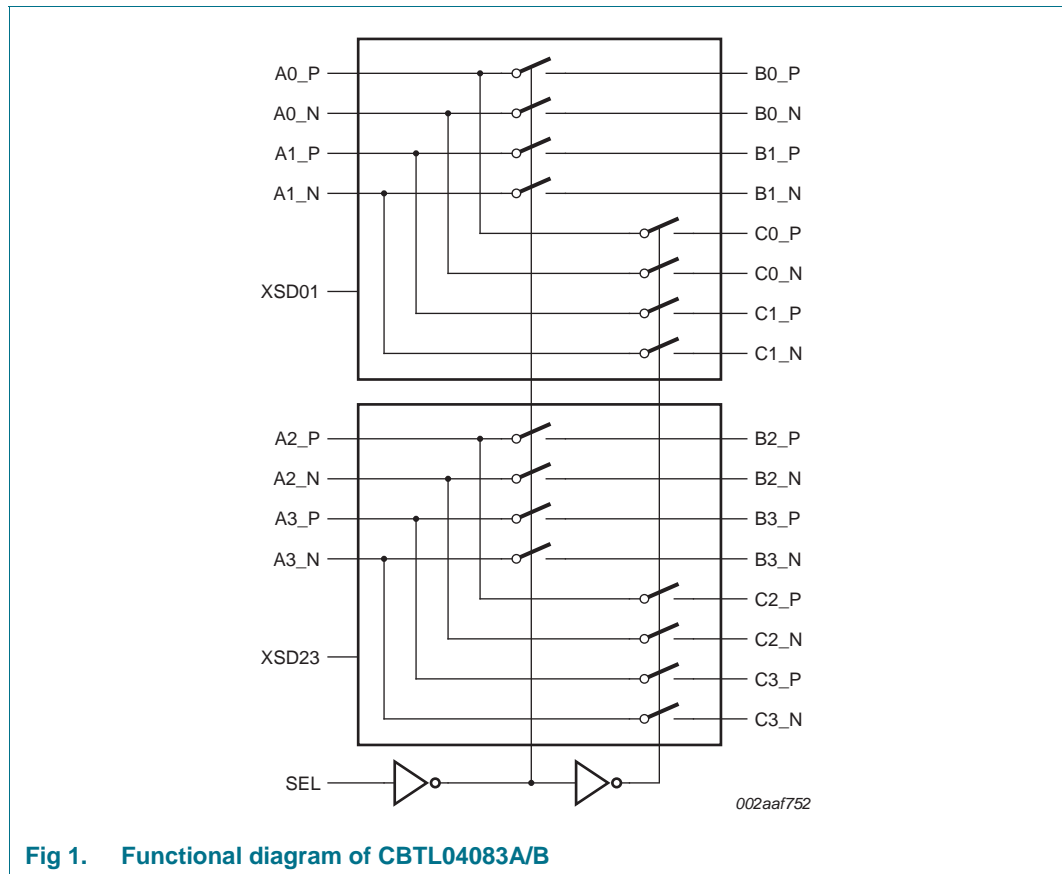
4. Ordering information

Table 1. Ordering information

| Type number | Package | | |
|-----------------------------|---------|---|-----------|
| | Name | Description | Version |
| CBTL04083ABS ^[1] | HVQFN42 | plastic thermal enhanced very thin quad flat package; no leads; 42 terminals; body 3.5 × 9 × 0.85 mm ^[3] | SOT1144-1 |
| CBTL04083BBS ^[2] | HVQFN42 | plastic thermal enhanced very thin quad flat package; no leads; 42 terminals; body 3.5 × 9 × 0.85 mm ^[3] | SOT1144-1 |

- [1] CBTL04083ABS is available in tape and reel formats with different tape widths — 16 mm and 24 mm:
For 16 mm tape width, order CBTL04083ABS 9352 941 24518 ("518" indicates 16 mm wide carrier tape).
For 24 mm tape width, order CBTL04083ABS 9352 941 24558 ("558" indicates 24 mm wide carrier tape).
- [2] CBTL04083BBS is available in tape and reel formats with different tape widths — 16 mm and 24 mm:
For 16 mm tape width, order CBTL04083BBS 9352 941 25518 ("518" indicates 16 mm wide carrier tape).
For 24 mm tape width, order CBTL04083BBS 9352 941 25558 ("558" indicates 24 mm wide carrier tape).
- [3] Total height after printed-circuit board mounting = 1.0 mm maximum.

5. Functional diagram



6. Pinning information

6.1 Pinning

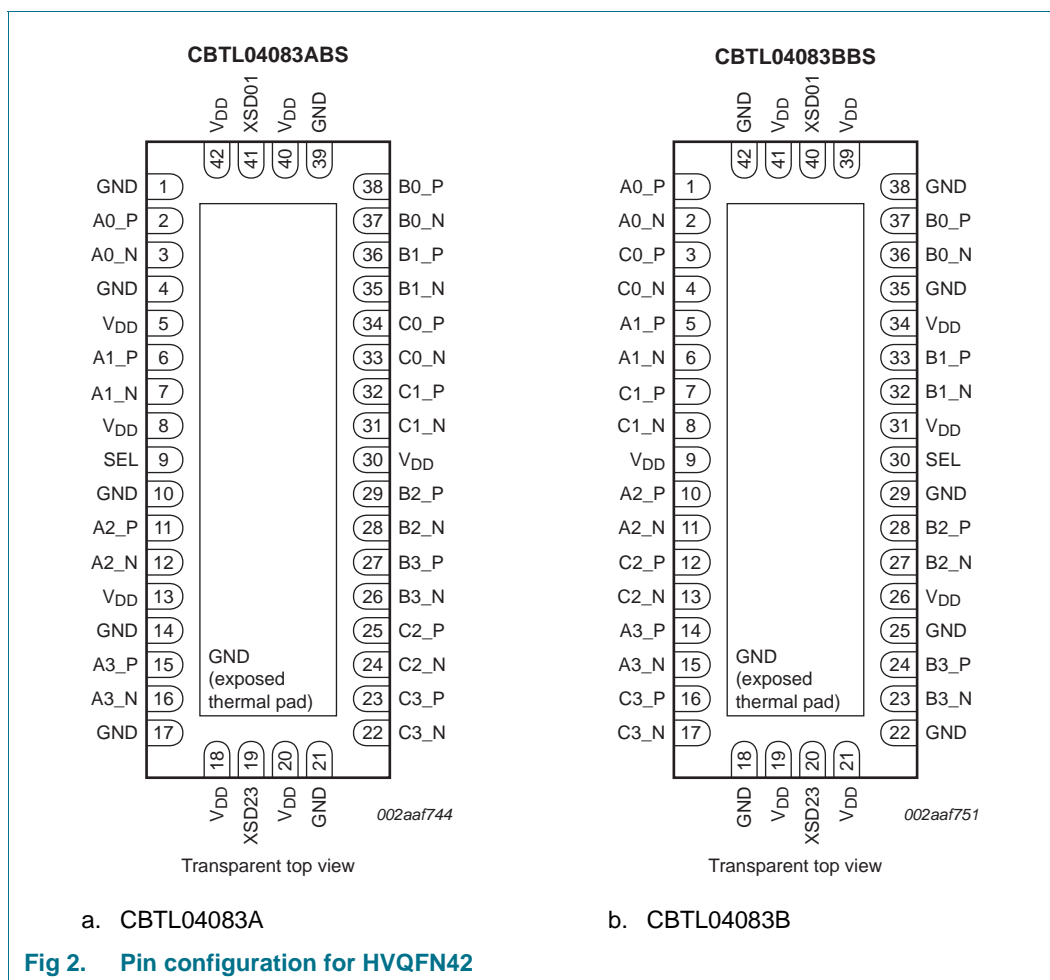


Fig 2. Pin configuration for HVQFN42

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | | Type | Description |
|--------|------------|------------|------|--|
| | CBTL04083A | CBTL04083B | | |
| A0_P | 2 | 1 | I/O | channel 0, port A differential signal input/output |
| A0_N | 3 | 2 | I/O | |
| A1_P | 6 | 5 | I/O | channel 1, port A differential signal input/output |
| A1_N | 7 | 6 | I/O | |
| A2_P | 11 | 10 | I/O | channel 2, port A differential signal input/output |
| A2_N | 12 | 11 | I/O | |
| A3_P | 15 | 14 | I/O | channel 3, port A differential signal input/output |
| A3_N | 16 | 15 | I/O | |

Table 2. Pin description ...continued

| Symbol | Pin | | Type | Description |
|--------------------|--------------------------------------|--|----------------------------|--|
| | CBTL04083A | CBTL04083B | | |
| B0_P | 38 | 37 | I/O | channel 0, port B differential signal input/output |
| B0_N | 37 | 36 | I/O | |
| B1_P | 36 | 33 | I/O | channel 1, port B differential signal input/output |
| B1_N | 35 | 32 | I/O | |
| B2_P | 29 | 28 | I/O | channel 2, port B differential signal input/output |
| B2_N | 28 | 27 | I/O | |
| B3_P | 27 | 24 | I/O | channel 3, port B differential signal input/output |
| B3_N | 26 | 23 | I/O | |
| C0_P | 34 | 3 | I/O | channel 0, port C differential signal input/output |
| C0_N | 33 | 4 | I/O | |
| C1_P | 32 | 7 | I/O | channel 1, port C differential signal input/output |
| C1_N | 31 | 8 | I/O | |
| C2_P | 25 | 12 | I/O | channel 2, port C differential signal input/output |
| C2_N | 24 | 13 | I/O | |
| C3_P | 23 | 16 | I/O | channel 3, port C differential signal input/output |
| C3_N | 22 | 17 | I/O | |
| SEL | 9 | 30 | CMOS single-ended input | operation mode select SEL = LOW: A → B SEL = HIGH: A → C |
| XSD01 | 41 | 40 | CMOS single-ended input | Shutdown pin; should be driven LOW or connected to GND for normal operation. When HIGH, channel 0 and channel 1 are switched off (non-conducting high-impedance state), and supply current consumption is minimized. |
| XSD23 | 19 | 20 | CMOS single-ended input | Shutdown pin; should be driven LOW or connected to GND for normal operation. When HIGH, channel 2 and channel 3 are switched off (non-conducting high-impedance state), and supply current consumption is minimized. |
| V _{DD} | 5, 8, 13, 18, 20, 30, 40, 42 | 9, 19, 21, 26, 31, 34, 39, 41 | power | positive supply voltage, 3.3 V ± 10 % |
| GND ^[1] | 1, 4, 10, 14, 17, 21, 39, center pad | 18, 22, 25, 29, 35, 38, 42, center pad | ground | supply ground |

[1] HVQFN32 package die supply ground is connected to both GND pins and exposed center pad. GND pins and the exposed center pad must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer to [Figure 1 “Functional diagram of CBTL04083A/B”](#).

7.1 Function selection

Table 3. Function selection

X = Don't care.

| XSD01 | XSD23 | SEL | Function |
|-------|-------|------|---|
| HIGH | - | X | An, Bn and Cn pins are high-Z, n = 0, 1 |
| LOW | - | LOW | An to Bn, n = 0, 1 |
| LOW | - | HIGH | An to Cn, n = 0, 1 |
| - | HIGH | X | An, Bn and Cn pins are high-Z, n = 2, 3 |
| - | LOW | LOW | An to Bn, n = 2, 3 |
| - | LOW | HIGH | An to Cn, n = 2, 3 |

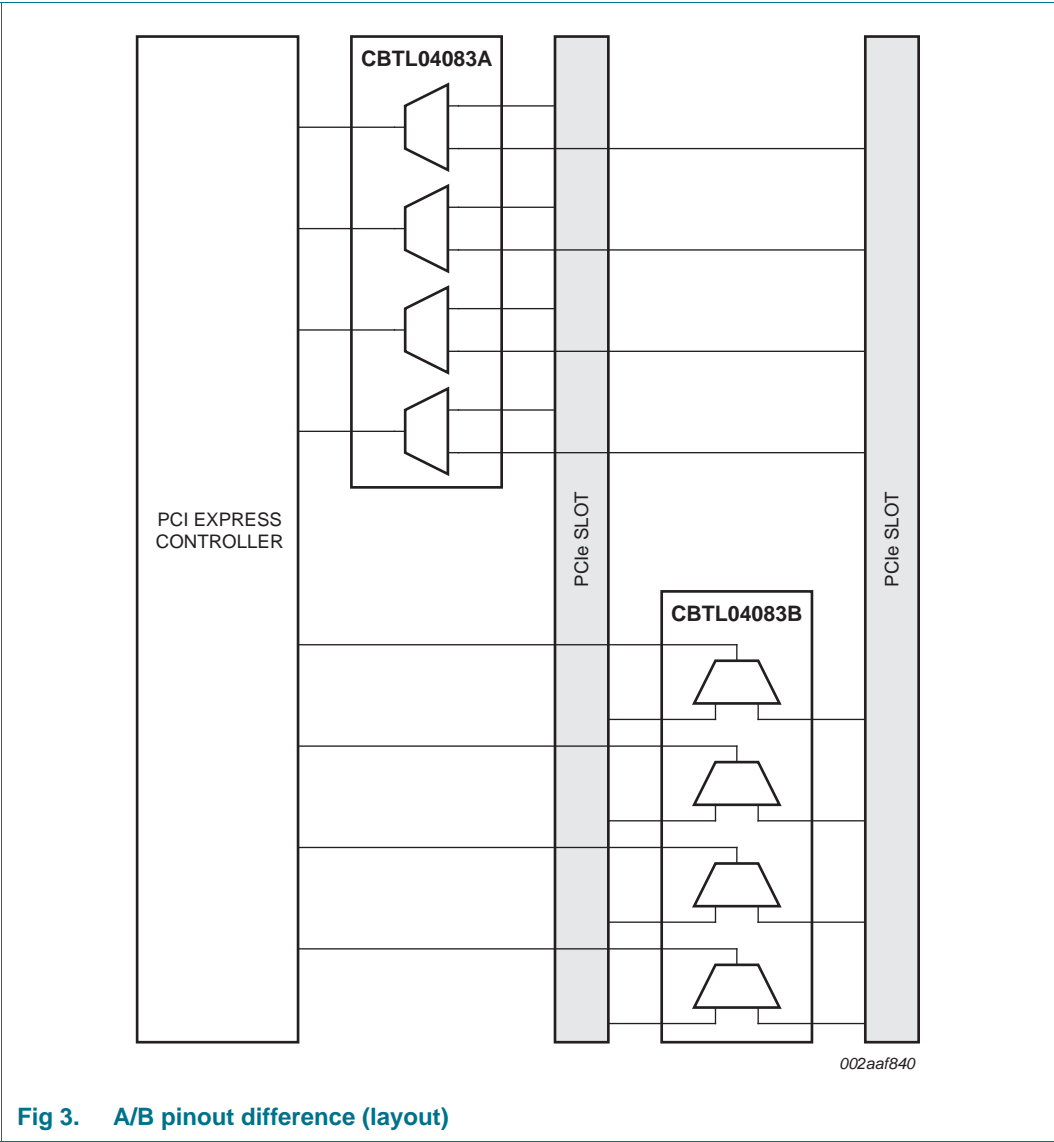
7.2 Shutdown function

The CBTL04083A/B provides a shutdown function to minimize power consumption when the application is not active, but power to the CBTL04083A/B is provided. Pin XSD01 and XSD23 (active HIGH) puts channel 0/1 and 2/3 (respectively) in high-impedance state (non-conducting) while reducing current consumption to near-zero.

Table 4. Shutdown function

| XSD01 | XSD23 | Channel 0 | Channel 1 | Channel 2 | Channel 3 |
|-------|-------|-----------|-----------|-----------|-----------|
| HIGH | - | high-Z | high-Z | - | - |
| LOW | - | active | active | - | - |
| - | HIGH | - | - | high-Z | high-Z |
| - | LOW | - | - | active | active |

8. Application design-in information



9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|---------------------------------|------------|-------|------|------|
| V_{DD} | supply voltage | | -0.3 | +4.6 | V |
| T_{case} | case temperature | | -40 | +85 | °C |
| V_{ESD} | electrostatic discharge voltage | HBM | [1] - | 2000 | V |
| | | CDM | [2] - | 1000 | V |

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

10. Recommended operating conditions

Table 6. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---------------------|-----------------------|-----|-----|----------|------|
| V_{DD} | supply voltage | | 3.0 | 3.3 | 3.6 | V |
| V_I | input voltage | | - | - | V_{DD} | V |
| T_{amb} | ambient temperature | operating in free air | -40 | - | +85 | °C |

11. Static characteristics

Table 7. Static characteristics

$V_{DD} = 3.3\text{ V} \pm 10\%$; $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|----------|----------------------------|---|--------------|--------------------|------------------------|------|
| I_{DD} | supply current | operating mode (both XSD01 and XSD23 are LOW); $V_{DD} = \text{max.}$ | - | 2.7 | 5 | mA |
| | | shutdown mode (both XSD01 and XSD23 are HIGH); $V_{DD} = \text{max.}$ | - | - | 1 | μA |
| I_{IH} | HIGH-level input current | $V_{DD} = \text{max.}; V_I = V_{DD}$ | - | - | ± 5 ^[2] | μA |
| I_{IL} | LOW-level input current | $V_{DD} = \text{max.}; V_I = \text{GND}$ | - | - | ± 5 ^[2] | μA |
| V_{IH} | HIGH-level input voltage | SEL, XSD01, XSD23 pins | $0.65V_{DD}$ | - | - | V |
| V_{IL} | LOW-level input voltage | SEL, XSD01, XSD23 pins | -0.5 | - | $0.35V_{DD}$ | V |
| V_I | input voltage | differential pins | - | - | 2.4 | V |
| | | SEL, XSD01, XSD23 pins | - | - | V_{DD} | V |
| V_{IC} | common-mode input voltage | | 0 | - | 2 | V |
| V_{ID} | differential input voltage | peak-to-peak | - | - | 1.6 | V |

[1] Typical values are at $V_{DD} = 3.3\text{ V}$, $T_{amb} = 25\text{ °C}$, and maximum loading.

[2] Input leakage current is $\pm 50\text{ μA}$ if differential pairs are pulled to HIGH and LOW.

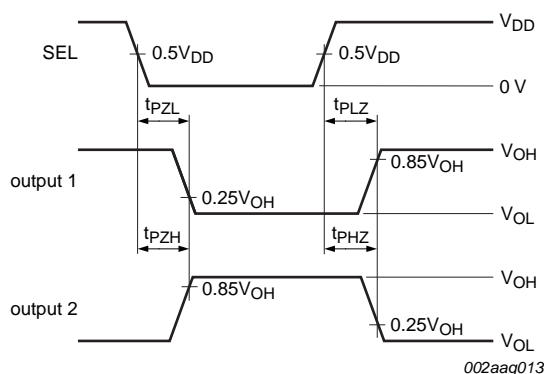
12. Dynamic characteristics

Table 8. Dynamic characteristics

$V_{DD} = 3.3\text{ V} \pm 10\%$; $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|----------------------------------|-------------------------------------|--|-----|--------------------|-----|----------|
| DDNEXT | differential near-end crosstalk | adjacent channels are ON | | | | |
| | | f = 4 GHz | - | -29 | - | dB |
| | | f = 100 MHz | - | -45 | - | dB |
| DDIL | differential insertion loss | channel is OFF | | | | |
| | | f = 4 GHz | - | -20 | - | dB |
| | | f = 100 MHz | - | -50 | - | dB |
| | | channel is ON | | | | |
| | | f = 4 GHz | - | -1.3 | - | dB |
| | | f = 100 MHz | - | -0.5 | - | dB |
| DDRRL | differential return loss | f = 4 GHz | | -14 | | dB |
| | | f = 100 MHz | - | -24 | - | dB |
| R _{on} | ON-state resistance | $V_{DD} = 3.3\text{ V}$; $V_I = 2\text{ V}$; $I_I = 19\text{ mA}$ | - | 6 | - | Ω |
| C _{io(on)} | on-state input/output capacitance | | - | 1.5 | - | pF |
| B _{-3dB} | -3 dB bandwidth | CBTL04083A | - | 8.3 | - | GHz |
| | | CBTL04083B | - | 8.0 | - | GHz |
| t _{PD} | propagation delay | from left-side port to right-side port, or vice versa | - | 60 | - | ps |
| Switching characteristics | | | | | | |
| t _{startup} | start-up time | supply voltage valid or XSD01/XSD23 going LOW to channel specified operating characteristics | - | - | 10 | ms |
| t _{PZH} | OFF-state to HIGH propagation delay | | - | - | 300 | ns |
| t _{PZL} | OFF-state to LOW propagation delay | | - | - | 70 | ns |
| t _{PHZ} | HIGH to OFF-state propagation delay | | - | - | 50 | ns |
| t _{PLZ} | LOW to OFF-state propagation delay | | - | - | 50 | ns |
| t _{sk(dif)} | differential skew time | intra-pair | - | 5 | - | ps |
| t _{sk} | skew time | inter-pair | - | - | 35 | ps |

[1] Typical values are at $V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$, and maximum loading.



Output 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.

Output 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

The outputs are measured one at a time with one transition per measurement.

Fig 4. Voltage waveforms for enable and disable times

13. Test information

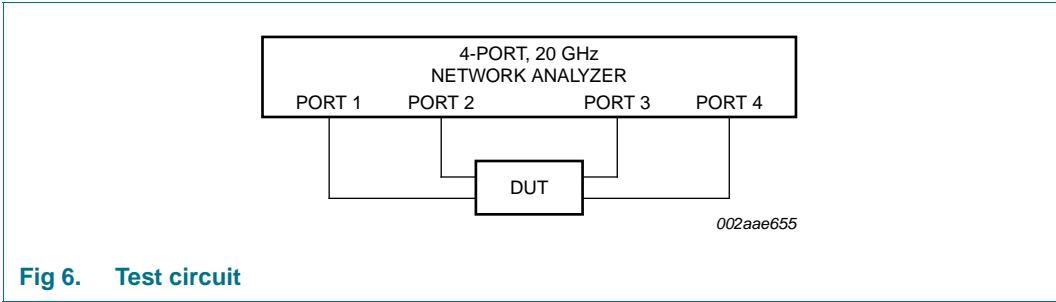
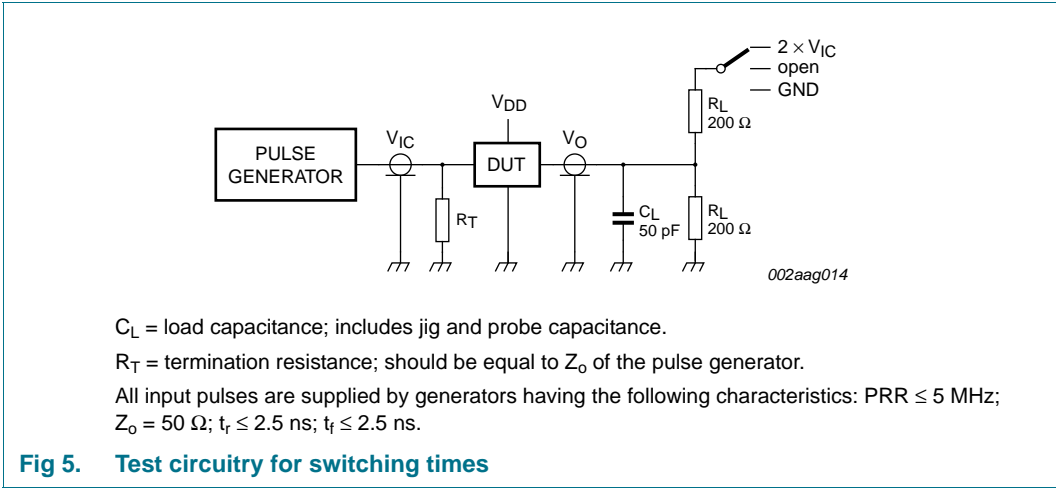


Table 9. Test data

| Test | Load | | Switch |
|--|-------|--------------|-------------------|
| | C_L | R_L | |
| t_{PLZ} , t_{PZL} (output on B side) | 50 pF | 200 Ω | $2 \times V_{IC}$ |
| t_{PHZ} , t_{PZH} (output on B side) | 50 pF | 200 Ω | GND |
| t_{PD} | - | 200 Ω | open |

14. Package outline

HVQFN42: plastic thermal enhanced very thin quad flat package; no leads;
 42 terminals; body 3.5 x 9 x 0.85 mm

SOT1144-1

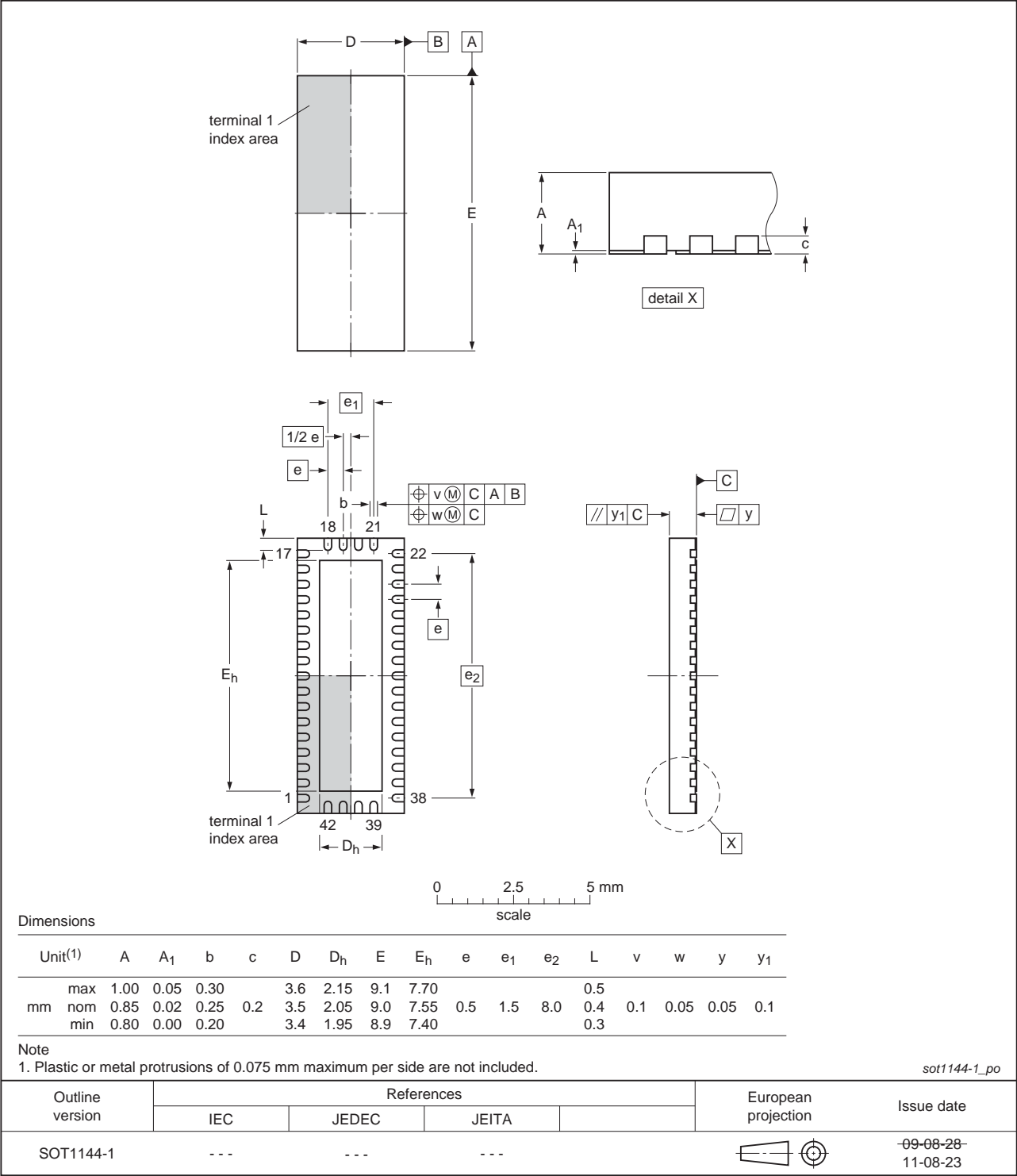


Fig 7. Package outline SOT1144-1 (HVQFN42)

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 8](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 10](#) and [11](#)

Table 10. SnPb eutectic process (from J-STD-020C)

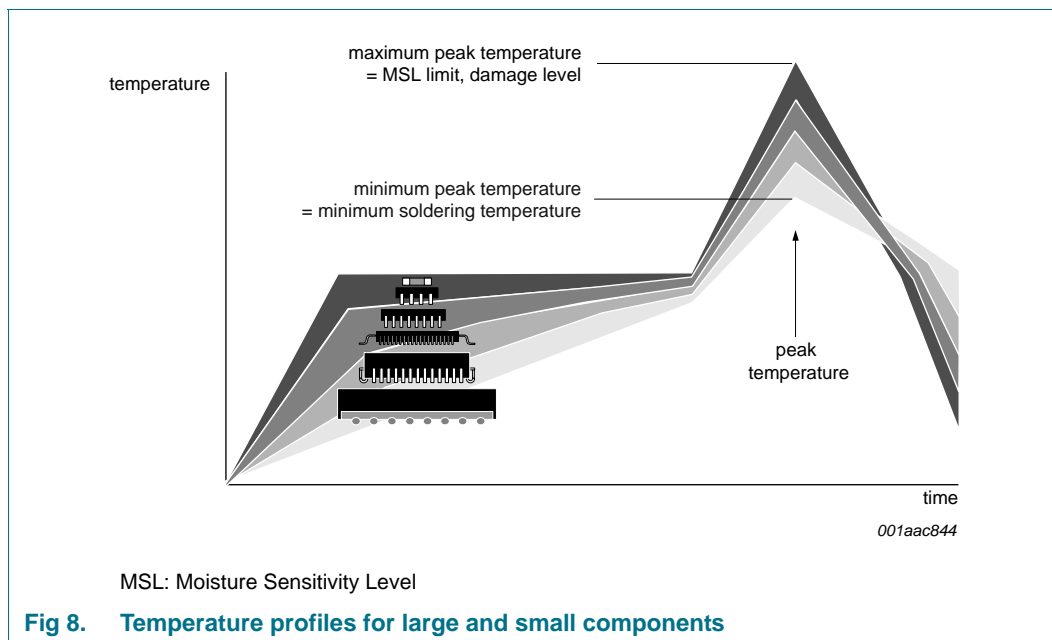
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 11. Lead-free process (from J-STD-020C)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 8](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

16. Abbreviations

Table 12. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged-Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| I/O | Input/Output |
| PCI | Peripheral Component Interconnect |
| PCIe | PCI express |
| PRR | Pulse Repetition Rate |
| SATA | Serial Advanced Technology Attachment |
| USB | Universal Serial Bus |

17. Revision history

Table 13. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--|--------------|--------------------|---------------|---------------------------|
| CBTL04083A_CBTL04083B v.4 | 20120625 | Product data sheet | - | CBTL04083A_CBTL04083B v.3 |
| Modifications: <ul style="list-style-type: none"> • Section 2 "Features and benefits": <ul style="list-style-type: none"> – sixth bullet changed from "–35 dB" to "–29 dB" – ninth bullet changed from "–20 dB" to "–14 dB" • Table 1 "Ordering information": <ul style="list-style-type: none"> – added (new) Table note [1] – added (new) Table note [2] • Table 2 "Pin description", last table row: GND "Type" changed from "power" to "ground" • Table 8 "Dynamic characteristics": <ul style="list-style-type: none"> – DDNEXT (condition "f = 4 GHz") typical value changed from "–35 dB" to "–29 dB" – DDRL (condition "f = 4 GHz") typical value changed from "–20 dB" to "–14 dB" – DDRL (condition "f = 100 MHz") typical value changed from "–25 dB" to "–24 dB" | | | | |
| CBTL04083A_CBTL04083B v.3 | 20110824 | Product data sheet | - | CBTL04083A_CBTL04083B v.2 |
| CBTL04083A_CBTL04083B v.2 | 20110524 | Product data sheet | - | CBTL04083A_CBTL04083B v.1 |
| CBTL04083A_CBTL04083B v.1 | 20110228 | Product data sheet | - | - |

18. Legal information

18.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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