

MOSFETs Silicon N-channel MOS (U-MOSIX-H)

TPH1R405PL

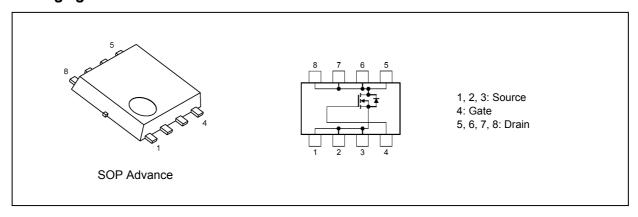
1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators
- · Motor Drivers

2. Features

- (1) High-speed switching
- (2) Small gate charge: $Q_{SW} = 22 \text{ nC (typ.)}$
- (3) Small output charge: $Q_{oss} = 67 \text{ nC (typ.)}$
- (4) Low drain-source on-resistance: $R_{DS(ON)} = 1 \text{ m}\Omega$ (typ.) ($V_{GS} = 10 \text{ V}$)
- (5) Low leakage current: $I_{DSS} = 10 \mu A \text{ (max) (V}_{DS} = 45 \text{ V)}$
- (6) Enhancement mode: V_{th} = 1.4 to 2.4 V (V_{DS} = 10 V, I_{D} = 0.5 mA)

3. Packaging and Internal Circuit





4. Absolute Maximum Ratings (Note) (Ta = 25 °C unless otherwise specified)

Characteristics			Symbol	Rating	Unit
Drain-source voltage			V_{DSS}	45	V
Gate-source voltage			V_{GSS}	±20	
Drain current (DC)	(T _c = 25 °C)	(Note 1)	Ι _D	120	Α
Drain current (DC)	(Silicon limit)	(Note 1), (Note 2)	I_D	232	
Drain current (pulsed)	(t = 100 μs)	(Note 1)	I _{DP}	500	
Power dissipation	(T _c = 25 °C)		P_{D}	132	W
Power dissipation		(Note 3)	P_{D}	3	
Power dissipation		(Note 4)	P_{D}	0.96	
Single-pulse avalanche energy		(Note 5)	E _{AS}	114	mJ
Single-pulse avalanche current		(Note 5)	I _{AS}	120	Α
Channel temperature			T_ch	175	Ĵ
Storage temperature			T _{stg}	-55 to 175	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteristics			Symbol	Max	Unit
Channel-to-case thermal resistance	(T _c = 25 °C)		R _{th(ch-c)}	1.13	°C/W
Channel-to-ambient thermal resistance	(T _a = 25 °C)	(Note 3)	R _{th(ch-a)}	50	
Channel-to-ambient thermal resistance	(T _a = 25 °C)	(Note 4)	R _{th(ch-a)}	156	

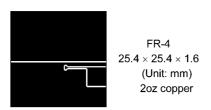
Note 1: Ensure that the channel temperature does not exceed 175 °C.

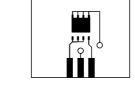
Note 2: Limited 120 A by package capability.

Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5: V_{DD} = 36 V, T_{ch} = 25 °C (initial), L = 6.1 μ H, I_{AS} =120 A





FR-4 $25.4 \times 25.4 \times 1.6$ (Unit: mm) 2oz copper

Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)

Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.



6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I _{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±0.1	μΑ
Drain cut-off current	I _{DSS}	V _{DS} = 45 V, V _{GS} = 0 V			10	
Drain-source breakdown voltage	V _{(BR)DSS}	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	45			V
Drain-source breakdown voltage (Note 6)	V _{(BR)DSX}	$I_D = 10 \text{ mA}, V_{GS} = -20 \text{ V}$	30			
Gate threshold voltage	V_{th}	V _{DS} = 10 V, I _D = 0.5 mA	1.4	_	2.4	
Drain-source on-resistance	R _{DS(ON)}	$V_{GS} = 4.5 \text{ V}, I_D = 50 \text{ A}$	_	1.6	2.3	mΩ
		V_{GS} = 10 V, I_{D} = 50 A		1	1.4	

Note 6: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	V _{DS} = 22.5 V, V _{GS} = 0 V, f = 1 MHz	_	4830	6300	pF
Reverse transfer capacitance	C _{rss}		_	66	122	
Output capacitance	C _{oss}		_	1210	_	
Gate resistance	r _g	_	_	0.37	1	Ω
Switching time (rise time)	t _r	See Fig. 6.2.1	_	11	_	ns
Switching time (turn-on time)	t _{on}		_	27	_	
Switching time (fall time)	t _f		_	21	_	
Switching time (turn-off time)	t _{off}		_	70	_	

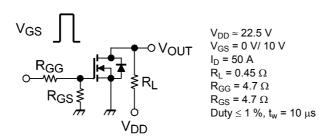


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus	Q_g	$V_{DD} \approx 22.5 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$	_	74	1	nC
gate-drain)		$V_{DD} \approx 22.5 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 50 \text{ A}$	_	36		
Gate-source charge 1	Q _{gs1}	$V_{DD} \approx 22.5 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$	_	18		
Gate-drain charge	Q_{gd}		_	13		
Gate switch charge	Q_{SW}		_	22	_	
Output charge	Q _{oss}	V _{DS} = 22.5 V, V _{GS} = 0 V, f = 1 MHz	_	67		

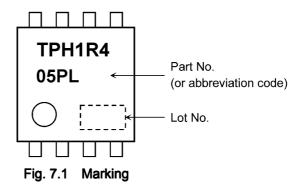


6.4. Source-Drain Characteristics ($T_a = 25$ °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Reverse drain current (pulsed) (Note 7)	I _{DRP}	(t = 100 μs)	_	_	500	Α
Diode forward voltage	V _{DSF}	I _{DR} = 120 A, V _{GS} = 0 V	1	_	-1.2	V
Reverse recovery time	t _{rr}	V _R = 22.5 V, I _{DR} = 30 A,	-	49	_	ns
Reverse recovery charge	Q _{rr}	$V_{GS} = 0 \text{ V}, -dI_{DR}/dt = 100 \text{ A/}\mu\text{s}$	1	54	_	nC

Note 7: Ensure that the channel temperature does not exceed 175 $^{\circ}\text{C}$.

7. Marking



8. Characteristics Curves (Note)

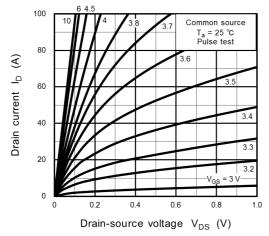
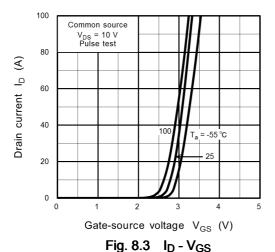


Fig. 8.1 I_D - V_{DS}



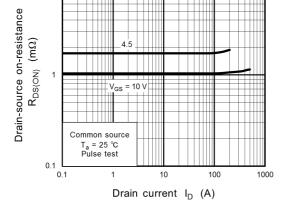


Fig. 8.5 R_{DS(ON)} - I_D

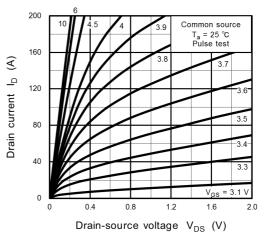


Fig. 8.2 I_D - V_{DS}

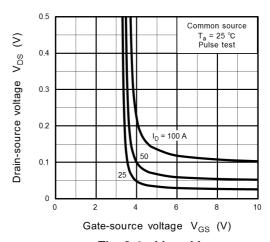


Fig. 8.4 V_{DS} - V_{GS}

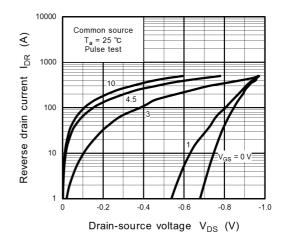


Fig. 8.6 IDR - VDS

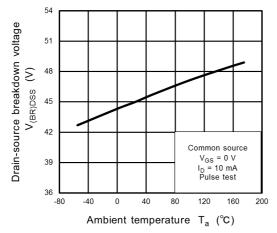


Fig. 8.7 V_{(BR)DSS} - T_a

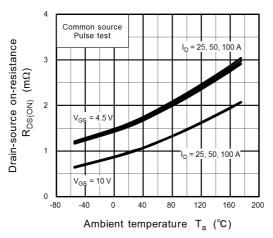


Fig. 8.9 R_{DS(ON)} - T_a

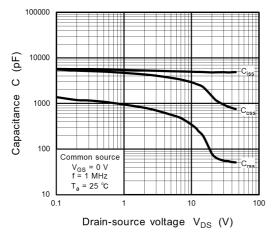


Fig. 8.11 Capacitance - V_{DS}

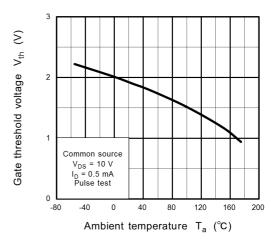


Fig. 8.8 V_{th} - T_a

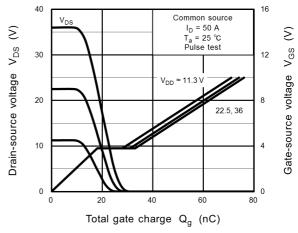


Fig. 8.10 Dynamic Input/Output Characteristics

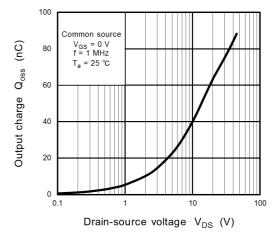


Fig. 8.12 Qoss - VDS

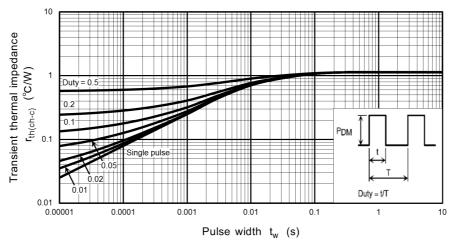


Fig. 8.13 r_{th} - t_w (Guaranteed Maximum)

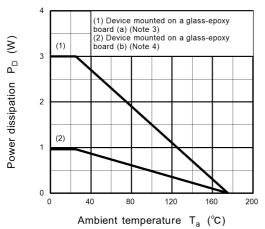


Fig. 8.14 P_D - T_a (Guaranteed Maximum)

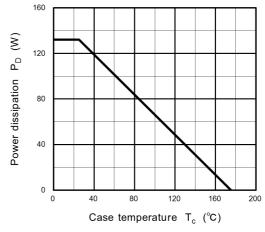


Fig. 8.15 P_D - T_c (Guaranteed Maximum)

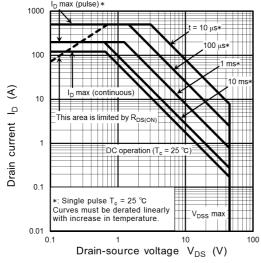


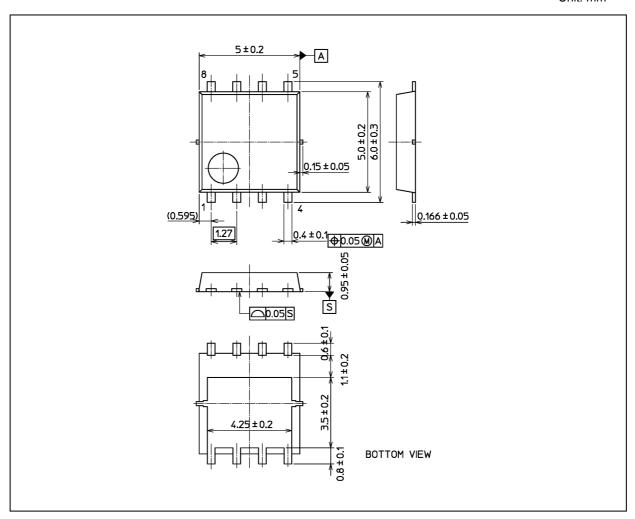
Fig. 8.16 Safe Operating Area (Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 0.069 g (typ.)

F	Package Name(s)
TOSHIBA: 2-5Q1S	
Nickname: SOP Advance	



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