Data Sheet October 6, 2011 FN9131.7

High Voltage ORing MOSFET Controller

The ISL6144 ORing MOSFET Controller and a suitably sized N-Channel power MOSFET(s) increases power distribution efficiency and availability when replacing a power ORing diode in high current applications.

In a multiple supply, fault tolerant, redundant power distribution system, paralleled similar power supplies contribute equally to the load current through various power sharing schemes. Regardless of the scheme, a common design practice is to include discrete ORing power diodes to protect against reverse current flow should one of the power supplies develop a catastrophic output short to ground. In addition, reverse current can occur if the current sharing scheme fails and an individual power supply voltage falls significantly below the others.

Although the discrete ORing diode solution has been used for some time and is inexpensive to implement, it has some drawbacks. The primary downside is the increased power dissipation loss in the ORing diodes as power requirements for systems increase. Another disadvantage when using an ORing diode would be failure to detect a shorted or open ORing diode, jeopardizing power system reliability. An open diode reduces the system to single point of failure while a diode short might pose a hazard to technical personnel servicing the system while unaware of this failure.

The ISL6144 can be used in 9V to 75V systems having similar power sources and has an internal charge pump to provide a floating gate drive for the N-Channel ORing MOSFET. The High Speed (HS) Comparator protects the common bus from individual power supply shorts by turning off the shorted feed's ORing MOSFET in less than 300ns and ensuring low reverse current.

An external resistor-programmable detection level for the HS Comparator allows users to set the N-Channel MOSFET "V_{OUT} - V_{IN}" trip point to adjust control sensitivity to power supply noise.

The Hysteretic Regulating (HR) Amplifier provides a slow turn-off of the ORing MOSFET. This turn-off is achieved in less than 100µs when one of the sourcing power supplies is shutdown slowly for system diagnostics, ensuring zero reverse current. This slow turn-off mechanism also reacts to output voltage droop, degradation, or power-down.

An open drain $\overline{FAULT}$ pin will indicate that a fault has occurred. The fault detection circuitry covers different types of failures; including dead short in the sourcing supply, a short of any two ORing MOSFET terminals, or a blown fuse in the power distribution path.

Features

- Wide Supply Voltage Range +9V to +75V
- Transient Rating to +100V
- Reverse Current Fault Isolation
- Internal Charge Pump Allows the use of N-Channel MOSFET
- HS Comparator Provides Very Fast <0.3µs Response Time to Dead Shorts on Sourcing Supply. HS Comparator also has Resistor-adjustable Trip Level
- HR Amplifier allows Quiet, <100µs MOSFET Turn-off for Power Supply Slow Shut Down
- Open Drain, Active Low Fault Output with 120µs Delay
- Provided in Packages Compliant to UL60950 (UL1950) Creepage Requirements
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free (RoHS Compliant)

Applications

- ORing MOSFET Control in Power Distribution Systems
- N + 1 Redundant Distributed Power Systems
- File and Network Servers (12V and 48V)
- Telecom/Datacom Systems

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information

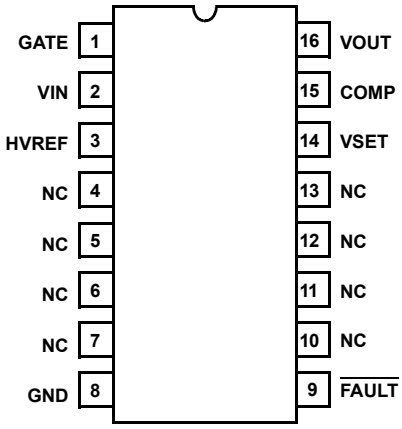
PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6144IVZA (Note 1)	ISL61 44IVZ	-40 to +105	16 Ld TSSOP	M16.173
ISL6144IRZA (Note 1)	ISL6144 IRZ	-40 to +105	20 Ld 5x5 QFN	L20.5x5
ISL6441EVAL1Z	Evaluation Platform			

NOTES:

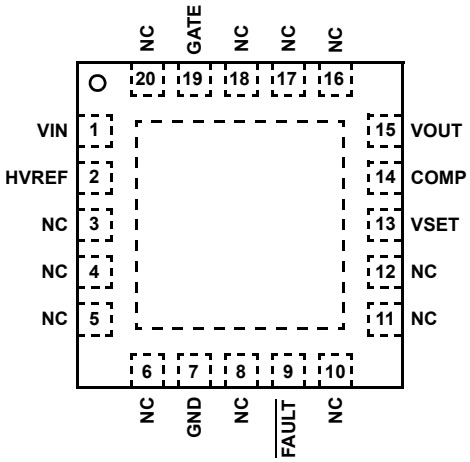
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6144. For more information on MSL please see techbrief TB363.

Pinouts

ISL6144
(16 LD TSSOP)
TOP VIEW



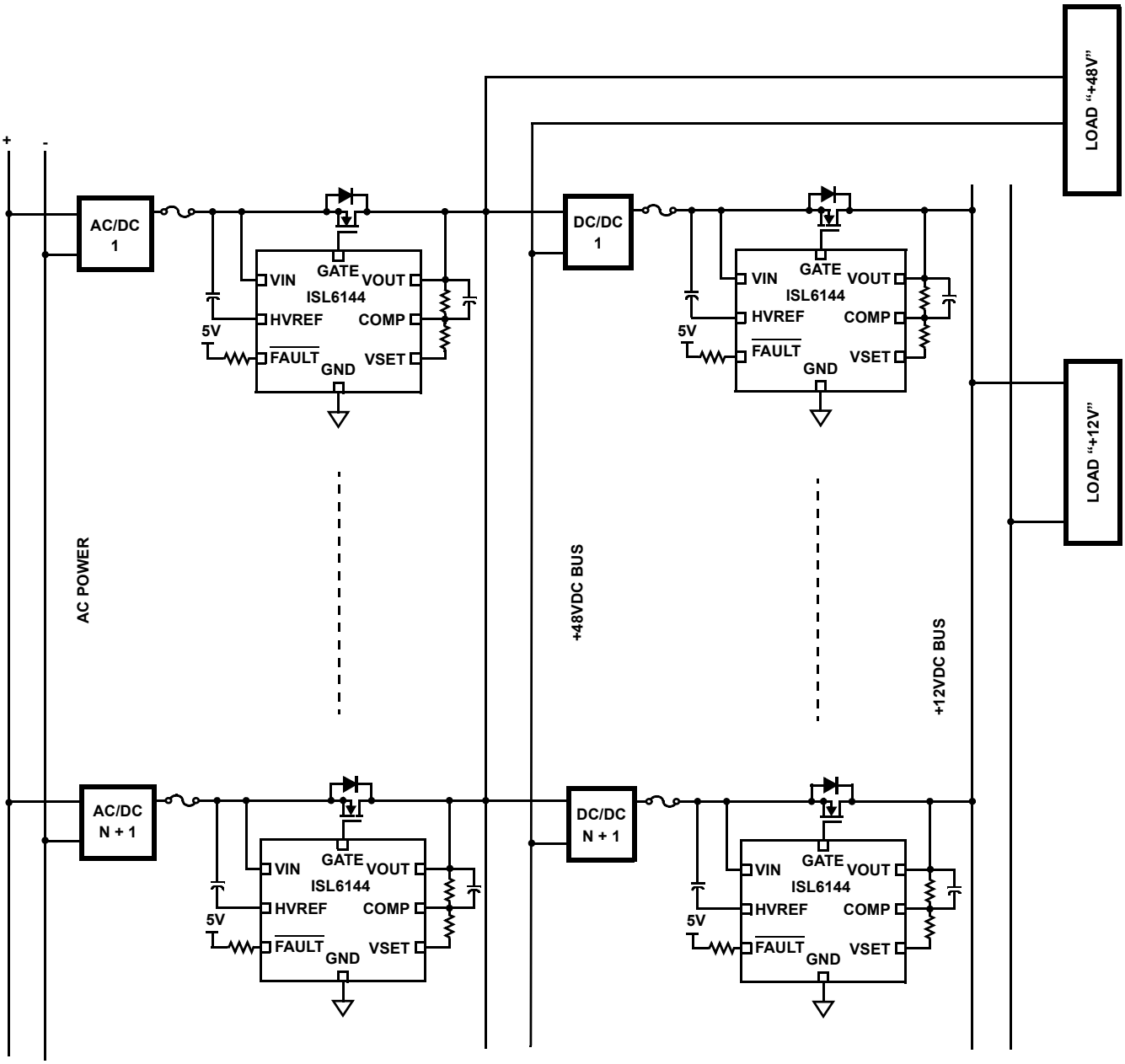
ISL6144
(20 LD 5x5 QFN)
TOP VIEW



Pin Descriptions

TSSOP PIN #	QFN PIN #	SYMBOL	FUNCTION	DESCRIPTION
1	19	GATE	External FET Gate Drive	Allows active control of external N-Channel FET gate to perform ORing function.
2	1	VIN	Power Supply Connection	Chip bias input. Also provides a sensing node for external FET control.
3	2	HVREF	Chip High Voltage Reference	Low side of floating high voltage reference for all of the HV chip circuitry.
8	7	GND	Chip Ground Reference	Chip ground reference point.
9	9	$\overline{\text{FAULT}}$	Fault Output	Provides an open drain active low output as an indication that a fault has occurred: GATE is OFF (GATE < V_{IN} + 0.37V) or other types of faults resulting in V_{IN} - V_{OUT} > 0.41V.
14	13	VSET	Low Side Connection for Trip Level	Resistor connected to COMP provides adjustable "Vd - Vs" trip level along with pin COMP.
15	14	COMP	High Side Connection for HS Comparator Trip Level	Resistor connected to V_{OUT} provides sense point for the adjustable Vd - Vs trip level along with pin VSET.
16	15	VOUT	Chip Bias and Load Connection	Provides the second sensing node for external FET control and chip output bias.
4, 5, 6, 7, 10, 11, 12, 13	3, 4, 5, 6, 8, 10, 11, 12, 16, 17, 18, 20	NC	No Connection	

General Application Circuit

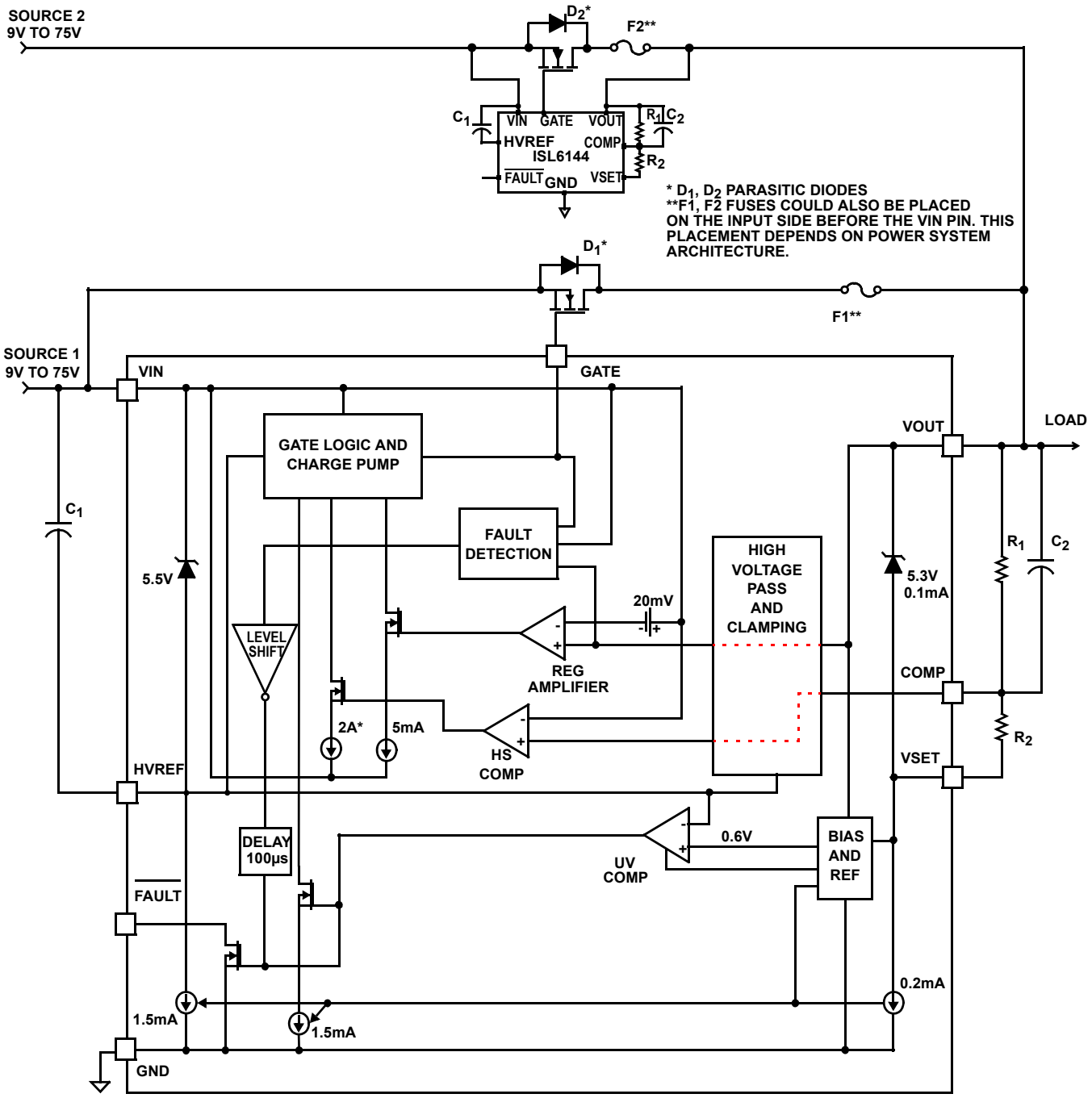


NOTES:

4. AC/DC 1 through (N + 1) are multistage AC/DC converters which include AC/DC rectification stage and a DC/DC Converter with a +48VDC output (also might include a Power Factor Correction stage).
5. DC/DC Converter 1 through (N + 1) are DC/DC converters to provide additional Intermediate Bus.
6. Load "+12V" and Load "+48V" might include other DC/DC converter stages to provide lower voltages such as ±15V, ±5V, +3.3V, +2.5V, +1.8V etc.
7. Fuse location might vary depending on power system architecture.

FIGURE 1. ISL6144 GENERAL APPLICATION CIRCUIT IN A DISTRIBUTED POWER SYSTEM

Simplified Block Diagram



Absolute Maximum Ratings (Note 8) T_A = +25°C

V_{IN}, V_{OUT} . . . . . -0.3V to +100V
GATE . . . . . -0.3V to V_{IN} +12V
HVREF. . . . . -0.3V to V_{IN} -5V
COMP . . . . . -0.3V to V_{OUT}
VSET . . . . . -0.3V to V_{OUT} -5V
FAULT . . . . . -0.3V to 16V
ESD Classification . . . . . Class 2

Operating Conditions

Supply Voltage Range . . . . . +9V to +75V
Temperature Range (T_A) . . . . . -40°C to +105°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TSSOP Package (Note 9)	90	N/A
QFN Package (Notes 10, 11)	35	5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

8. All voltages are relative to GND, unless otherwise specified.
9. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
10. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
11. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{IN} = 48V, T_A = -40°C to +105°C, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 12)	TYP	MAX (Note 12)	UNITS
BIAS “V_{IN}”						
POR Rising	POR_{L2H}	V_{IN} Rising to V_{GATE} > V_{IN} + 7.5V	**8.9**	-	-	V
12V Bias Current	I_{12V}	V_{IN} = 12V, V_{GATE} = V_{IN} + V_{GQP}	-	3.5	-	mA
48V Bias Current	I_{48V}	V_{IN} = 48V, V_{GATE} = V_{IN} + V_{GQP}	-	4.5	-	mA
75V Bias Current	I_{75V}	V_{IN} = 75V, V_{GATE} = V_{IN} + V_{GQP}	-	5	-	mA
GATE						
Charge Pump Voltage	V_{GQP}	V_{IN} = 12V to 75V	**V_{IN} + 9**	V_{IN} + 10.5	**V_{IN} + 12**	V
Gate Low Voltage Level	V_{GL}	V_{IN} - V_{OUT} < 0V	**-0.3**	V_{IN}	**V_{IN} + 0.5**	V
Low Pull Down Current	I_{PDL}	Cgs = 39nF, I_{PDL} = Cgs*dVgs/T_{tofs}	-	5	-	mA
High Pull Down Current	I_{PDH}	Cgs = 39nF, I_{PDH} = Cgs*dVgs/T_{toff}	-	2	-	A
Slow Turn-off Time	t_{toffs}	Cgs = 39nF	-	-	**100**	µs
Fast Turn-off Time	t_{toff}	Turn-off from V_{GATE} = V_{IN} + V_{GQP} to V_{IN} + 1V with Cgs = 39nF (includes HS Comparator delay time)	-	250	**300**	ns
Start-up “Turn-On” Time	t_{ON}	Turn-on from V_{GATE} = V_{IN} to V_{IN} + 7.5V into 39nF	-	1	-	ms
GATE Turn-On Current	I_{ON}	V_{IN} = 9V to 75V	-	1	-	mA
CONTROL AND REGULATION I/O						
HR Amplifier Forward Voltage Regulation	V_{FWD_HR}	ISL6144 controls voltage across FET Vds to V_{FWD_HR} during static forward operation at loads resulting in I * $r_{DS(ON)}$ < V_{FWD_HR}	**10**	20	**30**	mV
HS COMP Externally Programmable Threshold	$V_{TH(HS)}$	Externally programmable threshold for noise sensitivity (system dependent), typical 0.05V to 0.3V	**0**	0.05	**5.3**	V
HS Comparator Offset Voltage	$V_{OS(HS)}$		**-40**	0	**25**	mV
Comp Input Current (Bias Current)	I_{COMP}		-	1.1	-	µA
HVREF Voltage (V_{IN} - HVREF)	$HV_{REF(VZ)}$	V_{IN} = 9V to 75V	-	5.5	-	V

Electrical Specifications V_{IN} = 48V, T_A = -40°C to +105°C, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 12)	TYP	MAX (Note 12)	UNITS
VSET Voltage (V_{OUT} - VSET)	$V_{REF(VSET)}$	V_{IN} = 9V to 75V	-	5.3	-	V
$\overline{\text{Fault}}$ Low Output Voltage	V_{FLT_L}	V_{IN} - V_{OUT} < 0V, V_{GATE} = V_{GL}	-	-	**0.5**	V
$\overline{\text{Fault}}$ Sink Current	I_{FLT_SINK}	$\overline{FAULT}$ = V_{FLT_L}, V_{IN} < V_{OUT}, V_{GATE} = V_{GL}	**4**	-	-	mA
$\overline{\text{Fault}}$ Leakage Current	I_{FLT_LEAK}	$\overline{FAULT}$ = "V_{FLT_H}", V_{IN} > V_{OUT}, V_{GATE} = V_{IN} + V_{GQP}	-	-	**10**	µA
$\overline{\text{Fault}}$ Delay - Low to High	t_{FLT}	GATE = V_{GL} to $\overline{FAULT}$ = V_{FLT_L}	-	120	-	µs

NOTES:

12. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Functional Pin Descriptions

GATE

This is the Gate Drive output of the external N-Channel MOSFET generated by the IC internal charge pump. Gate turn-on time is typically 1ms.

VIN

Input bias pin connected to the sourcing supply side (ORing MOSFET Source). Also serves as the sense pin to determine the sourcing supply voltage. The ORing MOSFET will be turned off when VIN becomes lower than VOUT by a value more than the externally set threshold.

VOUT

Connected to the Load side (ORing MOSFET Drain). This is the VOUT sense pin connected to the load. This is the common connection point for multiple paralleled supplies. VOUT is compared to VIN to determine when the ORing FET has to be turned off.

HVREF

Low side of the internal IC High Voltage Reference used by internal circuitry, also available as an external pin for additional external capacitor connection.

COMP

This is the high side connection for the HS Comparator trip level setting ($V_{TH(HS)}$). Resistor R_1, connected between COMP and V_{OUT} along with resistor R_2, provides adjustable V_{OUT} - V_{IN} trip level (0V to 5V). This provides flexibility to externally set the desired level depending on particular system requirement.

VSET

Low side connection for the HS Comparator trip level setting A second resistor R_2 connected between VSET and COMP provides adjustable "V_{IN} - V_{OUT}" level along with R_1.

$\overline{\text{FAULT}}$

Open-Drain pull-down $\overline{FAULT}$ Output with internal on-chip filtering (t_{FLT}). The ISL6144 fault detection circuitry will pull-down this pin to GND as soon as it detects a fault. Different types of faults and their detection mechanisms are discussed in more detail in the "Functional Block Description" on page 6.

GND

IC ground reference.

Detailed Description

The ISL6144 and a suitably sized N-Channel power MOSFET(s) increases power distribution efficiency and availability when replacing a power ORing diode in high current applications. Refer to "Application Considerations" on page 8 for power saving when using ISL6144 with an N-channel ORing MOSFET compared to a typical ORing diode.

Functional Block Description

Regulating Amplifier-Slow (Quiet) Turn-off

A Hysteretic Regulating (HR) Amplifier is used for a Quiet/Slow turn-off mechanism. This slow turn-off is initiated when the sourcing power supply is turned off slowly for system diagnostics. Under normal operating conditions as V_{OUT} pulls up to 20mV below V_{IN} (V_{IN} - 20mV > V_{OUT}), the HR Amplifier regulates the gate voltage to keep the 20mV (V_{FWD_HR}) forward voltage drop across the ORing MOSFET (Vs - Vd). This will continue until the load current exceeds the MOSFET ability to deliver the current with Vsd of 20mV. In this case, Gate will be charged to the full charge pump voltage (V_{GQP}) to fully enhance the MOSFET. At this point, the MOSFET will be fully enhanced and behave as a constant resistor valued at the $r_{DS(ON)}$. Once V_{IN} starts to drop below V_{OUT}, regulation cannot be maintained and the output of the HR Amp is pulled high and the gate is pulled down to V_{IN} slowly in less than a 100µs. As a result, the ORing FET is turned off, avoiding reverse current as well as voltage and current stresses on supply components.

The slow turn-off is achieved in two stages. The first stage starts with a slow turn-off action and lasts for up to 20µs. The gate pull down current for the first stage is 2mA. The second slow turn-off stage completes the gate turn-off with a 10mA pull down current. The 20µs delay filters out any false trip off due to noise or glitches that might be present on the supply line.

The gate turn-on and gate turn-off drivers have a 50kHz filter to reduce the variation in FET forward voltage drop (and FET gate voltage) due to normal SMPS system switching noises (typically higher than 50kHz). These filters do not affect the total turn-on or slow turn-off times.

Special system design precautions must be taken to insure that no AC mains related low frequency noise will be present at the input or output of ISL6144. Filters and multiple power conversion stages, which are part of any distributed DC power system, normally filter out all such noise.

HS Comparator-Fast Turn-off

There is a High Speed (HS) Comparator used for fast turn-off of the ORing MOSFET to protect the common bus against hard short faults at a sourcing power supply output (refer to Figure 1).

During normal operation the gate of the ORing MOSFET is charge pumped to a voltage that depends on whether it is in the 20mV regulation mode or fully enhanced. In this case:

$$V_{OUT} = V_{IN} - I_{OUT} \bullet r_{DS(ON)} \quad \text{(EQ. 1)}$$

If a dead short fault occurs in the sourcing supply, it causes V_{IN} to drop very quickly while V_{OUT} is not affected as more than one supply are paralleled. In the absence of the ISL6144 functionality, a very high reverse current will flow from Output to the Input supply pulling down the common DC Bus, resulting in an overall “catastrophic” system failure.

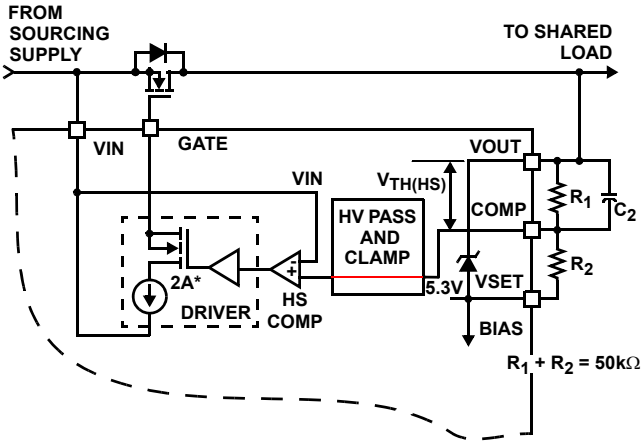


FIGURE 1. HS COMPARATOR

The fault can be detected and isolated by using the ISL6144 and an N-Channel ORing MOSFET. V_{IN} is compared to V_{COMP}, and whenever:

$V_{IN} < V_{COMP}$; where

$$V_{COMP} = V_{OUT} - V_{TH(HS)} \quad \text{(EQ. 2)}$$

$V_{TH(HS)}$ is defined below

The fast turn-off mechanism will be activated and the MOSFET(s) will be turned off very quickly. The speed of this turn-off depends on the amount of equivalent gate loading capacitance. For an equivalent Cgs = 39nF. The gate turn-off time is <300ns and gate pull down current is 2A.

The level of $V_{TH(HS)}$ (HS Comparator trip level) is adjustable by means of external resistors R_1 and R_2 to a value theoretically ranging from 0V to 5.3V. Typical values are 0.05V to 0.3V. This is done in order to avoid false turn-off due to noise or minor glitches present in the DC switching power supply. The threshold voltage is calculated as Equation 3:

$$V_{TH(HS)} = \frac{R_1}{(R_1 + R_2)} V_{REF(VSET)} \quad \text{(EQ. 3)}$$

Where $V_{REF(VSET)}$ is an internal zener reference (5.3V typical) between V_{OUT} and VSET pins. R_1 and R_2 must be chosen such that their sum is about 50kΩ. An external capacitor, C_2, is needed between V_{OUT} and COMP pins to provide high frequency decoupling. The HS comparator has an internal delay time on the order of 50ns, which is part of the <300ns overall turn-off time specification (with Cgs = 39nF).

Gate Logic and Charge Pump

The IC has two charge pumps. The first charge pump generates the floating gate drive for the N-Channel MOSFET. The second charge pump output current opposes the pull down current of the slow turn-off transistor to provide regulation of the GATE voltage.

The presence of the charge pump allows the use of an N-Channel MOSFET with a floating gate drive. The N-Channel MOSFETs normally have lower $r_{DS(ON)}$ (not to mention cost saving) compared to P-Channel MOSFETs, allowing further reduction of conduction losses.

BIAS and REF

Bias currents for the two internal zener supplies (HVREF and VSET) is provided by this block. This block also provides a 0.6V band-gap reference used in the UV detection circuit.

Undervoltage Comparator

The undervoltage comparator compares HVREF to 0.6V internal reference. Once it falls below this level the UV circuitry pulls and holds down the gate pin as long as the HVREF UV condition is present. Voltage at both VIN and HVREF pins track each other.

High Voltage Pass and Clamp

A high voltage pass and clamping circuit prevents the high output voltage from damaging the comparators in case of quick drop in V_{IN}. The comparators are running from the 5V supply between HVREF and V_{IN}. These devices are rated for 5V and will be damaged if V_{OUT} is allowed to be present (as the output is powered from other parallel supplies), and does not fall when V_{IN} is falling. For example, if V_{IN} falls to 30V, V_{OUT} remains at 48V and the differential Voltage between the "-" and "+" terminals of the comparator would be 18V, exceeding the rating of the devices and causing permanent damage to the IC.

Fault Detection Block

The fault detection block has two monitoring circuits (refer to Figure 2):

1. Gate monitoring detects when the GATE < V_{IN} + 0.37V
2. V_{OUT} monitoring detects when V_{IN} - 0.41V > V_{OUT}

These two outputs are ORed, inverted, level shifted, and delayed using an internal filter (t_{FLT})

The following failures can be detected by the fault detection circuitry:

1. ORing FET off due to dead short in the sourcing supply, leading to V_{IN} < V_{OUT}
2. Shorted terminals of the ORing FET
3. Blown fuse in the power path of the sourcing supply
4. Open Gate terminal
5. HVREF UV

The $\overline{\text{FAULT}}$ pin is not latched off and the pull down will shut off as soon as the fault is removed and the pin becomes high impedance. Typically, an external pull-up resistor is connected to an external voltage source (for example 5V, 3.3V) to pull the pin high, an LED can be used to indicate the presence of a fault.

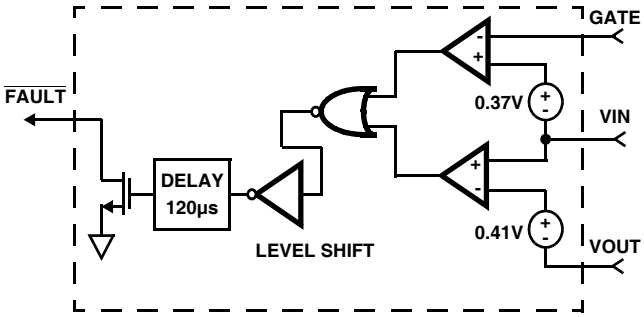


FIGURE 2. FAULT DETECTION BLOCK

Application Considerations

ORing MOSFET Selection

Using an ORing MOSFET instead of an ORing diode results in increased overall power system efficiency as losses across the ORing elements are reduced. The use of ORing MOSFETs becomes more important at higher current levels, as power loss across the traditionally used ORing diode is very high. The high power dissipation across these diodes requires special thermal design precautions such as heat sinks and forced airflow.

For example, in a 48V, 40A (1+1) redundant system with current sharing, using a Schottky diode as the ORing (auctioneering) device (see Figure 3), the forward voltage drop is in the 0.4V to 0.7V range. Let us assume it is 0.5V, power loss across each diode is as shown in Equation 4:

$$P_{loss(D1)} = P_{loss(D2)} = \frac{I_{OUT}}{2} \cdot V_F = 20A \cdot 0.5V = 10W \quad \text{(EQ. 4)}$$

Total power loss across the two ORing diodes is 20W.

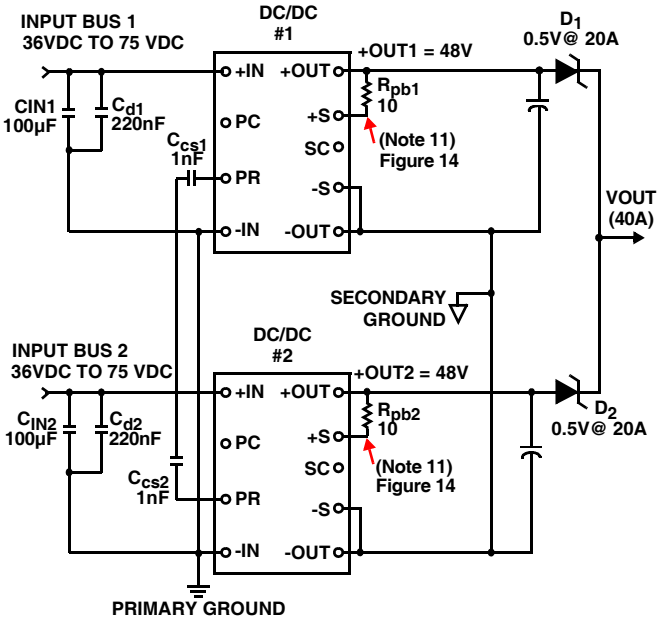


FIGURE 3. 1 + 1 REDUNDANT SYSTEM WITH DIODE ORing

If a 5mΩ single MOSFET per feed is used, the power loss across each MOSFET is as shown in Equation 5:

$$P_{loss(M1)} = P_{loss(M2)} = \left(\frac{I_{OUT}}{2}\right)^2 \cdot r_{DS(ON)} \quad \text{(EQ. 5)}$$

$$P_{loss(M1)} = (20A)^2 \cdot 5m\Omega = 2W$$

Total power loss across the two ORing MOSFETs is 4W.

In case of failure of current sharing scheme, or failure of DC/DC #1, the full load will be supplied by DC/DC #2. ORing MOSFET M2 or ORing Diode D_2 will be conducting the full

load current. Power loss across the ORing devices is as shown in Equation 6:

$$P_{loss(D2)} = I_{OUT} \cdot V_F = 40A \cdot 0.5V = 20W \quad \text{(EQ. 6)}$$

$$P_{loss(M2)} = (I_{OUT})^2 \cdot r_{DS(ON)} = (40A)^2 \cdot 5m\Omega = 8W$$

This shows that worst-case failure scenario has to be accounted for when choosing the ORing MOSFET. In this case we need to use two MOSFETs in parallel per feed to reduce overall power dissipation and prevent excessive temperature rise of any single MOSFET. Another alternative would be to choose a MOSFET with lower $r_{DS(ON)}$.

The final choice of the N-Channel ORing MOSFET depends on the following aspects:

1. **Voltage Rating:** The drain-source breakdown voltage V_{DSS} has to be higher than the maximum input voltage including transients and spikes. Also the gate to source voltage rating has to be considered, The ISL6144 maximum Gate charge voltage is 12V, make sure the used MOSFET has a maximum V_{GS} rating >12V.
2. **Power Losses:** In this application the ORing MOSFET is used as a series pass element, which is normally fully enhanced at high load currents; switching losses are negligible. The major losses are conduction losses, which depend on the value of the on-state resistance of the MOSFET $r_{DS(ON)}$, and the per feed load current. For an N + 1 redundant system with perfect current sharing, the per feed MOSFET losses are as shown in Equation 7:

   $$P_{loss(FET)} = \left(\frac{I_{LOAD}}{N+1}\right)^2 \cdot r_{DS(ON)} \quad \text{(EQ. 7)}$$

   The $r_{DS(ON)}$ value also depends on junction temperature; a curve showing this relationship is usually part of any MOSFET's data sheet. The increase in the value of the $r_{DS(ON)}$ over temperature has to be taken into account.
3. Current handling capability, steady state and peak, are also two important parameters that must be considered. The limitation on the maximum allowable drain current comes from limitation on the maximum allowable device junction temperature. The thermal board design has to be able to dissipate the resulting heat without exceeding the MOSFET's allowable junction temperature.

Another important consideration when choosing the ORing MOSFET is the forward voltage drop across it. If this drop approaches the 0.41V limit, which is used in the V_{OUT} fault monitoring mechanism, then this will result in a permanent fault indication. Normally the voltage drop would be chosen not to exceed a value around 100mV.

"ISL6144 + ORing FET" vs "ORing Diode" Solution

"ISL6144 + ORing FET" solution is more efficient, which will result in simplified PCB and thermal design. It will also eliminate the need for a heat sink for the ORing diode. This will result in cost savings. In addition, the ISL6144 solution provides a more flexible, reliable and controllable ORing functionality and protects against system fault scenarios (refer to "Fault Detection Block" on page 8).

On the other hand, the most common failures caused by diode ORing include open circuit and short circuit failures. If one of these diodes (Feed A) has failed open, then the other Feed B will provide all of the power demand. The system will continue to operate without any notification of this failure, reducing the system to a single point of failure. A much more dangerous failure is where the diode has failed short. The system will continue to operate without notification that the short has occurred. With this failure, transients and failures on Feed B propagate to Feed A. Also, this silent short failure could pose a significant safety hazard for technical personnel servicing these feeds.

"ISL6144 + ORing FET" vs "Discrete ORing FET" Solution

If we compare the ISL6144 integrated solution to discrete ORing MOSFET solutions, the ISL6144 wins in all aspects. The main ones are: PCB real estate saving, cost savings, and reduction in the MTBF of this section of the circuit as the overall number of components is reduced.

In brief, the solution offered by this IC enhances power system performance and protection while not adding any considerable cost. This solution provides both a PCB board real estate savings and a simple to implement integrated solution.

Setting the External HS Comparator Threshold Voltage

In general, paralleled modules in a redundant power system have some form of active current sharing, to realize the full benefit of this scheme, including lower operating temperatures, lower system failure rate, and better transient response when load step is shared. Current sharing is realized using different techniques; all of these techniques will lead to similar modules operating under similar conditions in terms of switching frequency, duty cycle, output voltage and current. When paralleled modules are current sharing, their individual output ripple will be similar in amplitude and frequency and the common bus will have the same ripple as these individual modules and will not cause any of the turn-off mechanisms to be activated, as the same ripple will be present on both sensing nodes (V_{IN} and V_{OUT}). This would allow setting the high speed comparator threshold ($V_{TH(HS)}$) to a very low value. As a starting point, a $V_{TH(HS)}$ of 50mV could be used, the final value of this TH will be system dependent and has to be finalized in the system prototype stage. If the gate experiences false turn-off due to system noise, the $V_{TH(HS)}$ has to be increased.

The reverse current peak can be estimated as:

$$I_{reverseP} = \frac{V_{TH(HS)} + V_{SD} + V_{OS(HS)}}{r_{DS(ON)}} \quad \text{(EQ. 8)}$$

where:

V_{SD} is the MOSFET forward voltage drop.

$V_{OS(HS)}$ is the voltage offset of HS Comparator.

The duration of the reverse current pulse is a few hundred nanoseconds and is normally kept well below current rating of the ORing MOSFET.

Reducing the value of $V_{TH(HS)}$ results in lower reverse current amplitude and reduces transients on the common bus output voltage.

HVREF and COMP Capacitor Values

HVREF CAPACITOR (C1)

this capacitor is necessary to stabilize the $HV_{REF(VZ)}$ supply and a value of 150nF is sufficient. Increasing this value will result in gate turn-on time increase.

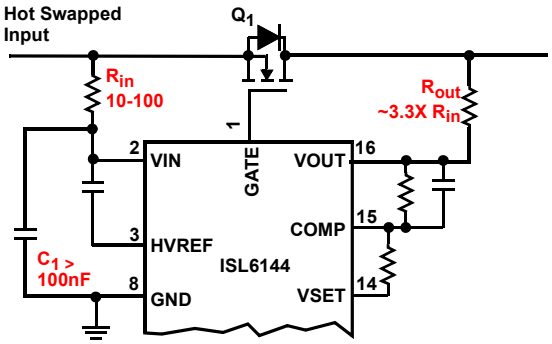
COMP CAPACITOR (C2)

Placed between V_{OUT} and COMP pins to provide filtering and decoupling. A 10nF capacitor is adequate for most cases.

Protecting VIN and VOUT from High dv/dt Events

In hot swap applications lacking adequate VIN and VOUT bulk capacitance and where the ISL6144 is directly connected to a prebiased bus exposing either the VIN or VOUT pins directly to high dv/dt transients, these pins must be filtered to prevent catastrophic damage caused by the high dv/dt transients. A simple RC filter using a pin 2 series resistor, of 10 -100Ω and the 100nF or greater best design practices decoupling capacitor to ground. This will provide a >1µs rise time on the VIN pin to protect it. A resistor of ~3.3 times the value should be added in series with the VOUT pin to reduce the introduced HS Vth error.

Alternately, the programmed HS Vth can be adjusted upward by the voltage across R_{VIN} as described on page 9.



Typical Performance Curves and Waveforms

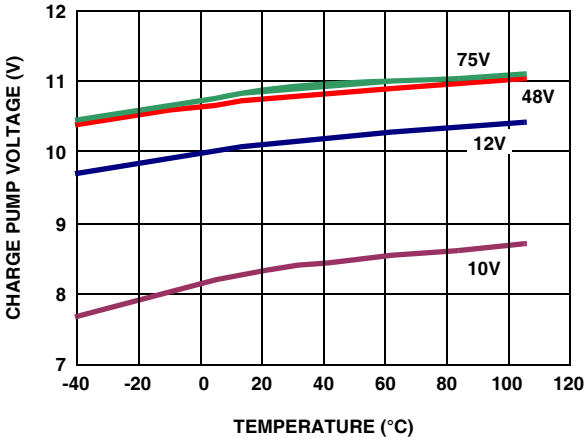


FIGURE 4. CHARGE PUMP VOLTAGE (V_{GQP}) vs TEMPERATURE

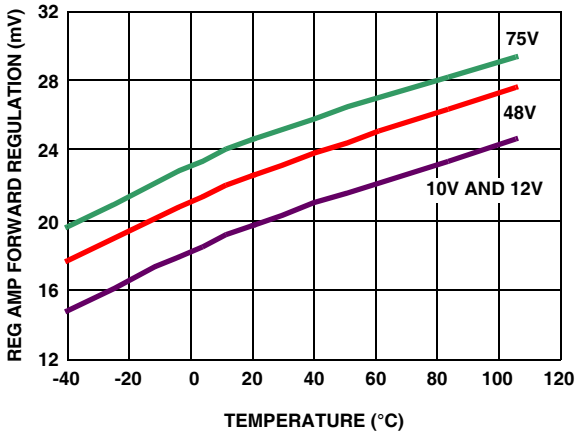


FIGURE 5. REG. AMP FORWARD REGULATION

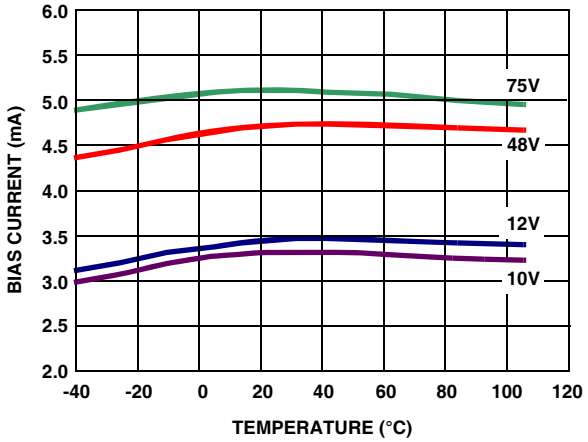


FIGURE 6. I BIAS CURRENT vs TEMPERATURE

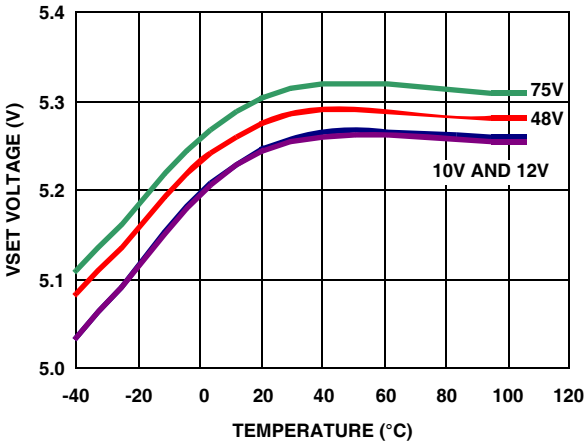


FIGURE 7. VSET VOLTAGE

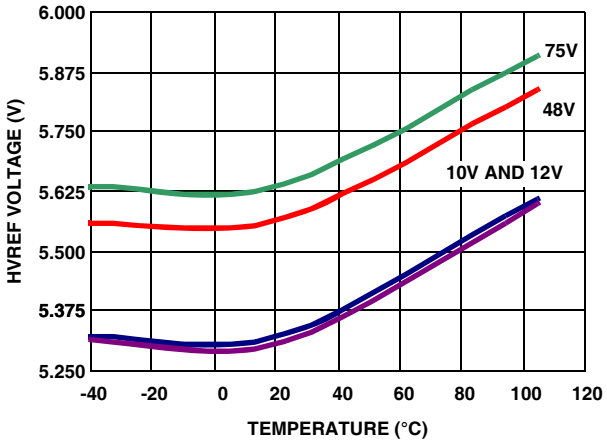


FIGURE 8. HVREF VOLTAGE

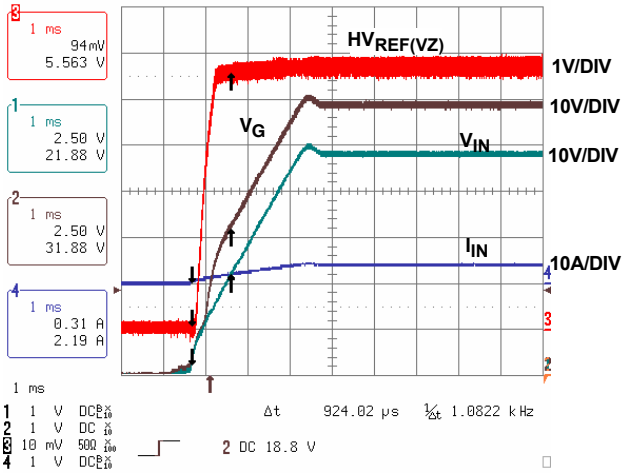


FIGURE 9. FIRST SUPPLY START-UP

Typical Performance Curves and Waveforms (Continued)

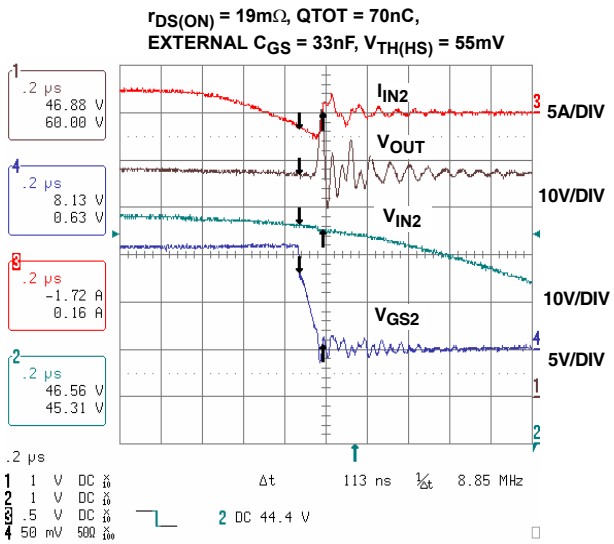


FIGURE 10. HIGH SPEED TURN-OFF, V_{IN} = 48V, COMMON LOAD IS SMPS (C_{LOAD} = 100µF) WITH EQUIVALENT 4A LOAD

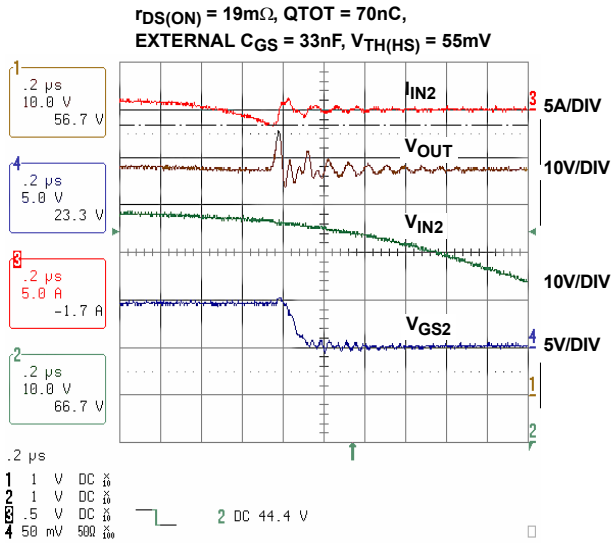


FIGURE 11. HIGH SPEED TURN-OFF, V_{IN} = 48V, COMMON LOAD IS SMPS (C_{LOAD} = 100µF) WITH EQUIVALENT 1.3A LOAD

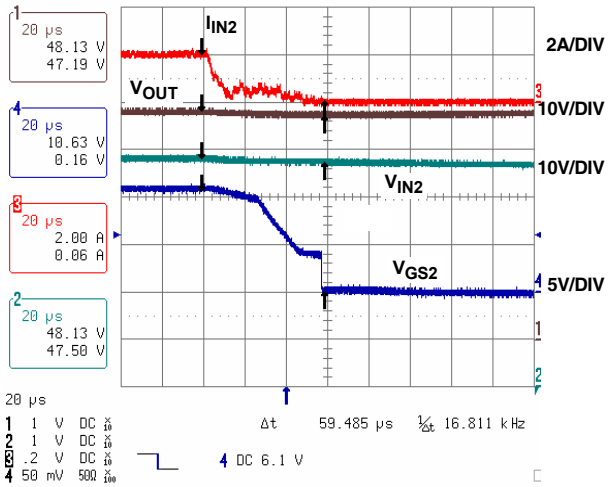


FIGURE 12. SLOW SPEED TURN-OFF, V_{IN} = 48V, COMMON LOAD IS SMPS (C_{LOAD} = 100µF) WITH EQUIVALENT 4A LOAD

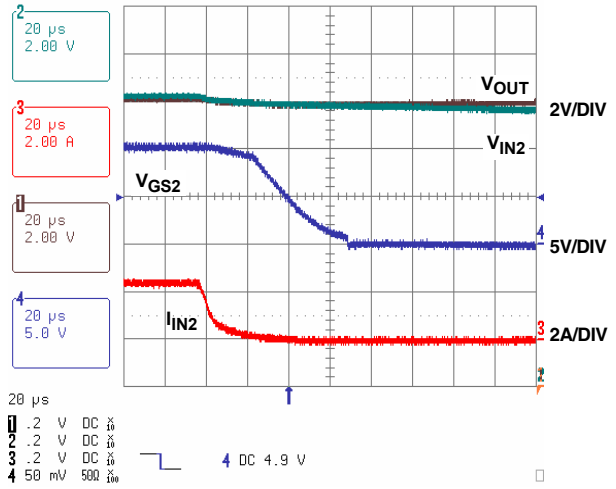
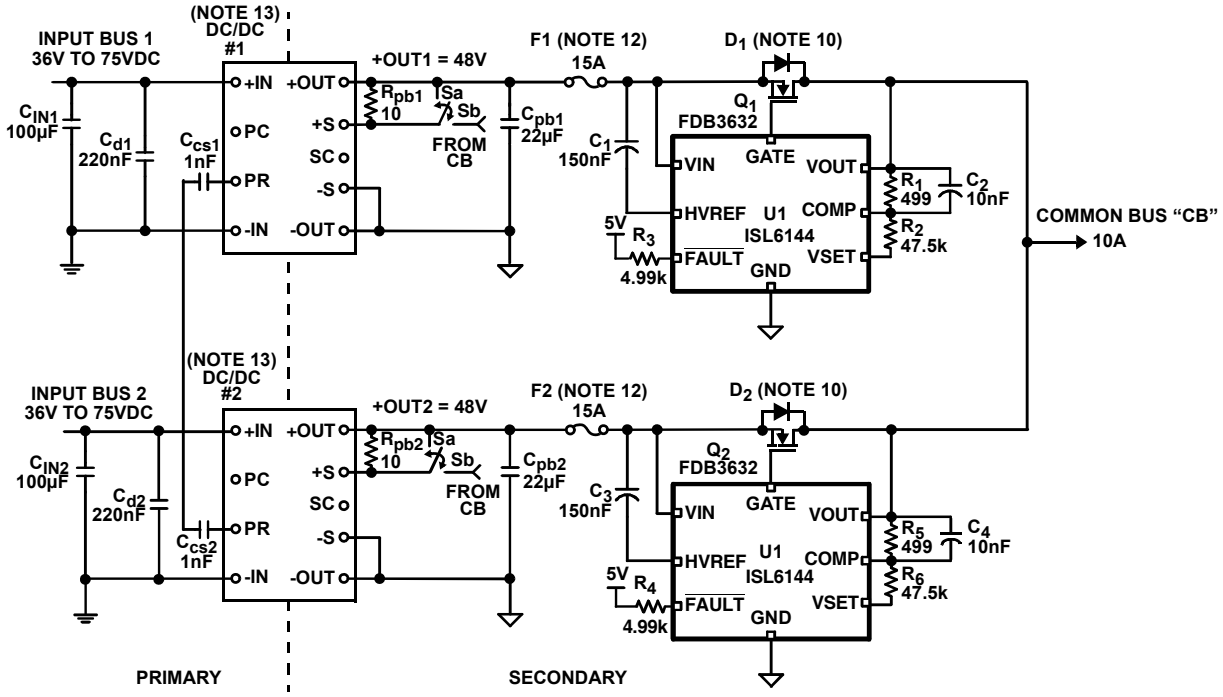


FIGURE 13. SLOW SPEED TURN-OFF, V_{IN} = 12V, COMMON LOAD IS SMPS (C_{LOAD} = 100µF) WITH EQUIVALENT 4A LOAD

Application Circuit



NOTES:

10. D_1, D_2 are parasitic MOSFET diodes.
11. Remote Sense pin (+S) on both DC/DC converters has to be connected either directly at the module output (Sa closed) or to the CB point (Sb closed). Connecting to CB is not recommended as it might cause Fault propagation in case of short circuit on a PS output.
12. F1, F2 are optional and can be eliminated depending on power system configuration and requirements.
13. DC/DC #1, 2 configuration is based on Vicor V48B48C250AN3.

FIGURE 14. APPLICATION CIRCUIT FOR A 1 + 1 REDUNDANT 48V SYSTEM

Using the ISL6144EVAL1Z High Voltage ORing MOSFET Controller Evaluation Board

In a multiple supply, fault tolerant, redundant power distribution system, paralleled power supplies contribute equally to the load current through various power sharing schemes. Regardless of the scheme, a common design practice is to include discrete ORing power diodes to protect against reverse current flow should one of the power supplies develop a catastrophic output short to ground. In addition, reverse current can occur if the current sharing scheme fails and an individual power supply voltage falls significantly below the others.

Although the discrete ORing diode solution has been used for some time and is inexpensive to implement, it has some drawbacks. The primary downside is the increased power dissipation loss in the ORing diodes as power requirements for systems increase. In some systems this lack of efficiency results in a cost that surpasses the cost of the ISL6144 and power FET implementation. The power loss across a typical ORing diode with 20A is about 10W. Many diodes will be paralleled to help distribute the heat. In comparison, a FET with 5mΩ on-resistance dissipates 2W, which constitutes an 80% reduction. When multiplied by the number of paralleled supplies, the power savings are significant. Another disadvantage when using an ORing diode would be failure to detect a shorted or open ORing diode, jeopardizing power system reliability. An open diode reduces the system to a single point of failure while a diode short might pose a hazard to technical personnel servicing the system while unaware of this failure.

The ISL6144 ORing MOSFET Controller and a suitably sized N-Channel power MOSFET(s) increase power distribution efficiency and availability when replacing a power ORing diode in high current applications. It can be used in +9V to +75V systems and has an internal charge pump to provide a floating gate drive for the N-Channel ORing MOSFET.

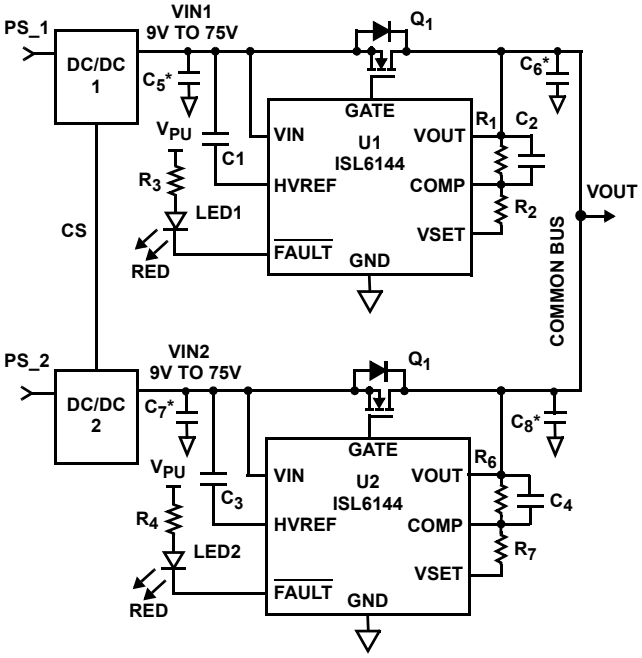
The input/output differential trip point "V_{OUT} - V_{IN}" can be programmed by two external resistors (R_1, R_2 or R_6, R_7). This trip point can be adjusted to avoid false gate trip off due to power supply noise.

The high speed comparator action protects the common bus from being affected due to individual power supply shorts by turning off the ORing MOSFET of the shorted feed in less than 300ns (when using an ORing MOSFET with equivalent gate to source capacitance equal to 39nF).

The Hysteretic Regulating (HR) Amplifier provides a slow turn-off of the ORing MOSFET. This turn-off is achieved in less than 100µs when one of the sourcing power supplies is shutdown slowly for system diagnostics, ensuring zero reverse current. This slow turn-off mechanism also reacts to output voltage droop, degradation, or power-down.

A circuit fault condition is indicated on an open drain $\overline{FAULT}$ pin. The fault detection circuitry covers different types of failures; including dead short in the sourcing supply, a dead-short of any two ORing MOSFET terminals, or a blown fuse in the power distribution path.

Typical Application



R_1 = R_6 = 499Ω (5%)
R_2 = R_7 = 47.5kΩ (5%)
R_3 = R_4 = 1.21kΩ (5%)

C_1 = C_2 = 150nF (10V)
C_3 = C_4 = 10nF (10V)
C_5* TO C_8* = 100nF *(100V) Optional Decoupling Caps

- LED1, LED2 are red LEDs to indicate a fault, different interfaces are possible to the FAULT pin.
- V_{PU} is an external pull up voltage source. Also, V_{OUT} can be used as the pull up source. In this case if it is higher than 16V, use a zener diode from the $\overline{FAULT}$ pin to GND with a clamping voltage less than the rating of the $\overline{FAULT}$ pin which is 16V.

Related Literature

- TB389 (PCB Land Pattern Design and Surface Mount Guidelines for QFN (MLFP) Packages)
- Manufacturer's MOSFET data sheets

DC/DC CONVERTERS (NOT PART OF THE EVAL BOARD) ISL6144EVAL1Z CONTROL BOARD

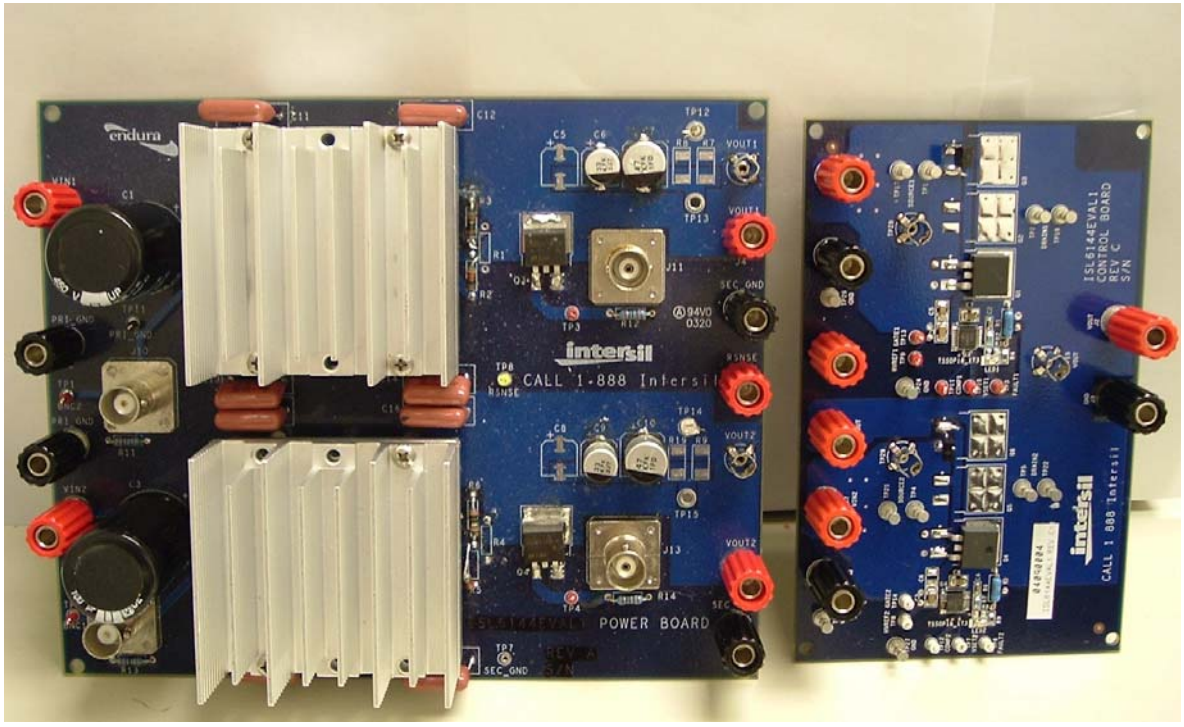


FIGURE 15. TEST SETUP USING DC/DC MODULES

ISL6144 Evaluation Board Overview

This section of the data sheet serves as an instruction manual for the ISL6144EVAL1Z board. It also provides design guidelines and recommendations for using the ISL6144 for ORing MOSFET control. The ISL6144EVAL1Z Control Board has two parallel feeds connected to each other through N-channel ORing MOSFETs. Each ORing MOSFET has an ISL6144 connected to it. This board demonstrates the operation of Intersil's ISL6144 HV ORing MOSFET Controller IC in a typical 1 + 1 redundant power system.

To demonstrate the functionality of the ISL6144, two power supplies with identical output voltages are required as the input to the ISL6144EVAL1Z board. This will show the ability of the ISL6144 to provide the gate drive voltage for the ORing N-Channel MOSFET. The ISL6144 also monitors the drain (V_{OUT}), source (V_{IN}) and gate voltages in order to provide reverse current protection and protection against power feeds' related faults.

Figure 15 shows a test setup used in the characterization of ISL6144 in a 1 + 1 redundant power system.

ISL6144EVAL1Z Control Board (Rev C)

This board is configured with two input power feeds connected in parallel for redundancy using ORing MOSFETs. The ISL6144 allows the two rails to operate in active ORing mode (This means that both feeds can share the current if their respective voltages are close to each other). ORing MOSFET's gate drive voltage, control and monitoring for each of these feeds are implemented using the ISL6144.

The board has the following features:

- Evaluation of the ISL6144 in a 1 + 1 redundant power system using a single board
- Has footprint for a total of three parallel MOSFETs per feed. Number of MOSFETs used will depend on the load current (on the standard ISL6144EVAL1Z board only one MOSFET is populated per feed)
- Allows the user to test turn-on, slow turn-off, fast turn-off and different fault scenarios
- Visual fault indication with Red LEDs
- Banana Connectors and test points for all inputs, outputs and IC pins
- Can be easily connected to the power system prototype for initial evaluation

Note that the board was designed to handle high load currents (up to 20A per feed) with the appropriate MOSFET selection.

Input Voltage Range (+9V to +75V)

The ISL6144 can operate in equipment with voltages in the +9V to +75V range. The ISL6144 can also be used in systems with negative voltages -9V to -75V, but it has to be placed on the return (high) side. For example, in ATCA systems, an ORing of both the low (-48V) and high (-48V Return) sides is required. In this case the ISL6144 can be used on the high side.

The ISL6144 draws bias from both the input and output sides. External bias voltage rail is not needed and cannot be used. As soon as the Input voltage reaches the minimum operational voltage, the internal charge pump turns on and provides gate voltage to turn-on the ORing FET.

Multiple Feed ORing (ISL6144EVAL1Z)

In today's high availability systems, two or more power supplies can be paralleled to provide redundancy and fault tolerance. These paralleled power supplies operate in an active ORing mode where all of these supplies share the load current, depending on the redundancy scheme implemented in the particular system. The power system must be able to continue its normal operation, even in the event of one or more failures of these power supplies. Faults occurring on the power supply side need to be isolated from the common bus point connected to the system critical loads. This fault isolation device is known as the ORing device. The function of the ORing device is to pass the forward supply current flowing from the power supply side and block the reverse fault current. A fault current might flow if a short occurs on the input side (typically this could be a power supply output capacitor short). In this case, the input voltage drops and current may flow in the reverse direction from the load to the input, causing the common bus to drop and the system to fail. Although ORing diodes are simple to implement in such systems, they suffer from many drawbacks, as outlined earlier.

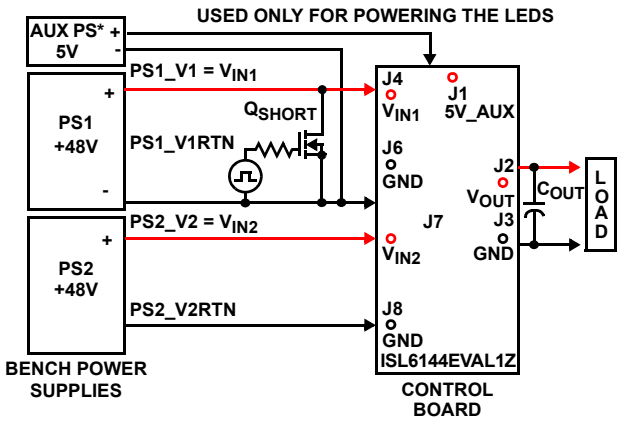
The ISL6144 (with an external N-Channel MOSFET) provides an integrated solution to perform the ORing function in high availability systems, while increasing power system efficiency at the same time.

Operating Instructions and Functional Tests

Test setup for ISL6144EVAL1Z is shown in Figures 16 and 17 with two options for the input power sources.

Option 1: Using two identical bench power supplies (BPS) connected directly to the ISL6144EVAL1Z Control Board (refer to Figure 16). Just make sure to program the voltages on PS1_V1 and PS2_V2 to identical values so that they share the load current. A MOSFET (Q_{short}) is connected at the Input of one or both feeds as close as possible to the input connectors of the ISL6144EVAL1Z board. Slow turn-off of the input BPS can be performed by the on/off button (depending on the output capacitance value of the power supply/module, a local loading resistor might be needed to help discharge the BPS output capacitor). An output capacitor C_{OUT} (equivalent to the capacitor that will be used in the final power system solution) is connected to the Common Bus point (V_{OUT}). Different types of loads can be used (power resistors, electronic load or simply another DC/DC converter).

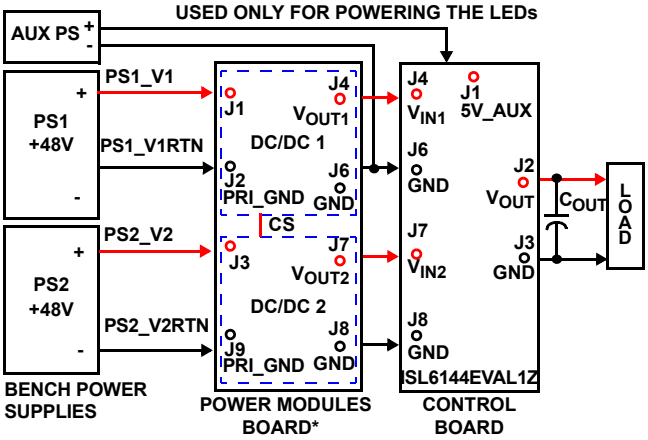
Option 2: Using a custom designed DC/DC converter Power Board which consists of two DC/DC modules connected in current sharing configuration, each DC/DC module output can be turned off slowly using the ON/OFF pin or can be shorted using on-board Power MOSFET (Refer to Figure 17). In this case also, similar considerations for C_{OUT} and type of load apply as in option 1.



*Auxiliary power supply is used to power the LED circuit. If V_{OUT} is less than 16V, J1 can be connected directly to V_{OUT} (J5). If V_{OUT} is higher than 16V, we still can use V_{OUT} to replace AUX PS, but a zener diode has to be connected from FAULT to GND to clamp the voltage across the pin to 16V or lower.

FIGURE 16. TEST SETUP USING BENCH PS

.



*Power Modules Board can be replaced by bench power supplies or any discrete DC/DC modules. Just make sure to adjust both V_{OUT1} and V_{OUT2} close to each other to allow current sharing between the two modules (Refer to option 1 and Figure17).

FIGURE 17. TEST SETUP USING DC/DC MODULES

DC/DC Converter Power Board (not part of the ISL6144EVAL1Z board)

The DC/DC converter board consists of two DC/DC converters with independent input voltage rails. In reality, two identical power supplies can be used in the test setup to replace this board (contact Intersil Applications Engineering if you need assistance in your test setup). This DC/DC converter board is configured for operation at different output voltage levels depending on the choice of DC/DC modules. Most evaluation results are provided for a mix of +48V and +12V input voltages. Any other voltage within the +9V to +75V range can also be used.

Each DC/DC converter has a low $r_{DS(ON)}$ MOSFET connected in parallel to the output terminals. This MOSFET is normally off. When turned on it simulates a short across the output. Another MOSFET is connected at the ON/OFF pin of the modules to simulate a slow turn-off of the module.

Single-Feed Evaluation

The ISL6144EVAL1Z is hooked up to two input power supplies using test setup shown in Figure 16 or Figure 17. Note that the ISL6144EVAL1Z is populated with one FDB3632 MOSFET per feed (Nominal value of the MOSFET's $r_{DS(ON)}$ is approximately 8mΩ at V_{GS} = 10V).

1. Connect the input power supplies, auxiliary 5V power supply, load and output capacitor to the ISL6144EVAL1Z.
2. Connect test equipment (Oscilloscope, DMM) to the signals of interest using on-board test points and scope probe jacks.
3. Turn-on PS1 with V_{IN1} = +48V (V_{IN1} can be any voltage within +9V to +75V). Turn-on the auxiliary power supply (AUX PS powering the LED circuit) with +5V. Adjust load current to 2A. Verify the main operational parameters such as the 20mV forward regulation at light loads, and gate voltage as a function of load current.
4. The forward voltage drop across the MOSFET terminals V_{SD1} (TP1-TP2) is equal to the maximum of the 20mV forward regulated voltage drop across the source-drain "V_{FWD_HR}" or the product of the load current and the MOSFET on-state resistance "I_{Load} * $r_{DS(ON)}$".
5. For I_{Load} = 2A, V_{SD1} is equal to V_{FWD_HR} = 20mV. The gate-source voltage is modulated as a function of load current and MOSFET transconductance. Gate-source voltage V_{GS1} (TP13 -TP17) is approximately 4V. In this case, LED1 is off. LED2 will be RED as V_{IN2} is still off.
6. Increase the load current I_{Load} to 4A. Note that V_{DS1} is increased to above V_{FWD_HR} and operation in the 20mV forward regulation cannot be maintained. The MOSFET cannot deliver the required load current with a 20mV constant V_{SD1}. In this case, gate voltage is fully charge-pumped to V_{GQP} (10.6V nominal).
7. Turn-off V_{IN1} and turn-on V_{IN2} and repeat the same tests listed above. Make sure the ISL6144 is providing gate voltage, which is modulated based on the load current. V_{SD2} is measured between (TP4-TP5), V_{GS2} is measured between (TP14-TP21).

Two-Feed Parallel Evaluation

Two Feed parallel operation verification can be performed after completion of the single feed evaluations. Make sure that the two Input power supplies connected to the ISL6144EVAL1Z board are identical in voltage value. Identical input voltages are needed to enable the two feeds to share the load current (In real world power systems, current sharing is most likely insured by the power supplies/modules that have an active current sharing feature).

1. Turn-on PS1 and PS2 in sequence (hot plugging is not recommended). Adjust V_{IN1} and V_{IN2} close to each other. Verify the input current of both feeds to be within acceptable current sharing accuracy (~10%). Current sharing accuracy will be very poor at light loads and becomes better with higher load currents.
2. Adjust the load current to different values and verify that both V_{SD1} (TP1 to TP2) and V_{SD2} (TP4 to TP5) are close to each other. These two voltages might be different depending on the amount of load current passing through each of the two feeds.
3. At light loads, I_{Load} * $r_{DS(ON)}$ is less than 20mV, the ISL6144 operates in the forward regulation mode and gate voltage is modulated as a function of load current. When I_{Load}*$r_{DS(ON)}$ becomes higher than the regulated 20mV, the charge pump increases and clamps the gate voltage to the maximum possible charge pump voltage, V_{GQP}.
4. Verify the Gate voltage of both MOSFETs V_{GS1} (TP13 to TP17) and V_{GS2} (TP14 to TP21) with different load currents.
5. Both LED1 and LED2 are off when both feeds are on.
6. For I_{Load} = 4A, turn-off V_{IN2} and note that V_{GS2} has turned off. LED2 is RED and V_{GS1} has increased from around 4V to V_{GQP}.
7. Turn V_{IN2} back on and turn V_{IN1} off. V_{GS1} is now off. LED1 is RED. V_{GS2} has increased to V_{GQP}.

Performance Tests

Performance tests can be carried out after the two feeds have been verified and found to be operational in active, 1 + 1 redundancy (when two feeds share the load current, current sharing is ensured by the incoming power supplies.) These include gate turn-on at power supply start-up, fast speed turn-off (in case of fast dropping input rail), slow speed turn-off (in response to slow dropping input rail) and fault detection in response to different faults.

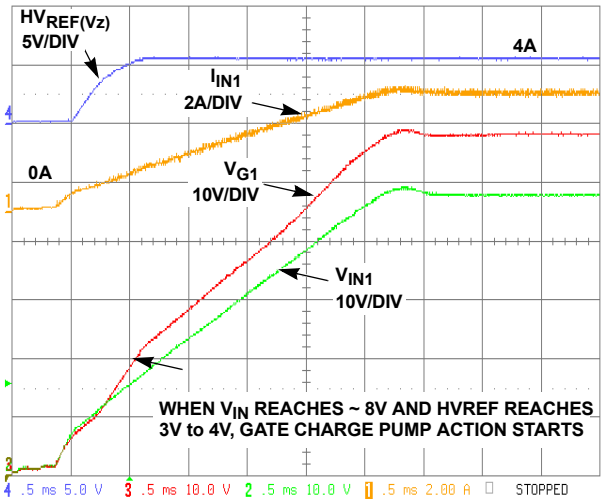
Gate Start-Up Test

FIRST-FEED START-UP

When the first feed is turned on, as V_{IN1} rises, conduction occurs through the body diode of the MOSFET. This only occurs for a short time until the MOSFET gate voltage can be charge-pumped on. This conduction is necessary for proper operation of the ISL6144. It provides bias for the gate

hold off and other internal bias and reference circuitry. The charge pump circuitry starts functioning as the input voltage at the V_{IN} pin reaches a value around 8V. The gate voltage depends on the load current (as explained in previous sections), The maximum gate voltage will be clamped to a maximum of V_{GQP} when load current becomes too high to be handled with 20mV across the source-drain terminals. Overall, it takes less than 1ms to reach the load-dependent final gate voltage value. Note that the Input voltage cannot be hot swapped and has to rise slowly. A rise time of at least 1ms is recommended for the voltage at VIN pin.

V_{IN} = 48V; RESISTIVE LOAD = 4A, C_{GSEXT} = 33nF
V_{IN1},V_{G1},I_{IN1} and $HV_{REF(VZ)}$ WAVEFORMS



V_{IN1}, V_{G1}, I_{IN1} and V_{OUT} WAVEFORMS

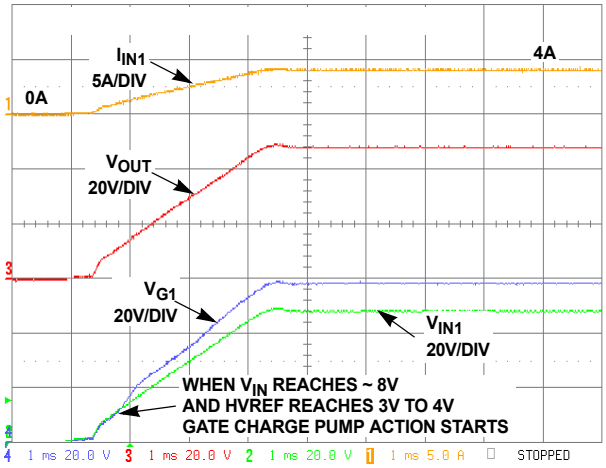


FIGURE 18. FIRST FEED V_{IN1} START-UP (48V CASE)

V_{IN} = 12V; RESISTIVE LOAD = 5A, C_{GSEXT} = 33nF

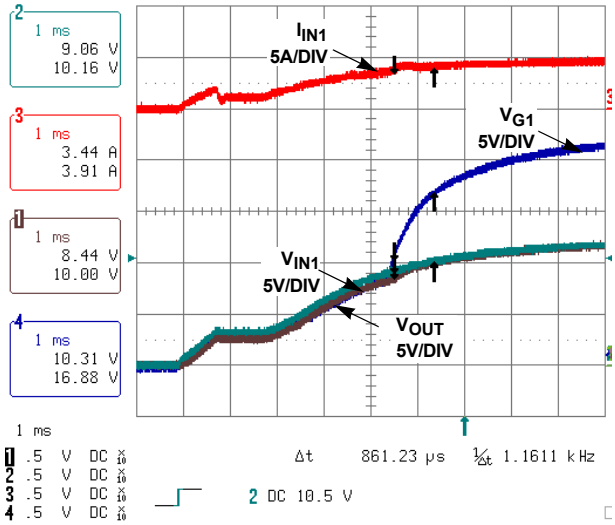


FIGURE 19. FIRST FEED V_{IN1} START-UP (12V CASE)

The start-up tests were done with the addition of an external gate to source capacitor to demonstrate start-up time with a total equivalent gate-source capacitance around 39nF.

SECOND (CONSECUTIVE) FEED START-UP

In this case, the ISL6144 for the second (consecutive) feed (U4) already has output bias voltage as the first parallel feed has been turned on and V_{OUT} is present on the common bus. As V_{IN2} rises, V_{G2} rises with it (V_{G2} is GATE2 voltage with respect to GND). When V_{IN2} approaches V_{IN1} value, Gate 2 is turned. Second feed gate turn-on is faster than the first feed as the HVREF capacitor (C_3) is already charged.The second or consecutive power supply to be started can be turned on faster than the first power supply, a rise time of at least 200µs of the second rail is recommended.

V_{IN} = 48V; RESISTIVE LOAD = 4A, $C_{GS(EXT)}$ = 33nF

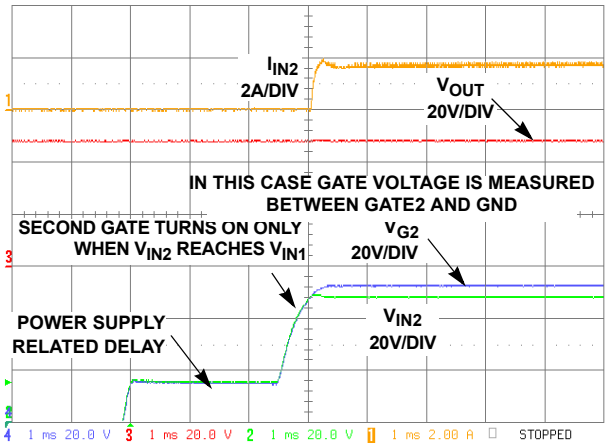


FIGURE 20. SECOND (CONSECUTIVE) FEED V_{IN2} START-UP

Gate Fast Turn-off Test

During normal operation, the ISL6144 provides gate drive voltage for the ORing MOSFET when the Input voltage exceeds the output voltage. The current flows in the forward direction from the input to the output. Now, what happens if the input voltage drops quickly below the output voltage as a result of a failure on the input sourcing power supply while the MOSFET remained on? The answer is: If the MOSFET is kept on, current starts to flow in the reverse direction from the output to the input. Of course this is not desired nor acceptable. It will lead to effectively shorting the output and causing an overall system failure. In order to block this reverse current, the ISL6144 senses the voltage at both VIN and COMP pins (this is V_{OUT} voltage reduced by a resistor programmable threshold ($V_{TH(HS)}$), it is programmed to 55mV on the EVAL board and could be adjusted by changing R_1, R_4 values for both feeds. If V_{IN} drops below COMP (V_{OUT} - $V_{TH(HS)}$), the High Speed Comparator turns off the gate of the ORing MOSFET very quickly, the gate pull down current I_{PDH} is 2A. As a result the reverse current flow is prevented. The maximum turn-off time is less than 300ns when using an ORing MOSFET(s) with an equivalent gate-source capacitance of 39nF (equivalent to Q_{TOT} = 390nC at V_{GS} = 10V).

On the ISL6144EVAL1Z board, FDB3632 has an equivalent gate-source capacitance of 8.4nF, some of the tests are performed while an external gate to source capacitance is added to demonstrate gate current sink capability.

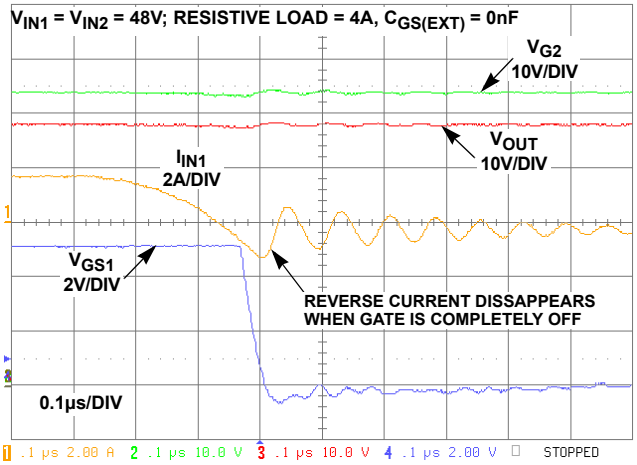


FIGURE 21. FAST SPEED TURN-OFF (MOSFET WITH Q_{TOT} = 8.4nc)

Worst-case turn-off time can be calculated as:

$$t_{toff(WC)} = t_{DELAY(HS)} + \left(C_{GS}\frac{V_{GS}}{I_{PDH}}\right) \qquad \text{(EQ. 9)}$$

$$t_{toff(WC)} = 50ns + \left(39nF\frac{12V}{2A}\right) = 284ns$$

$t_{DELAY(HS)}$ is the High Speed Comparator internal worst-case time delay. The setup in Figure 17 can be used to perform the Input dead-short test; a pulse generator is connected between Gate-Source of Q_{SHORT1} (use pulse mode single shot, set the frequency to <10Hz and pulse width of approximately 10ms, t_{RISE} = 1µs). Follow steps 1 through 5 in the two feed parallel operation section. Make sure that both feeds operate in parallel current sharing mode. Proceed with the short test by applying the single pulse to the gate of Q_{SHORT1}. Once turned on, Q_{SHORT1} shorts V_{IN1} causing it to fall quickly (in less than 10µs). Figures 21, 22 and 23 show the results for different combinations of C_{GS1} and load current. Make sure to connect the V_{IN1} shorting-MOSFET terminals as close as possible to the V_{IN}-GND (J4 to J6) terminals on the EVAL board to minimize lead impedance and reduce parasitic ringing.

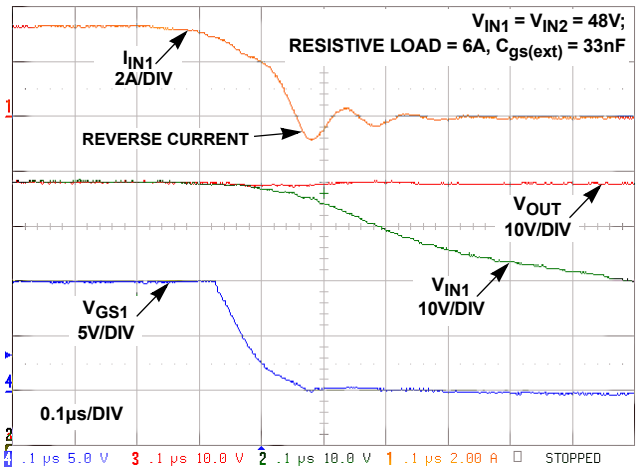


FIGURE 22. FAST SPEED TURN-OFF (MOSFET WITH Q_{TOT} = 8.4nc) AND 33nF EXTERNAL C_{GS}

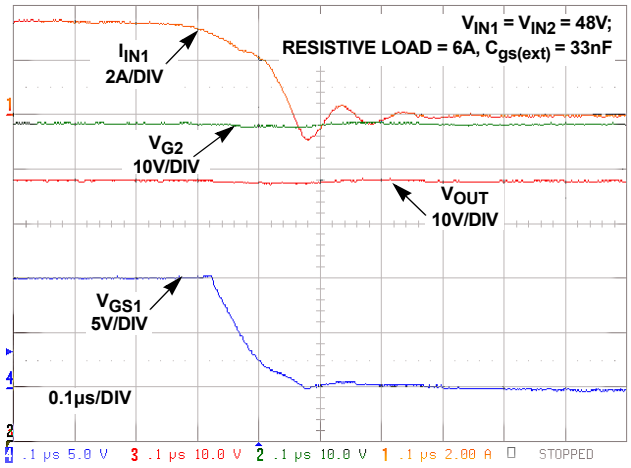


FIGURE 23. FAST SPEED TURN-OFF (MOSFET WITH Q_{TOT} = 8.4nc) AND 33nF EXTERNAL C_{gs}

The ISL6144EVAL1Z board has $V_{TH(HS)}$ of 55mV. It can be changed if performance is found to be unacceptable with this value. $V_{TH(HS)}$ can affect the amplitude of the reverse current (short pulse) that might flow before the gate is effectively turned off (details on how to select $V_{TH(HS)}$ is included in a later section of this application note). The $r_{DS(ON)}$ and internal HS comp offset also contribute to the amplitude of the reverse current pulse. A short event on a single feed may cause ringing on the ground pins, the V_{IN}, and on the V_{OUT} pins. This ringing may cause false turn-off on the healthy feeds. Using decoupling capacitors both at the V_{IN} and V_{OUT} pins help in filtering this high frequency ringing and prevent false turn-off of parallel feeds. Figure 23 shows that the gate of second feed V_{G2} (measured with respect to ground) is not affected when feed 1 input is shorted.

Power Supply Slow Turn-off

In many cases, a single power feed is turned off for diagnosis, maintenance or replacement. The Input voltage drops slowly (most probably in few ms). When voltage at V_{IN} pin starts dropping with respect to V_{OUT} pin. The Hysteretic Regulating Amplifier starts pulling down current (I_{PDL}) opposite to the charge pump current. This reduces the gate voltage gradually until the MOSFET is completely turned off. The slow turn-off is accomplished with zero reverse current. An internal 20µs delay filters out any false trip off due to noise or glitches that might be present on the supply line.

The slow speed turn-off mechanism is shown in Figure 24:

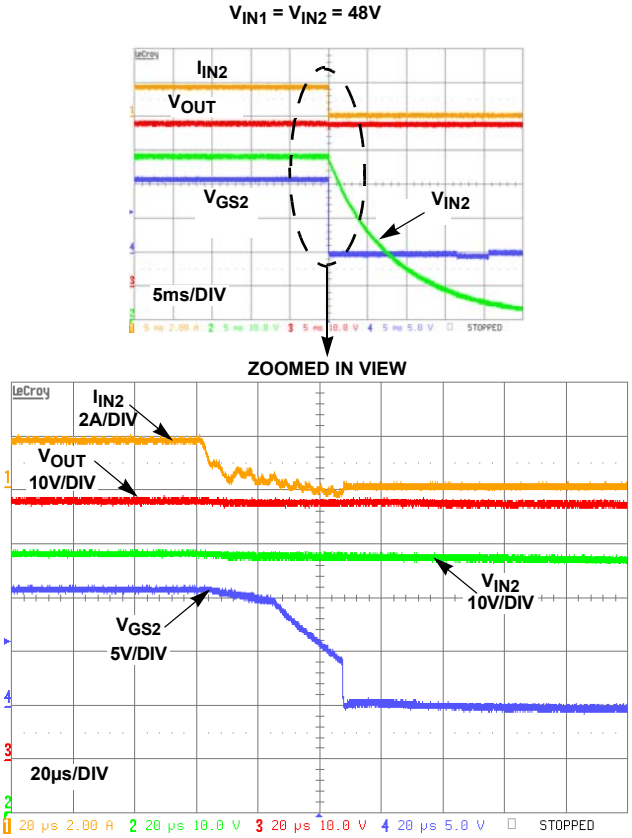


FIGURE 24. SLOW SPEED TURN-OFF (C_{GSTOT} = 8.4nF + 33nF)

Input Voltage is falling at a slow rate (Figure 24, top scope shot shows a 20ms fall time for the input voltage).

V_{OUT} (Common Bus) remains almost unchanged at around 48V. It drops by a value equivalent to the increase in the portion of the load current passing through the remaining feed multiplied by the MOSFET's $r_{DS(ON)}$.

At the beginning of the slow turn-off, the gate drive Voltage V_{GS1} (measured between the Gate and Source of the ORing MOSFET using a differential probe) starts to drop at a slower rate. This is attributed to the effect of the 20µs filtering-delay. Afterwards a stronger pull down current starts and finally the high-speed turn-off completes the gate turn-off. Current through the turned off feed is also shown to be positive and the turn-off is complete with no reverse current.

Figure 25 shows the same slow turn-off for a 12V input voltage case.

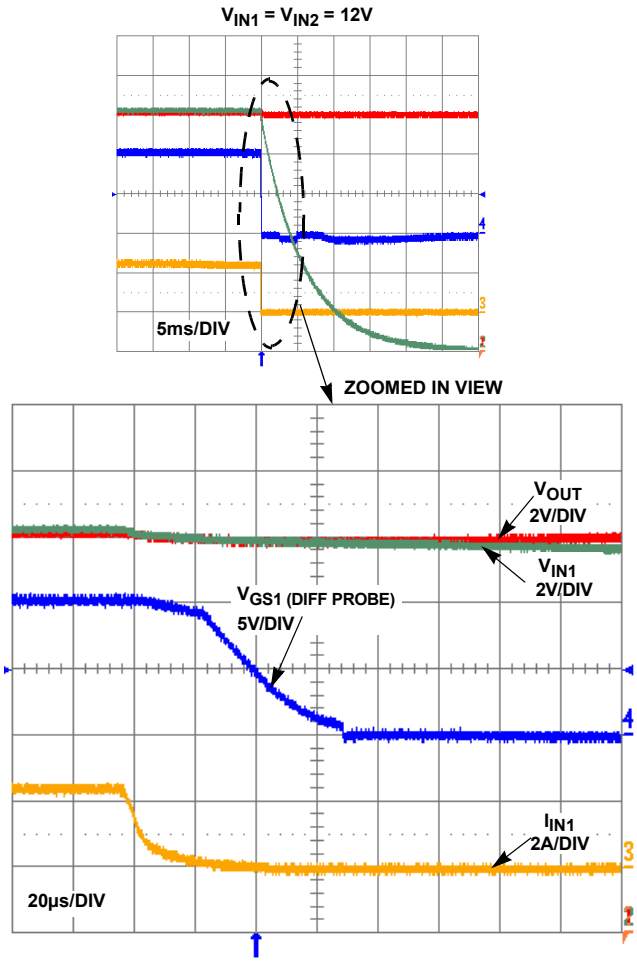


FIGURE 25. SLOW SPEED TURN-OFF (C_{GSTOT} = 8.4nF + 33nF)

Detection of Power Feed Faults

The ISL6144 have two built-in mechanisms that monitor voltages at VIN, VOUT and GATE pins. The first mechanism monitors GATE with respect to VIN (with a 410mV threshold) and the second mechanism monitors V_{IN} with respect to VOUT (with 370mV threshold). The open-drain $\overline{FAULT}$ pin will be pulled low when any of the two above conditions is met.

Some of the typical system faults detected by the ISL6144 are:

Fault 1: Open Fuse at the Input Side

(Fuse has to be placed before the V_{IN} tap, between the power supply and the source of the ORing MOSFET), note that the EVAL board does not have footprint for installing this fuse. This feature can be tested by adding a fuse externally. The open fuse results in near zero current flow through the ORing MOSFET, only a very low current drawn by the IC bias will flow. The voltage at VIN pin is effectively disconnected from the power source and will start dropping slowly. The regulated source-drain voltage falls below its 20mV level and the gate of the MOSFET is pulled down and turned off. GATE will become low and a fault is indicated with internal built in delay (t_{FLT}).

Fault 2: Drain to Source Short

In this case V_{IN} is shorted to V_{OUT}, and in theory the voltage drop across the shorted MOSFET terminals will be close to 0V. The Gate will be pulled down and a fault will be indicated. The resistance of the Drain to Source short multiplied by the Drain short current must be low enough to result in $V_{SD} < V_{FWD_HR}$ (refer to data sheet for worst case values), Otherwise this fault cannot be detected.

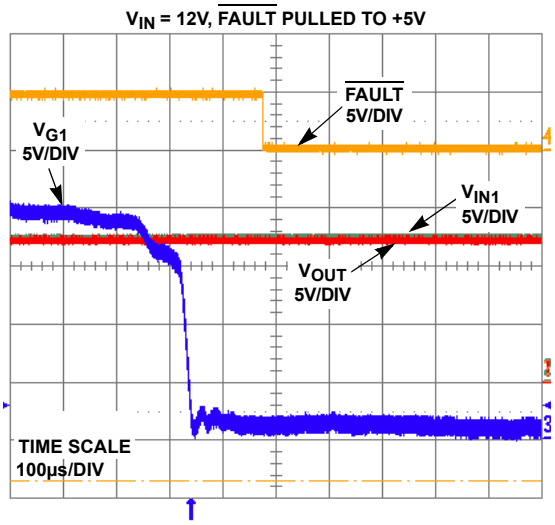


FIGURE 26. MOSFET DRAIN TO SOURCE FAULT

Fault 3: MOSFET Gate to Source Dead Short

GATE voltage will be equal to V_{IN}, GATE $<V_{IN}$ + 0.37V and a fault is indicated.

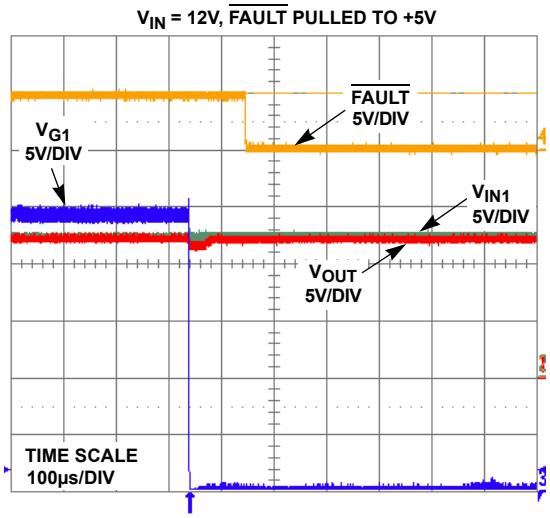


FIGURE 27. MOSFET GATE TO SOURCE FAULT

Fault 4: ORing FET Off Condition

When $V_{IN} < V_{OUT}$, the Gate is off to block reverse current flow. This means that if an ORing feed is not sharing current, a fault will be indicated. Also if a feed (PS) is off while bias is applied from V_{OUT} to that feed, then a fault is also indicated.

Fault 5: MOSFET Gate to Drain Dead Short

In this case, the following condition will be violated GATE $<V_{IN}$ + 0.37V and a fault is issued.

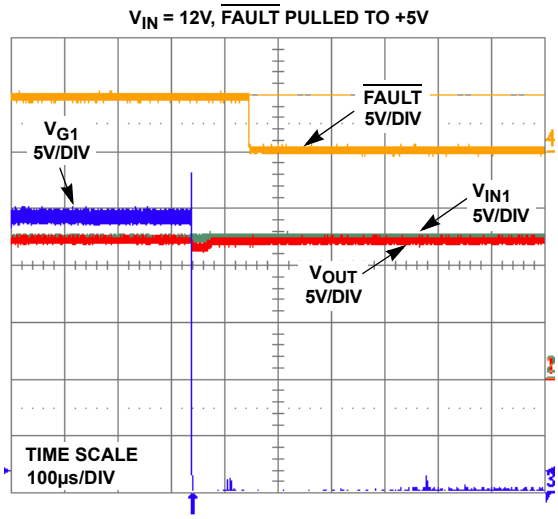


FIGURE 28. MOSFET GATE TO DRAIN FAULT

Fault 6: ORing FET Body Diode Conduction

(V_{IN} - 0.41V > V_{OUT}). If the voltage drop across the MOSFET approaches 410mV, a fault will be indicated. Make sure the selection of the ORing MOSFET takes this fact into account.

Application Considerations and Component Selection

"ISL6144 + ORing FET" vs "ORing Diode" Solution

"ISL6144 + ORing FET" solution is more efficient than the "ORing Diode" Solution, which will result in simplified PCB and thermal design. It will also eliminate the need for a heat sink for the ORing diode. This will result in cost savings. In addition is the fact that the ISL6144 solution provides a more flexible, reliable and controllable ORing functionality and protects against system fault scenarios (Refer to the "Fault Detection Block" on page 8.)

On the other hand the most common failures caused by diode ORing include open circuit and short circuit failures. If one of these diodes (Feed A) has failed open, then the other Feed B will provide all of the power demand. The system will continue to operate without any notification of this failure, reducing the system to a single point of failure. A much more dangerous failure is where the diode has failed short. The system will continue to operate without notification that the short has occurred. With this failure, transients and failures on Feed B propagate to Feed A. Also, this silent short failure could pose a significant safety hazard for technical personnel servicing these feeds.

"ISL6144 + ORing FET" vs "Discrete ORing FET" Solution

If we compare the ISL6144 integrated solution to discrete ORing MOSFET solutions (with similar performance parameters), the ISL6144 wins in all aspects, the main ones being simplicity of an integrated solution, PCB real estate saving, cost savings, and reduction in the MTBF of this section of the circuit as the overall number of components is reduced.

In brief, the solution offered by this IC enhances power system performance and protection while not adding any considerable cost, on the contrary saving PCB board real estate and providing a simple to implement integrated solution.

ORing MOSFET Selection

Using an ORing MOSFET instead of an ORing diode results in increased overall power system efficiency as losses across the ORing elements are reduced. The benefit of using ORing MOSFETs becomes even more significant at higher load currents as power loss and forward voltage drop across the traditionally used ORing diode is increased. The high power dissipation across these diodes requires paralleling of many diodes as well as special thermal design precautions such as heat sinks (heat dissipating pads) and forced airflow.

For example, in a 48V, 32A (1 + 1) redundant system with current sharing, using a Schottky diode as the ORing device (Refer to Figure 29), the forward voltage drop is in the 0.4V to 0.7V range, (let us assume it is 0.5V). The power loss across each diode is shown in Equation 10:

$$P_{loss(D1)} = P_{loss(D2)} = \frac{I_{OUT}}{2} \cdot V_F = 16A \cdot 0.5V = 8W \quad \text{(EQ. 10)}$$

The total power loss across the two ORing diodes is 16W.

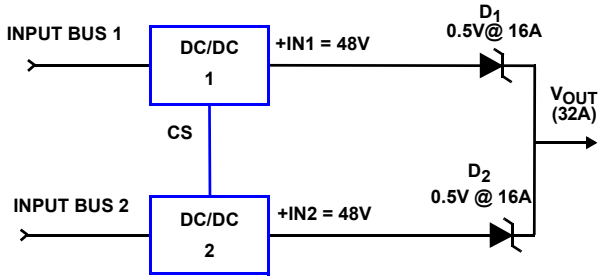


FIGURE 29. 1 + 1 REDUNDANT SYSTEM WITH DIODE ORING

If we use a 4.5mΩ MOSFET (refer to Figure 30), the nominal Power loss across each MOSFET is:

$$P_{loss(M1)} = P_{loss(M2)} = \left(\frac{I_{OUT}}{2}\right)^2 \cdot r_{DS(ON)}$$
$$P_{lossNOM(M1)} = (16A)^2 \cdot 4.5m\Omega = 1.152W \quad \text{(EQ. 11)}$$

The total power loss across the two ORing MOSFETs is 2.304W.

In case of failure of current sharing scheme, or failure of DC/DC 1, the full load will be supplied by DC/DC 2. ORing MOSFET M2 or ORing Diode D_2 will be conducting the full load current. Power lost across the ORing devices are:

$$P_{lossMAX(D2)} = I_{OUT} \cdot V_F = 32A \cdot 0.5V = 16W \quad \text{(EQ. 12)}$$

$$P_{lossMAX(M2)} = (I_{OUT})^2 \cdot r_{DS(ON)} = (32A)^2 \cdot 4.5m\Omega = 4.6W \quad \text{(EQ. 13)}$$

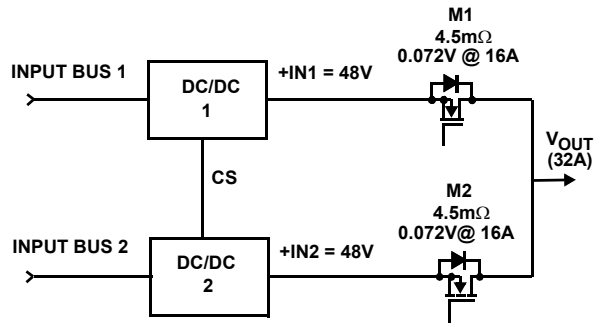


FIGURE 30. 1+1 REDUNDANT SYSTEM WITH MOSFET ORING

This shows that worst-case failure scenario has to be accounted for when choosing the ORing MOSFET. In both cases, more than one ORing MOSFET/diode has to be paralleled on each feed. Using parallel devices reduces power dissipation per device and limits the junction temperature rise to acceptable safe levels. Another alternative is to choose a MOSFET with lower $r_{DS(ON)}$ (Refer to Tables 1 and 2 for some examples).

If parallel MOSFETs are used on each feed, make sure to use the same part number. Also it is preferable to have parts from the same lot to insure load sharing between these paralleled devices.

The final choice of the N-Channel ORing MOSFET depends on the following aspects:

- Voltage Rating: The drain-source breakdown voltage V_{DSS} has to be higher than the maximum input voltage, including transients and spikes. Also, the gate to source voltage rating has to be considered. The ISL6144 maximum Gate charge voltage is 12V. Make sure the used MOSFET has a maximum V_{GS} rating >12V.
- Power Losses: In this application, the ORing MOSFET is used as a series pass element, which is normally fully enhanced at high load currents. Switching losses are negligible. The major losses are conduction losses, which depend on the value of the on-state resistance of the MOSFET $r_{DS(ON)}$, and the per feed load current. For an N + 1 redundant system with perfect current sharing, the per feed MOSFET losses are:

$$P_{loss(FET)} = \left(\frac{I_{LOAD}}{N+1}\right)^2 \cdot r_{DS(ON)} \quad \text{(EQ. 14)}$$

- The final MOSFET selection has to be based on the worse case current when the system is reduced to N parallel supplies due to a permanent failure of one unit. The remaining units have to provide the full load current. In this case, losses across each remaining ORing MOSFET become Equation 15:

$$P_{loss(FET)} = \left(\frac{I_{LOAD}}{N}\right)^2 \cdot r_{DS(ON)} \quad \text{(EQ. 15)}$$

- In the particular cases illustrated in the previous examples of Figures 29 and 30 with N = 1, each of the two ORing feeds have to be able to handle the full load current.
- The MOSFET's $r_{DS(ON)}$ value also depends on junction temperature; a curve showing this relationship is usually part of any MOSFET's data sheet. The increase in the value of the $r_{DS(ON)}$ over-temperature has to be taken into account.
- Current handling capability, steady state and peak, are also two important parameters that must be considered. The limitation on the maximum allowable drain current comes from limitation on the maximum allowable device junction temperature. The thermal board design has to be able to dissipate the resulting heat without exceeding the MOSFET's allowable junction temperature.

Suppose P_{Loss} = 1W in a D2PAK MOSFET, junction to ambient thermal resistance $R_{\theta JA}$ = +43°C/W (with 1 inch^2 copper pad area), T_{JMAX} = +175°C, $r_{DS(ON)}$ = 4.5mΩ, maximum ambient board temperature = +85°C.

We need to make sure that the MOSFET's junction temperature during operation does not exceed the maximum allowable device junction temperature.

$$T_J = T_{A_max} + P_{Loss} \cdot R_{\theta JA}$$

$$T_J = +85°C+1W. +43°C/W = +128°C$$

$$T_J < T_{JMAX}$$

In the example of Figure 30 with a load of 32A, at least 3 MOSFETs with $r_{DS(ON)}$ = 4.5mΩ are paralleled to limit the dissipation to below 1W and operate with safe junction temperature.

Tables 1 and 2 show MOSFET selection for some typical applications with different input voltages and load currents in a 1 + 1 redundant power system (a maximum of 1W of power dissipation across each MOSFET is assumed).

For a 48V Input:

TABLE 1. INPUT VOLTAGE = 48V

I_{Load_Max}	MOSFET PART NUMBER	N (Note 13)
8A	FDB3632 (Note 14) SUM110N10-08 (Note 15)	1 1
16A	FDB3632 (Note 14) SUM110N10-08 FDB045AN08A0 (Note 16)	2 2 1
32A	FDB3632 (Note 14) SUM110N10-08 FDB045AN08A0	4 4 3

NOTES:

13. Number of parallel MOSFETs per feed
14. V_{DSS} = 100V;I_D = 80A; $r_{DS(ON)}$ = 9mΩ
15. V_{DSS} = 100V; I_D = 110A; $r_{DS(ON)}$ = 9.5mΩ
16. V_{DSS} = 75V; I_D = 80A; $r_{DS(ON)}$ = 4.5mΩ

For a 12V to 24V Input:

TABLE 2. INPUT VOLTAGE = 12V TO 24V

I_{Load_Max}	MOSFET PART NUMBER	N
15A	IRF1503S (Note 17) SUM110N03-03P (Note 18) STB100NF03L-03 (Note 19)	1 1 1
40A	IRF1503S SUM110N03-03P STB100NF03L-03	2 2 2
75A	IRF1503S SUM110N03-03P STB100NF03L-03	3 3 3

NOTES:

17. V_{DSS} = 30V; I_D = 190A; $r_{DS(ON)}$ = 3.3mΩ
18. V_{DSS} = 30V; I_D = 110A; $r_{DS(ON)}$ = 2.6mΩ
19. V_{DSS} = 30V; I_D = 100A; $r_{DS(ON)}$ = 3.2mΩ
20. All Above listed $r_{DS(ON)}$ values are at V_{GS} = 10V

Another important consideration when choosing the ORing MOSFET is the forward voltage drop across the drain-source. If this drop approaches the 0.41V limit, (which is used in the V_{OUT} fault monitoring mechanism), this will result in a permanent fault indication. Normally, this voltage drop is chosen to be less than 100mV.

Setting the External HS Comparator Threshold Voltage

Typically, DC/DC modules used in redundant power systems have some form of active current sharing to realize the full benefit of this scheme including lower operating temperatures, lower system failure rate, as well as better transient response when load step is shared. Current sharing is realized using different techniques; all of these techniques will lead to similar modules operating under similar conditions in terms of switching frequency, duty cycle, output voltage and current. When paralleled modules are current sharing, their individual output ripple will be similar in amplitude and frequency and the common bus will have the same ripple as these individual modules and will not cause any of the turn-off mechanisms to be activated as the same ripple will be present on both sensing nodes (V_{IN} and V_{OUT}). This would allow setting the high speed comparator threshold ($V_{TH(HS)}$) to a very low value. As a starting point, a $V_{TH(HS)}$ of 55mV could be used, the final value of this TH will be system dependent and has to be finalized in the system prototype stage. If the gate experiences false turn-off due to system noise, the $V_{TH(HS)}$ has to be increased.

The reverse current peak can be estimated as:

$$I_{REVERSEP} = \frac{V_{TH(HS)} + V_{SD} \pm V_{OS(HS)}}{r_{DS(ON)}}; \text{ where} \qquad \text{(EQ. 16)}$$

V_{SD} is the MOSFET forward voltage drop

$V_{OS(HS)}$ is the voltage offset of HS Comparator

The duration of the reverse current pulse is in the order of a few hundred nanoseconds and is normally kept well below the current rating of the ORing MOSFET.

Reducing the value of $V_{TH(HS)}$ results in lower reverse current amplitude and reduces transients on the common bus voltage.

Just a reminder, this is not an operating scenario, but it is rather a fault scenario and should not occur frequently. As explained above, different power supplies have different noise spectrum and might need adjustment of the $V_{TH(HS)}$.

The following procedure can be used for $V_{TH(HS)}$ selection:

Choose a value of $V_{TH(HS)}$ such that the net HS comparator threshold voltage is positive to allow turn-off only when V_{IN} is lower than COMP. Take into account the worst-case of the HS Comp offset ($V_{OS(HS)}$ = +25mV to -40mV). A good starting value is 55mV. The sum of R_1 and R_2 is not to exceed 50kΩ. It is suggested to choose R_2 = 47.5kΩ and calculate R_1 according to Equation 17:

$$R_1 = \frac{V_{TH(HS)}}{V_{REF(VSET)} - V_{TH(HS)}} R_2 \qquad \text{(EQ. 17)}$$

R_1 = 499Ω

R_1 resistor connected between VOUT and COMP pins

R_2 resistor connected between COMP and VSET pins

$V_{REF(VSET)}$ = 5.3V

1. Operate all parallel feeds in current sharing mode (either by using current sharing techniques or by simply adjusting the voltages very close to each other for natural current sharing).
2. Vary the load current from 1A to its maximum value, monitor the gate voltages, and make sure all gates are on (note that at very light loads the current sharing scheme might stop functioning and only one feed carries this light current, at this point gate voltages will be just above the gate threshold, and even maybe one gate will be on while the others are not).
3. If at medium to maximum load currents all feeds have their gates on, then the chosen $V_{TH(HS)}$ is suitable.
4. If only one feed has its gate on, the threshold value is too low and the gate is turning off due to power supply noise and needs to be increased. Also, the feeds may not be sharing the load current due to discrepancy in output voltages and current sharing failure.
5. Verify the current sharing scheme and output voltages. If the output voltages and currents of each feed are equal but one or more of the gates is still off, increase $V_{TH(HS)}$ by increasing R_1 in 250Ω to 500Ω increments (this increases $V_{TH(HS)}$ by 25mV to 50mV) until all feeds have their FETs turned on.

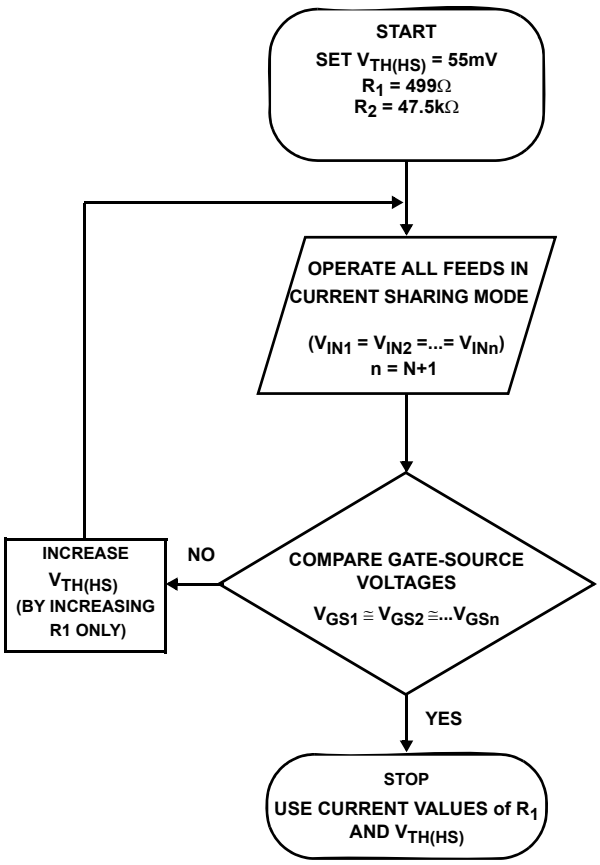


FIGURE 31. SELECTING $V_{TH(HS)}$ VALUE

Configuring ISL6144 for Backup Redundancy (Rail Selector)

The ISL6144 can be used as a rail selector in applications with backup redundancy. In this case, the backup power source voltage (for example battery) should be selected in such a manner that it is lower than the prime source voltage.

Prime_PS > Backup_PS

Also, the voltage difference between the two rails has to be higher than the High Speed Comparator threshold voltage.

Prime_PS - Backup_PS >> $V_{TH(HS)}$

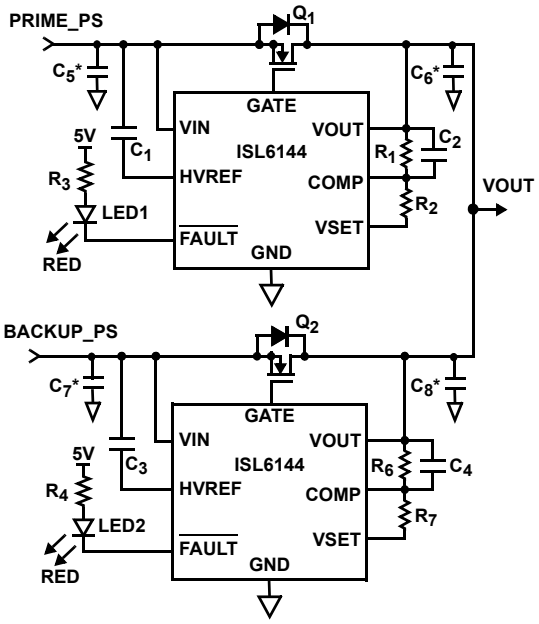


FIGURE 32. USING ISL6144 FOR BACKUP REDUNDANCY

Remote Sense in Redundant Power Systems

Remote output voltage sensing is a feature implemented in most of today's power supplies. This feature is used to compensate for any resistive voltage drops between the power supply output and the load-connection point. The remote sensing pin (RS/+S) must be connected as close as possible to the load in order to compensate for any resistive voltage drops across the power path from the power supply output to the load. The output of many such power supplies can be connected in parallel to provide redundancy and fault tolerance. An ORing device (MOSFET/Diode) is typically used to provide the required isolation of any fault on the power supply side from propagating to the load side. In this case it is not recommended to connect the remote sense pins of the parallel units to the Common Bus point (at load terminals), as this can provide an alternative path for fault currents. The remote sense pins can be connected on the input side of the ORing device to compensate for any drop prior to it. Using an ORing MOSFET (compared to an ORing diode) reduces the forward voltage drop. By using a low $r_{DS(ON)}$ N-Channel ORing MOSFET in redundant power systems, the forward voltage drop can be reduced to less than 100mV. This is another advantage over the ORing diode solution (that has 400mV to 600mV drop) when tight regulation is imposed on the Common Bus voltage. If remote sense is absolutely required, one has to make sure that it will not lead to fault propagation when one power supply output is shorted. The remote sense configuration has to be looked at and design precautions has to be made to make sure the redundancy and fault tolerance are not compromised by the remote sense connection to the Common Bus.

PCB Layout Considerations

The ISL6144EVAL1Z uses a 4 layer PCB with 1oz external layers and 2oz internal layers, dedicated ground and power planes are used to insure good efficiency and EMC performance. Other layer stack-up and thickness is possible depending on the particular power system.

The power traces are designed to handle at least 20A of load per feed. Power and ground planes are made of 2oz copper and external signal/power layers are 1oz copper.

The loop area for all power traces is minimized to reduce parasitic inductance.

A ground island can be created under the IC and connected to the power ground at a single point for reduction of noise that may be injected from the power ground into the IC ground.

Component Selection Summary

Component selection is listed for one feed and is applicable for all other parallel feeds.

R_1, R_2 - are resistors that define the HS comparator threshold voltage used in the high speed turn-off. The sum of R1+ R2 ≅ 50kΩ. R1 and R2 are found using Equation 17.

R_3 - is a pull-up resistor on the $\overline{FAULT}$ pin that can be used if LED1 is not used. $\overline{FAULT}$ is an open drain that can be used to interface with an optocoupler, LED or directly to a logic circuit. This resistor is not populated on the EVAL board.

R_4 - is the $\overline{FAULT}$ pin LED current limit resistor, R4 is chosen to have an LED current of about 4mA.

C_1 - is the HVREF Capacitor, placed between VIN and HVREF pins, this capacitor is necessary to stabilize the $HV_{REF(VZ)}$ supply and a value of 150nF is sufficient. Increasing this value will result in gate turn-on time increase.

C_2 - is the COMP Capacitor, Placed between VOUT and COMP pins to provide filtering and decoupling. A 10nF capacitor is adequate for most cases.

C_5, C_6 - are VIN and VOUT local decoupling capacitors, help immunize the pins against transients that might result in case of fast speed gate turn-off.

Q_1-Q_3 - are ORing MOSFET(s), number of paralleled MOSFETs depends on device $r_{DS(ON)}$, maximum allowable losses and junction temperature of the ORing MOSFETs.

U3 - is Intersil's ISL6144 High Voltage ORing MOSFET Controller IC.

LED1 - is a red LED used to indicate first feed faults. When $V_{IN}1$ is off while V_{OUT} and auxiliary 5V supply are present LED1 will be red.

List of Test Points and Connectors

$V_{IN}1$ - J4

SOURCE1 - TP1, TP17

DRAIN1 - TP2, TP18

GATE1 - TP13

HVREF1 - TP9

COMP1 - TP11

VSET1 - TP10

FAULT1 - TP3

$V_{IN}2$ - J7

SOURCE2 - TP4, TP21

DRAIN2 - TP5, TP22

GATE2 - TP14

HVREF2 - TP8

COMP2 -TP12

VSET2 - TP7

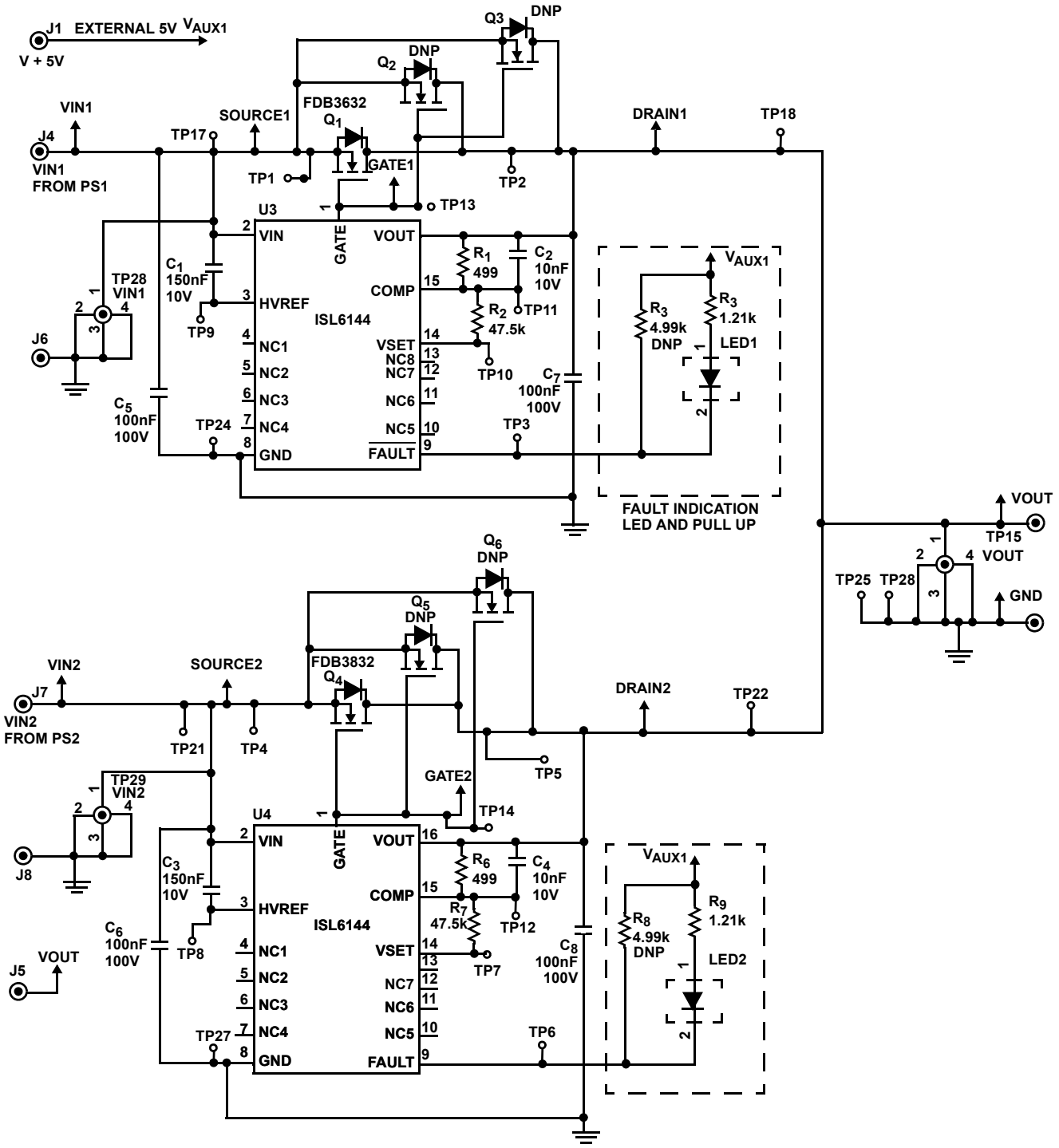
FAULT2 - TP6

V_{OUT} - J2 and J5 (connect to J1 when V_{OUT} replace LED AUX PS)

GND - J3, J6, J8, TP24-TP27

V+5V - (AUX PS for LEDs) - J1

ISL6144EVAL1Z Schematics



Bill of Materials

TABLE 3. BILL OF MATERIALS

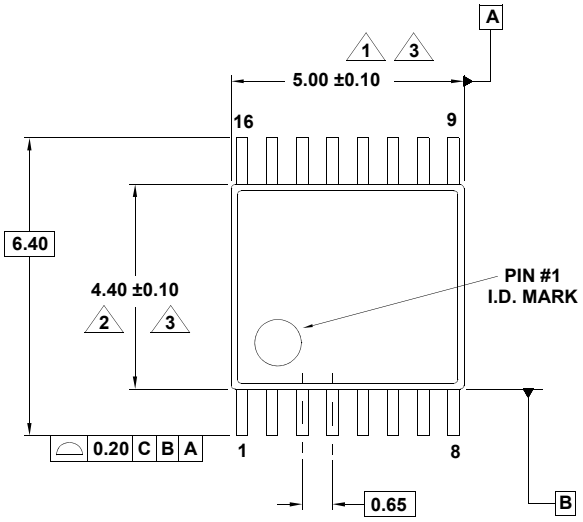
COMPONENT	NAME	SIZE, VALUE, RATING	DESCRIPTION/COMMENTS
CONTROL BOARD BOM			
R_1, R_6	$V_{TH(HS)}$ Programming Resistor	499Ω, RNC55, 1/8W	TH on EVAL board, could be replaced by SMT
R_2, R_7	$V_{TH(HS)}$ Programming Resistor	47.5kΩ, 0603, 1/8W	SMT, 0603
R_3, R_8	$\overline{FAULT}$ Pull-up Resistor	4.99kΩ, 0603, 1/8W	SMT, 0603 (DNP)
R_4, R_9	FAULT LED Current Limit Resistor	1.21kΩ, 0603, 1/8W	SMT, 0603 (used with LED connected to +5V)
LED1	Feed 1 Fault Indication RED LED	Red LED, 0805 ceramic	SMT
LED2	Feed 2 Fault Indication RED LED	Red LED, 0805 ceramic	SMT
C_1, C_3	HVREF Capacitor	150nF, SM1206, 10V	SMT
C_2, C_4	COMP Decoupling Capacitor	10nF, SM0805, 10V	SMT
C_5, C_6	V_{IN} Pin Decoupling Capacitor	100nF, SM1206, 100V	SMT
C_7, C_8	V_{OUT} Pin Decoupling Capacitor	100nF, SM1206, 100V	SMT
Q_1-Q_3	Feed 1 ORing MOSFET(s)	FDB3632, 100V, 9mΩ, D2PAK	Q2, Q3 - DNP (populate for higher current applications if needed)
Q_4-Q_6	Feed 2 ORing MOSFET(s)	FDB3632, 100V, 9mΩ, D2PAK	Q5, Q6 - DNP (populate for higher current applications if needed)
U_3, U_4	ORing MOSFET Controller	ISL6144IV, 10V to 75V	TSSOP16
U_5, U_6	ORing MOSFET Controller	ISL6144IR, 10V to 75V	20 Ld QFN 5x5 - DNP (alternative footprint)

NOTE: DNP = Do Not Populate

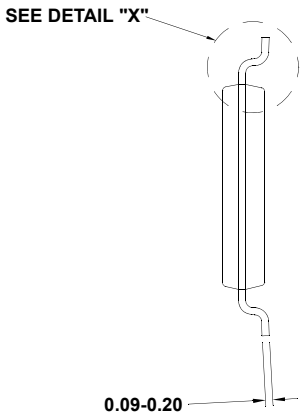
Package Outline Drawing

M16.173

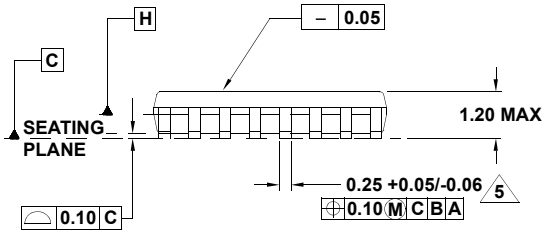
16 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 2, 5/10



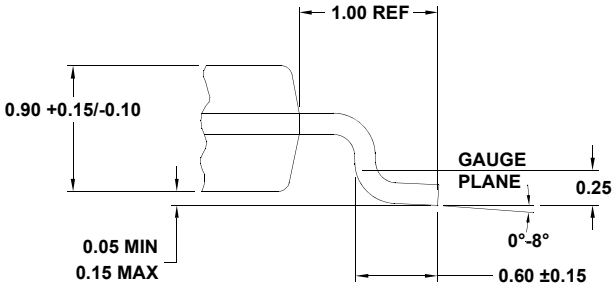
TOP VIEW



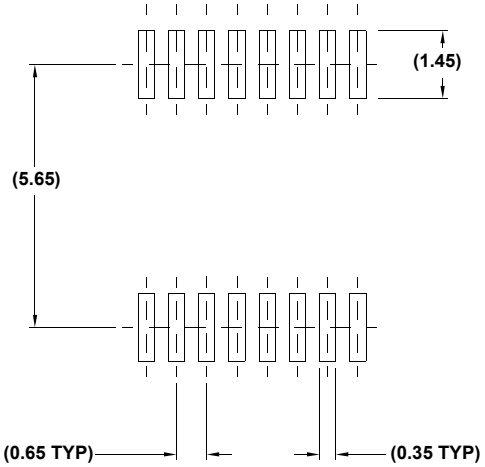
END VIEW



SIDE VIEW



DETAIL "X"

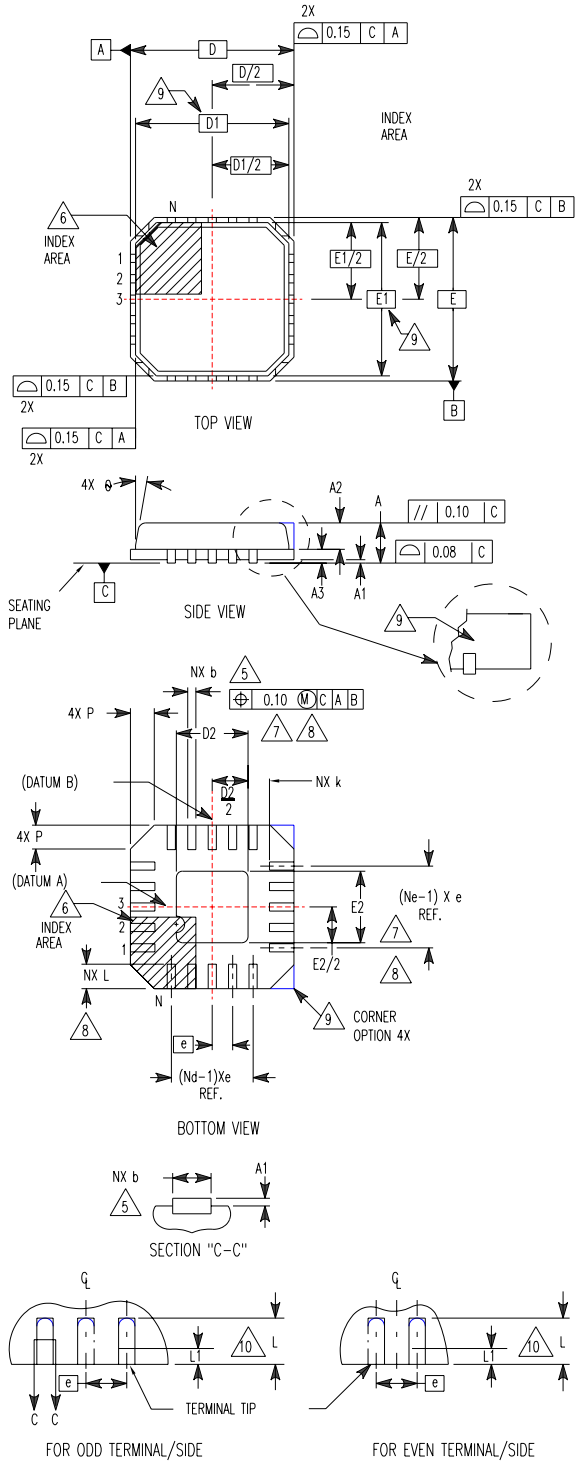


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

Quad Flat No-Lead Plastic Package (QFN) Micro Lead Frame Plastic Package (MLFP)



L20.5x5

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	0.02	0.05	-
A2	-	0.65	1.00	9
A3		0.20 REF		9
b	0.23	0.30	0.38	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7, 8
e		0.65 BSC		-
k	0.20	-	-	-
L	0.35	0.60	0.75	8
N		20		2
Nd		5		3
Ne		5		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Compliant to JEDEC MO-220VHHC Issue I except for the "b" dimension.

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