Advanced PMU for Microcontrollers and Solid State Drive Applications

BENEFITS and FEATURES

- **Wide input voltage range**
  - **Vin = 2.7V to 5.5V**
- **Complete integrated power solution**
  - **One 4A DC/DC Step-Down (Buck) Regulator**
  - **Three 2.5A DC/DC Step-Down (Buck) Regulators**
  - **One 800mA LDO**
  - **Two 200mA LDOs**
- **Space Savings**
  - **Fully integrated**
  - **High Fsw =2.25MHz or 1.125MHz**
  - **Integrated sequencing**
- **Easy system level design**
  - **Configurable sequencing**
  - **Seamless sequencing with external supplies**
- **Buck 1 Bypass Mode for 3.3V system level compliance**
- **Highly configurable**
  - **uP interface for status reporting and controllability**
  - **Programmable Reset and Power Good GPIO's**
  - **Flexible Sequencing Options**
- **I²C Interface – 1MHz**

APPLICATIONS

- Computer Vision
- Microcontroller Applications
- Solid-State Drives
- FPGA
- Video Processor

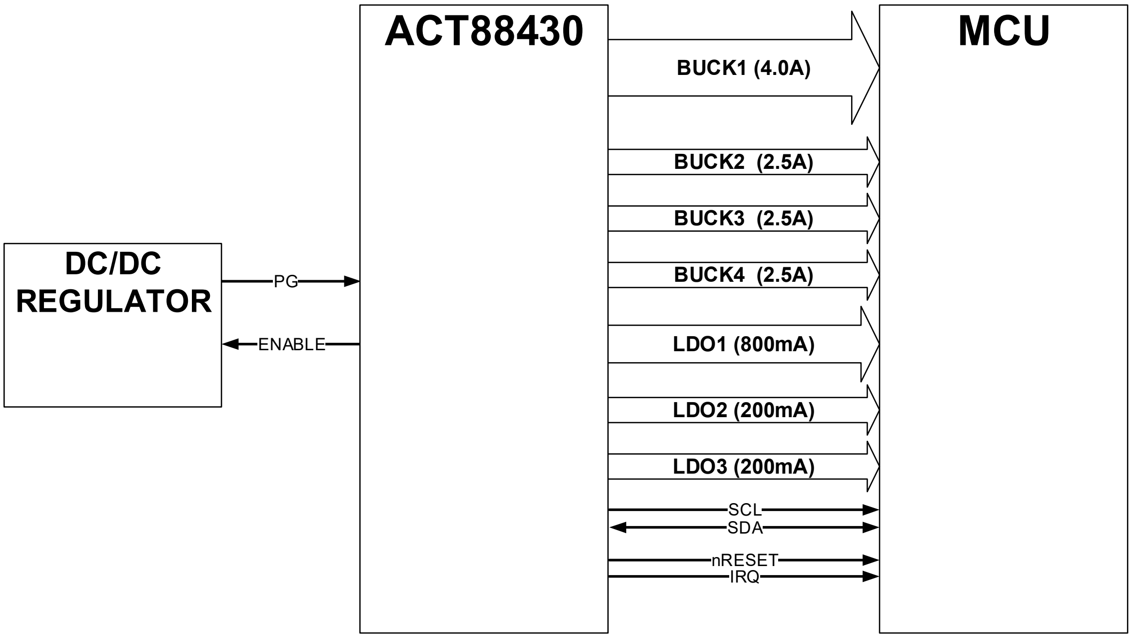
GENERAL DESCRIPTION

The ACT88430 PMIC is an integrated ActivePMU power management unit. It is designed to power a wide range of processors, including video processors, FPGA's, peripherals, microcontrollers, and solid-state drive applications. It is highly flexible and can be reconfigured via I²C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speeds time to market. Examples of configurable options include output voltage, startup time, slew rate, system level sequencing, switching frequency, sleep modes, operating modes etc. ACT88430 is programmed at the factory with default configuration. These settings can be optimized for a specific design through the I²C interface. The ACT88430 comes in several default configuration. Contact the factory for specific default configurations.

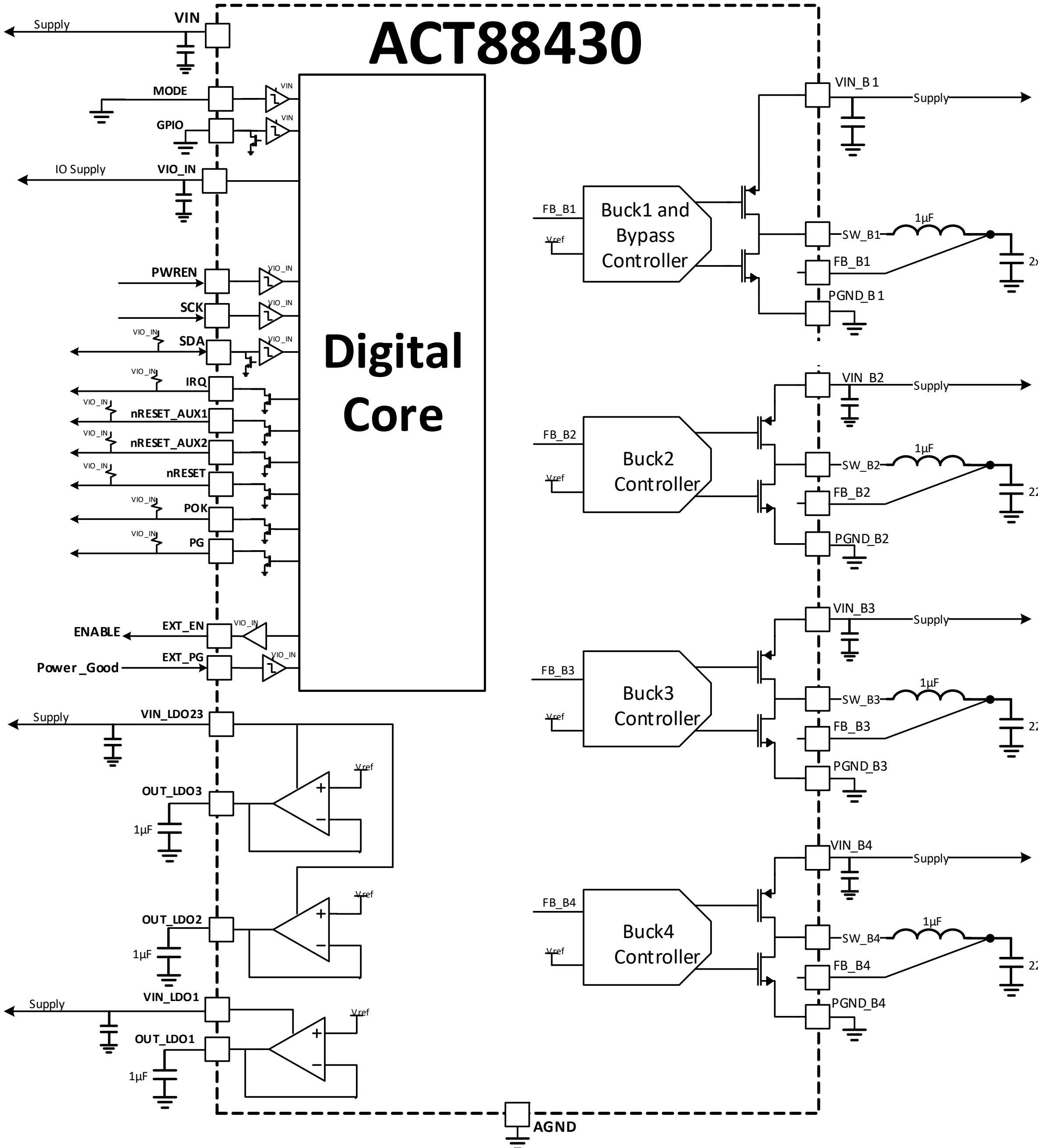
The core of the device includes four DC/DC step down converters using integrated power FETs, three low-dropout regulators (LDOs), and an optional load switch. Each DC/DC regulator switches at 2.25MHz, requiring only three small components for operation. The LDOs only require small ceramic capacitors. All are highly configurable via the I²C interface.

The ACT88430 PMIC is available in a 5 x 5 mm 40 pin QFN package.

Typical Application Diagram

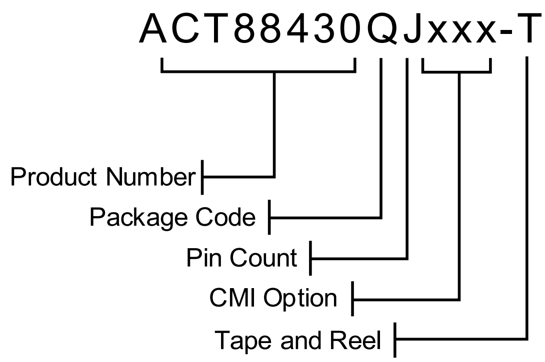


FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{OUT4}	V_{LDO1}	V_{LDO2}	V_{LDO3}	Device ID 0x7Dh	Package
ACT88430QJ101-T	0.95V	0.95V	0.95V	1.2V	1.8V	1.8V	2.5V	0x01h	5x5 40 pin
ACT88430QJ102-T	0.74V	0.88V	1.8V	1.2V	0.9V	1.2V	2.5V	0x00h	5x5 40 pin



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

Note 3: Package Code designator "Q" represents QFN

Note 4: Pin Count designator "J" represents 40 pins

Note 5: "xxx" represents the CMI (Code Matrix Index) option The CMI identifies the IC's default register settings.

PIN CONFIGURATION - QFN

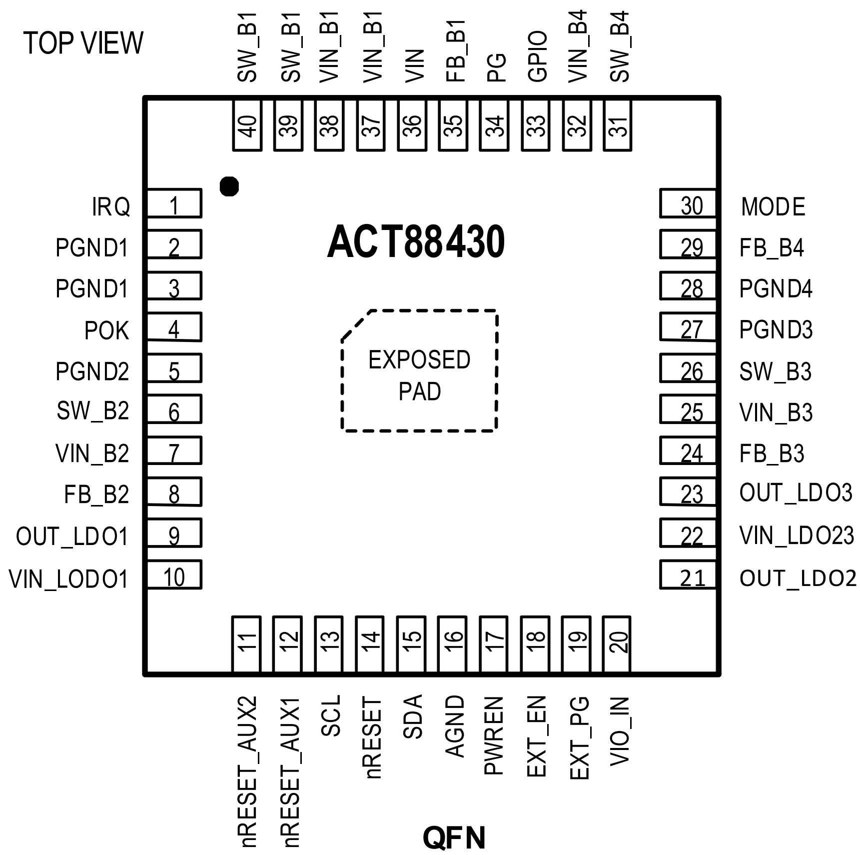


Figure 1: Pin Configuration – Top View – QFN55-40

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	IRQ	Interrupt IRQ Open Drain Output indicates a fault occurred.
2,3	PGND1	Dedicated Power Ground for BUCK1 Regulator.
4	POK	Power OK Open Drain Output, indicates Overvoltage or Undervoltage on VIN input supply.
5	PGND2	Dedicated Power Ground for Buck 2 Regulator.
6	SW_B2	Switch Pin for BUCK2 Regulator.
7	VIN_B2	Dedicated VIN power input for BUCK2 Regulator.
8	FB_B2	Feedback for BUCK2 Regulator. Connect to the BUCK2 output.
9	OUT_LDO1	Output for LDO1 Regulator (Leave unconnected if LDO1 is not used and disabled).
10	VIN_LDO1	Dedicated VIN power input for LDO1 Regulator.
11	nRESET_AUX2	A configurable auxiliary reset signal. Open Drain Output (configurable as an input).
12	nRESET_AUX1	A configurable auxiliary reset signal. Open Drain Output (configurable as an input).
13	SCL	I^2C Clock Input.
14	nRESET	nRESET Open Drain Output. This pin is configurable.
15	SDA	I^2C Data Input and Output.
16	AGND	Analog Ground.
17	PWREN	Power Enable Digital Input. This pin is configurable.
18	EXT_EN	External Regulator Enable Push-Pull Digital Output.
19	EXT_PG	External Power Good Digital Input. This pin is configurable.
20	VIO_IN	Digital Input Reference Voltage Input. Connect a 0.1uF ceramic capacitor between VIN_IN and AGND
21	OUT_LDO2	Output for LDO2 Regulator (Leave unconnected if LDO2 is not used and disabled).
22	VIN_LDO23	Dedicated VIN power input for LDO2 and LDO3 Regulator.
23	OUT_LDO3	Output for LDO3 Regulator (Leave unconnected if LDO3 is not used and disabled).
24	FB_B3	Feedback for BUCK3 Regulator. Connect to the BUCK3 output.
25	VIN_B3	Dedicated VIN power input for BUCK3 Regulator.
26	SW_B3	Switch Pin for BUCK3 Regulator.
27	PGND3	Dedicated Power Ground for BUCK3 Regulator.
28	PGND4	Dedicated Power Ground for BUCK4 Regulator.
29	FB_B4	Feedback for BUCK4 Regulator. Connect to the BUCK4 output.
30	MODE	Configuration input pin. This pin is read at power up to configure BUCK1.
31	SW_B4	Switch Pin for BUCK4 Regulator.
32	VIN_B4	Dedicated VIN power input for BUCK4 Regulator.
33	GPIO	Configurable General purpose input/open drain output.
34	PG	Power Good Output. This pin is configurable. Open Drain Output.
35	FB_B1	Feedback for BUCK1 Regulator. Connect to the BUCK1 output.
36	VIN	Analog Input supply monitored by POK thresholds.
37,38	VIN_B1	Dedicated VIN power input for BUCK1 Regulator.
39,40	SW_B1	Switch pin for BUCK1 Regulator.
Exposed Pad		Tie to Ground Plane for best performance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE	UNIT
All I/O and Power pins except PGND_B1, PGND_B2, PGND_B3, PGND_B4, GND	-0.3 to 6	V
Grounds: Any PGND referenced to GND	-0.3 to +0.3	V
SW_Bx to PGNDx	-0.3 to VIN + 1	V
FB_Bx to PGNDx	-0.3 to VIN + 0.3	V
OUT_LDOx to PGNDx	-0.3 to VINx + 0.3	V
EXT_PG	-0.3 to VIN + 0.3	V
EXT_EN	-0.3 to VIO_IN + 0.3	V
SW1 HBM ESD (Note 2)	-2 to 1.6	kV
Junction to Ambient Thermal Resistance, QFN (Note3)	26	°C/W
Operating Junction Temperature	-40 to 125	°C
Storage Temperature	-55 to 150	°C

Note1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Note2: All other pins meet +/- 2kV HBM ESD

Note3: Measured on Active-Semi Evaluation Kit

RECOMMENDED OPERATING CONDITIONS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN, VIN_B1, VIN_B2, VIN_B3, VIN_B4, VIN_LDO1, VIN_LDO23		2.7		5.5	V
VIO_IN		1.62		5.5	V
VIN_LDO1		2.4		5.5	
VIN_LDO23		1.62		5.5	V
Average lifetime operating current. QFN. (Note 1)	SW_B2,SW_B3,SW_B4 SW_B1			1.6 3.2	A
Operating Junction Temperature		-40		125	°C

Note1: This temperature range is used for lifetime reliability testing.

DIGITAL I/O ELECTRICAL CHARACTERISTICS

(VIN_IO = 1.8V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWREN, EXT_PG Input Low	VIN_IO = 1.8V			0.4	V
PWREN, EXT_PG Input High	VIN_IO = 1.8V	1.25			V
PWREN, EXT_PG Input Low	VIN_IO = 3.3V			1.0	V
PWREN, EXT_PG Input High	VIN_IO = 3.3V	2.3			V
POK, IRQ, nRESET, nRESET_AUX1, nRESET_AUX2, PG_B4 Leakage Current	Output = 5V			1	µA
POK, IRQ, nRESET, nRESET_AUX1, nRESET_AUX2, PG_B4 Output Low	I_{OL} = 5mA			0.35	V
EXT_EN Output Low	I_{OL} = 1mA			0.35	V
EXT_EN Output High	I_{OH} = 1mA	VIO_IN-0.35			V
MODE, GPIO Input Low	V_{VIN} = 3.3V			1.0	V
MODE, GPIO Input High	V_{VIN} = 3.3V	2.3			V
MODE, GPIO Input Low	V_{VIN} = 5.0V			1.5	V
MODE, GPIO Input High	V_{VIN} = 5.0V	3.5			V
EXT_PG, MODE Deglitch Time			10		µs
PWREN Deglitch Time			2		µs

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(VIN_IO = 1.8V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Inputs Voltage Range: VIN_B1 referenced to PGND_B1 VIN_B2 referenced to PGND_B2 VIN_B3 referenced to PGND_B3 VIN_B4 referenced to PGND_B4		2.7		5.5	V
VIN_LDO1 referenced to AGND		2.4		5.5	V
VIN_LDO2 referenced to AGND VIN_LDO3 referenced to AGND		1.62		5.5	V
UVLO Threshold Falling (Note 1)	VIN_LVL=0	2.6	2.7	2.8	V
	VIN_LVL=1, VIN_FULL_RANGE = 0	3.35	3.5	3.65	V
	VIN_LVL=1 VIN_FULL_RANGE = 0	2.6	2.7	2.8	V
UVLO Hysteresis (Note 1)	VIN_LVL=0	50	100	150	mV
	VIN_LVL=1 VIN_FULL_RANGE = 1	250	300	350	mV
	VIN_LVL=1 VIN_FULL_RANGE = 0	50	100	150	mV
OV Threshold Rising (Note 1)	VIN_LVL = 0, VIN_FULL_RANGE = 0	3.86	3.98	4.10	V
	VIN_LVL = 0 VIN_FULL_RANGE = 1	5.60	5.85	6.00	V
	VIN_LVL = 1	5.60	5.85	6.00	V
OV Hysteresis (Note 1)	VIN_LVL = 0, VIN_FULL_RANGE = 0	50	100	150	mV
	VIN_LVL = 0, VIN_FULL_RANGE = 1	100	150	200	mV
	VIN_LVL = 1	100	150	200	mV
Thermal Shutdown Temperature TSD_SHUTDWN	Temperature rising	150	165	180	°C
Thermal Shutdown Hysteresis			20		°C
Startup Delay after initial VIN	start of first regulator output assuming start delay=41usec minimum (Note 2)		335	400	µs
Thermal Interrupt Threshold, TSD_ALERT	Temperature rising - Referenced to TSD_SHUTDWN		TSD_SHUTDWN - 30		°C
Thermal Interrupt Hysteresis			15		°C
POK UV Interrupt Threshold Falling - 3.3V Input Setting (VIN_LVL=0)	POK_SET=00 (91% of 3.3V) POK_SET=01 (88% of 3.3V) POK_SET=10 (84% of 3.3V) POK_SET=11 (Disable)	2.90 2.80 2.67 N/A	3.00 2.90 2.77 N/A	3.10 3.00 2.87 N/A	V

POK UV Interrupt Threshold Falling - 5V Input Setting (VIN_LVL=1, VIN_FULL_RANGE = 0)	POK_SET=00 (88% of 5V) POK_SET=01 (86% of 5V) POK_SET=10 (84% of 5V) POK_SET=11 (Disable)	4.26 4.16 4.06 N/A	4.40 4.30 4.20 N/A	4.54 4.44 4.34 N/A	V
POK OV Interrupt Threshold Falling - 3.3V Input Setting (VIN_LVL= 1, VIN_FULL_RANGE = 1)	POK_SET=00 (91% of 3.3V) POK_SET=01 (88% of 3.3V) POK_SET=10 (84% of 3.3V) POK_SET=11 (Disable)	2.90 2.80 2.67 N/A	3.00 2.90 2.77 N/A	3.10 3.00 2.87 N/A	V
POK OV Interrupt Threshold Rising - 3.3V Input Setting (VIN_LVL=0, VIN_FULL_RANGE = 0)	POK_SET=00 (110% of 3.3V) POK_SET=01 (112% of 3.3V) POK_SET=10 (114% of 3.3V) POK_SET=11 (Disable)	3.53 3.6 3.66 N/A	3.63 3.7 3.76 N/A	3.73 3.8 3.86 N/A	V
POK OV Interrupt Threshold Rising – 5V Input Setting (VIN_LVL=0, VIN_FULL_RANGE = 1)	POK_SET=00 (110% of 5V) POK_SET=01 (112% of 5V) POK_SET=10 (114% of 5V) POK_SET=11 (Disable)	5.33 5.43 5.53 N/A	5.50 5.60 5.70 N/A	5.67 5.77 5.87 N/A	V
POK OV Interrupt Threshold Rising - 5V Input Setting (VIN_LVL=1)	POK_SET=00 (110% of 5V) POK_SET=01 (112% of 5V) POK_SET=10 (114% of 5V) POK_SET=11 (Disable)	5.33 5.43 5.53 N/A	5.50 5.60 5.70 N/A	5.67 5.77 5.87 N/A	V
POK Deglitch Time OV or UV			5		μs

Notes:

1. All Under-voltage Lockout, Overvoltage measurements are referenced to the VIN Input and AGND Pins
2. This delay can be affected by programming sequence, soft-start ramps, and startup delays

BUCK1 ELECTRICAL CHARACTERISTICS, REGULATOR:

(VIN_B1 = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configured for 9.375mV steps	0.6		3.0	V
	Configured for 12.5mV steps	0.8		4.0	
Maximum Output Current		4			A
Supply Current, Standby	Low Power Mode Enabled Regulator Only, No Load (VOUT = VSET*1.05)		50		µA
Supply Current, Shutdown	Regulator Disabled		0.1	1	µA
Output Voltage Accuracy – PWM	Default output voltage, I_{OUT} = 2A	-1%	V_{NOM}	1%	V
Output Voltage Accuracy - PFM	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1%	V_{NOM}	1%	V
Line Regulation	Default output voltage, V_{IN_B1} = 3.3V to 5.5V, PWM mode		0.02		%/V
Load Regulation	Default output voltage, PWM Mode		0.04		%/A
Power Good Threshold	V_{OUT_B1} Rising	92	93	94	%V_{NOM}
Power Good Hysteresis	V_{OUT_B1} Falling		3		%V_{NOM}
Overvoltage Fault Threshold	V_{OUT_B1} Rising	107.5	110	112.5	%V_{NOM}
Overvoltage Fault Hysteresis	V_{OUT_B1} Falling		3		%V_{NOM}
Switching Frequency	V_{OUT_B1} ≥ 20% of V_{NOM}	2.15 1.075	2.25 1.125	2.36 1.18	MHz
Soft-Start Period – Programmable Range	Configurable in 50us Steps 10% to 90% V_{NOM}	150	300	485	µs
Soft-Start Period	Variation from set point	-25		+25	%
Internal High Side Peak Current Limit (Cycle-by-Cycle) ILIMSET	B1_ILIMSET=00 B1_ILIMSET=01 B1_ILIMSET=10 B1_ILIMSET=11		5.3 4.6 3.8 3.0		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIMSET	-10%	ILIMSET	+10%	
	At other set points	-15%	ILIMSET	+15%	
Internal High Side Peak Current Limit, Shutdown Level	Above ILIMSET = 00	+15%	+22.5%	+30%	
	Above ILIMSET = 01	+15%	+22.5%	+30%	
	Above ILIMSET = 10	+15%	+22.5%	+30%	
	Above ILIMSET = 11	+12.5%	+22.5%	+32.5%	
Internal High Side Peak Current Limit, IRQ Triggered Level	Below ILIMSET = 00	-17.5%	-25%	-32.5%	
	Below ILIMSET = 01	-17.5%	-25%	-32.5%	
	Below ILIMSET = 10	-17.5%	-25%	-32.5%	
	Below ILIMSET = 11	-15%	-25%	-35%	
Internal High Side Peak Current Limit IRQ Signal Deglitch Time	16 consecutive clocks at 2.25MHz	6.78	7.11	7.44	µs
PMOS On-Resistance	I_{SW} = -1A, VIN_B1 = 3.3V		0.025	0.040	Ω

NMOS On-Resistance	I_{SW} = 1A, VIN_B1 = 3.3V		0.025	0.045	Ω
SW Leakage Current – NMOS	V_{IN_B1} = 5.5V, V_{SW} = 5.5V			12.5	µA
SW Leakage Current – PMOS	V_{IN_B1} = 5.5V, V_{SW} = 0V			1	µA
Dynamic Voltage Scaling Rate	B1_SLEW=00 B1_SLEW=01 B1_SLEW=10 B1_SLEW=11		Immediate 14.0 3.50 0.88		mV/µs
Switching Rise / Fall Times	V_{IN_B1} = 5V B1_DRVADJ=00 B1_DRVADJ=01 B1_DRVADJ=10 B1_DRVADJ=11		10 / 11.5 6.75 / 8.3 5.25 / 6.5 4 / 5.5		ns
Output Pull Down Resistance	Enabled when regulator disabled	2.75	4.4	8.75	Ohms

BUCK1 ELECTRICAL CHARACTERISTICS, REGULATOR: – BYPASS MODE OPTION

(VIN_B1 = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Bypass Mode					
Input Voltage Range for By-Pass Mode		2.7	3.3	3.7	V
PMOS On-Resistance	I_{SW} = -1A, VIN = 3.3V Max=125°C at $T_{Junction}$		0.025	0.040	Ω
Internal PMOS Current Detection	Triggers Interrupt on IRQ Pin	1.4	3	4.6	A
Internal PMOS Current Detection De-glitch Time			10		µs
Internal PMOS Current Shutdown	Shuts down after deglitch time and stays off for Off Time	4.8	6	7.2	A
Internal PMOS Current Shutdown De-glitch Time			10		µs
Internal PMOS Current Shutdown Off time			100		ms
Internal PMOS Softstart	Only used with 3.3V Input	5.94	6.6	7.26	mV/us

BUCK2 ELECTRICAL CHARACTERISTICS, REGULATORS:

(VIN_B2 = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configured for 9.375mV steps	0.6		3.0	V
	Configured for 12.5mV steps	0.8		4.0	V
Maximum Output Current		2			A
Supply Current, Standby	Low Power Mode Enabled Regulator Only, No Load (VOUT = VSET*1.05)		40		µA
Supply Current, Shutdown	Regulator Disabled		0.1	1	µA
Output Voltage Accuracy – PWM	Default output voltage, I_{OUT} = 1A	-1%	V_{NOM}	1%	V
Output Voltage Accuracy - PFM	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1%	V_{NOM}	1%	V
Line Regulation	Default output voltage, V_{IN_B2} = 3.3V to 5.5V, PWM mode		0.02		%/V
Load Regulation	Default output voltage, PWM Mode		0.04		%/A
Power Good Threshold	V_{OUT_B2} Rising	92	93	94	%V_{NOM}
Power Good Hysteresis	V_{OUT_B2} Falling		3		%V_{NOM}
Overvoltage Fault Threshold	V_{OUT_B2} Rising	107.5	110	112.5	%V_{NOM}
Overvoltage Fault Hysteresis	V_{OUT_B2} Falling		3		%V_{NOM}
Switching Frequency	V_{OUT_B2} ≥ 20% of V_{NOM}	2.15	2.25	2.36	MHz
Soft-Start Period – Programmable Range	Configurable in 50us Steps 10% to 90% V_{NOM}	150	300	485	µs
Soft-Start Period	Variation from set point	-25		+25	%
Internal High Side Peak Current Limit (Cycle-by-Cycle) ILIMSET	B2_ILIMSET=00 B2_ILIMSET=01 B2_ILIMSET=10 B2_ILIMSET=11		N/A 4.0 3.0 2.0		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIMSET	-10%	ILIMSET	+10%	
	At other set points	-15%	ILIMSET	+15%	
Internal High Side Peak Current Limit, Shutdown Level	Above ILIMSET = all settings	+15%	+22.5%	+30%	
nternal High Side Peak Current Limit, IRQ Triggered Level	Below ILIMSET = all settings	-17.5%	-25%	-32.5%	
Internal High Side Peak Current Limit IRQ Signal Deglitch Time	16 consecutive clocks at 2.25MHz	6.78	7.11	7.44	µs
PMOS On-Resistance	I_{sw} = -500mA, VIN_B2 = 3.3V		0.08		Ω
NMOS On-Resistance	I_{sw} = 500mA, VIN_B2 = 3.3V		0.05		Ω
SW Leakage Current – NMOS	V_{IN_B2} = 5.5V, V_{SW} = 5.5V			1	µA
SW Leakage Current – PMOS	V_{IN_B2} = 5.5V, V_{SW} = 0V			1	µA
Dynamic Voltage Scaling Rate	B2_SLEW=00 B2_SLEW=01 B2_SLEW=10 B2_SLEW=11		Immediate 14.0 3.50 0.88		mV/µs
Switching Rise / Fall Times	V_{IN_B2} = 5V		3 / 5.5		ns

	B2_DRVADJ=00 B2_DRVADJ=01 B2_DRVADJ=10 B2_DRVADJ=11		2.6 / 3.7 2.4 / 3.3 2.3 / 3.0		
Output Pull Down Resistance	Enabled when regulator disabled	6.25	9.40	20	Ohms

BUCK3 ELECTRICAL CHARACTERISTICS, REGULATORS:

(VIN_B3 = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configured for 9.375mV steps	0.6		3.0	V
	Configured for 12.5mV steps	0.8		4.0	V
Maximum Output Current		2			A
Supply Current, Standby	Low Power Mode Enabled Regulator Only, No Load (VOUT = VSET*1.05)		40		µA
Supply Current, Shutdown	Regulator Disabled		0.1	1	µA
Output Voltage Accuracy – PWM	Default output voltage, I_{OUT} = 1A	-1%	V_{NOM}	1%	V
Output Voltage Accuracy - PFM	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1%	V_{NOM}	1%	V
Line Regulation	Default output voltage, V_{IN_B3} = 3.3V to 5.5V, PWM mode		0.02		%/V
Load Regulation	Default output voltage, PWM Mode		0.04		%/A
Power Good Threshold	V_{OUT_B3} Rising	92	93	94	%V_{NOM}
Power Good Hysteresis	V_{OUT_B3} Falling		3		%V_{NOM}
Overvoltage Fault Threshold	V_{OUT_B3} Rising	107.5	110	112.5	%V_{NOM}
Overvoltage Fault Hysteresis	V_{OUT_B3} Falling		3		%V_{NOM}
Switching Frequency	V_{OUT_B3} ≥ 20% of V_{NOM}	2.15	2.25	2.36	MHz
Soft-Start Period – Programmable Range	Configurable in 50us Steps 10% to 90% V_{NOM}	150		485	µs
Soft-Start Period	Variation from set point	-25		+25	%
Internal High Side Peak Current Limit (Cycle-by-Cycle) ILIMSET	B3_ILIMSET=00 B3_ILIMSET=01 B3_ILIMSET=10 B3_ILIMSET=11		N/A 4.0 3.0 2.0		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIMSET	-10%	ILIMSET	+10%	
	At other set points	-15%	ILIMSET	+15%	
Internal High Side Peak Current Limit, Shutdown Level	Above ILIMSET = all settings	+15%	+22.5%	+30%	
Internal High Side Peak Current Limit, IRQ Triggered Level	Below ILIMSET = all settings	-17.5%	-25%	-32.5%	
Internal High Side Peak Current Limit IRQ Signal Deglitch Time	16 consecutive clocks at 2.25MHz	6.78	7.11	7.44	µs
PMOS On-Resistance	I_{SW} = -500mA, VIN_B3 = 3.3V		0.08		Ω
NMOS On-Resistance	I_{SW} = 500mA, VIN_B3 = 3.3V		0.05		Ω
SW Leakage Current – NMOS	V_{IN_B3} = 5.5V, V_{SW} = 5.5V			1	µA
SW Leakage Current – PMOS	V_{IN_B3} = 5.5V, V_{SW} = 0V			1	µA
Dynamic Voltage Scaling Rate	B3_SLEW=00 B3_SLEW=01 B3_SLEW=10 B3_SLEW=11		Immediate 14.0 3.50 0.88		mV/µs
Switching Rise / Fall Times	V_{IN_B3} = 5V		3 / 5.5		ns

	B3_DRVADJ=00 B3_DRVADJ=01 B3_DRVADJ=10 B3_DRVADJ=11		2.6 / 3.7 2.4 / 3.3 2.3 / 3.0		
Output Pull Down Resistance	Enabled when regulator disabled	6.25	9.40	20	Ohms

BUCK4 ELECTRICAL CHARACTERISTICS, REGULATORS:

(VIN_B4 = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configurable in 12.5mV steps	0.8		4.0	V
Maximum Output Current		2			A
Supply Current, Standby	Low Power Mode Enabled Regulator Only, No Load (VOUT = VSET*1.05)		40		µA
Supply Current, Shutdown	Regulator Disabled		0.1	1	µA
Output Voltage Accuracy – PWM	Default output voltage, I_{OUT} = 2A	-1%	V_{NOM}	1%	V
Output Voltage Accuracy - PFM	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1%	V_{NOM}	1%	V
Line Regulation	Default output voltage, V_{IN_B4} = 3.3V to 5.5V, PWM mode		0.02		%/V
Load Regulation	Default output voltage, PWM Mode		0.04		%/A
Power Good Threshold	V_{OUT_B4} Rising	94	95	96	%V_{NOM}
Power Good Hysteresis	V_{OUT_B4} Falling		2		%V_{NOM}
Overvoltage Fault Threshold	V_{OUT_B4} Rising	107.5	110	112.5	%V_{NOM}
Overvoltage Fault Hysteresis	V_{OUT_B4} Falling		3		%V_{NOM}
Switching Frequency	V_{OUT_B4} ≥ 20% of V_{NOM}	2.15	2.25	2.36	MHz
Soft-Start Period – Programmable Range	Configurable in 25us steps 10% to 90% V_{NOM}	25		204	µs
Soft-Start Period	Variation from set point	-25		+25	%
Internal High Side Peak Current Limit (Cycle-by-Cycle) ILIMSET	B4_ILIMSET=00 B4_ILIMSET=01 B4_ILIMSET=10 B4_ILIMSET=11		N/A 4.0 3.0 2.0		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIMSET	-10%	ILIMSET	+10%	
	At other set points	-15%	ILIMSET	+15%	
Internal High Side Peak Current Limit, Shutdown Level	Above ILIMSET = all settings	+15%	+22.5%	+30%	
nternal High Side Peak Current Limit, IRQ Triggered Level	Below ILIMSET = all settings	-17.5%	-25%	-32.5%	
Internal High Side Peak Current Limit IRQ Signal Deglitch Time	16 consecutive clocks at 2.25MHz	6.78	7.11	7.44	µs
PMOS On-Resistance	I_{SW} = -500mA, VIN_B4 = 3.3V		0.08		Ω
NMOS On-Resistance	I_{SW} = 500mA, VIN_B4 = 3.3V		0.05		Ω
SW Leakage Current – NMOS	V_{IN_B4} = 5.5V, V_{SW} = 5.5V			1	µA
SW Leakage Current – PMOS	V_{IN_B4} = 5.5V, V_{SW} = 0V			1	µA
Dynamic Voltage Scaling Rate	B1_SLEW=00 B1_SLEW=01 B1_SLEW=10 B1_SLEW=11		Immediate 14.0 3.50 0.88		mV/µs
Switching Rise / Fall Times	V_{IN_B4} = 5V B1_DRVADJ=00 B1_DRVADJ=01		3 / 5.5 2.6 / 3.7 2.4 / 3.3		ns

	B1_DRVADJ=10 B1_DRVADJ=11		2.3 / 3.0		
Output Pull Down Resistance	Enabled when regulator disabled	6.25	9.40	20	Ohms

LDO1 ELECTRICAL CHARACTERISTICS

(VIN_LDO1 = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.4		5.5	V
Output Voltage Range	Configurable in 25mV steps	0.8		4	V
Output Current	V_{IN_LDO1} = 2.7V to 5.5V, LDO1_ILIM=11	0.75			A
	V_{IN_LDO1} = 2.4V to 2.7V, LDO1_ILIM=1X	0.4			A
Output Voltage Accuracy	At default output voltage setting V_{IN_LDO1} - V_{LDO1_OUT} > 0.4V	-1	V_{NOM}	1	%
Line Regulation	V_{IN_LDO1} - V_{LDO1_OUT} > 0.4V V_{IN_LDO1} = 2.7V to 5.5V I_{LDO1_OUT} = 1mA		0.005		% / V
Load Regulation	I_{LDO1_OUT} = 1mA to 750mA		0.15		% / A
Supply Current	Regulator Enabled No Load		25	42	µA
	Regulator Disabled		0	1	
Soft-Start Period	LDO1_SS=00 (Default) LDO1_SS=01 V_{LDO1_OUT} = 10% to 90% LDO1_SS=10 V_{LDO1_OUT} = 1.8V Setting LDO1_SS=11		226 323 440 570		µs
Power Good Threshold	V_{LDO1_OUT} Rising	92	93	94	%V_{NOM}
Power Good Hysteresis	V_{LDO1_OUT} Falling		3		%V_{NOM}
Overvoltage Fault Threshold	V_{LDO1_OUT} Rising	107.5	110	112.5	%V_{NOM}
Overvoltage Fault Hysteresis	V_{LDO1_OUT} Falling		3		%V_{NOM}
Discharge Resistance	Enabled when regulator disabled	10	25	75	Ω
Dropout Voltage	I_{LDO1_OUT} = 200mA, V_{IN_LDO1} > 2.7V			200	mV
	I_{LDO1_OUT} = 400mA, LDO1_ILIM=1X			300	mV
	I_{LDO1_OUT} = 750mA V_{IN_LDO1} > 2.7V LDO_ILIM=11			400	mV
Output Current Limit	LDO1_ILIM=00 LDO1_ILIM=01 LDO1_ILIM=10 LDO1_ILIM=11	-15%	350 500 630 1000	+15%	mA
Startup Delay	Additional startup delay required before soft start ramp LDO1_SS=00	31	44	65	µs

LDO1 ELECTRICAL CHARACTERISTICS – LOAD SWITCH

(VIN_LDO1 = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
PMOS On-Resistance	VINL1 = 2.7V, VOUT_L1_SET = 3V, I_Load = 200mA		180	220	mΩ
Output Current	V_{IN_LDO1} = 2.7V to 5.5V, LDO1_ILIM=11	0.75			A
Supply Current per Output	Load Switch Enabled No Load		25	42	µA
	Load Switch Disabled		0	1	µA
Soft-Start Period	LDO1_SS=00 LDO1_SS=01 V_{LDO1_OUT} = 10% to 90% LDO1_SS=10 V_{LDO1_OUT} = 1.8V Setting LDO1_SS=11		226 323 440 570		µs
Output Current Limit	LDO1_ILIM=00 LDO1_ILIM=01 LDO1_ILIM=10 LDO1_ILIM=11	-15%	350 500 630 1000	+15%	mA

LDO2 ELECTRICAL CHARACTERISTICS

(VIN_LDO23 = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		1.62		5.5	V
Output Voltage Range	LDO2_RANGE=0 Configurable in 25mV steps	2.000		3.575	V
	LDO2_RANGE=1 Configurable in 25mV steps	0.800		2.375	V
Output Current	V_{IN_LDO23} = 2.7V to 5.5V, LDO2_ILIM=1X	0.1			A
Output Voltage Accuracy	At default output voltage setting V_{IN_LDO23} - V_{LDO2_OUT} > 0.4V	-1	V_{SET}	1	%
Output Voltage Accuracy	At default output voltage setting V_{IN_LDO23} - V_{LDO2_OUT} > 0.4V	-2	V_{SET}	2	%
Line Regulation	V_{IN_LDO23} - V_{LDO2_OUT} > 0.4V V_{IN_LDO23} = 2.7V to 5.5V I_{LDO2_OUT} = 1mA		0.007		% / V
Load Regulation	I_{LDO2_OUT} = 1mA to 100mA, LDO2_ILIM=1X		-1		% / A
Supply Current (each LDO output)	Regulator Enabled, No Load		15		µA
	Regulator Disabled		0	1	µA
Soft-Start Period	LDO2_SS=00 V_{LDO2_OUT} = 10% to 90% LDO2_SS=01 V_{LDO2_OUT} = 2.5V Setting LDO2_SS=10 LDO2_SS=11	60 90 135 180	130 133 170 220	255 255 255 270	µs
Power Good Threshold	V_{LDO2_OUT} Rising	92	93	94	$\%V_{NOM}$
Power Good Hysteresis	V_{LDO2_OUT} Falling		3		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{LDO2_OUT} Rising	107.5	110	112.5	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{LDO2_OUT} Falling		3		$\%V_{NOM}$
Dropout	ILDO2_OUT = 150mA V_{IN_LDO23} > 2.7V LDO2_ILIM=11			200	mV
Discharge Resistance	Enabled when regulator disabled	20	50	125	Ω
Output Current Limit	LDO2_ILIM=00 LDO2_ILIM=01 LDO2_ILIM=10 LDO2_ILIM=11	-35%	110 150 210 315	+35%	mA
Startup Delay	Additional startup delay required before soft start ramp LDO2_SS=01	20	36	55	µs

LDO3 ELECTRICAL CHARACTERISTICS

(VIN_LDO23 = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		1.62	2.7	5.5	V
Output Voltage Range	LDO3_RANGE=0 Configurable in 25mV steps	2.0		3.575	V
	LDO3_RANGE=1 Configurable in 25mV steps	0.8		2.375	V
Output Current	V_{IN_LDO23} = 1.8V to 5.5V, LDO3_ILIM=11	160			mA
Output Voltage Accuracy	V_{IN_LDO23} - V_{LDO3_OUT} > 0.4V	-1	V_{NOM}	1	%
Line Regulation	V_{IN_LDO23} - V_{LDO3_OUT} > 0.4V V_{IN_LDO23} = 2.7V to 5.5V I_{LDO3_OUT} = 1mA		0.01		% / V
Load Regulation	I_{LDO3_OUT} = 1mA to 100mA, LDO3_ILIM=1X		-1.8		% / A
Power Supply Rejection Ratio			See Graphs		dB
Supply Current (each LDO output)	Regulator Enabled No Load		15		µA
	Regulator Disabled		0	1	µA
Soft-Start Period	LDO3_SS=00 V_{OUT} = EN to POK LDO3_SS=01 V_{OUT} = 0.9V Setting LDO3_SS=10 LDO3_SS=11	15 40 60 80	36 64 96 126	60 90 140 180	µs
Power Good Threshold	V_{LDO3_OUT} Rising	92	93	94	%V_{NOM}
Power Good Hysteresis	V_{LDO3_OUT} Falling		3		%V_{NOM}
Overvoltage Fault Threshold	V_{LDO3_OUT} Rising	107.5	110	112.5	%V_{NOM}
Overvoltage Fault Hysteresis	V_{LDO3_OUT} Falling		3		%V_{NOM}
Discharge Resistance	Enabled when regulator disabled	20	50	125	Ω
Dropout Voltage	I_{LDO3_OUT} = 150mA V_{IN_LDO3} > 1.8V LDO3_ILIM=11			500	mV
Output Current Limit	LDO3_ILIM=00 LDO3_ILIM=01 LDO3_ILIM=10 LDO3_ILIM=11	-35% -35% -35% -28.5%	130 183 255 390	+35%	mA
Startup Delay	Additional startup delay required before soft start ramp LDO3_SS=01	8	16	25	µs

OVERALL SYSTEM TIMING REQUIREMENTS

(Full timing requirements to follow)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Regulator Programmable Startup Delay Timings between turn on events	ONDLY=000 ONDLY=001 ONDLY=010 ONDLY=011 ONDLY=100 ONDLY=101 ONDLY=110 ONDLY=111	32.6 101 196 291 386 481 576 671	41 113 213 313 413 513 613 713	88 165 270 375 480 585 690 795	µs
nRESET Delay Timing Programming Range		199		996	µs
nRESET_AUX1 Delay Timing Programming Range		398		1991	
nRESET_AUX2 Delay Timing Programming Range		57		882	µs
nRESET, nRESET_AUX2 Min Delay Timing[1]	Setting nRST_DLY=110 Setting nRESET_AUX2=111	40		60	µs
nRESET Max Delay Timing[1]	Setting nRST_DLY=111	920	996	1080	µs
nRESET_AUX1 Max Delay Timing[1]	Setting nRESET_AUX1_DLY=110	823	882	942	µs

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{IO_IN} = 1.8V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{IO_IN} = 1.8V			0.4	V
SCL, SDA Input High	V_{IO_IN} = 1.8V	1.25			V
SCL, SDA Input Low	V_{IO_IN} = 3.3V			1.0	V
SCL, SDA Input High	V_{IO_IN} = 3.3V	2.3			V
SDA Leakage Current	SDA=5V			1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Frequency, f_{SCL}		0		1000	kHz
SCL Low Period, t_{LOW}		0.5			µs
SCL High Period, t_{HIGH}		0.26			µs
SDA Data Setup Time, t_{SU}		50			ns
SDA Data Hold Time, t_{HD}	(Note1)	0			ns
Start Setup Time, t_{ST}	For Start Condition	260			ns
Stop Setup Time, t_{SP}	For Stop Condition	260			ns
Capacitance on SCL or SDA Pin				10	pF
SDA Fall Time SDA, T_{of}	Device requirement			120	ns
Pulse Width of spikes must be suppressed on SCL and SDA		0		50	ns

Note1: Comply to I²C timings for 1MHz operation - “Fast Mode Plus”.
Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering RESET, IDLE, OVUVFLT, and THERMAL states to clear any transactions that may have been occurring when entering the above states.
Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the device.
Note4: Device Address is 7’h5A

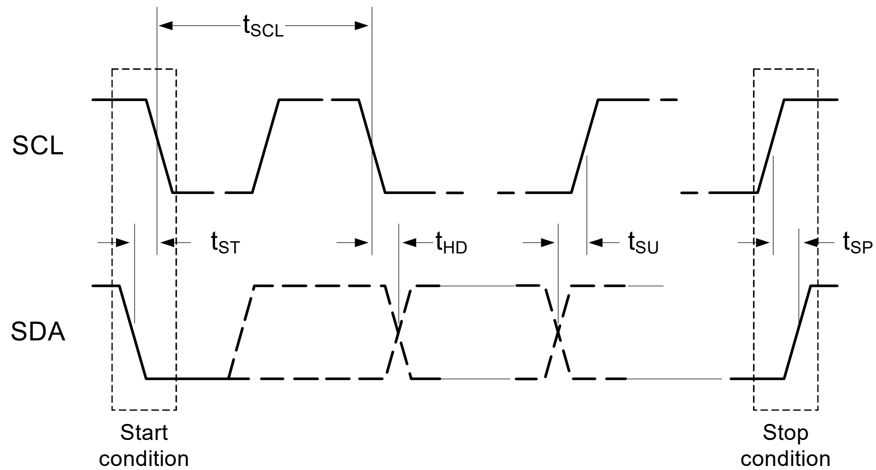


Figure 2: I²C Data Transfer

SYSTEM CONTROL INFORMATION

General

The ACT88430 is a single-chip integrated power management solution designed to power many processors. It integrates four highly efficient buck regulators, three LDOs, and an integrated load bypass switch. Its high integration and high switching frequency result in an extremely small footprint and lost power solution. It contains a master controller that manages startup sequencing, timing, voltages, slew rates, sleep states, and fault conditions. I²C configurability allows system level changes without the need for costly PCB changes. The built-in load bypass switch enables full sequencing configurability in 3.3V systems.

The ACT88430 master controller monitors all outputs and reports faults via I²C and hardwired status signals. Faults can masked and fault levels and responses are configurable via I²C.

Many of the ACT88430 pins and functions are configurable. The IC's default functionality is defined by the default CMI (Code Matrix Index), but much of this functionality can be changed via I²C. The first part of the datasheet describes basic IC functionality and default pin functions. The end of the datasheet provides the configuration and functionality specific to each CMI version. Contact sales@active-semi.com for additional information about other configurations.

I₂C Serial Interface

To ensure compatibility with a wide range of systems, the ACT88430 uses standard I²C commands. The ACT88430 always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. As an example, the 7-bit slave address 0x5Ah follows the format 1011010x where "x" is a 0 for write operation and 1 for a read operation. This results in 0xB4h for write operations and 0xB5h for read operations. Refer to each specific CMI for the IC's slave address

There is no timeout function in the I²C packet processing state machine, however, any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet.

The ACT88430 holds the I²C state machine in reset during the RESET, Idle, OVUVFLT, and THERMAL states to avoid a corruption of registers when the voltage regulators are out of spec.

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pullup resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics Table.

Table 1: ACT88430 I²C Addresses

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x53h	101 0011b	0xA6h	0xA7h
0x55h	101 0101b	0xAAh	0xABh
0x5Ah	101 1010b	0xB4h	0xB5h
0x5Bh	101 1011b	0xB6h	0xB7h

I²C Registers

The ACT88430 has an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, switching frequency, fault thresholds, fault masks, etc. These registers give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult sales@active-semi.com for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected device behavior.

State Machine

The ACT88430 contains an internal state machine with five internal states.

RESET State

In the RESET, or "cold" state, the ACT88430 is waiting for the input voltage on VIN to be within a valid range defined by I²C bits POK_OV_SET and POK_UV_SET. All regulators are off in RESET. nRESET, nRESET_AUX1, and nRESET_AUX2 are asserted low. All volatile registers are reset to defaults and Non-Volatile registers are reset to programmed defaults. The IC transitions from RESET to ACTIVE when the input voltage enters the valid range. The IC transitions from any other state to RESET if the input voltage drops below the UVLO threshold voltage.

ACTIVE State

The ACTIVE state is the normal operating state when the input voltage is within the allowable range, all outputs are turned on, and no faults are present. When entering the ACTIVE state from the RESET state, all regulators are powered on following their programmed power up sequence. The regulators are not sequenced when entering ACTIVE from SLEEP.

SLEEP State

The SLEEP state is a low power mode for the operating system. Each output can be programmed to be on or off in the SLEEP state. The outputs do not follow any sequencing when turning on or off as they enter or exit the SLEEP state. They do turn on with their programmed softstart time. Buck1/2/3/4 can be programmed to regulate to their VSET0 voltage, VSET1 voltage, or be turned off in the SLEEP state. LDO1/2/3 can be programmed to regulate to their VSET0 voltage or can be programmed to be turned off. Note that LDO1/2/3 do not have a VSET1 voltage.

The IC can enter SLEEP via a hardware input pin or an I²C command. The hardware input is typically the PWREN pin, but this can be reconfigured to other pins. To enable SLEEP via I²C, program the following:

Set register 0x08h bit1 (PWR_DN_MODE) = 1

Set register 0x00h bit0 (PWR_DN_EN) = 1

To enter SLEEP, program register 0x01h bit1 (SLP_ENTR) = 1.

I²C is disabled in SLEEP mode, to the only way to exit SLEEP mode is to toggle the PWREN pin.

THERMAL State

In the THERMAL state the chip has exceeded the thermal shutdown temperature. To protect the device, all the regulators are shut down and all three nRESETx pins are asserted low. This state can be disabled by setting register 0x0Ah bit4 (TSD_nMASK) = 0. Note that thermal shutdown fault flag, TSD_SHUTDWN, still provides the thermal status even TSD_nMASK = 0.

OVUVFLT State

In the OVUVFLT state one of the regulators has exceed an OV level at any time or UV level after the soft start ramp has completed. All regulators shutdown and all three nRESETx outputs are asserted low when the IC enters OVUVFLT state. The OVUVFLT state is timed to retry after 100ms and enter the ACTIVE state. If the OV or UV condition still exists in the ACTIVE state the IC returns back to the OVUVFLT state. The cycle continues until the OV or UV fault is removed or the input power is removed. This state can be disabled by setting the OV_nMASK or UV_nMASK non-volatile bits low. The IC does not directly enter OVUVFLT in an overcurrent condition, but does enter this state due to the resulting UV condition.

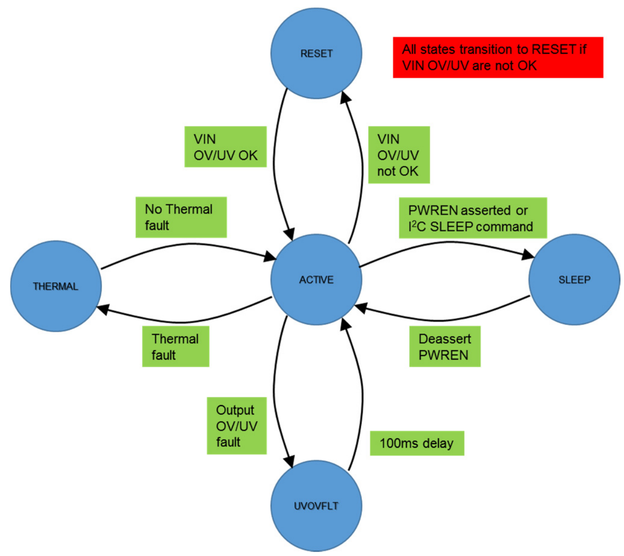


Figure 3. State Machine

Sequencing

The ACT88430 provides the end user with extremely versatile sequencing capability that can be optimized for many different applications. Each of the seven outputs has four basic sequencing parameters: input trigger, turn-on delay, softstart time, and output voltage. Each of these parameters is controlled via the ICs internal registers. Contact sales@active-semi.com for custom sequencing configurations. Refer to the Active-Semi Application Note describing the Register Map for full details on I²C functionality and programming ranges.

Input trigger. The input trigger for a regulator is the event that turns that regulator on. Each output can have a separate input trigger. The input trigger can be the internal power ok (POK) signal from one of the other regulators, the internal VIN POK signal, or an external signal applied to an input pin such as EXT_PG or GPIO. This flexibility allows a wide range of sequencing possibilities, including have some of the outputs be sequenced with another external power supply or a control signal from the host. As an example, if the LDO1 input trigger is Buck1, LDO1 will not turn on until Buck1 is in regulation. Input triggers are defined at the factory and can only be changed with a custom CMI configuration. The nRESETx, POK, PG, and EXT_EN outputs can be connected to a power supply's internal POK signal and used to trigger external supplies in the overall sequencing scheme.

Turn-on Delay. The turn-on delay is the time between an input trigger going active and the output starting to turn on. Each output's turn-on delay is configured via its I²C bit ONDLY. Turn-on delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Softstart Time. The softstart time is the time it takes an output to ramp from 0V to its programmed voltage. Each output's softstart time is configured via its I²C bit SS_RAMP. Softstart times can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Output Voltage. The output voltage is each regulator's desired voltage. Each buck's output voltage is programmed via its I²C bits Bx_VSET0 and Bx_VSET1. The output regulates to Bx_VSET0 in ACTIVE mode. They can be programmed to regulate to Bx_VSET1 in DVS mode or SLEEP mode. Each output's voltage can be changed after the IC is powered on, but the new setting is volatile and is reset to the factory defaults when power is recycled. Output voltages can be changed on the fly. If a large output voltage change is required, it is best to make multiple smaller changes. This prevents the IC from detecting an instantaneous over or under voltage condition because the fault threshold are immediately changed, but the output takes time to respond.

Dynamic Voltage Scaling

On-the-fly dynamic voltage scaling (DVS) for the four buck converters is available via the I²C interface. This allows systems to save power by quickly adjusting the microprocessor performance level when the workload changes. Note that DVS is not a different operating state. The IC operates in the ACTIVE state, but just regulates the outputs to a different voltage. For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

Enter DVS by programming register 0x00h bit1 (DVS_EN) = 1 and then pulling the EXT_PG pin high. Note that some CMI configurations may not require DVS_EN = 1 and may use different input pins.

Input Voltage Operating Range

The ACT88430 operates from VIN=2.7V to 5.5V. This operating range can be tailored for this full range, a 3.3V input range, or a 5V input range. The full range is suitable for battery inputs like a Li-Ion battery where the input voltage has large variations. I²C registers VIN-FULL_RANGE and VIN_LVL set the input voltage UVLO and OV thresholds to be compatible with these operating ranges. Note that VIN_FULL_RANGE register is set at the factory and cannot be changed. Table 2 shows how to configure the registers to set each input voltage range setting. See the EC table for details on

Table 2: ACT88430 Input Voltage Range Settings

	VIN_FULL_RANGE	VIN_LVL
3.3V Input Range	0	0
5V Input Range	0	1
Wide Input Range	1	x

Fault Protection

The ACT88430 contains several levels of fault protection, including the following:

Input Voltage UVLO

Input Voltage OV

Output Overvoltage

Output Undervoltage

Output Current Limit

Thermal Warning

Thermal Shutdown

There are three types of I²C register bits associated with each fault condition: fault flag bits, fault bits, and mask bits. The fault flag bits display the real-time fault status. Their status is valid regardless of whether or not that fault is masked. The mask bits either block or allow the fault to affect the fault bit. Each potential fault condition can be masked via I²C if desired. Any unmasked fault condition results in the fault bit going high, which asserts the IRQ pin. IRQ is typically active low. The IRQ pin only de-asserts after the fault condition is no longer present and the corresponding fault bit is read via I²C. Note that masked faults can still be read in the fault flag bit. Refer to Active-Semi Application Note describing the Register Map for full details on I²C functionality and programming ranges

Input Voltage UVLO

The ACT88430 monitors its input voltage at the VIN pin for a UVLO condition. When the input voltage is below the UVLO threshold, the IC is turned off and nRESET is held low. When the input voltage goes above UVLO, the IC transitions to the ACTIVE state and starts up normally.

The UVLO thresholds are determined by the operating range that is programmed by the VIN_FULL_RANGE and VIN_LVO registers. See Table 2 for these settings.

Input Voltage OV

The ACT88430 monitors its input voltage at the VIN pin for an OV condition. When the input voltage is above the OV threshold, the IC outputs turn off and nRESET asserts low. When the input voltage goes below OV, the IC transitions back to the ACTIVE state and starts up normally. The OV thresholds are determined by the operating range that is programmed by the VIN_FULL_RANGE and VIN_LVO registers. See Table 2 for these settings.

Output Under/Over Voltage

The ACT88430 monitors the output voltages for under voltage and over voltage conditions. If one output enters an UV/OV fault condition, the IC shuts down all outputs for 100ms and restarts with the programmed power up sequence. If an output is in current limit, it is possible that its voltage can drop below the UV threshold which also shuts down all outputs. If that behavior is not desired, mask the appropriate fault bit. Each output still provides its real-time UV/OV fault status via its fault flag, even if the fault is masked. Masking an OV/UV fault just prevents the fault from being reported via the IRQ pin. A UV/OV fault condition pulls the nRESETx pins low. Note that nRESETx pins are configurable via CMI settings.

Output Current Limit

The ACT88430 incorporates a three level overcurrent protection scheme for the buck converters and a single level scheme for the LDOs. For the buck converters, the overcurrent current threshold refers to the peak switch current. The first protection level is when a buck converter's peak switch current reaches 80% of the Cycle-by-Cycle current limit threshold for greater than 16 switching cycles. Under this condition, the IC reports the fault via the appropriate fault flag bit. If the fault is unmasked, it asserts the IRQ pin. This may or may not turn off that output or other outputs depending on the specific CMI. The next level is when the current increases to the Cycle-by-Cycle threshold. The buck converter limits the peak switch current in each switching cycle. This reduces the effective duty cycle and causes the output voltage to drop, potentially creating an undervoltage condition. When the overcurrent condition results in an UV condition, and UV is not masked, the IC turns off all supplies off for 100ms and restarts. The third level is when the peak switch current reaches 120% of the Cycle-by-Cycle current limit threshold. This immediately shuts down the regulator and waits 14ms before restarting.

For LDOs, the overcurrent thresholds are set by each LDO's Output Current Limit setting. When the output current reaches the Current Limit threshold, the LDO limits the output current. This reduces the output voltage, creating an undervoltage condition, causing all supplies to turn off for 100ms before restarting.

The overcurrent fault limits for each output are adjustable via I2C. Overcurrent fault reporting can be masked via I2C, but the overcurrent limits are always active and will shut down the IC when exceeded.

Thermal Warning and Thermal Shutdown

The ACT88430 monitors its internal die temperature and reports a warning via IRQ when the temperature rises above the Thermal Interrupt Threshold of typically 135 deg C. It reports a fault when the temperature rises above the Thermal Shutdown Temperature of typically 165 deg C. A temperature fault shuts down all outputs unless the fault is masked. Both the fault and the warning can be masked via I^{2}C. The temperature warning and fault flags still provide real-time status even if the faults are masked. Masking just prevents the faults from being reported via the IRQ pin.

Pin Descriptions

The ACT88430 input and output pins are configurable via CMI configurations. The following descriptions are refer to the most common pin functions. Refer to the CMI Options section in the back of the datasheet for specific pin functionality for each CMI.

PWREN

The PWREN pin controls the IC's SLEEP state. When I^{2}C bit PWREN_MODE = 0, the PWREN pin moves the IC between the SLEEP and ACTIVE states.

PWREN must be enabled via the PWRDN_EN I^{2}C bit after power up. PWREN is ignored if the PWRDN_EN bit is low. The PWREN polarity is controlled by the PWREN_POL I^{2}C bit. PWREN is active low when PWREN_POL is high, and active high when PWREN_POL is low. The host processor can read the PWREN status via I^{2}C in the PWREN_STAT I^{2}C bit.

PWREN is referenced to the VIO_IN pin, and is 5.5V tolerant meaning that PWREN can go to 5.5V even if VIO_IN is less than 5.5V. PWREN has a 10us bidirectional filter to prevent noise from triggering unwanted operation.

EXT_PG

The EXT_PG pin is a dual purpose input. Note that EXT_PG can only be configured as an input. It functions as either a power good input from an external supply or a dynamic voltage scaling control input. Configure EXT_PG as a power good input by setting I^{2}C bit DVS_EN = 0. When configured as a power good input, EXT_PG can be used as an input to the nRESETx pins. EXT_PG polarity is controlled by the EXT_PG_POL bit. EXT_PG is active high when EXT_PG_POL = 0 and active low when EXT_PG_POL = 1.

Configure EXT_PG as a dynamic voltage scaling (DVS) control input by setting I²C bit DVS_EN = 1. When EXT_PG is de-asserted, all buck regulators regulate to their VSET0 voltage. When EXT_PG is asserted, the buck regulators regulate to their VSET1 voltage. Note that EXT_PG input is only valid for DVS toggling when the IC is in the ACTIVE state of operation. I²C bit EXT_PG_POL has no effect in DVS Mode.

EXT_PG is referenced to the VIN pin, and should not be pulled above VIN. The EXT_PG input has a 10us bidirectional filter to prevent noise from triggering unwanted operation.

VIO_IN

VIO_IN is the input bias supply for the IC. Apply an input voltage between 1.62V and 5.5V. Bypass to AGND with a high quality, 1uF ceramic capacitor.

MODE

Setting MODE = 0 configures Buck1 as a standard integrated buck regulator. Setting MODE = 1 configures Buck1 as an integrated bypass switch. Buck1 can only operate as a bypass switch when VIN=3.3V. In bypass mode, the Buck1 P-ch power FET is used to sequence the 3.3V supply to the downstream load. This provides full sequencing flexibility for 3.3V systems by allowing the 3.3V input to be used as the input supply for the other regulators but still be sequenced in any order for the downstream loads. Bypass mode is only valid for a 3.3V input voltage. The MODE pin must be tied directly to VIN or AGND. I²C bit MODE_STAT shows the status of the MODE pin when it was read at startup.

GPIO

The GPIO pin can be configured as a digital input or an open drain output. It has multiple uses, including a sequencing input, sequencing output, status output, or control input to toggle a supply's output voltage. Set I²C bit GPIO_OUT = 0 to configure GPIO as an input. When using GPIO as an output, GPIO_OUT = 0 configures it as an open drain output, and GPIO_OUT = 1 configures it as a logic low output. When used as either an input or an output, I²C bit GPIO_STAT always provides the real-time status of the GPIO pin. GPIO_STAT = 0 when GPIO pin is a logic 0. GPIO_STAT = 1 when GPIO pin is a logic 1.

GPIO pin is referenced to the VIN pin, and is 5.5V tolerant meaning that GPIO can go to 5.5V even if VIN is less than 5.5V.

IRQ

The IRQ pin is an output that issues an interrupt to the host CPU/Controller when an ACT88430 fault or warning condition occurs.

IRQ is triggered by:

Die temperature exceeding Thermal Interrupt Threshold of 135C.

Any buck regulator reaching peak current limit, ILIMSET, for 16 cycles after softstart.

Any LDO regulator reaching current limit, LDOx_ILIM, for more than 16us after softstart.

BUCK1 PMOS switch exceeding Current Detection threshold 75% of ILIMSET when system is configured in bypass mode.

IRQ is masked by the I²C register 0x00h bit2 (IRQ_nMASK) by default to mask all IRQ conditions. To enable IRQ functionality, set IRQ_nMASK = 1. IRQ is an active-low open drain 5.5V compatible output.

POK

POK indicates that the voltage on the VIN pin is inside the POK UV and OV Interrupt Thresholds. If the VIN voltage is above or below these values, POK pulls low to interrupt the host CPU/Controller. POK is masked by the I²C bit POK_nMASK by default. To enable POK functionality, set I²C bit POK_nMASK = 1. I²C bits POK_OV and POK_UV provide real-time UV and OV status, even when POK is masked. The POK UV and OV threshold are configurable via the I²C bits POK_UV_SET and POK_OV_SET.

POK is an open drain output and is 5.5V tolerant meaning that POK can be pulled up to 5.5V even if VIO_IN is less than 5.5V.

nRESET_AUX1 and nRESET_AUX2

nRESET_AUX1 and nRESET_AUX2 pins can be used to signal that the IC is in the SLEEP state or that the input voltage is above or below the UV or OV threshold. They can also be tied to one or a combination of the power supply's internal POK signals. When asserted by the internal POK signals they immediately assert. They follow a programmed delay when de-asserted. The nRESET_AUX1 delay time is controlled by the I²C bits RST_AUX1_DLY[2:0], which programs the delay between 400us and 2mS in 227us steps. The nRESET_AUX2 delay time is controlled by the I²C bits RST_AUX2_DLY[2:0], which programs the delay between 200us and 1ms in 114us steps. These pins can also be used as inputs to control different power rail enable signals. They are configurable, so refer to the back of the datasheet for their specific functionality for each CMI. Contact the factory for available options. They are open drain outputs and are 5.5V tolerant meaning that they can be pulled up to 5.5V even if VIO_IN is less than 5.5V.

nRESET

nRESET issues the main reset to the CPU/controller. nRESET is immediately asserted low when either the VIN voltage is above or below the UV or OV thresholds or any valid output supply voltage is below its Power Good (POK) threshold. After startup, nRESET de-asserts after a programmable delay time after all outputs are above their respective UVLO thresholds. The nRESET delay time is controlled by the I²C bits nRST_DLY[2:0], which programs the delay between 200us and 1ms in 114us steps. nRESET is configurable, so refer to the CMI Options section in the back of the datasheet for its specific functionality for each CMI. nRESET is an open drain output and is 5.5V tolerant meaning that nRESET can be pulled up to 5.5V even if VIO_IN is less than 5.5V.

EXT_EN

EXT_EN is used to control an external regulator or to provide a control signal to other system components. When the MODE pin = 0 to configure Buck1 as a standard power supply, EXT_EN is the output of the ACT88430's internal BUCK1 enable signal. When the MODE pin = 1 to configure Buck1 as a bypass switch, EXT_EN is the output of the bypass switch enable signal.

The I²C bit EXT_EN_POL controls the EXT_EN polarity. EXT_EN is active high when EXT_EN_POL is low and EXT_EN is active low when EXT_EN_POL is high. EXT_EN is a push-pull CMOS output using VIO_IN supply. Note that the EXT_EN output is enabled and valid in all modes of operation. EXT_EN is configurable, so refer to the CMI Options section in the back of the datasheet for its specific functionality for each CMI.

EXT_EN is referenced to the VIO_IN pin. It should not be pulled higher than VIO_IN.

PG

The PG pin shows the status of a regulator's Power Good / UV comparator. When the regulator is below the Power Good threshold, the PG pin is pulled low. When above the threshold, the PG pin is open drain. The PG functionality is enabled by default, but can be disabled by I²C. PG can be disabled by using the appropriate regulator's UV_FLTMSK bit. Table 3 shows the possible regulators that can drive the PG pin.

Table 3: ACT88430 PG Input Choices

Allowable PG Inputs
Buck1
Buck2
Buck3
Buck4
LDO1
LDO2 AND Buck4
LDO3
LDO3 AND Buck4

PG is configurable, so refer to the back of the datasheet for its specific functionality for each CMI. PG is an open drain output and is 5V tolerant meaning that PG can be pulled up to 5.5V even if VIO_IN is less than 5.5V.

Step-down dc/dc Converters

General Description

The ACT88430 contains four fully integrated step-down converters. Buck1 is a 4A output, while Buck2, Buck3, and Buck4 are 2.5A outputs. All buck converters are fixed frequency, current-mode controlled, synchronous PWM converters that achieve peak efficiencies of up to 96.5%. The buck converters switch at 2.25MHz and are internally compensated, requiring only three small external components (Cin, Cout, and L) for operation. They ship with default output voltages that can be modified via the I²C interface for systems that require advanced power management functions.

Each buck converter has a dedicated input pin and power ground pin. Each buck converter should have a dedicated input capacitor that is optimally placed to minimize the power routing loops for each buck converter. Note that even though each buck converter has separate inputs, all buck converter inputs must be connected to the same voltage potential.

Buck1 is configurable as a bypass switch for systems with a 3.3V bus voltage. The bypass switch provides full sequencing capability by allowing the 3.3V bus to be used as the input to the other supplies and still be properly sequenced to the downstream load.

Tie MODE to AGND to configure Buck1 for a switching power supply. Tie MODE to VIN to configure Buck1 as a bypass switch. MODE is only sampled when VIN reaches its UVLO threshold. Changing the MODE pin after startup has no effect. When Buck1 is configured as a power supply, EXT_EN is a direct output of the ACT88430 Buck1 enable signal. When Buck1 is configured as a bypass switch, EXT_EN is a direct output of the bypass switch enable signal.

The ACT88430 buck regulators are highly configurable and can be quickly and easily reconfigured via I²C. This allows them to support changes in hardware requirements without the need for PCB changes. Examples of I²C functionality are given below:

Real-time power good, OV, and current limit status

Ability to mask individual faults

Dynamically change output voltage

On/Off control

Softstart ramp

Slew rate control

Switching delay and phase control

Low power mode

Overcurrent thresholds

Refer to the Active-Semi Application Note describing the Register Map for full details on I²C functionality and programming ranges.

Operating Mode

The buck converters operate in fixed-frequency PWM mode at medium to heavy loads. They transition to a proprietary power-saving low power mode (LPM) at light loads in order to save power. Each buck converter's LPM can be independently enabled or disabled via its DISLPM I²C bit. Setting DISLPM = 0 enables LPM while setting DISLPM = 1 disables LPM. Disabling LPM effectively puts the regulator into forced PWM mode. Operating in LPM saves power, while operating in forced PWM mode gives better transient response.

Synchronous Rectification

Buck1/2/3/4 each feature integrated synchronous rectifiers (or LS FETs) to maximize efficiency and minimize the total solution size and cost by eliminating the need for external rectifiers.

Enable / Disable Control

When power is applied to the IC, all converters automatically turn on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), each converter can be independently disabled via I²C. Each CMI version requires a different set of command to disable a converter, so contact the factory for specific instructions if needed. Each converter contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. The discharge function is enabled via the I²C bit Bx_DisPulldown.

Soft-Start

Each buck regulator contains a softstart circuit that limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the outputs power up monotonically. This circuitry is effective any time the regulator is enabled, as well as after responding to a short circuit or other fault condition. Buck1/2/3 softstart time is adjustable between 150µs to 485µs via their I²C SS_RAMP registers. Buck4 softstart time is adjustable between 25µs to 204µs via I²C SS_RAMP register. Table 4 summarizes the softstart settings.

Table 4: Buck Softstart Time (0.8V Reference)

SS_RAMP	Buck1/2/3 Softstart (µs)	Buck4 Softstart (µs)
000	150	25
001	200	51
010	250	76
011	300	102
100	350	127
101	395	153
110	440	178
111	485	204

Note that when an output's reference voltage is changed to 0.6V, the softstart time changes to 75% of the time in Table 4.

Output Voltage Setting

Buck1/2/3/4 regulate to the voltage defined by I²C register VSET0 in normal operation and by VSET1 in DVS mode. Buck1/2/3/4 each have two programmable output voltage ranges, Output-Low Range and Output-High Range. Each buck converter's output range can be programmed independently of the others. Note that the output voltage range can NOT be changed while the output is enabled. Active Semi does not recommend changing the output voltage range from its default setting because its internal voltage reference is only trimmed to its default setting. The following table shows which I²C bits set the output ranges.

Table 5: Buck Output Voltage Programming Ranges

	Register	Bit	Setting	Range
Buck1	0x74h	SEL_REF0P8_BUCK1	0	Output-Low
			1	Output-High
Buck2	0x72h	SEL_REF0P8_BUCK2	0	Output-Low
			1	Output-High
Buck3	0x89h	SEL_REF0P8_BUCK3	0	Output-Low
			1	Output-High
Buck4	n/a	n/a	n/a	Output-High

The programming range for Output-Low is 0.6V to 3.000V in 9.375mV steps.

V_{BUCKx} = 0.6V * VOUTx * 0.009375V

Where VOUTx is the decimal equivalent of the value in each regulator's I²C VOUTx register. The VOUTx registers contain an unsigned 8-bit binary value. As an example, if Buck 1's VOUT0 register contains 10000000b (128 decimal), the output voltage is 1.8V.

The programming range for Output-High is 0.8V to 3.988V in 12.5mV steps.

V_{BUCKx} = 0.8V * VOUTx * 0.0125V

Where VOUTx is the decimal equivalent of the value in each regulator's I²C VOUTx register. The VOUTx registers contain an unsigned 8-bit binary value. As an example, if Buck 1's VOUT0 register contains 01010000b (80 decimal), the output voltage is 1.8V.

Active Semi recommends that a buck converter's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

100% Duty Cycle Operation

The buck regulators are capable of operating at up to 100% duty cycle. During 100% duty cycle operation, the high-side power MOSFETs are held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

Dynamic Voltage Scaling

Each buck converter supports Dynamic Voltage Scaling (DVS). DVS allows the user to optimize the processor's energy to complete tasks by lowering the processor's operating frequency and input voltage when lower performance is acceptable. In normal operation, each output regulates to the voltage programmed in the I²C register Bx_VSET0. During DVS, each output regulates to Bx_VSET1. The output transitions from Bx_VSET0 to Bx_VSET1 at a rate determined by the output capacitance and the load current. The outputs transition between VSET1 and VSET0 by the rate determined by the I²C bits SLEW.

For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

Enter DVS by programming register 0x00h bit1 (DVS_EN) = 1 and then pulling the EXT_EN pin high. Note that some CMI configurations may not require DVS_EN = 1 and may use different input pins.

Bx_VSET0 must be higher than Bx_VSET1. PWR_GOOD, OV, and ILIM are automatically masked during DVS transitions to avoid asserting nRESET.

Optimizing Noise

Each buck converter contains several features available via I²C to further optimize functionality. The top P-ch FET's turn-on timing can be shifted 100ns from the master clock edge via the PHASE_DELAY I²C bit. It can also be aligned to the rising or falling clock edge via the PHASE I²C bit. The internal FET rise and fall times can be optimized to minimize switching noise at the cost of lower efficiency via the DRVADJ I²C bit.

Overcurrent and Short Circuit Protection

Each buck converter provides overcurrent and short circuit protection. Overcurrent protection is achieved with cycle-by-cycle current limiting. The peak current threshold is set by the Bx_ILIM I2C bits. If the peak current reaches the programmed threshold for 16 consecutive switching cycles, the IC asserts IRQ low. A short circuit condition that results in the peak switch current being 122% of Bx_ILIMSET immediately shuts down all supplies, asserts IRQ low and restarts the system in 100ms. If a buck converter reaches overcurrent or short circuit protection, the status is reported in the ILIM_REG[x] I2C registers. The contents of these registers are latched until read via I2C. Overcurrent and short circuit conditions can be masked via the I2C bit Bx_ILIM_FLTMSK.

Compensation

The buck converters utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guide lines described below when choosing external components.

Minimum On-Time

The ACT88430 minimum on-time is 120ns. If the calculated on-time is less than 120ns with 2.25MHz operation, then the user must configure the output to switch at 1.125MHz. Setting I²C bits Bx_HalfFreq = 0 sets Fsw = 2.25MHz. Setting Bx_HalfFreq = 1 sets Fsw = 1.125MHz. The following equation calculates the on-time.

$$T_{ON} = \frac{V_{OUT}}{V_{IN} * F_{SW}}$$

Where V_{out} is the output voltage, V_{in} is the input voltage, and F_{SW} is the switching frequency.

BUCK1 Bypass Switch

The ACT88430 provides a bypass mode for 3.3V systems. This allows the 3.3V input voltage to power the ACT88430 regulators and also be sequenced to the downstream loads. In bypass mode, the Buck1 P-ch FET acts as a switch and the N-ch FET is disabled. The bypass switch turns on the 3.3V rail with the programmed delay and softstart time.

In bypass mode, the ACT88430 I²C registers are reconfigured to the following.

1. B1_PWR_GOOD register bit reconfigured to the output of the Soft Start ramp. When soft start is complete, this bit goes high to allow the sequencing of the other regulators to continue. B1_PWR_GOOD no longer reports the Buck1 output voltage status. It stays high as long as the bypass switch is enabled.
2. B1_ILIM bit is the output of the internal PMOS Current Detection circuit. This is set to 3A typical. If the bypass current exceeds the Internal PMOS Current Detection current, B1_ILIM triggers an IRQ output and gets latched in the ILIM_REG[0] if configured by the IRQ_nMASK. The B1_ILIM can also be masked with the B1_ILIM_FLTMSK register.

B1_UV register bit reconfigured to the output of the Internal PMOS Current Shutdown circuit. This is set to 6A typical. If the bypass switch current exceeds 6A, limits the current which triggers an under voltage fault condition and moves the IC into the OVUVFLT state. This immediately shuts down all regulators including the bypass switch. The system restarts in 100ms, following the programmed startup sequencing. This fault can be masked with I²C bit UV_nMASK. This fault is latched in the UV_REG I²C bit. Shutdown due to overcurrent can also be masked via the I²C bit B1_PG_FLTMSK.

B1_OV is disabled. There is no overvoltage detection circuitry on the output of the bypass switch.

Input Capacitor Selection

Each regulator requires a high quality, low-ESR, ceramic input capacitor. Note that even though each buck converter has separate input pins, all input pins must be connected to the same voltage potential. 10uF capacitors are typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output loads. Choose the input capacitor value to keep the input voltage ripple less than 50mV.

$$\mathrm{V_{ripple}} = Iout * \frac{\frac{Vout}{Vin} * \left(1 - \frac{Vout}{Vin}\right)}{Fsw * Cin}$$

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics is not recommended. Input capacitor placement is critical for proper operation. Each buck's input capacitor must be placed as close to the IC as possible. The traces from VIN_Bx to the capacitor and from the capacitor to PGNDx should as short and wide as possible.

Inductor Selection

The Buck converters utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. The ACT88430 is optimized for operation with 1.0-1.5µH inductors. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%. The following equation calculates the inductor ripple current.

$$\Delta I_L = \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) * V_{OUT}}{F_{SW} * L}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, F_{SW} is the switching frequency, and L is the inductor value.

Output Capacitor Selection

The ACT88430 is designed to use small, low ESR, ceramic output capacitors. Buck1 typically requires a 44uF output capacitor while Buck2, Buck3, and Buck4 require a 22uF output capacitor each. In order to ensure stability, the actual Buck1 capacitance should be greater than 33uF while Buck2, Buck3, and Buck4 should be greater than 15uF. The output capacitance can be increased to reduce output voltage ripple and improve load transients if needed. Design for an output ripple voltage less than 1% of the output voltage. The following equation calculates the output voltage ripple as a function of output capacitance.

$$V_{RIPPLE} = \frac{\Delta I_L}{8 * F_{SW} * C_{OUT}}$$

Where ΔI_L is the inductor ripple current, F_{SW} is the switching frequency, and C_{OUT} is the output capacitance after taking DC bias into account.

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The output capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics are not recommended due to their wide variation in capacitance over temperature and voltage ranges.

LDO Converters

General Description

The ACT88430 contains three fully integrated low dropout linear regulators (LDO). LDO1 is an 800mA output, while LDO2 and LDO3 are 200mA outputs. The LDOs are require only two small external components (Cin, Cout) for operation. They ship with default output voltages that can be modified via the I²C interface for systems that require advanced power management functions.

LDO1 has a dedicated input pin. LDO2 and LDO3 share an input pin. The LDOs can operate from different input voltages than the buck converters. LDO1 and LDO2/3 can operate from different input voltage from each other.

LDO1 has the option to be operated as a standard LDO or as a load switch.

Enable / Disable Control

When power is applied to the IC, all LDOs automatically turn on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), each converter can be independently disabled via I²C. Each CMI version requires a different set of command to disable a converter, so contact the factory for specific instructions if needed. Each converter contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. Each LDO's discharge function is enabled via its I²C bit DIS_PULLDOWN.

Soft-Start

Each LDO contains a softstart circuit that limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the outputs power up in a monotonically. This circuitry is effective any time the LDO is enabled, as well as after responding to a short circuit or other fault condition. Each LDO's softstart time is adjustable via its I²C bits SS_RAMP.

LDO1 is adjustable between 226µs and 570µs, depending on output voltage.

LDO2 is adjustable between 130µs and 220µs, depending on output voltage

LDO3 is adjustable between 65µs and 130µs, depending on output voltage

Table 6 summarizes the LDO softstart programming ranges.

Table 6: LDO Softstart Ranges

LDOx Softstart Register	Setting	LDO1 softstart (us)	LDO2 softstart (us)	LDO3 softstart (us)
LDOx_SS	00	226	130	36
	01	323	133	64
	10	440	170	96
	11	570	220	126

Output Voltage Setting

LDO1/2/3 regulate to the voltage defined by I²C registers LDO VSET registers. Unlike the buck converters, the LDOs only have one VSET register. LDO2/3 each have two programmable output voltage ranges, Output-Low Range and Output-High Range. Each LDO's output range can be programmed independently of the others. Note that the output voltage range can NOT be changed while the output is enabled. Active Semi does not recommend changing the output voltage range from its default setting because its internal voltage reference is only trimmed to its default setting. The following table shows which I²C bits set the output ranges.

Table 7: LDO Output Voltage Programming Ranges

	Register	Bit	Setting	Range
LDO1	n/a	n/a	n/a	Output-High
LDO2	0x81h	RANGE_LDO2	1	Output-Low
			0	Output-High
			1	Output-Low

LDO3	0x81h	RANGE_LDO3	0	Output-High

The programming range for Output-Low is 0.8V to 2.375V in 25mV steps.

V_{LDOx} = 0.8V * LDOxVSET * 0.025V

Where LDOxVSET is the decimal equivalent of the value in each regulator's I²C LDOxVSET register. The LDOxVSET registers contain an unsigned 6-bit binary value. As an example, if LDO 1's LDOxVSET register contains 101000b (40 decimal), the output voltage is 1.8V.

The programming range for Output-High is 2.0V to 3.575V in 25mV steps.

V_{LDOx} = 2.0V * LDOxVSET * 0.025V

Where LDOxVSET is the decimal equivalent of the value in each regulator's I²C LDOxVSET register. The LDOxVSET registers contain an unsigned 6-bit binary value. As an example, if LDO 1's LDOxVSET register contains 01010000b (52 decimal), the output voltage is 3.3V.

Active Semi recommends that an LDO's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

Overcurrent and Short Circuit Protection

Each LDO provides overcurrent and short circuit protection. The overcurrent threshold is set by the LDOx_ILIM I2C bits. In both an overload and a short circuit condition, the LDO limits the output current which causes the output voltage to drop. This can result in an undervoltage fault in addition to the current limit fault. If an LDO reaches current limit protection, the status is reported in the ILIM_REG[x] I2C registers. The contents of these registers are latched until read via I2C. When the current limiting results in a drop in output voltage that triggers an undervoltage condition, the IC shuts down all power supplies, asserts IRQ low, and enters the UVLOFLT state. The IC restarts in 100ms and starts up with default sequencing. Overcurrent and short circuit conditions can be masked via the I2C bit LDOx_ILIM_FLTMSK.

Input Capacitor Selection

Each LDO requires a high quality, low-ESR, ceramic input capacitor. A 1uF is typically suitable, but this value can be increased without limit. The input capacitor is should be a X5R, X7R, or similar dielectric.

Output Capacitor Selection

Each LDO requires a high quality, low-ESR, ceramic output capacitor. A 1uF is typically suitable, but this value can be increased without limit. The input capacitor is should be a X5R, X7R, or similar dielectric.

LDO1 Load Switch Mode

LDO1 has an option to be used as a load switch. This option is only accessible via factory I²C bits and requires a custom CMI. When in load switch mode, LDO1 still retains overcurrent protection. Overvoltage and undervoltage protection are disabled.

The load switch mode softstart times are the same as the LDO mode times.

The following table shows the load switch Current limit settings

Table 8: Load Switch Current Limit Settings

ILIM_SET<1:0>	ILIM(mA)
0	1415
1	1503
2	1626
3	1904

Both Overvoltage and Undervoltage functionality are disabled.

The LDO1 POK is functional in Load Switch mode. The POK signal is asserted when the switch is enabled and is not in current limit.

PC board layout guidance

Proper parts placement and PCB layout are critical to the operation of switching power supplies. Follow the following layout guidelines when designing the ACT88430 PCB. Refer to the Active-Semi ACT88430 Evaluation Kits for layout examples

1. Place the buck input capacitors as close as possible to the IC. Connect the capacitors directly to the corresponding VIN_Bx input pin and PGNDx power ground pin. Avoid the use of vias if possible.

2. Minimize the switch node trace length between each SW_Bx pin and the inductor. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.

3. Place the LDO input capacitors close to their input pins. Connect their ground pins into the ground plane that connects the IC's exposed pad.

4. The input capacitor and output capacitor grounds should be connected as close together as possible, with short, direct, and wide traces.

5. Connect the PGNDx ground pins and the AGND ground pin directly to the exposed pad under the IC. The AGND ground plane should be routed separately from the other ground planes and only connect to the main ground plane under the IC at the AGND pin.

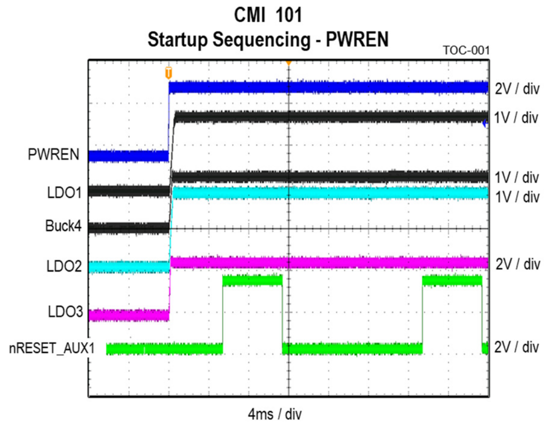
6. Connect the VIO_IN input capacitor to the AGND ground pin.

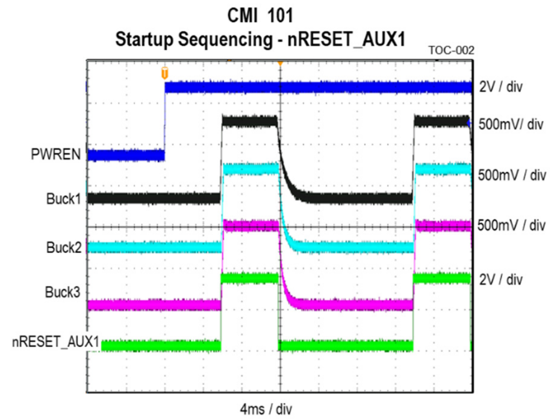
7. Connect the VIN input capacitor to the AGND ground pin.

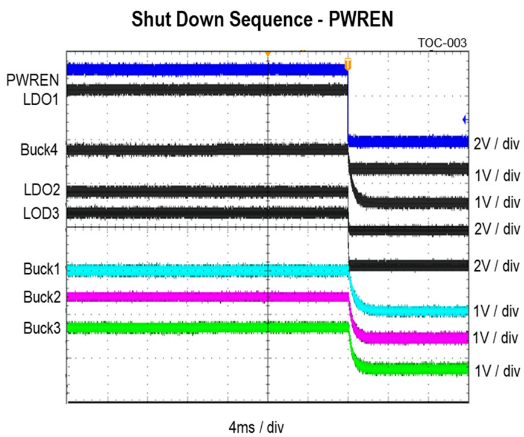
8. Remember that all open drain outputs need pullup resistors.

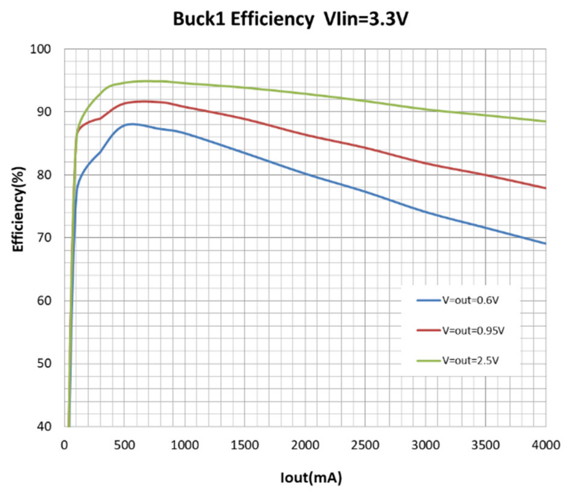
9. Connect the exposed pad directly the top layer ground plane. Connect the top layer ground plane to both internal ground planes and the PCB backside ground plane with thermal vias. Provide ground plane routing on multiple layers that allows the IC's heat to flow into the PCB and then spread radially from the IC. Avoid cutting the ground planes and adding vias that restrict the radial flow of heat of operating conditions, and are relatively insensitive to layout considerations.

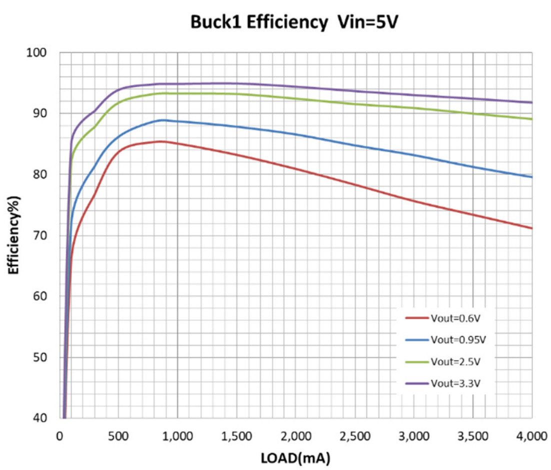
Typical Operating Characteristics

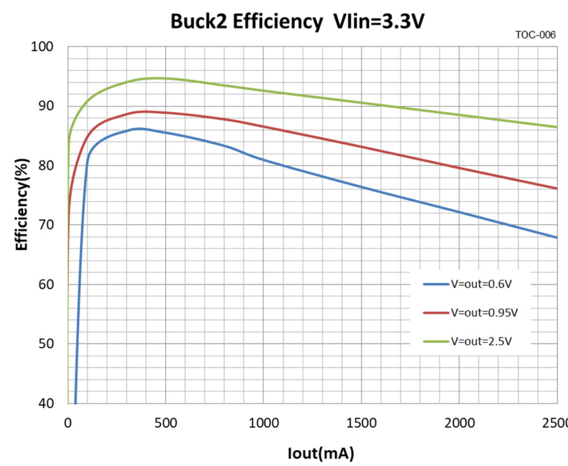


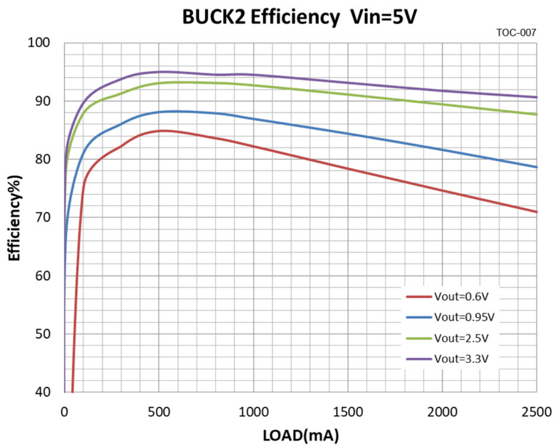


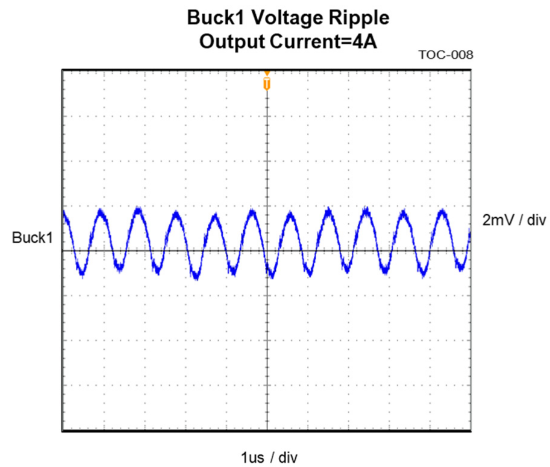


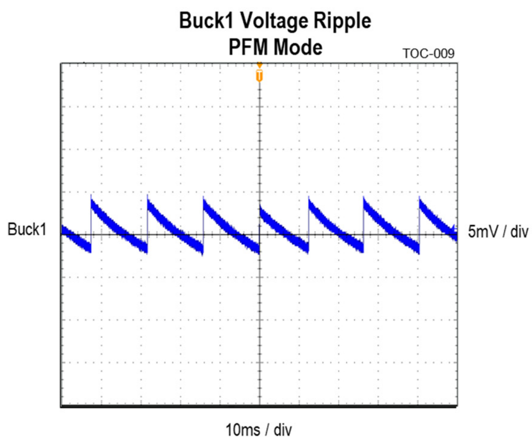


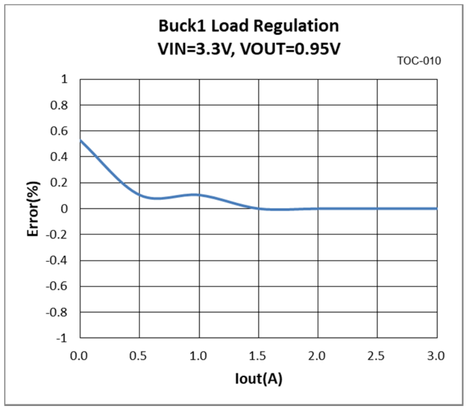


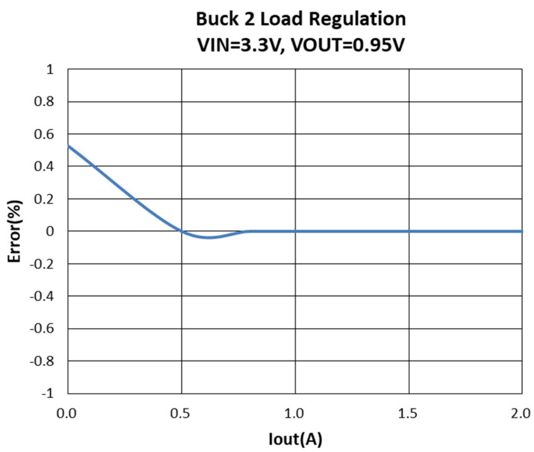


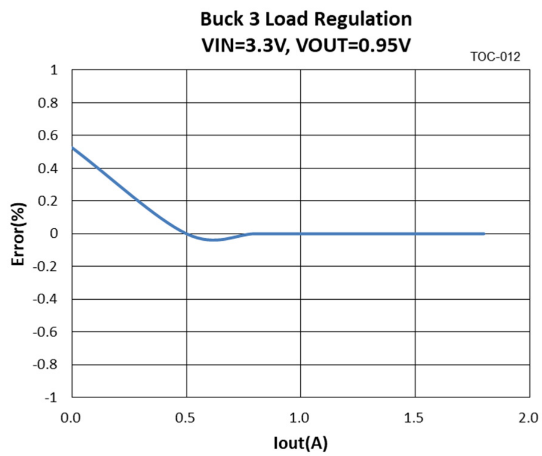

BUCK2 Efficiency Vin=5V
TOC-007
Efficiency%)
LOAD(mA)
Vout=0.6V
Vout=0.95V
Vout=2.5V
Vout=3.3V


Buck1 Voltage Ripple
Output Current=4A
TOC-008
Buck1
2mV / div
1us / div

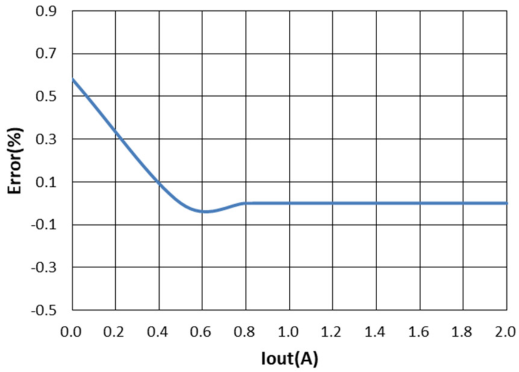

Buck1 Voltage Ripple
PFM Mode
TOC-009
Buck1
5mV / div
10ms / div


Buck1 Load Regulation
VIN=3.3V, VOUT=0.95V
TOC-010
Error(%)
Iout(A)

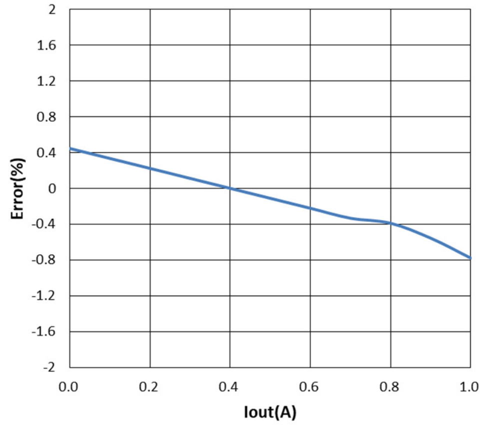

Buck 2 Load Regulation
VIN=3.3V, VOUT=0.95V
Error(%)
Iout(A)


Buck 3 Load Regulation
VIN=3.3V, VOUT=0.95V
TOC-012
Error(%)
Iout(A)

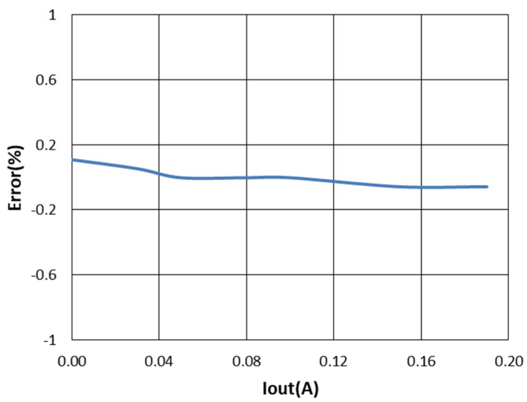
Buck4 Load Regulation
VIN=3.3V, VOUT=1.2V



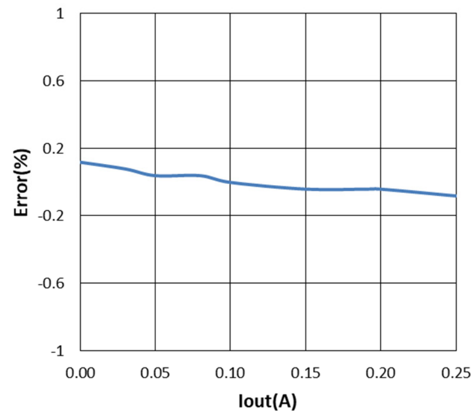
LDO1 Load Regulation
VIN=3.3V, VOUT=1.8V



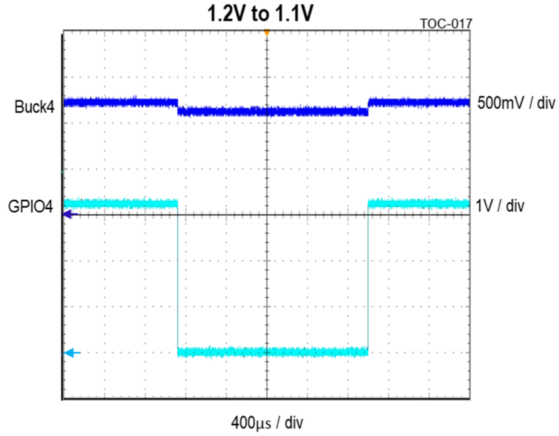
LDO2 Load Regulation
VIN=3.3V, VOUT=1.8V



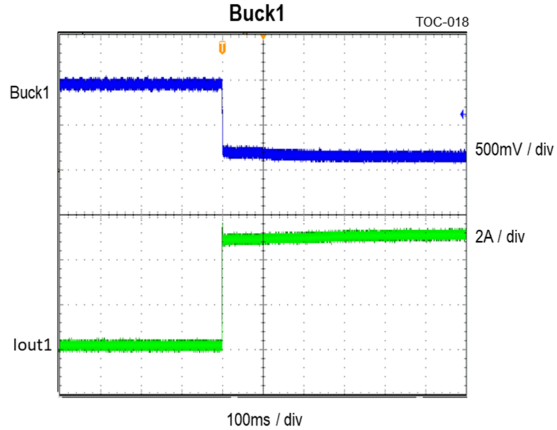
LDO3 Load Regulation
VIN=3.3V, VOUT=2.5V



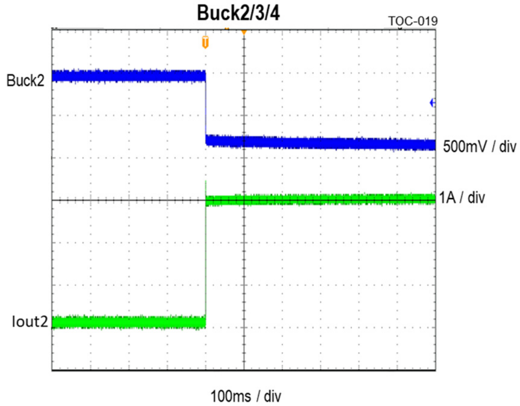
DVS Transition
Buck4
1.2V to 1.1V



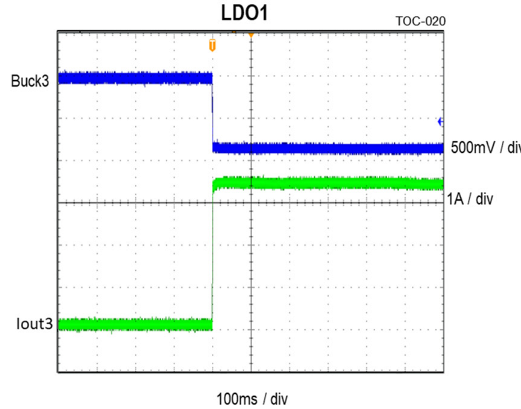
Short Circuit
Buck1



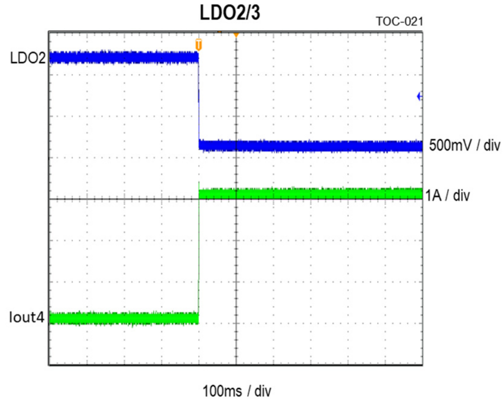
Short Circuit
Buck2/3/4



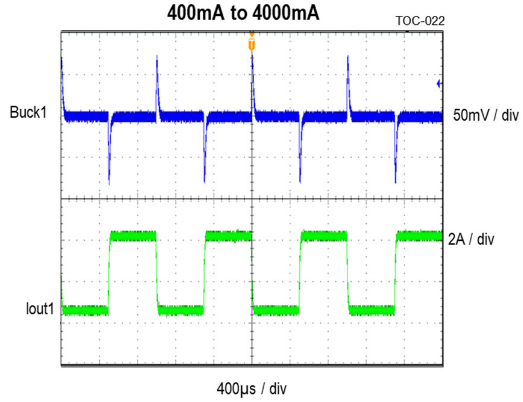
Short Circuit
LDO1



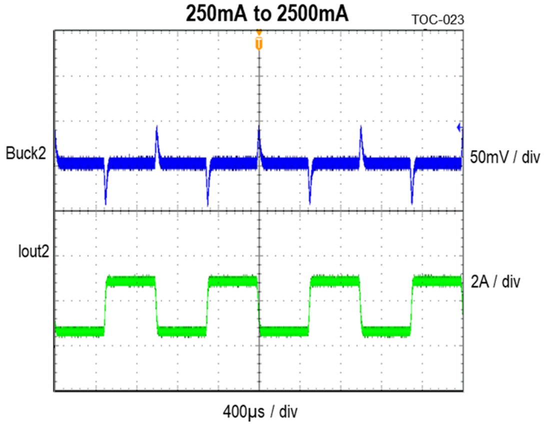
Short Circuit
LDO2/3



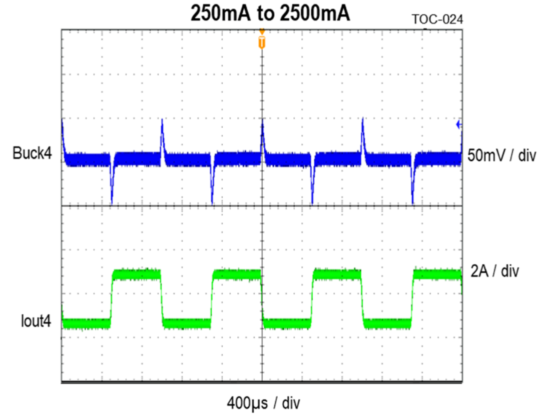
Load Transient
Buck1 Vout=0.95V
400mA to 4000mA



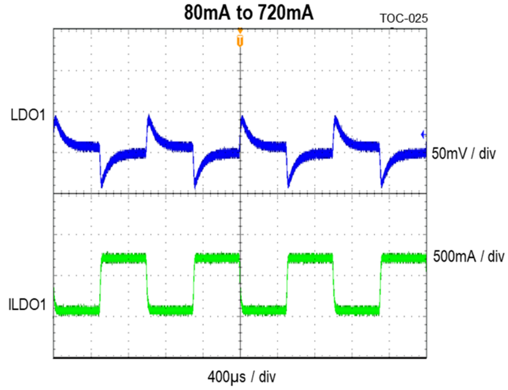
Load Transient
Buck2/3 Vout=0.95V
250mA to 2500mA



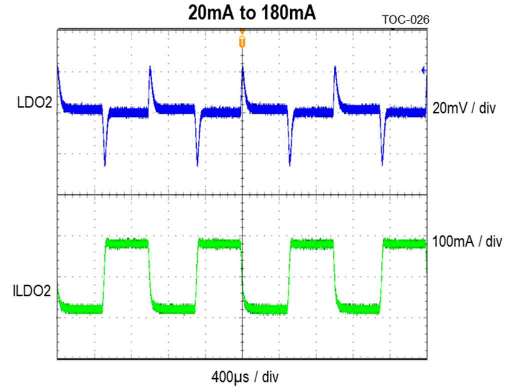
Load Transient
Buck4 Vout=1.2V
250mA to 2500mA



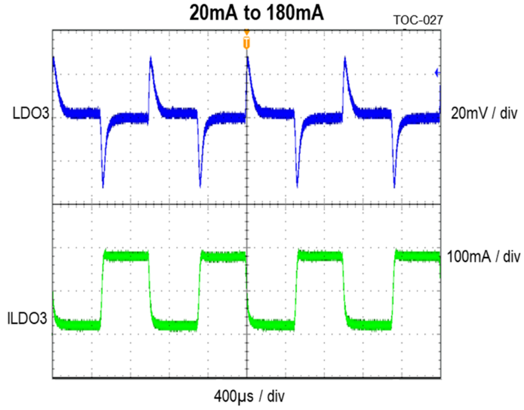
Load Transient
LDO1 Vout=1.8V
80mA to 720mA



Load Transient
LDO2 Vout=1.8V
20mA to 180mA



Load Transient
LDO3 Vout=2.5V
20mA to 180mA



CMI OPTIONS

This section provides the basic default configuration settings for each available ACT88430 CMI option. IC functionality in this section supersedes functionality in the main datasheet. Generating the desired functionality for a custom CMI sometimes requires reassigning internal resources, resulting in removal of base IC functionality. The following sections attempt to describe any removed functionality from the base IC functionality. The user is required to fully test all required functionality to ensure the CMI fully meets their requirements.

CMI 101: ACT88430QJ101-T

CMI 101 is optimized for the HiSilicon Hi3519 video processor. It is designed to operate from a 3V to 5V input voltage.

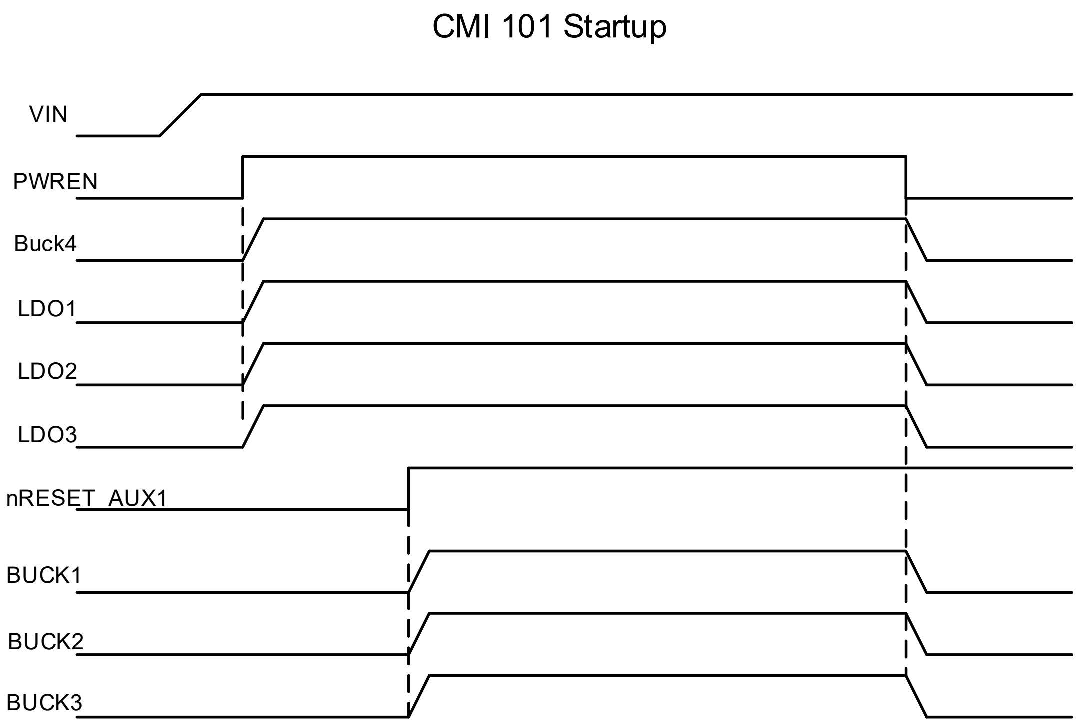
Voltage and Currents

Rail	Active Mode Voltage VSET0 (V)	DVS Voltage VSET1 (V)	DVS Voltage Trigger	Sleep Mode Voltage (V)	Current Limit (A)	Fsw (kHz)
Buck1	0.95	0.95	n/a	0	4	1125
Buck2	0.95	0.95	n/a	0	2.5	1125
Buck3	0.95	0.95	n/a	0	2.5	1125
Buck4	1.2	1.1	GPIO	1.2	2.5	1125
LDO1	1.8	n/a	n/a	1.8	0.8	n/a
LDO2	1.8	n/a	n/a	1.8	0.2	n/a
LDO3	2.5	n/a	n/a	2.5	0.2	n/a
EXT_EN	n/a	n/a	n/a	n/a	n/a	n/a
EXT_PG	n/a	n/a	n/a	n/a	n/a	n/a

Startup and Sequencing

Rail	Sequence Order	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)
LDO1	1	PWREN	41	200
Buck4	1	PWREN	41	200
LDO2	1	PWREN	41	200
LDO3	1	PWREN	41	200
Buck1	2	RESET_AUX1 AND PWREN	41	323
Buck2	2	RESET_AUX1 AND PWREN	41	200
Buck3	2	RESET_AUX1 AND PWREN	41	126

Startup



SLEEP Mode

Pull PWREN high to operate in ACTIVE mode. Pull PWREN low to operate in SLEEP. Outputs Buck4, LDO1/2/3 are on in ACTIVE mode and off in SLEEP mode.

DVS Mode

GPIO is the DVS control input. When GPIO = H, the VSET0 register controls the buck converter output voltages. When GPIO = L the VSET1 register controls the buck converter output voltages. Note that the default VSET0 and VSET1 settings are the same for each buck converter except Buck4. Buck 4 operates at 1.2V in ACTIVE mode and at 1.1V when DVS is activated.

POK Thresholds

POK_UV = 2.8V

POK_OV = 5.5V

PG

The PG pin is triggered by Buck1.

POK

The POK pin is functional with CMI 101.

EXT_EN

The EXT_EN pin is functional with CMI 101. Connect to the enable signal of an external power supply.

nRESET

nRESET is not functional with CMI 101. Leave nRESET floating.

nRESET_AUX1

The nRESET_AUX1 pin is programmed as a digital input. The nRESET_AUX1 input should default L when power is applied to the IC. When nRESET_AUX1 = H, Buck1, Buck2, and Buck3 turn on. When nRESET_AUX1 = L, these outputs turn off. Note that PWREN must be H before nRESET_AUX1 is pulled high.

nRESET_AUX2

The nRESET_AUX2 pin is not functional with CMI 101. Leave the nRESET_AUX2 pin floating.

EXT_PG

The EXT_PG pin is not functional with CMI 101. Leave the EXT_PG pin floating.

MODE

The MODE pin must be tied to ground.

GPIO

GPIO is the DVS control input. When GPIO = H, the VSET0 register controls the buck converter output voltages. When GPIO = L the VSET1 register controls the buck converter output voltages. Note that the default VSET0 and VSET1 settings are the same for each buck converter except Buck4. Buck 4 operates at 1.2V in ACTIVE mode and at 1.1V when DVS is activated.

Buck1/2/3 Voltage Setting

Buck1/2/3 reference voltage is 0.6V. This sets the allowable voltage range between 0.6V to 3.000V in 9.375mV steps.

LDO1/3 Voltage Setting

The LDO1/3 reference voltage is 0.8V. This sets the allowable voltage range between 2.0V to 3.575V in 25mV steps.

LDO2 Voltage Setting

The LDO2 reference voltage is 0.6V. This sets the allowable voltage range between 0.8V to 2.375V in 25mV steps.

Device ID

The CMI 101 Device ID (register 0x7Dh) = 0x01h

I2C Address

The CMI 101 7-bit I2C address is 0x53h. This results in 0xA6h for a write address and 0xA7h for a read address.

CMI 102: ACT88430QJ102-T

CMI 102 is optimized for a custom solid state disk (SSD) drive controller. It is designed to operate from a 3.3V input voltage.

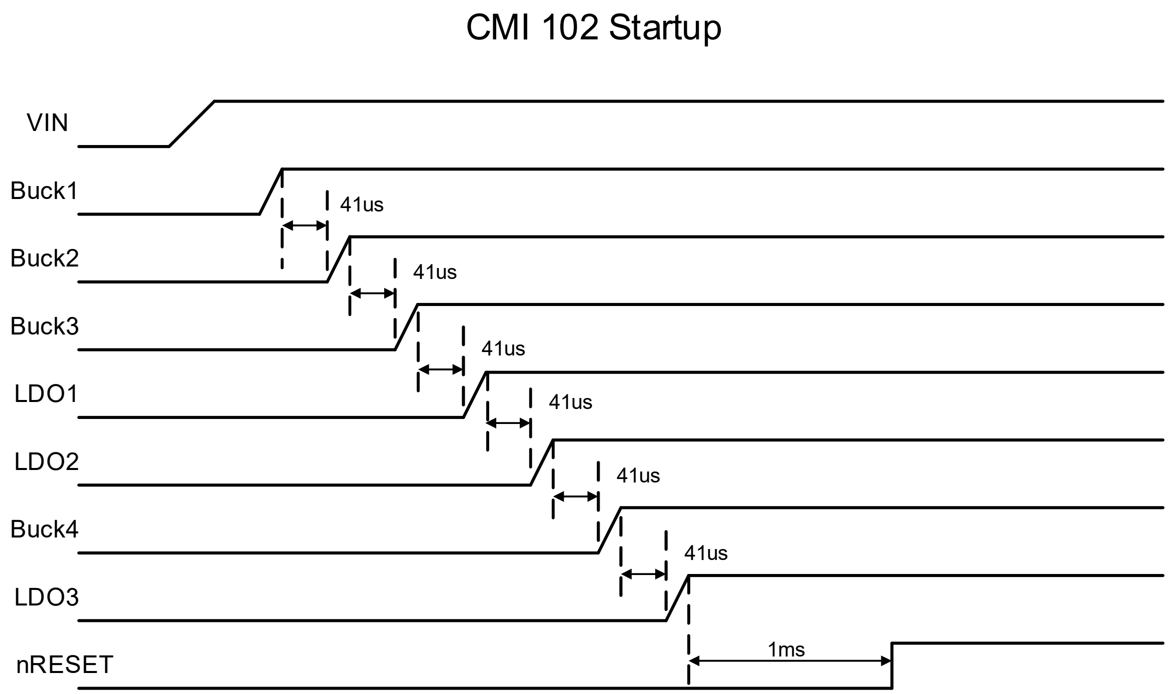
Voltage and Currents

Rail	Active Mode Voltage VSET0 (V)	DVS Voltage VSET1 (V)	DVS Voltage Trigger	Sleep Mode Voltage (V)	Current Limit (A)	Fsw (kHz)
Buck1	3.3	3.3	EXT_PG	n/a	5.3	2250
Buck2	0.7406	0.7406	EXT_PG	n/a	4	2250
Buck3	0.8813	0.8813	EXT_PG	n/a	3	2250
Buck4	1.8	1.8	EXT_PG	n/a	3	2250
LDO1	1.2	n/a	n/a	n/a	1	n/a
LDO2	0.9	n/a	n/a	n/a	0.315	n/a
LDO3	1.2	n/a	n/a	n/a	0.39	n/a
EXT_EN	n/a	n/a	n/a	n/a	n/a	n/a
EXT_PG	n/a	n/a	n/a	n/a	n/a	n/a

Startup and Sequencing

Rail	Sequence Order	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)
Buck1	1	GPIO	41	485
Buck2	2	Buck1	41	485
Buck3	3	Buck2	41	485
LDO1	4	Buck3	41	440
LDO2	5	LDO1	41	220
Buck4	6	LDO2	41	204
LDO3	7	Buck4	41	126

Startup



SLEEP Mode

CMI 102 does not use SLEEP Mode.

DVS Mode

EXT_PG is the DVS control input. When EXT_PG = L, the VSET0 register controls the buck converter output voltages. When EXT_PG = H the VSET1 register controls the buck converter output voltages. Note that the default VSET0 and VSET1 settings are the same for each buck converter.

POK Thresholds

POK_UV = 2.7V

POK_OV = 3.6V

PG

The PG pin is not functional with CMI 102. Leave the PG pin floating.

POK

The POK pin is not functional with CMI 102. Leave the POK pin floating.

EXT_EN

The EXT_EN pin is not functional with CMI 102. Leave the EXT_EN pin floating.

nRESET

nRESET is triggered from LDO3. It goes high 1ms after LDO3 goes into regulation.

nRESET_AUX1

The nRESET_AUX1 pin is not functional with CMI 102. Leave the nRESET_AUX1 pin floating.

nRESET_AUX2

The nRESET_AUX2 pin is not functional with CMI 102. Leave the nRESET_AUX2 pin floating.

EXT_PG

EXT_PG is the DVS control input for Buck4. When EXT_PG = L, Buck4 = 1.8V. When EXT_PG = H, Buck4 = 1.2V

MODE

The MODE pin must be tied to ground.

GPIO

The GPIO pin is the input trigger for Buck1. When GPIO goes high, Buck1 turns on and starts the turn on sequencing. When GPIO goes low, all outputs immediately turn off.

Buck1/2/3 Voltage Setting

Buck1/2/3 reference voltage is 0.6V. This sets the allowable voltage range between 0.6V to 3.000V in 9.375mV steps.

LDO1/3 Voltage Setting

The LDO1/3 reference voltage is 0.8V. This sets the allowable voltage range between 2.0V to 3.575V in 25mV steps.

LDO2 Voltage Setting

The LDO2 reference voltage is 0.6V. This sets the allowable voltage range between 0.8V to 2.375V in 25mV steps.

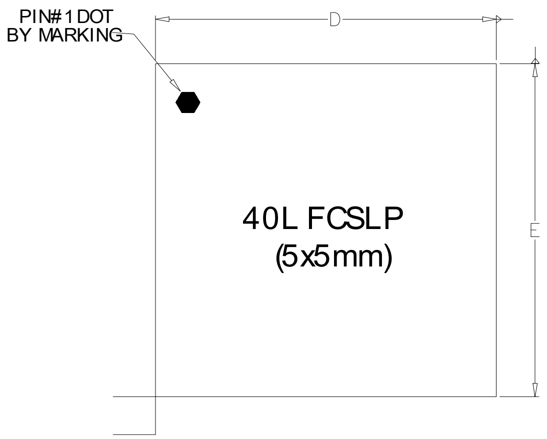
Device ID

The CMI 102 Device ID (register 0x7Dh) = 0x00h

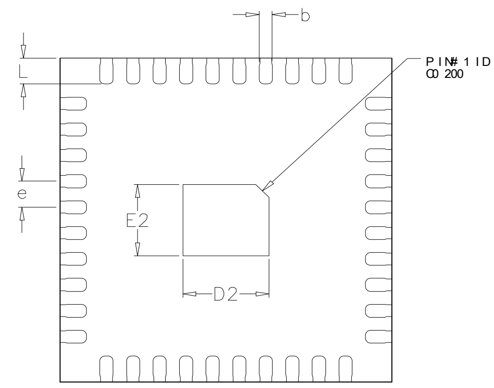
I2C Address

The CMI 102 7-bit I2C address is 0x53h. This results in 0xA6h for a write address and 0xA7h for a read address.

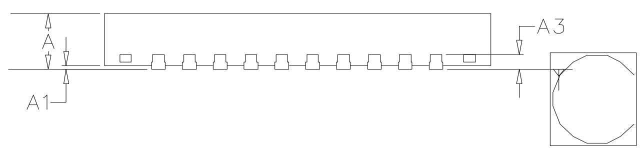
PACKAGE OUTLINE AND DIMENSIONS QFN55-40



Top View



Bottom View



Side View

SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	-	0.050	-	0.002
A3	0.203 REF		0.008 REF	
D	4.950	5.050	0.195	0.199
E	4.950	5.050	0.195	0.199
D2	1.250	1.350	0.049	0.053
E2	1.050	1.150	0.041	0.045
b	0.150	0.250	0.006	0.010
e	0.400 BSC		0.016 BSC	
L	0.350	0.450	0.014	0.018

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С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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