

Features

- 4A Source/Sink Drive Current
- Wide Operating Voltage Range: 4.5V to 35V
- -40°C to +125°C Extended Operating Temperature Range
- Logic Input Withstands Negative Swing of up to 5V
- Outputs May be Connected in Parallel for Higher Drive Current
- Matched Rise and Fall Times
- Low Propagation Delay Time
- Low, 10 μ A Supply Current
- Low Output Impedance

Applications

- Efficient Power MOSFET and IGBT Switching
- Switch Mode Power Supplies
- Motor Controls
- DC to DC Converters
- Class-D Switching Amplifiers
- Pulse Transformer Driver



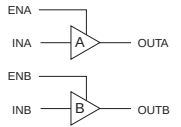
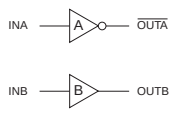
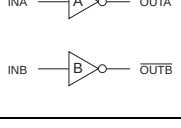
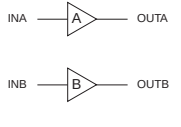
Description

The IXDD604/IXDF604/IXDI604/IXDN604 dual high-speed gate drivers are especially well suited for driving the latest IXYS MOSFETs and IGBTs. Each of the two outputs can source and sink 4A of current while producing voltage rise and fall times of less than 10ns. The input of each driver is virtually immune to latch up, and proprietary circuitry eliminates cross conduction and current "shoot-through." Low propagation delay and fast, matched rise and fall times make the IXD_604 family ideal for high-frequency and high-power applications.

The IXDD604 is a dual non-inverting driver with an enable. The IXDN604 is a dual non-inverting driver, the IXDI604 is a dual inverting driver, and the IXDF604 has one inverting driver and one non-inverting driver.

The IXD_604 family is available in a standard 8-pin DIP (PI), 8-pin SOIC (SIA), 8-pin Power SOIC with an exposed metal back (SI), and an 8-pin DFN (D2) package.

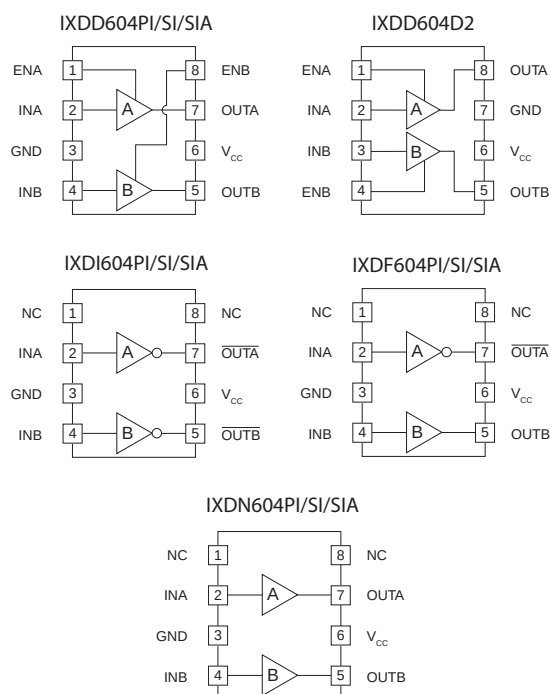
Ordering Information

Part Number	Logic Configuration	Package Type	Packing Method	Quantity
IXDD604D2TR		8-Pin DFN	Tape & Reel	2000
IXDD604PI		8-Pin DIP	Tube	50
IXDD604SI		8-Pin Power SOIC with Exposed Metal Back	Tube	100
IXDD604SITR		8-Pin Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDD604SIA		8-Pin SOIC	Tube	100
IXDD604SIATR		8-Pin SOIC	Tape & Reel	2000
IXDF604PI		8-Pin DIP	Tube	50
IXDF604SI		8-Pin Power SOIC with Exposed Metal Back	Tube	100
IXDF604SITR		8-Pin Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDF604SIA		8-Pin SOIC	Tube	100
IXDF604SIATR		8-Pin SOIC	Tape & Reel	2000
IXDI604PI		8-Pin DIP	Tube	50
IXDI604SI		8-Pin Power SOIC with Exposed Metal Back	Tube	100
IXDI604SITR		8-Pin Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDI604SIA		8-Pin SOIC	Tube	100
IXDI604SIATR		8-Pin SOIC	Tape & Reel	2000
IXDN604PI		8-Pin DIP	Tube	50
IXDN604SI		8-Pin Power SOIC with Exposed Metal Back	Tube	100
IXDN604SITR		8-Pin Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDN604SIA		8-Pin SOIC	Tube	100
IXDN604SIATR		8-Pin SOIC	Tape & Reel	2000

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1 Specifications

1.1 Pin Configurations



1.2 Pin Definitions

Pin Name	Description
INA	Channel A Logic Input
INB	Channel B Logic Input
ENA	Channel A Enable Input - Drive pin low to disable Channel A and force Channel A Output to a high impedance state
ENB	Channel B Enable Input - Drive pin low to disable Channel A and force Channel A Output to a high impedance state
OUTA OUTA	Channel A Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
OUTB OUTB	Channel B Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
V _{CC}	Supply Voltage - Provides power to the device
GND	Ground - Common ground reference for the device

1.3 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V _{CC}	-0.3	40	V
Input Voltage	V _{INx} , V _{ENx}	-5	V _{CC} +0.3	V
Output Current	I _{OUT}	-	±4	A
Output Pulsed Current (0.5μs)	I _{out_pulsed}	-	±5	A
Junction Temperature	T _J	-55	+150	°C
Storage Temperature	T _{STG}	-65	+150	°C

Absolute maximum electrical ratings are at 25°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Range	Units
Supply Voltage	V _{CC}	4.5 to 35	V
Operating Temperature Range	T _A	-40 to +125	°C

1.5 Electrical Characteristics: $T_A = 25^\circ\text{C}$

Test Conditions: $4.5\text{V} \leq V_{CC} \leq 35\text{V}$, one channel (unless otherwise noted).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Input Voltage, High	$4.5\text{V} \leq V_{CC} \leq 18\text{V}$	V_{IH}	3.0	-	-	V
Input Voltage, Low	$4.5\text{V} \leq V_{CC} \leq 18\text{V}$	V_{IL}	-	-	0.8	
Input Current	$0\text{V} \leq V_{IN} \leq V_{CC}$	I_{IN}	-	-	± 10	μA
High EN Input Voltage	IXDD604 only	V_{ENH}	$2/3V_{CC}$	-	-	V
Low EN Input Voltage	IXDD604 only	V_{ENL}	-	-	$1/3V_{CC}$	
Output Voltage, High	-	V_{OH}	$V_{CC}-0.025$	-	-	V
Output Voltage, Low	-	V_{OL}	-	-	0.025	
Output Resistance, High State	$V_{CC}=18\text{V}$, $I_{OUT}=-10\text{mA}$	R_{OH}	-	1.3	2.5	Ω
Output Resistance, Low State	$V_{CC}=18\text{V}$, $I_{OUT}=10\text{mA}$	R_{OL}	-	1.1	2	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	-	± 1	A
Rise Time	$V_{CC}=18\text{V}$, $C_{LOAD}=1000\text{pF}$	t_r	-	9	16	ns
Fall Time	$V_{CC}=18\text{V}$, $C_{LOAD}=1000\text{pF}$	t_f	-	8	14	
On-Time Propagation Delay	$V_{CC}=18\text{V}$, $C_{LOAD}=1000\text{pF}$	t_{ondly}	-	29	50	
Off-Time Propagation Delay	$V_{CC}=18\text{V}$, $C_{LOAD}=1000\text{pF}$	t_{offdly}	-	35	50	
Enable to Output-High Delay Time	IXDD604 only, $V_{CC}=18\text{V}$	t_{ENOH}	-	35	55	
Disable to High Impedance State Delay Time	IXDD604 only, $V_{CC}=18\text{V}$	t_{DOLD}	-	40	55	
Enable Pull-Up Resistor	-	R_{EN}	-	200	-	$k\Omega$
Power Supply Current	$V_{CC}=18\text{V}$, $V_{IN}=3.5\text{V}$	I_{CC}	-	1	3	μA
	$V_{CC}=18\text{V}$, $V_{IN}=0\text{V}$		-	<1	10	
	$V_{CC}=18\text{V}$, $V_{IN}=V_{CC}$		-	<1	10	

1.6 Electrical Characteristics: $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

Test Conditions: $4.5\text{V} \leq V_{CC} \leq 35\text{V}$, one channel (unless otherwise noted).

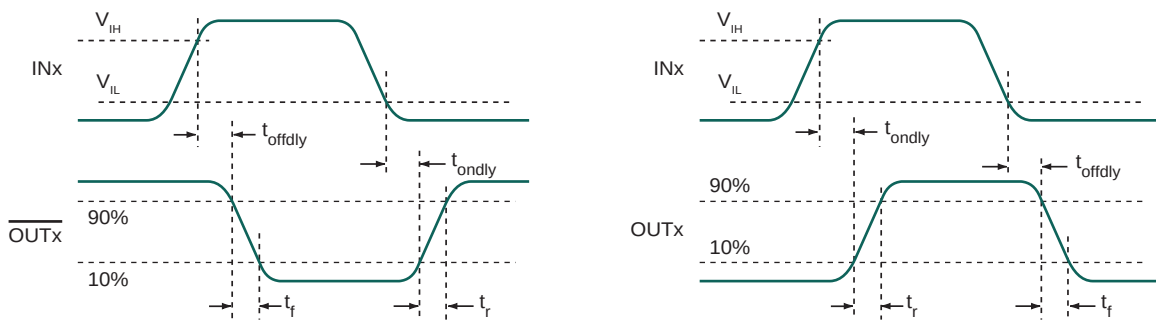
Parameter	Conditions	Symbol	Minimum	Maximum	Units
Input Voltage, High	$4.5\text{V} \leq V_{CC} \leq 18\text{V}$	V_{IH}	3.3	-	V
Input Voltage, Low	$4.5\text{V} \leq V_{CC} \leq 18\text{V}$	V_{IL}	-	0.65	
Input Current	$0\text{V} \leq V_{IN} \leq V_{CC}$	I_{IN}	-10	10	μA
Output Voltage, High	-	V_{OH}	$V_{CC}-0.025$	-	V
Output Voltage, Low	-	V_{OL}	-	0.025	
Output Resistance, High State	$V_{CC}=18\text{V}$, $I_{OUT}=-10\text{mA}$	R_{OH}	-	3	Ω
Output Resistance, Low State	$V_{CC}=18\text{V}$, $I_{OUT}=10\text{mA}$	R_{OL}	-	2.5	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	± 1	A
Rise Time	$V_{CC}=18\text{V}$, $C_{LOAD}=1000\text{pF}$	t_r	-	16	ns
Fall Time	$V_{CC}=18\text{V}$, $C_{LOAD}=1000\text{pF}$	t_f	-	14	
On-Time Propagation Delay	$V_{CC}=18\text{V}$, $C_{LOAD}=1000\text{pF}$	t_{ondly}	-	65	
Off-Time Propagation Delay	$V_{CC}=18\text{V}$, $C_{LOAD}=1000\text{pF}$	t_{offdly}	-	65	
Enable to Output-High Delay Time	IXDD604 only, $V_{CC}=18\text{V}$	t_{ENOH}	-	65	
Disable to High Impedance State Delay Time	IXDD604 only, $V_{CC}=18\text{V}$	t_{DOLD}	-	65	
Power Supply Current	$V_{CC}=18\text{V}$, $V_{IN}=3.5\text{V}$	I_{CC}	-	3.5	μA
	$V_{CC}=18\text{V}$, $V_{IN}=0\text{V}$		-	150	
	$V_{CC}=18\text{V}$, $V_{IN}=V_{CC}$		-	150	

1.7 Thermal Characteristics

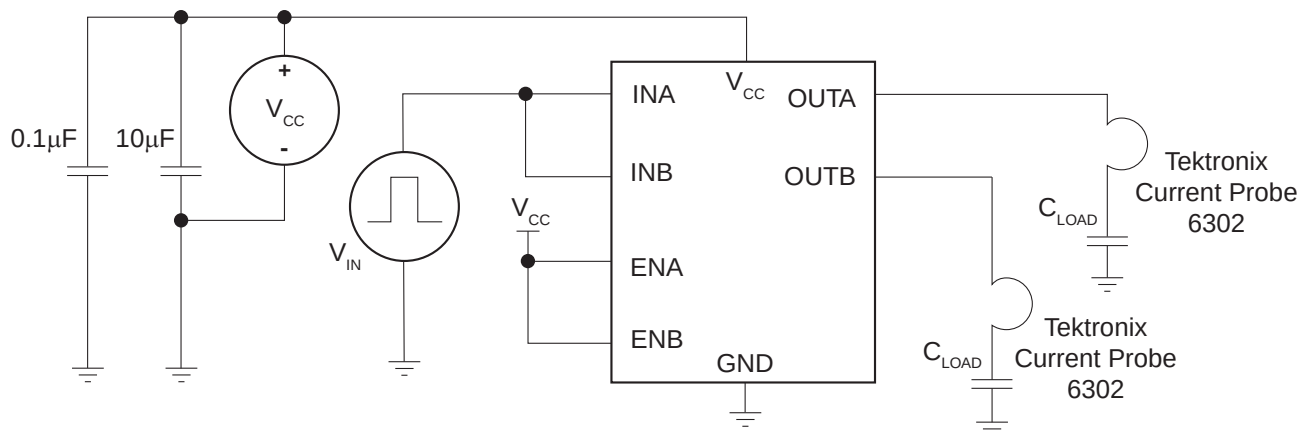
Package	Parameter	Symbol	Rating	Units
D2 (8-Pin DFN)	Thermal Resistance, Junction-to-Ambient	θ_{JA}	35	°C/W
PI (8-Pin DIP)			125	
SI (8-Pin Power SOIC)			85	
SIA (8-Pin SOIC)			120	
SI (8-Pin Power SOIC)	Thermal Resistance, Junction-to-Case	θ_{JC}	10	°C/W

2 IXD_604 Performance

2.1 Timing Diagrams

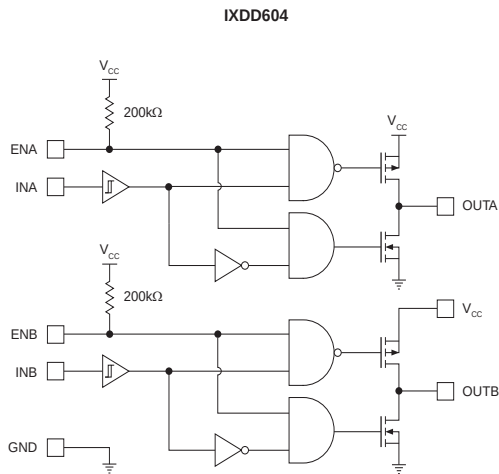


2.2 Characteristics Test Diagram



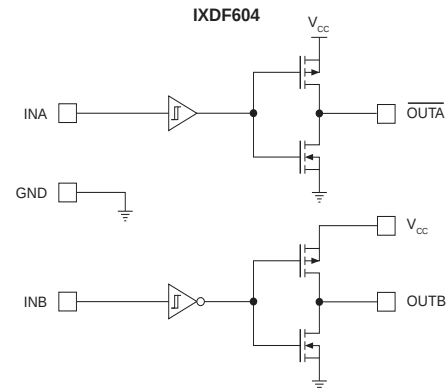
3 Block Diagrams & Truth Tables

3.1 IXDD604



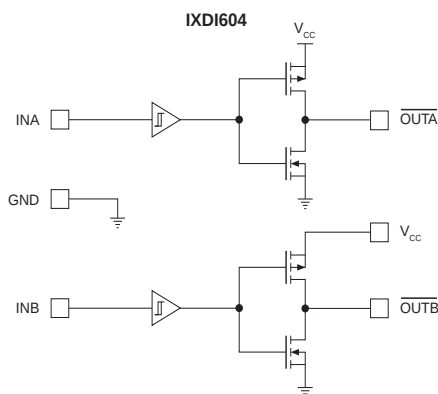
IN _x	EN _x	OUT _x
0	1 or open	0
1	1 or open	1
0	0	Z
1	0	Z

3.3 IXDF604



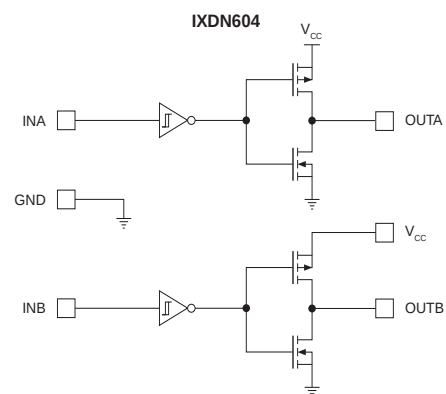
INA	OUTA
0	1
1	0
INB	OUTB
0	0
1	1

3.2 IXDI604



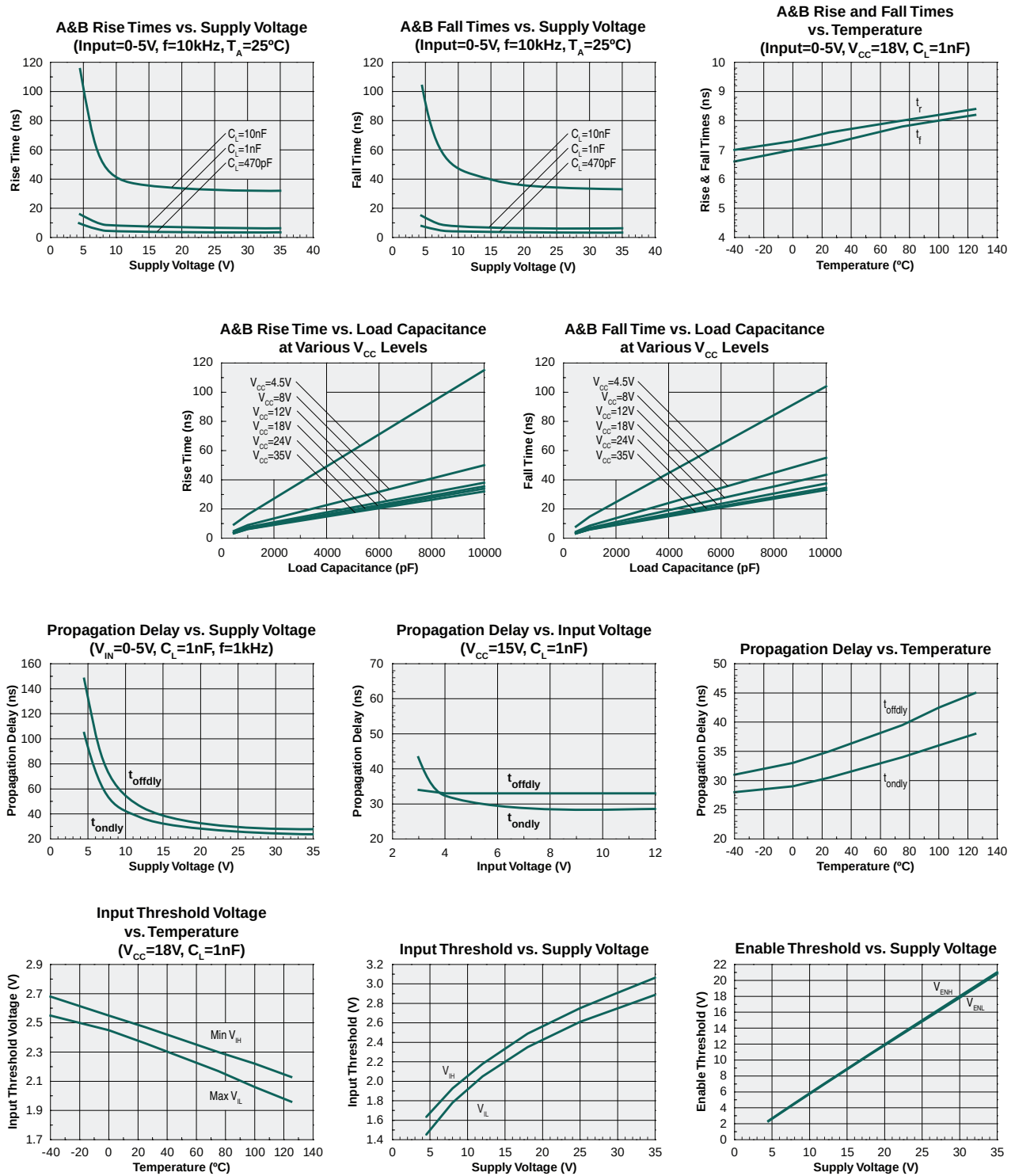
IN _x	OUT _x
0	1
1	0

3.4 IXDN604

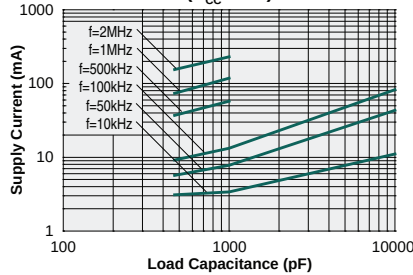


IN _x	OUT _x
0	0
1	1

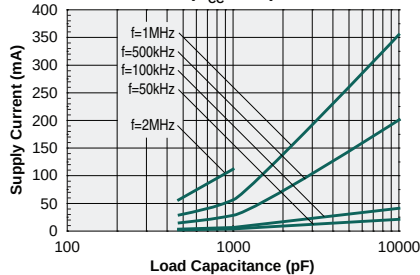
4 Typical Performance Characteristics



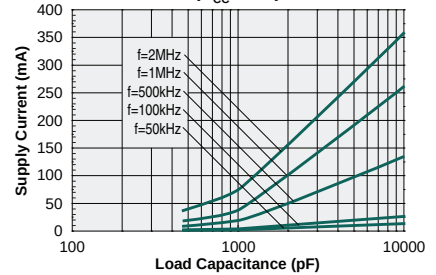
**Supply Current vs. Load Capacitance
Both Outputs Active
($V_{CC}=35V$)**



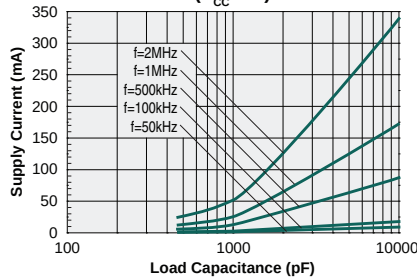
**Supply Current vs. Load Capacitance
Both Outputs Active
($V_{CC}=18V$)**



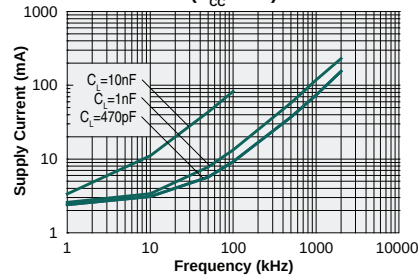
**Supply Current vs. Load Capacitance
Both Outputs Active
($V_{CC}=12V$)**



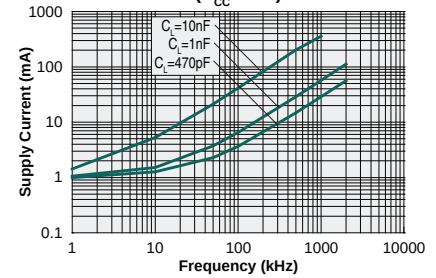
**Supply Current vs. Load Capacitance
Both Outputs Active
($V_{CC}=8V$)**



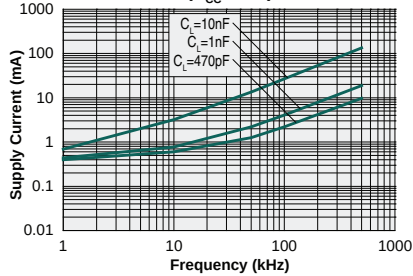
**Supply Current vs. Frequency
Both Outputs Active
($V_{CC}=35V$)**



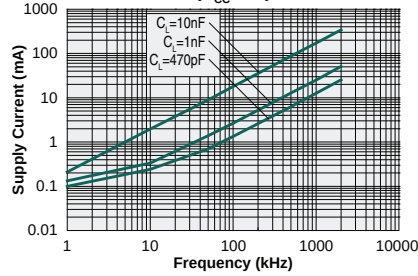
**Supply Current vs. Frequency
Both Outputs Active
($V_{CC}=18V$)**



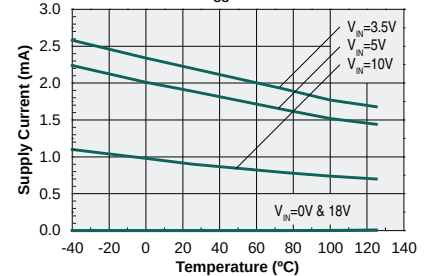
**Supply Current vs. Frequency
Both Outputs Active
($V_{CC}=12V$)**



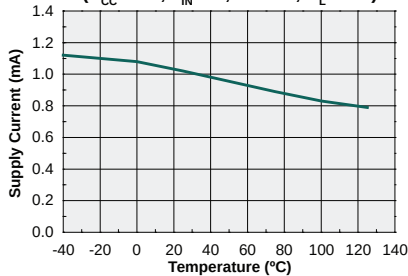
**Supply Current vs. Frequency
Both Outputs Active
($V_{CC}=8V$)**



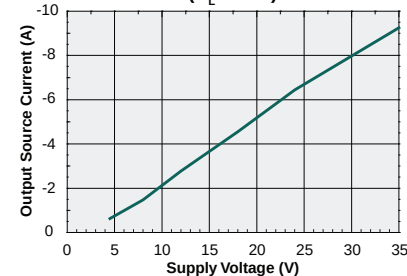
**Quiescent Supply Current
vs. Temperature
($V_{CC}=18V$)**



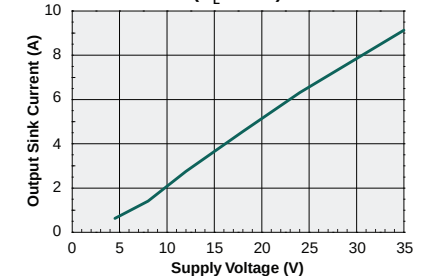
**Dynamic Supply Current
vs. Temperature
($V_{CC}=18V$, $V_{IN}=5V$, $f=1kHz$, $C_L=1nF$)**

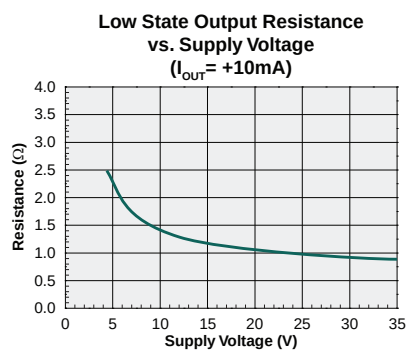
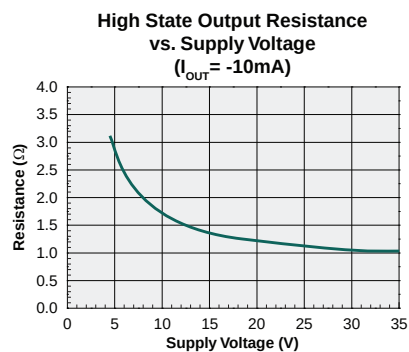
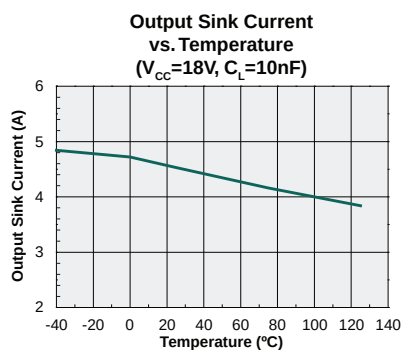
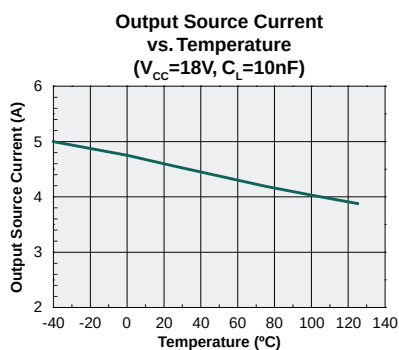


**Output Source Current
vs. Supply Voltage
($C_L=10nF$)**



**Output Sink Current
vs. Supply Voltage
($C_L=10nF$)**





5 Manufacturing Information

5.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation.

We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IXD_604 All Versions	MSL 1

5.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be ($T_C - 5^\circ\text{C}$) or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of J-STD-020 must be observed.

Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
IXD_604SI / IXD_604SIA / IXD_604D2	260°C	30 seconds	3
IXD_604PI	250°C	30 seconds	-

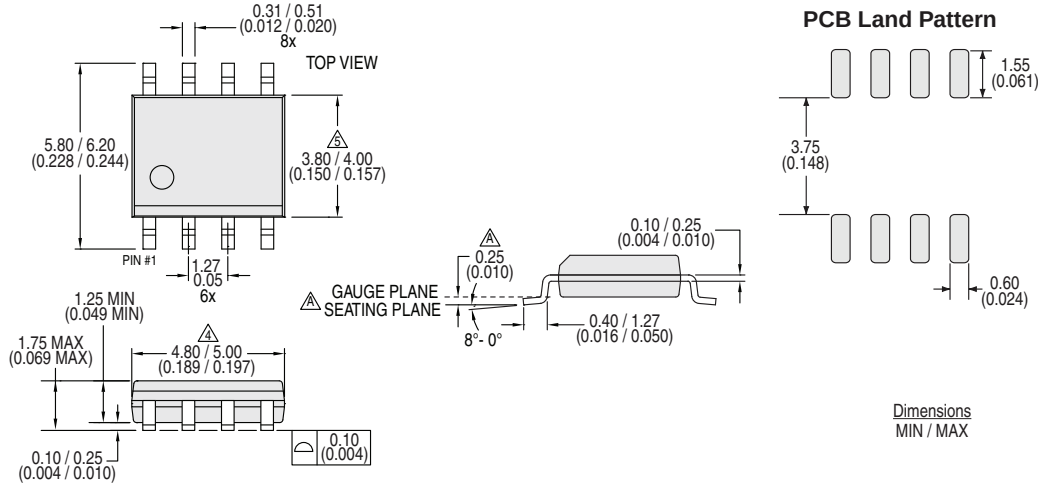
5.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based



5.5 Mechanical Dimensions

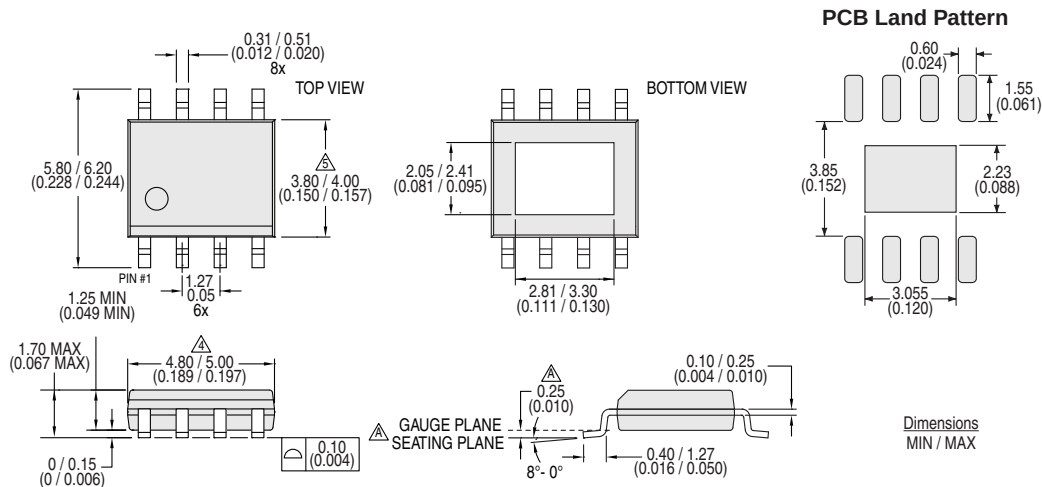
5.5.1 SIA (8-Pin SOIC)



Notes:

1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation AA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. Lead thickness includes plating.

5.5.2 SI (8-Pin Power SOIC with Exposed Metal Back)



Notes:

1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation BA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. The exposed metal pad on the back of the package should be connected to GND. It is not suitable for carrying current.
7. Lead thickness includes plating.

The diagram illustrates the dimensions and components of a 156-pin Quad Flat Pack (QFP) tape carrier assembly. It includes a perspective view of the carrier and a top-down view of the carrier with dimensions.

Carrier Dimensions and Components:

- 330.2 DIA. (13.00 DIA.):** The diameter of the carrier.
- Top Cover Tape Thickness 0.102 MAX. (0.004 MAX.):** The thickness of the top cover tape.
- Embossed Carrier:** The carrier with embossed features.
- Embossment:** The embossed feature on the carrier.

Carrier Dimensions:

- $K_0 = 2.10$ (0.083):** The distance from the center of the carrier to the center of the first pin.
- $B_0 = 5.30$ (0.209):** The distance from the center of the carrier to the center of the first pin.
- $A_0 = 6.50$ (0.256):** The distance from the center of the carrier to the center of the first pin.
- $P1 = 8.00$ (0.315):** The pitch of the pins.
- $W = 12.00$ (0.472):** The width of the carrier.

Dimensions: mm (inches)

NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

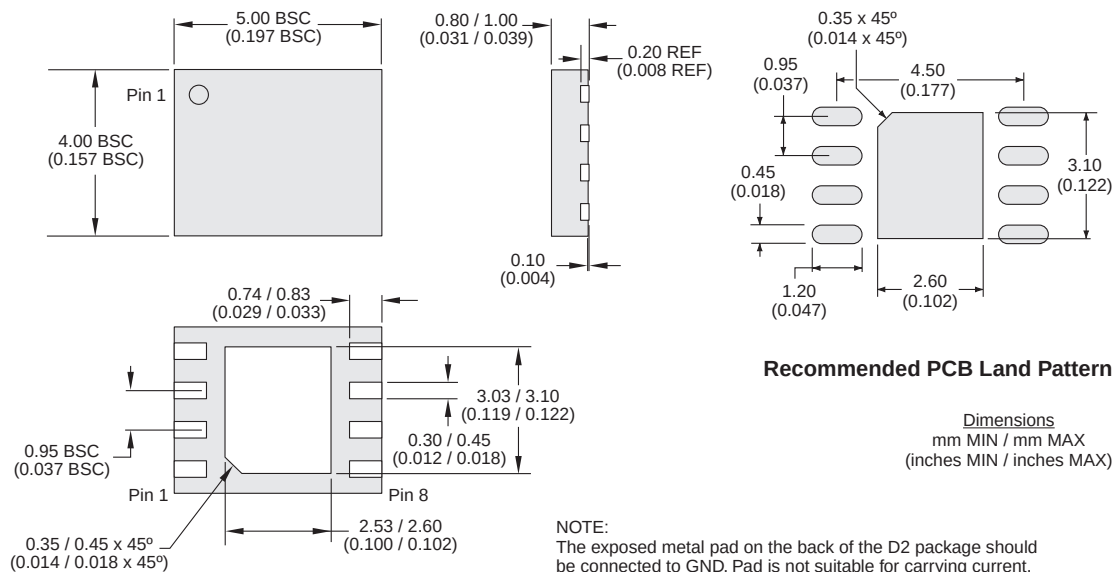
NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

The mechanical drawings illustrate the PCB Hole Pattern with the following dimensions:

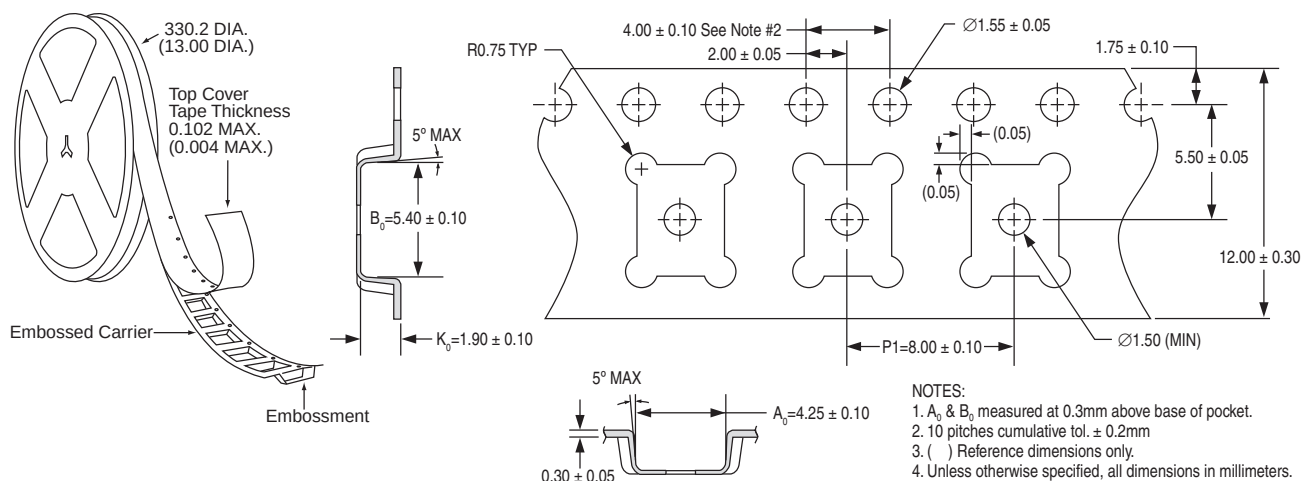
- Top View:**
 - Overall width: 9.652 ± 0.381 mm (0.380 ± 0.015)
 - Distance from left edge to first pin: 2.540 ± 0.127 mm (0.100 ± 0.005)
 - Pin pitch: 6.350 ± 0.127 mm (0.250 ± 0.005)
 - Pin 1 location: 0.457 ± 0.076 mm (0.018 ± 0.003) from the left edge.
 - Distance between pins: 4.064 TYP mm (0.160)
 - Pin diameter: 0.813 ± 0.102 mm (0.032 ± 0.004)
- Side View:**
 - Overall height: 7.620 ± 0.254 mm (0.300 ± 0.010)
 - Distance from top surface to pin base: 9.144 ± 0.508 mm (0.360 ± 0.020)
 - Pin height: 3.302 ± 0.051 mm (0.130 ± 0.002)
 - Pin width: 7.239 TYP mm (0.285)
 - Pin thickness: 0.254 ± 0.0127 mm (0.010 ± 0.0005)
- Hole Pattern View:**
 - Hole diameter: 8-0.800 DIA. (8-0.031 DIA.)
 - Distance between hole centers: 2.540 ± 0.127 mm (0.100 ± 0.005)
 - Distance from left edge to first hole: 7.620 ± 0.127 mm (0.300 ± 0.005)
 - Distance between hole rows: 7.620 ± 0.127 mm (0.300 ± 0.005)

Dimensions
mm
(inches)

5.5.5 D2 (8-Pin DFN)



5.5.6 Tape & Reel Information for D2 Package



For additional information please visit our website at: www.ixysic.com

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- Оценку стоимости проекта по компонентам.
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