ULTRA PRECISION 8:1 MUX WITH INTERNAL TERMINATION AND 1:2 LVPECL FANOUT BUFFER

Precision Edge™
SY58038U

## FEATURES

- Selects between 1 of 8 inputs, and provides 2 precision, low skew LVPECL output copies
- Ultra-low jitter design:
  - 72fs$_{rms}$ phase jitter (typ)
- Guaranteed AC performance over temperature and voltage:
  - DC to 4.5Gbps throughput
  - <500ps propagation delay IN-to-Q ($V_{IN}$ > 100mV)
  - <100ps $t_r$ / $t_f$ time
  - <15ps skew (output-to-output)
- Unique, patent-pending, channel-to-channel isolation design provides superior crosstalk performance
- Unique, patent-pending, input termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- 800mV LVPECL output swing
- Power supply 2.5V ±5% or 3.3V ±10%
- –40°C to +85°C temperature range
- Available in 44-pin (7mm ∗ 7mm) QFN package

Precision Edge™

## DESCRIPTION

The SY58038U is a low jitter, low skew, high-speed 8:1 multiplexer with a 1:2 differential fanout buffer optimized for precision telecom and enterprise server distribution applications. The SY58038U distributes clock frequencies from DC to 3.5GHz, and data rates to 4.5Gpbs guaranteed over temperature and voltage.

The SY58038U differential input includes Micrel's unique, 3-pin input termination architecture that directly interfaces to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. The outputs are 800mV, 100K compatible LVPECL with extremely fast rise/fall times guaranteed to be less than 100ps.

The SY58038U features a patent-pending isolation design that significantly improves channel-to-channel crosstalk performance.

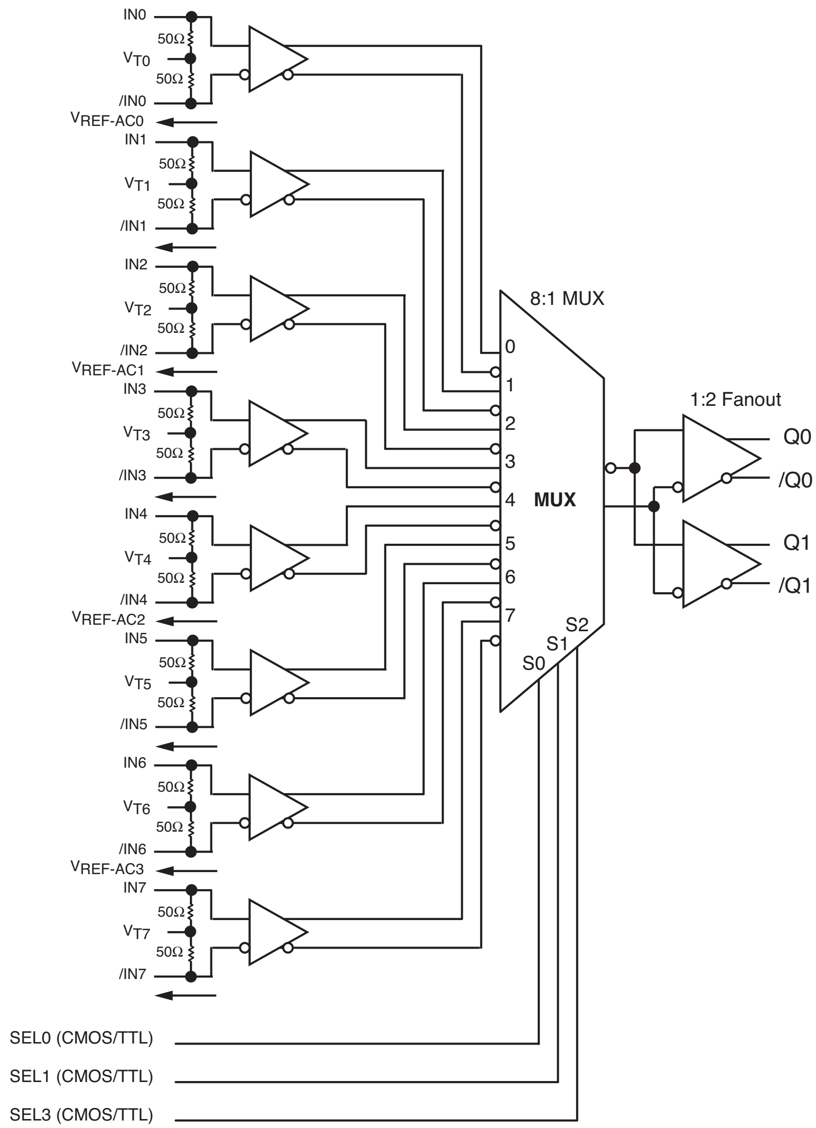
The SY58038U operates from a 2.5V ±5% or 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY58038U is part of Micrel's high-speed, Precision Edge™ product line.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

## APPLICATIONS

- Data communication systems
- All SONET/SDH data/clock applications
- All Fibre Channel applications
- All Gigabit Ethernet applications

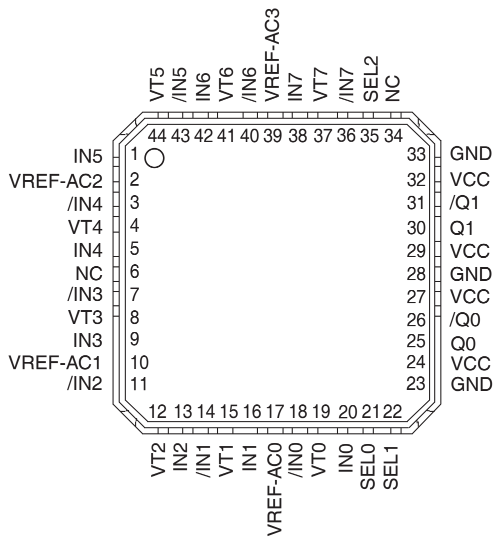
## FUNCTIONAL BLOCK DIAGRAM




## TRUTH TABLE

| SEL2 | SEL1 | SEL0 | Q | /Q |
|---|---|---|---|---|
| L | L | L | IN0 | /IN0 |
| L | L | H | IN1 | /IN1 |
| L | H | L | IN2 | /IN2 |
| L | H | H | IN3 | /IN3 |
| H | L | L | IN4 | /IN4 |
| H | L | H | IN5 | /IN5 |
| H | H | L | IN6 | /IN6 |
| H | H | H | IN7 | /IN7 |

## PACKAGE/ORDERING INFORMATION




**44-Pin QFN (QFN-44)**

### Ordering Information[1]

| Part Number | Package Type | Operating Range | Package Marking |
|---|---|---|---|
| SY58038UMI | QFN-44 Pb-Free | Industrial | SY58038U |
| SY58038UMITR[2] | QFN-44 Pb-Free | Industrial | SY58038U |

**Notes:**

1. Contact factory for die availability. Die are guaranteed at $T_A$ = 25°C, DC electricals only.
   All devices are Pb-Free.
2. Tape and Reel.

## PIN DESCRIPTION

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 20, 18, 16, 14, 13, 11, 9, 7, 5, 3, 1, 43, 42, 40, 38, 36 | IN0, /IN0, IN1, /IN1, IN2, /IN2, IN3, /IN3, IN4, /IN4, IN5,/IN5, IN6, /IN6, IN7, /IN7 | Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50ohms. Note that these inputs will default to an indeterminate state if left open.Please refer to the “Input Interface Applications” section for more details. |
| 19,15, 12, 8, 4, 44, 41, 37 | VT0, VT1 VT2, VT3, VT4, VT5, VT6, VT7 | Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details. For a CML or LVDS inputs, the VT pin is left floating. |
| 17, 10, 2 39 | VREF-AC0, VREF-AC1, VREF-AC2, VREF-AC3 | Reference Voltage: This output biases to $V_{CC}$–1.2V. It is used when AC coupling the inputs (IN, /IN). For AC-coupled applications, connect VREF_AC to the VT pin and bypass with a 0.01µF low ESR capacitor to $V_{CC}$. See “Input Interface Applications” section for more details. |
| 21, 22, 35 | SEL0, SEL1, SEL2 | The single-ended TTL/CMOS-compatible inputs select the inputs to the multiplexer. Note that this input is internally connected to a 25kohms pull-up resistor and will default to a logic HIGH state if left open. |
| 24, 27, 29, 32 | VCC | Positive Power Supply. Bypass with 0.1µF//0.01µF low ESR capacitors as close to each VCC pin. |
| 25, 26, 30, 31 | Q0,/Q0, Q1,/Q1 | Differential Outputs: These LVPECL output pairs are the outputs of the device. Unused output pairs may be left open. Each output is designed to drive 800mV into 50ohms terminated to $V_{CC}$–2V.(or $V_{CC}$–1.2V if AC-coupled). |
| 23, 28, 33 | GND, Exposed Pad | Ground. GND and exposed pad must both be connected to the most negative potential of chip ground. |

## Absolute Maximum Ratings[1]

Power Supply Voltage ($V_{CC}$) ...................... –0.5V to +4.0V
Input Voltage ($V_{IN}$) ........................................ –0.5V to $V_{CC}$
LVPECL Output Current ($I_{OUT}$)
  Continuous ........................................................ 50mA
  Surge ................................................................ 100mA
Termination Current[3]
  Source or sink current on VT pin ....................... ±100mA
Lead Temperature (soldering, 10 sec.) .................... 265°C
Storage Temperature Range ($T_S$) .......... –65°C to +150°C

## Operating Ratings[2]

Power Supply Voltage ($V_{CC}$) ................ +2.375V to +2.625V
 ........................................................... +3.0V to +3.6V
Ambient Temperature Range ($T_A$) ..............–40°C to +85°C
Package Thermal Resistance[4]
  QFN ($\theta_{JA}$)
    Still-Air ........................................................ 24°C/W
  QFN ($\psi_{JB}$)
    Junction-to-board ........................................... 12°C/W

## DC ELECTRICAL CHARACTERISTICS[5]

$T_A$= –40°C to +85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | $V_{CC}$ = 2.5V. | 2.375 | 2.5 | 2.625 | V |
| | | $V_{CC}$ = 3.3V. | 3.0 | 3.3 | 3.6 | V |
| $I_{CC}$ | Power Supply Current | No load, max. $V_{CC}$. | | 120 | 170 | mA |
| $R_{IN}$ | Input Resistance (IN-to-$V_T$) | | 40 | 50 | 60 | ohms |
| $R_{DIFF\_IN}$ | Differential Input Resistance (IN-to-/IN) | | 80 | 100 | 120 | ohms |
| $V_{IH}$ | Input HIGH Voltage (IN-to-/IN) | **Note 6** | $V_{CC}$–1.6 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage (IN-to-/IN) | | 0 | | $V_{IH}$–0.1 | V |
| $V_{IN}$ | Input Voltage Swing (IN-to-/IN) | See Figure 1a. | 0.1 | | 1.7 | V |
| $V_{DIFF\_IN}$ | Differential Input Voltage Swing (IN-to-/IN) | See Figure 1b. | 0.2 | | | V |
| $V_{T\_IN}$ | IN-to-$V_T$ (IN-to-/IN) | | | | 1.28 | V |
| $V_{REF-AC}$ | Output Reference Voltage | | $V_{CC}$–1.3 | $V_{CC}$–1.2 | $V_{CC}$–1.1 | V |

**Notes:**

1. Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB. $\Psi_{JB}$ uses 4-layer $\theta_{JA}$ in still-air number unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. $V_{IH}$ (min), not lower than 1.2V.

## LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS(7)

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $T_A$= –40°C to +85°C; $R_L$ = 50ohms to $V_{CC}$–2V, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage<br>Q, /Q | | $V_{CC}$–1.145 | | $V_{CC}$–0.895 | V |
| $V_{OL}$ | Output LOW Voltage<br>Q, /Q | | $V_{CC}$–1.945 | | $V_{CC}$–1.695 | V |
| $V_{OUT}$ | Output Differential Swing<br>Q, /Q | See Figure 1a. | 550 | 800 | | mV |
| $V_{DIFF\_OUT}$ | Differential Output Voltage Swing<br>Q, /Q | See Figure 1b. | 1100 | 1600 | | mV |

## LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS(7)

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $T_A$= –40°C to +85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | | –125 | | 30 | µA |
| $I_{IL}$ | Input LOW Current | | –300 | | | µA |

**Note:**

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC ELECTRICAL CHARACTERISTICS[8]

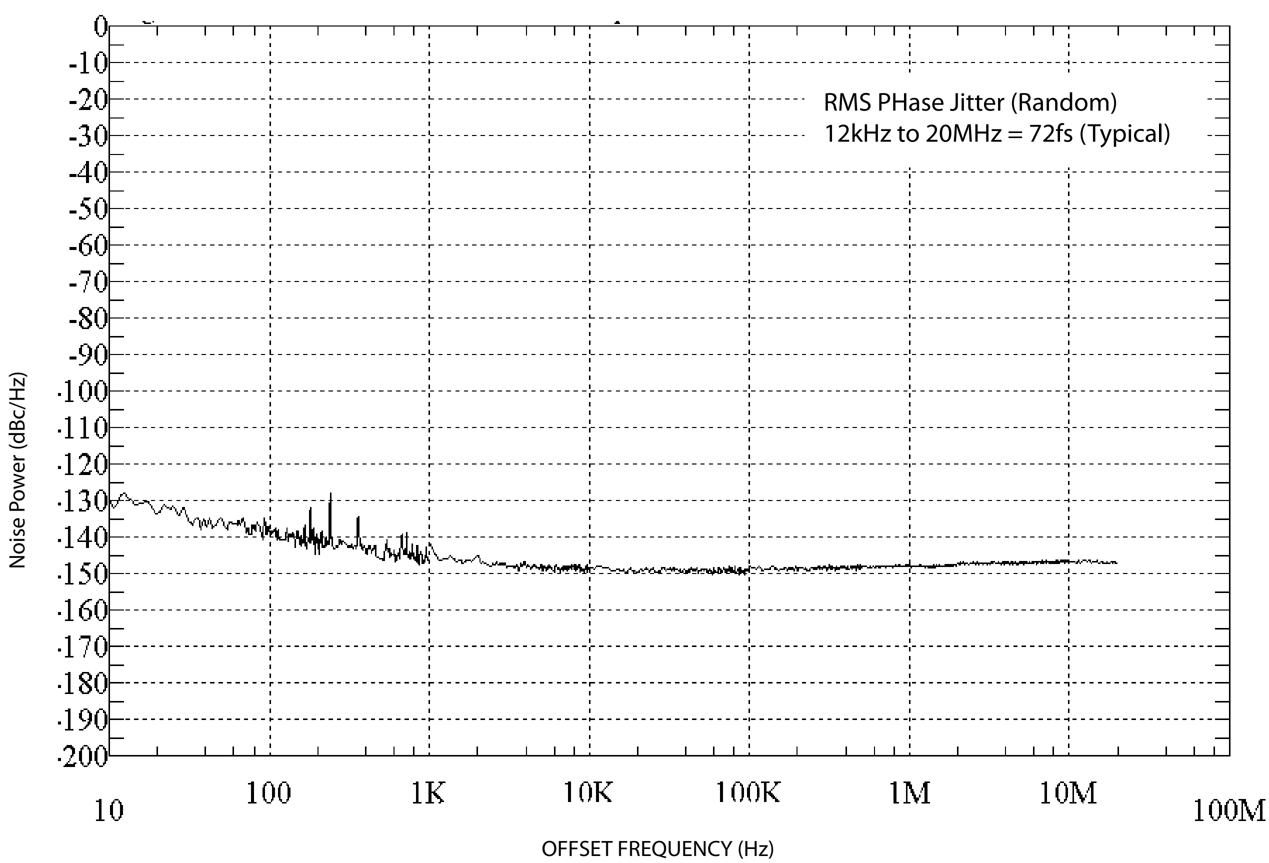
$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $T_A$= –40°C to +85°C, $R_L$ = 50ohms to $V_{CC}$–2V, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Operating Frequency | NRZ data | 4.5 | | | Gbps |
| | | $V_{OUT}$ > 400mV Clock | 3.5 | 5 | | GHz |
| $t_{pd}$ | Differential Propagation Delay (IN-to-Q) | $V_{IN}$ > 100mV | 280 | 390 | 500 | ps |
| | (SEL-to-Q) | | 150 | | 600 | ps |
| $\Delta t_{pd}$ Tempco | Differential Propagation Delay Temperature Coefficient | | | 220 | | fs/°C |
| $t_{SKEW}$ | Output-to-Output Skew | **Note 9** | | | 15 | ps |
| | Part-to-Part Skew | **Note 10** | | | 150 | ps |
| $t_{JITTER}$ | RMS Phase Jitter | Output = 622MHz Integration Range: 12kHz - 20MHz | | 72 | | $fs_{rms}$ |
| $t_r$, $t_f$ | Output Rise/Fall Time | At full output swing, 20% to 80%. | 35 | 65 | 100 | ps |

**Notes:**

8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Output-to-output skew is measured between two different outputs under identical input transitions.
10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

## PHASE NOISE




Phase Noise Plot: 622MHz @ 3.3V

## SINGLE-ENDED AND DIFFERENTIAL SWINGS

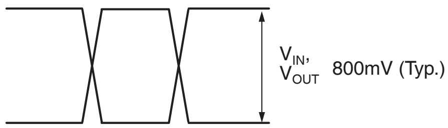



**Figure 1a. Single-Ended Voltage Swing**

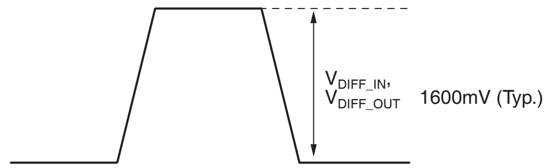
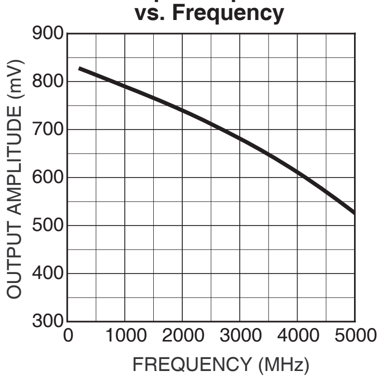



**Figure 1b. Differential Voltage Swing**

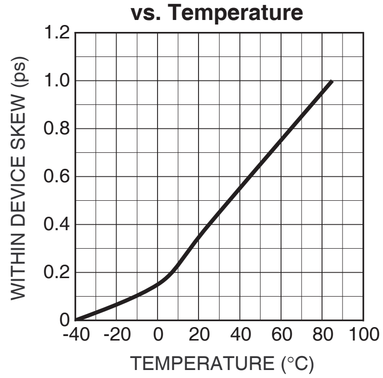
## TYPICAL OPERATING CHARACTERISTICS

$V_{CC}$ = 3.3V, GND = 0, $V_{IN}$ = 100mV, $T_A$ = 25°C, unless otherwise stated.

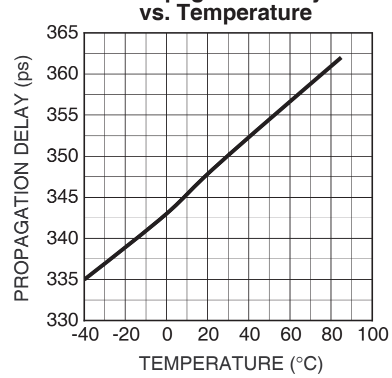
**Output Amplitude vs. Frequency**




**Within Device Skew vs. Temperature**



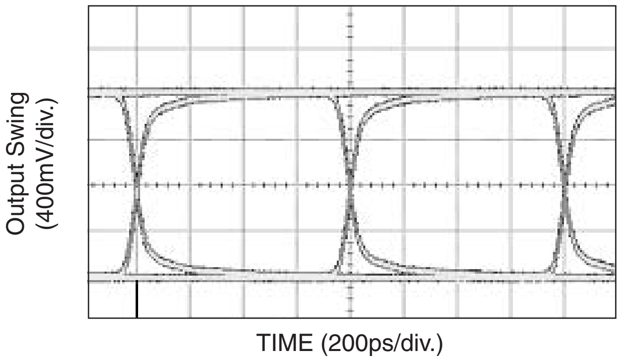

**Propagation Delay vs. Temperature**



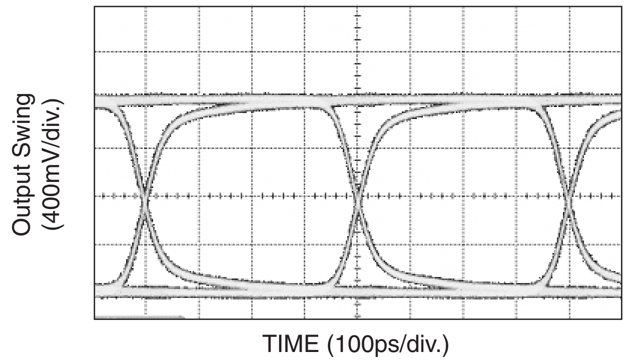
## FUNCTIONAL CHARACTERISTICS

$V_{CC}$ = 3.3V, GND = 0, $V_{IN}$ = 100mV, $T_A$ = 25°C, unless otherwise stated.

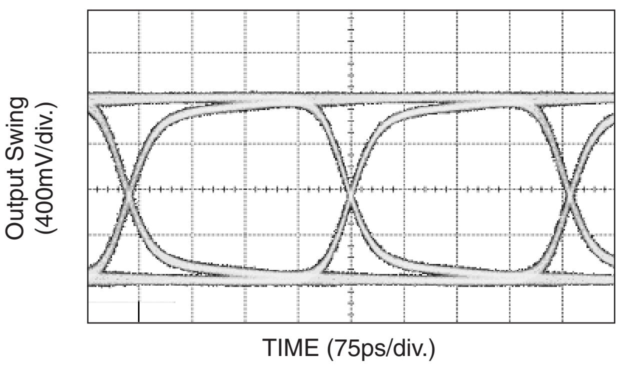
**1.25Gbps Output (Q – /Q)**



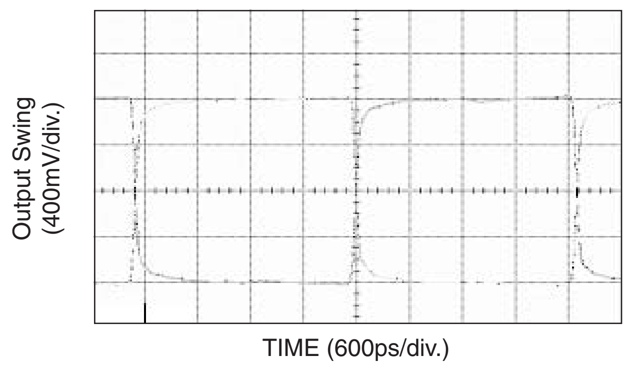

**2.5Gbps Output (Q – /Q)**



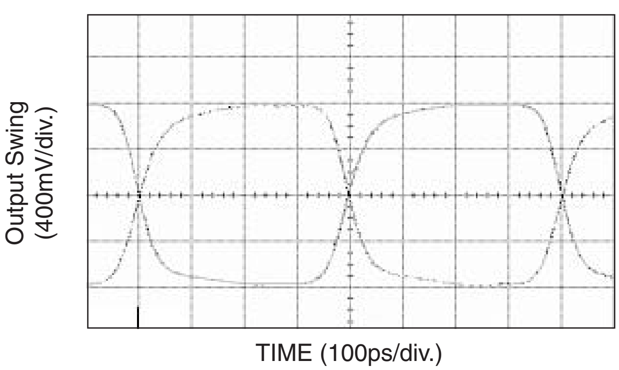

**3.2Gbps Output (Q – /Q)**



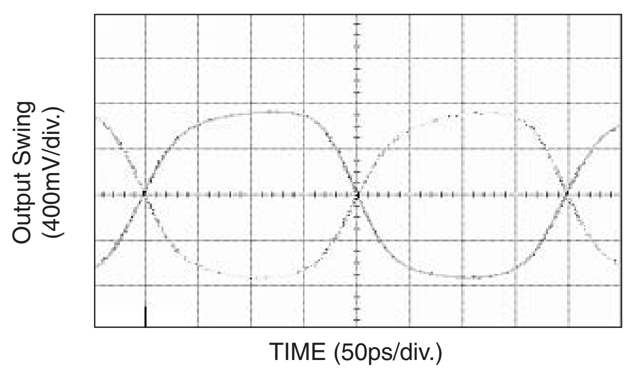

**200MHz Output (Q – /Q)**




**1.25GHz Output (Q – /Q)**



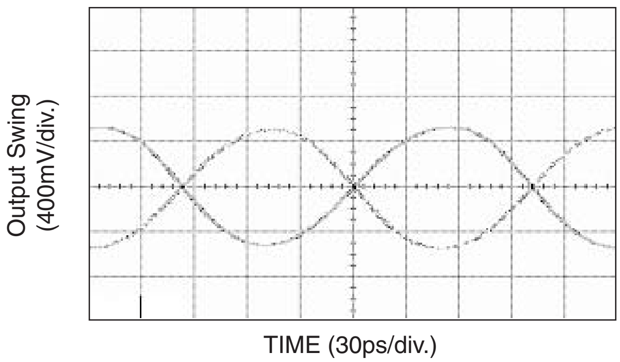

**2.5GHz Output (Q – /Q)**



## FUNCTIONAL CHARACTERISTICS (CONTINUED)

$V_{CC}$ = 3.3V, GND = 0, $V_{IN}$ = 100mV, $T_A$ = 25°C, unless otherwise stated.

**5GHz Output (Q – /Q)**



## INPUT AND OUTPUT STAGES

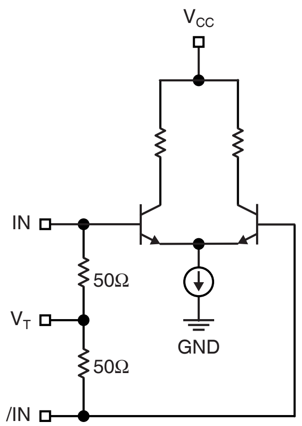



**Figure 2a. Simplified Differential Input Stage**

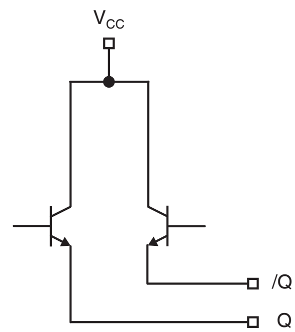
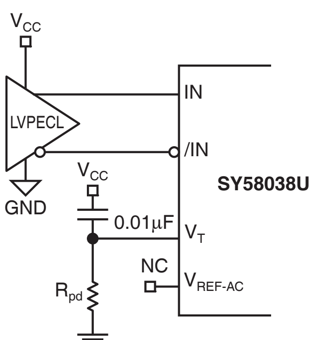


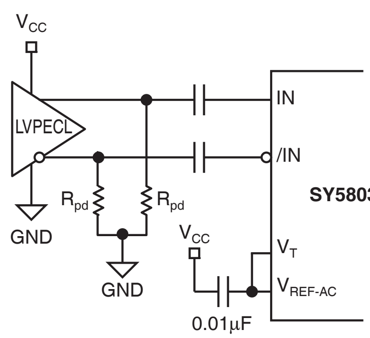

**Figure 2b. Simplified LVPECL Output Stage**

## INPUT INTERFACE APPLICATIONS



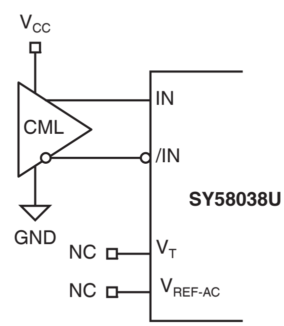

For $V_{CC}$ = 3.3V, $R_{pd}$ = 50Ω.
For $V_{CC}$ = 2.5V, $R_{pd}$ = 19Ω.

**Figure 3a. LVPECL Interface (DC-Coupled)**




For 3.3V, $R_{pd}$ = 100Ω.
For 2.5V, $R_{pd}$ = 50Ω.

**Figure 3b. LVPECL Interface (AC-Coupled)**




*Option: May connect $V_T$ to $V_{CC}$.*

**Figure 3c. CML Interface (DC-Coupled)**

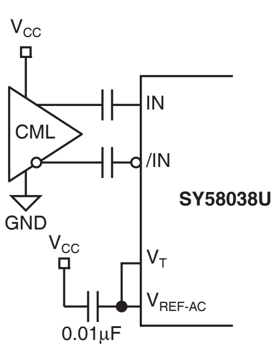



**Figure 3d. CML Interface (AC-Coupled)**

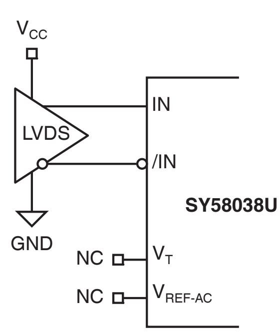



**Figure 3e. LVDS Interface**

## OUTPUT INTERFACE APPLICATIONS

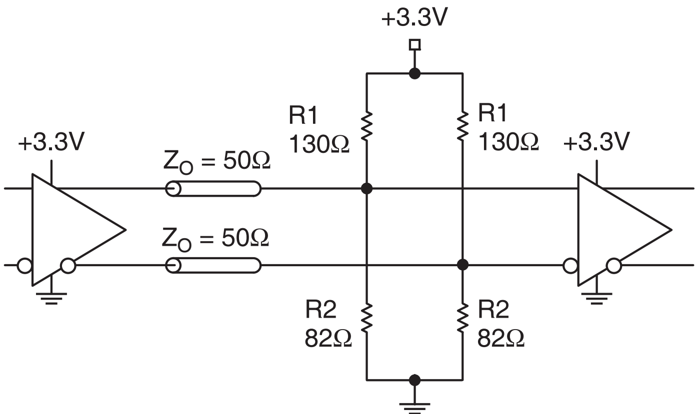



**Figure 4a. Parallel Thevenin-Equivalent Termination**

Note:
For +2.5V system, R1 = 250ý, R2 = 62.5ohms.

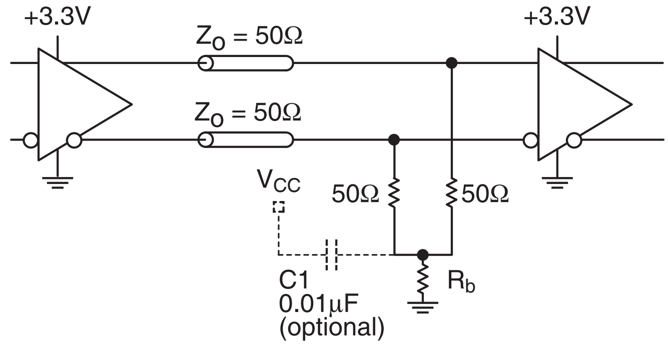


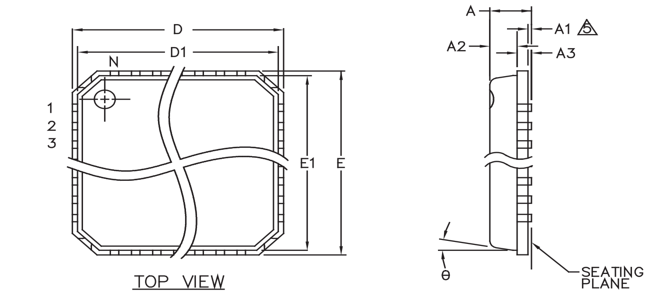

**Figure 4b. Parallel Termination (3-Resistor)**

Note:
For +2.5V system, $R_b$ =19ohms.
For +3.3V system, $R_b$ = 50ohms.

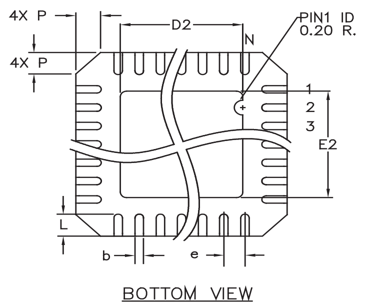
## RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

| Part Number | Function | Data Sheet Link |
|---|---|---|
| SY58037U | Ultra Precision 8:1 MUX with Internal Termination and 1:2 CML Fanout Buffer | http://www.micrel.com/product-info/products/sy58037u.shtml |
| SY58038U | Ultra Precision 8:1 MUX with Internal Termination and 1:2 LVPECL Fanout Buffer | http://www.micrel.com/product-info/products/sy58038u.shtml |
| SY58039U | Ultra Precision 8:1 MUX with Internal Termination and 1:2 400mV LVPECL Fanout Buffer | http://www.micrel.com/product-info/products/sy58039u.shtml |
| | MLF™ Application Note | www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf |
| HBW Solutions | New Products and Applications | www.micrel.com/product-info/products/solutions.shtml |

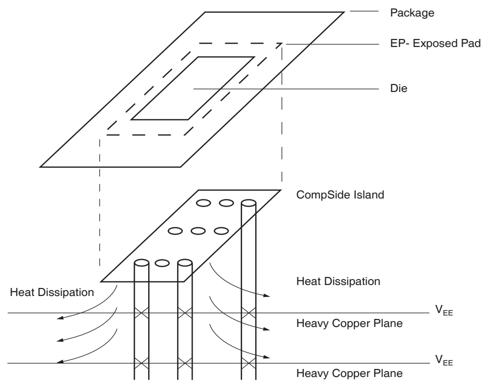
## 44 LEAD *QFN*\ (QFN 44)




| | DIMENSION (mm) | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | – | 0.85 | 0.90 |
| A1 | 0.00 | 0.01 | 0.05 |
| A2 | – | 0.65 | 0.70 |
| A3 | 0.20 REF. | | |
| D | 7.00 BSC | | |
| D1 | 6.75 BSC | | |
| D2 | 3.15 | 3.30 | 3.45 |
| E | 7.00 BSC | | |
| E1 | 6.75 BSC | | |
| E2 | 3.15 | 3.30 | 3.45 |
| θ | | | 12° |
| P | 0.24 | 0.42 | 0.60 |
| e | 0.50 BSC | | |
| N | 44 | | |
| L | 0.50 | 0.60 | 0.75 |
| b | 0.18 | 0.23 | 0.30 |




NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE NUMBER OF TERMINALS.
   THE NUMBER OF TERMINALS PER SIDE IS N/4.
3. THE PIN#1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. PACKAGE WARPAGE MAX 0.05mm.
5. APPLIED FOR EXPOSED PAD AND TERMINALS.




**PCB Thermal Consideration for 44-Pin QFN Package**
**(Always solder, or equivalent, the exposed pad to the PCB)**

**Package Notes:**

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

*Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.*

*С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров*

*Мы предлагаем:*

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

*В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.*

*Конструкторский отдел помогает осуществить:*

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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