

# 64K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

DECEMBER 2012

## FEATURES

- High-speed access time: 35ns, 45ns, 55ns
- CMOS low power operation:
  - 15 mW (typical) operating
  - 1.5  $\mu$ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 1.65V--2.2V  $V_{DD}$  (62WV6416DALL)
  - 2.3V--3.6V  $V_{DD}$  (65WV6416DBLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial and automotive temperature support
- 2CS Option Available
- Lead-free available

## DESCRIPTION

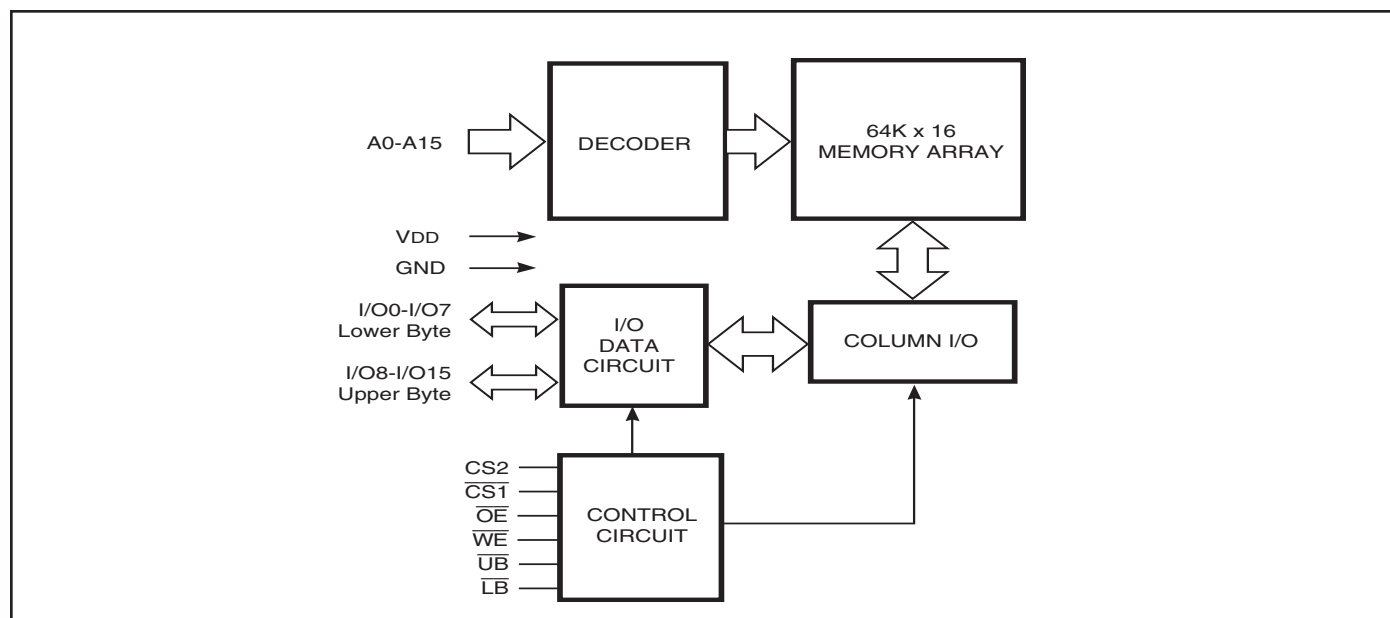
The *ISSI* IS62/65WV6416DALL and IS62/65WV6416DBLL are high-speed, 1M bit static RAMs organized as 64K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When  $\overline{CS1}$  is HIGH (deselected) or when CS2 is LOW (deselected) or when  $\overline{CS1}$  is LOW, CS2 is HIGH and both  $\overline{LB}$  and  $\overline{UB}$  are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory. A data byte allows Upper Byte ( $\overline{UB}$ ) and Lower Byte ( $\overline{LB}$ ) access.

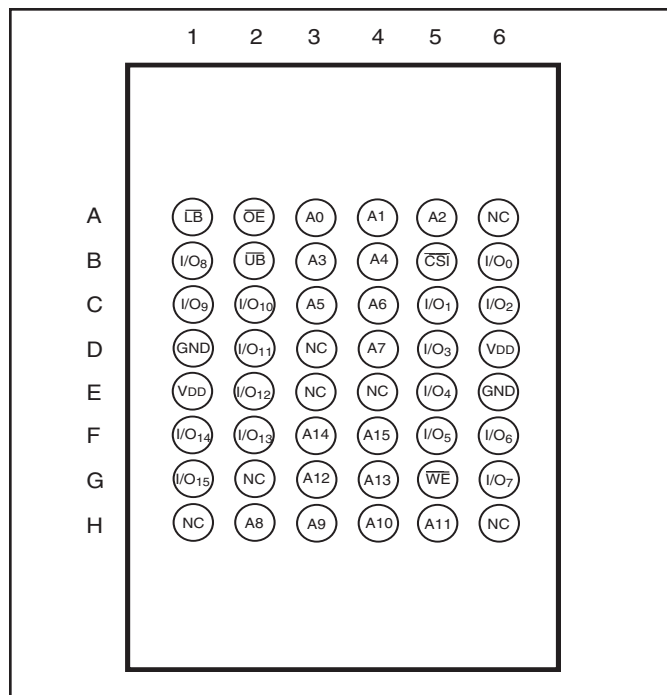
The IS62/65WV6416DALL and IS62/65WV6416DBLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm) and 44-Pin TSOP (TYPE II).

## FUNCTIONAL BLOCK DIAGRAM

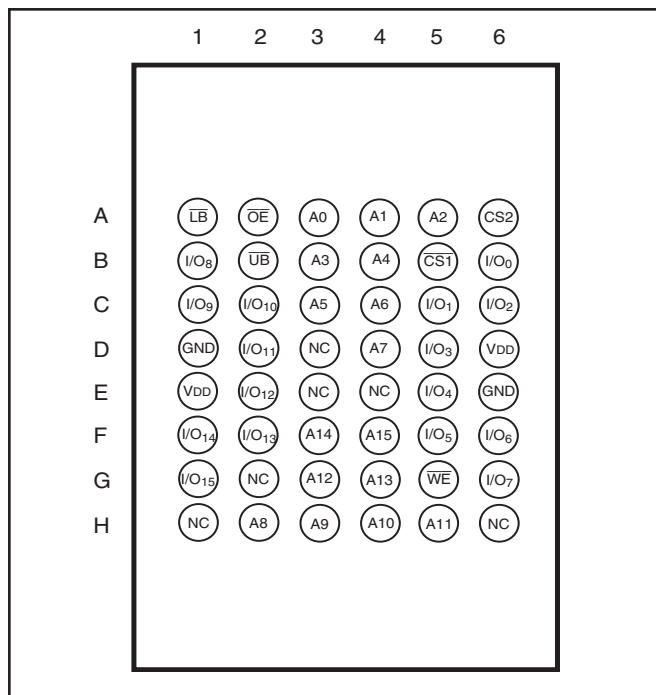


## PIN CONFIGURATIONS

### 48-Pin mini BGA (6mm x 8mm) (Package Code B)



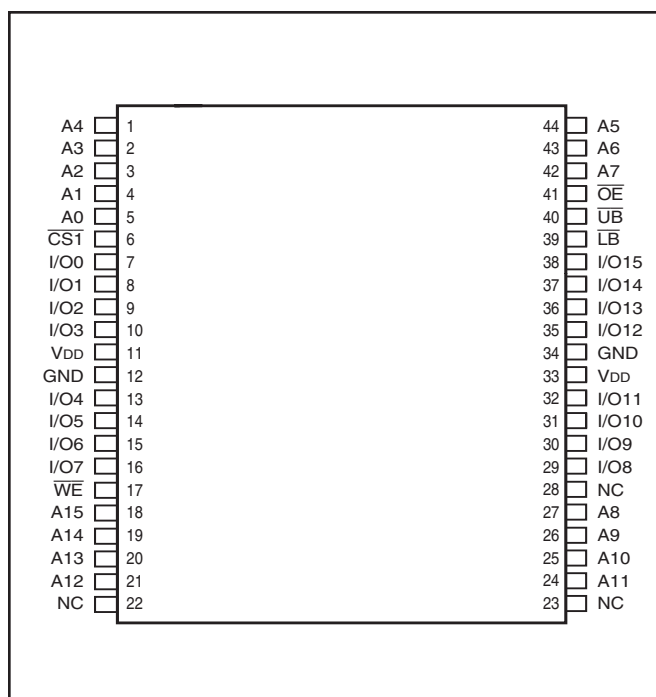
### 48-Pin mini BGA (6mm x 8mm) 2 CS Option (Package Code B2)



## PIN DESCRIPTIONS

|            |                                 |
|------------|---------------------------------|
| A0-A15     | Address Inputs                  |
| I/O0-I/O15 | Data Inputs/Outputs             |
| CS1, CS2   | Chip Enable Input               |
| OE         | Output Enable Input             |
| WE         | Write Enable Input              |
| LB         | Lower-byte Control (I/O0-I/O7)  |
| UB         | Upper-byte Control (I/O8-I/O15) |
| NC         | No Connection                   |
| VDD        | Power                           |
| GND        | Ground                          |

### 44-Pin mini TSOP (Type II) (Package Code T)



## TRUTH TABLE

| Mode            | WE | CS1 | CS2 | OE | LB | UB | I/O PIN   |            | V <sub>DD</sub> Current             |
|-----------------|----|-----|-----|----|----|----|-----------|------------|-------------------------------------|
|                 |    |     |     |    |    |    | I/O0-I/O7 | I/O8-I/O15 |                                     |
| Not Selected    | X  | H   | X   | X  | X  | X  | High-Z    | High-Z     | I <sub>SB1</sub> , I <sub>SB2</sub> |
|                 | X  | X   | L   | X  | X  | X  | High-Z    | High-Z     | I <sub>SB1</sub> , I <sub>SB2</sub> |
|                 | X  | X   | X   | X  | H  | H  | High-Z    | High-Z     | I <sub>SB1</sub> , I <sub>SB2</sub> |
| Output Disabled | H  | L   | H   | H  | L  | X  | High-Z    | High-Z     | I <sub>CC</sub>                     |
|                 | H  | L   | H   | H  | X  | L  | High-Z    | High-Z     | I <sub>CC</sub>                     |
| Read            | H  | L   | H   | L  | L  | H  | DOUT      | High-Z     | I <sub>CC</sub>                     |
|                 | H  | L   | H   | L  | H  | L  | High-Z    | DOUT       |                                     |
|                 | H  | L   | H   | L  | L  | L  | DOUT      | DOUT       |                                     |
| Write           | L  | L   | H   | X  | L  | H  | DIN       | High-Z     | I <sub>CC</sub>                     |
|                 | L  | L   | H   | X  | H  | L  | High-Z    | DIN        |                                     |
|                 | L  | L   | H   | X  | L  | L  | DIN       | DIN        |                                     |

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol            | Parameter                            | Value                         | Unit |
|-------------------|--------------------------------------|-------------------------------|------|
| V <sub>TERM</sub> | Terminal Voltage with Respect to GND | −0.5 to V <sub>DD</sub> + 0.5 | V    |
| V <sub>DD</sub>   | V <sub>DD</sub> Relates to GND       | −0.3 to 4.0                   | V    |
| T <sub>STG</sub>  | Storage Temperature                  | −65 to +150                   | °C   |
| P <sub>T</sub>    | Power Dissipation                    | 1.0                           | W    |

### Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE<sup>(1,2)</sup>

| Symbol           | Parameter                | Conditions            | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 6    | pF   |
| C <sub>I/O</sub> | Input/Output Capacitance | V <sub>OUT</sub> = 0V | 8    | pF   |

### Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 3.3V.

## AC TEST CONDITIONS

| Parameter                                                          | Unit<br>(2.3V-3.6V)            | Unit<br>(3.3V ± 5%)            | Unit<br>(1.65V-2.2V)           |
|--------------------------------------------------------------------|--------------------------------|--------------------------------|--------------------------------|
| Input Pulse Level                                                  | 0.4V to V <sub>DD</sub> - 0.3V | 0.4V to V <sub>DD</sub> - 0.3V | 0.4V to V <sub>DD</sub> - 0.3V |
| Input Rise and Fall Times                                          | 1V/ ns                         | 1V/ ns                         | 1V/ ns                         |
| Input and Output Timing<br>and Reference Level (V <sub>Ref</sub> ) | V <sub>DD</sub> /2             | $\frac{V_{DD}}{2} + 0.05$      | 0.9V                           |
| Output Load                                                        | See Figures 1 and 2            | See Figures 1 and 2            | See Figures 1 and 2            |
| R1 ( $\Omega$ )                                                    | 317                            | 317                            | 13500                          |
| R2 ( $\Omega$ )                                                    | 351                            | 351                            | 10800                          |
| V <sub>TM</sub> (V)                                                | 3.3V                           | 3.3V                           | 1.8V                           |

## AC TEST LOADS

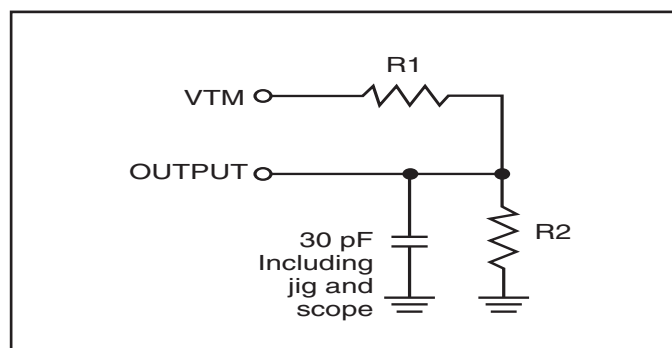


Figure 1.

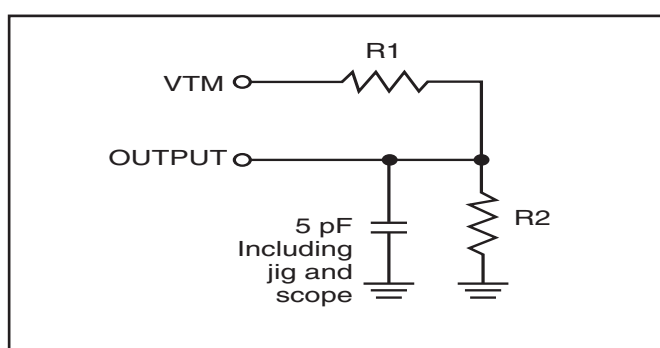


Figure 2.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

**V<sub>DD</sub> = 3.3V ± 5%**

| Symbol          | Parameter                        | Test Conditions                                             | Min. | Max.                  | Unit |
|-----------------|----------------------------------|-------------------------------------------------------------|------|-----------------------|------|
| V <sub>OH</sub> | Output HIGH Voltage              | V <sub>DD</sub> = Min., I <sub>OH</sub> = -1 mA             | 2.4  | —                     | V    |
| V <sub>OL</sub> | Output LOW Voltage               | V <sub>DD</sub> = Min., I <sub>OL</sub> = 2.1 mA            | —    | 0.4                   | V    |
| V <sub>IH</sub> | Input HIGH Voltage               |                                                             | 2    | V <sub>DD</sub> + 0.3 | V    |
| V <sub>IL</sub> | Input LOW Voltage <sup>(1)</sup> |                                                             | -0.3 | 0.8                   | V    |
| I <sub>LI</sub> | Input Leakage                    | GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>                     | -1   | 1                     | μA   |
| I <sub>LO</sub> | Output Leakage                   | GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled | -1   | 1                     | μA   |

**Note:**

- V<sub>IL</sub> (min.) = -0.3V DC; V<sub>IL</sub> (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.  
V<sub>IH</sub> (max.) = V<sub>DD</sub> + 0.3V DC; V<sub>IH</sub> (max.) = V<sub>DD</sub> + 2.0V AC (pulse width < 10 ns). Not 100% tested.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

**V<sub>DD</sub> = 2.3V-3.6V**

| Symbol          | Parameter                        | Test Conditions                                             | Min. | Max.                  | Unit |
|-----------------|----------------------------------|-------------------------------------------------------------|------|-----------------------|------|
| V <sub>OH</sub> | Output HIGH Voltage              | V <sub>DD</sub> = Min., I <sub>OH</sub> = -1.0 mA           | 1.8  | —                     | V    |
| V <sub>OL</sub> | Output LOW Voltage               | V <sub>DD</sub> = Min., I <sub>OL</sub> = 2.1 mA            | —    | 0.4                   | V    |
| V <sub>IH</sub> | Input HIGH Voltage               |                                                             | 2.0  | V <sub>DD</sub> + 0.3 | V    |
| V <sub>IL</sub> | Input LOW Voltage <sup>(1)</sup> |                                                             | -0.3 | 0.8                   | V    |
| I <sub>LI</sub> | Input Leakage                    | GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>                     | -1   | 1                     | μA   |
| I <sub>LO</sub> | Output Leakage                   | GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled | -1   | 1                     | μA   |

**Note:**

- V<sub>IL</sub> (min.) = -0.3V DC; V<sub>IL</sub> (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.  
V<sub>IH</sub> (max.) = V<sub>DD</sub> + 0.3V DC; V<sub>IH</sub> (max.) = V<sub>DD</sub> + 2.0V AC (pulse width < 10 ns). Not 100% tested.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

**V<sub>DD</sub> = 1.65V-2.2V**

| Symbol                         | Parameter           | Test Conditions                                             | V <sub>DD</sub> | Min. | Max.                  | Unit |
|--------------------------------|---------------------|-------------------------------------------------------------|-----------------|------|-----------------------|------|
| V <sub>OH</sub>                | Output HIGH Voltage | I <sub>OH</sub> = -0.1 mA                                   | 1.65-2.2V       | 1.4  | —                     | V    |
| V <sub>OL</sub>                | Output LOW Voltage  | I <sub>OL</sub> = 0.1 mA                                    | 1.65-2.2V       | —    | 0.2                   | V    |
| V <sub>IH</sub>                | Input HIGH Voltage  |                                                             | 1.65-2.2V       | 1.4  | V <sub>DD</sub> + 0.2 | V    |
| V <sub>IL</sub> <sup>(1)</sup> | Input LOW Voltage   |                                                             | 1.65-2.2V       | -0.2 | 0.4                   | V    |
| I <sub>LI</sub>                | Input Leakage       | GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>                     |                 | -1   | 1                     | μA   |
| I <sub>LO</sub>                | Output Leakage      | GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled |                 | -1   | 1                     | μA   |

**Note:**

- V<sub>IL</sub> (min.) = -0.3V DC; V<sub>IL</sub> (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.  
V<sub>IH</sub> (max.) = V<sub>DD</sub> + 0.3V DC; V<sub>IH</sub> (max.) = V<sub>DD</sub> + 2.0V AC (pulse width < 10 ns). Not 100% tested.

## OPERATING RANGE (V<sub>DD</sub>)

| Range      | Ambient Temperature | V <sub>DD</sub> | Speed |
|------------|---------------------|-----------------|-------|
| Commercial | 0°C to +70°C        | 1.65V-2.2V      | 45ns  |
| Industrial | -40°C to +85°C      | 1.65V-2.2V      | 55ns  |
| Automotive | -40°C to +125°C     | 1.65V-2.2V      | 55ns  |

## OPERATING RANGE (V<sub>DD</sub>)

| Range      | Ambient Temperature | V <sub>DD</sub> (45 ns) | V <sub>DD</sub> (35 ns) |
|------------|---------------------|-------------------------|-------------------------|
| Commercial | 0°C to +70°C        | 2.3V-3.6V               | 3.3V±5%                 |
| Industrial | -40°C to +85°C      | 2.3V-3.6V               | 3.3V±5%                 |

## OPERATING RANGE (V<sub>DD</sub>)

| Range      | Ambient Temperature | V <sub>DD</sub> (45 ns) |
|------------|---------------------|-------------------------|
| Automotive | -40°C to +125°C     | 2.3V-3.6V               |

## POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

| Symbol           | Parameter                                        | Test Conditions                                                                                                                                           |                     | -35  |      | -45  |      | -55  |      | Unit |
|------------------|--------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------|------|------|------|------|------|------|
|                  |                                                  |                                                                                                                                                           |                     | Min. | Max. | Min. | Max. | Min. | Max. |      |
| I <sub>CC</sub>  | V <sub>DD</sub> Dynamic Operating Supply Current | V <sub>DD</sub> = Max.,                                                                                                                                   | Com.                | —    | 8    | —    | 6    | —    | 5    | mA   |
|                  |                                                  | I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>                                                                                                             | Ind.                | —    | 12   | —    | 8    | —    | 7    |      |
|                  |                                                  | $\overline{CE} = V_{IL}$                                                                                                                                  | Auto.               | —    | 15   | —    | 12   | —    | 12   |      |
|                  |                                                  | V <sub>IN</sub> ≥ V <sub>DD</sub> – 0.3V, or V <sub>IN</sub> ≤ 0.4V                                                                                       | typ. <sup>(2)</sup> | 5    |      |      |      |      |      |      |
| I <sub>CC1</sub> | Operating Supply Current                         | V <sub>DD</sub> = Max.,                                                                                                                                   | Com.                | —    | 2.5  | —    | 2.5  | —    | 2.5  | mA   |
|                  |                                                  | I <sub>OUT</sub> = 0 mA, f = 0                                                                                                                            | Ind.                | —    | 2.5  | —    | 2.5  | —    | 2.5  |      |
|                  |                                                  | $\overline{CE} = V_{IL}$                                                                                                                                  | Auto.               | —    | 5    | —    | 5    | —    | 5    |      |
|                  |                                                  | V <sub>IN</sub> ≥ V <sub>DD</sub> – 0.3V, or V <sub>IN</sub> ≤ 0.4V                                                                                       |                     |      |      |      |      |      |      |      |
| I <sub>SB2</sub> | CMOS Standby Current (CMOS Inputs)               | V <sub>DD</sub> = Max.,                                                                                                                                   | Com.                | —    | 2    | —    | 2    | —    | 2    | μA   |
|                  |                                                  | $\overline{CS1} \geq V_{DD} - 0.2V$ ,                                                                                                                     | Ind.                | —    | 4    | —    | 4    | —    | 4    |      |
|                  |                                                  | CS2 ≤ 0.2V,                                                                                                                                               | Auto                | —    | 18   | —    | 18   | —    | 18   |      |
|                  |                                                  | V <sub>IN</sub> ≥ V <sub>DD</sub> – 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0                                                                                | typ. <sup>(2)</sup> | 0.6  |      |      |      |      |      |      |
| OR               |                                                  |                                                                                                                                                           |                     |      |      |      |      |      |      |      |
|                  | ULB Control                                      | V <sub>DD</sub> = Max., $\overline{CS1} = V_{IL}$ , CS2=V <sub>IH</sub><br>V <sub>IN</sub> ≤ 0.2V, f = 0; $\overline{UB} / \overline{LB} = V_{DD} - 0.2V$ |                     |      |      |      |      |      |      |      |

### Note:

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

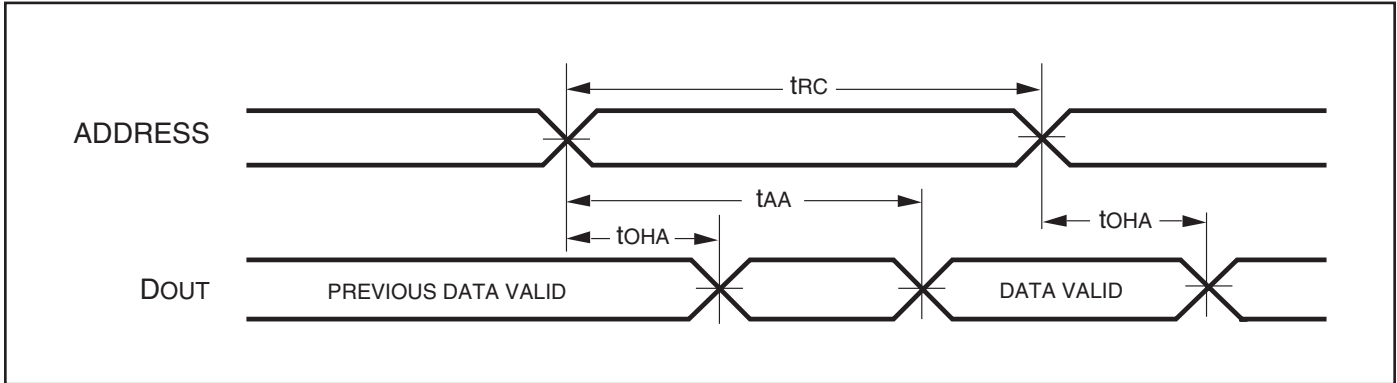
| Symbol                                                | Parameter                | 35 ns |      | 45 ns |      | 55 ns |      | Unit |
|-------------------------------------------------------|--------------------------|-------|------|-------|------|-------|------|------|
|                                                       |                          | Min.  | Max. | Min.  | Max. | Min.  | Max. |      |
| t <sub>RC</sub>                                       | Read Cycle Time          | 35    | —    | 45    | —    | 55    | —    | ns   |
| t <sub>AA</sub>                                       | Address Access Time      | —     | 35   | —     | 45   | —     | 55   | ns   |
| t <sub>OH</sub> A                                     | Output Hold Time         | 10    | —    | 10    | —    | 10    | —    | ns   |
| t <sub>ACS1</sub> /t <sub>ACS2</sub>                  | CS1/CS2 Access Time      | —     | 35   | —     | 45   | —     | 55   | ns   |
| t <sub>DOE</sub>                                      | OE Access Time           | —     | 10   | —     | 20   | —     | 25   | ns   |
| t <sub>HZOE</sub> <sup>(2)</sup>                      | OE to High-Z Output      | 0     | 10   | 0     | 15   | 0     | 20   | ns   |
| t <sub>LZOE</sub> <sup>(2)</sup>                      | OE to Low-Z Output       | 3     | —    | 5     | —    | 5     | —    | ns   |
| t <sub>HZCS1</sub> /t <sub>HZCS2</sub> <sup>(2)</sup> | CS1/CS2 to High-Z Output | 0     | 10   | 0     | 15   | 0     | 20   | ns   |
| t <sub>LZCS1</sub> /t <sub>LZCS2</sub> <sup>(2)</sup> | CS1/CS2 to Low-Z Output  | 5     | —    | 5     | —    | 10    | —    | ns   |
| t <sub>BA</sub>                                       | LB, UB Access Time       | —     | 35   | —     | 45   | —     | 55   | ns   |
| t <sub>HZB</sub>                                      | LB, UB to High-Z Output  | 0     | 15   | 0     | 15   | 0     | 20   | ns   |
| t <sub>LZB</sub>                                      | LB, UB to Low-Z Output   | 0     | —    | 0     | —    | 0     | —    | ns   |

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V<sub>DD</sub>-0.2V/V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

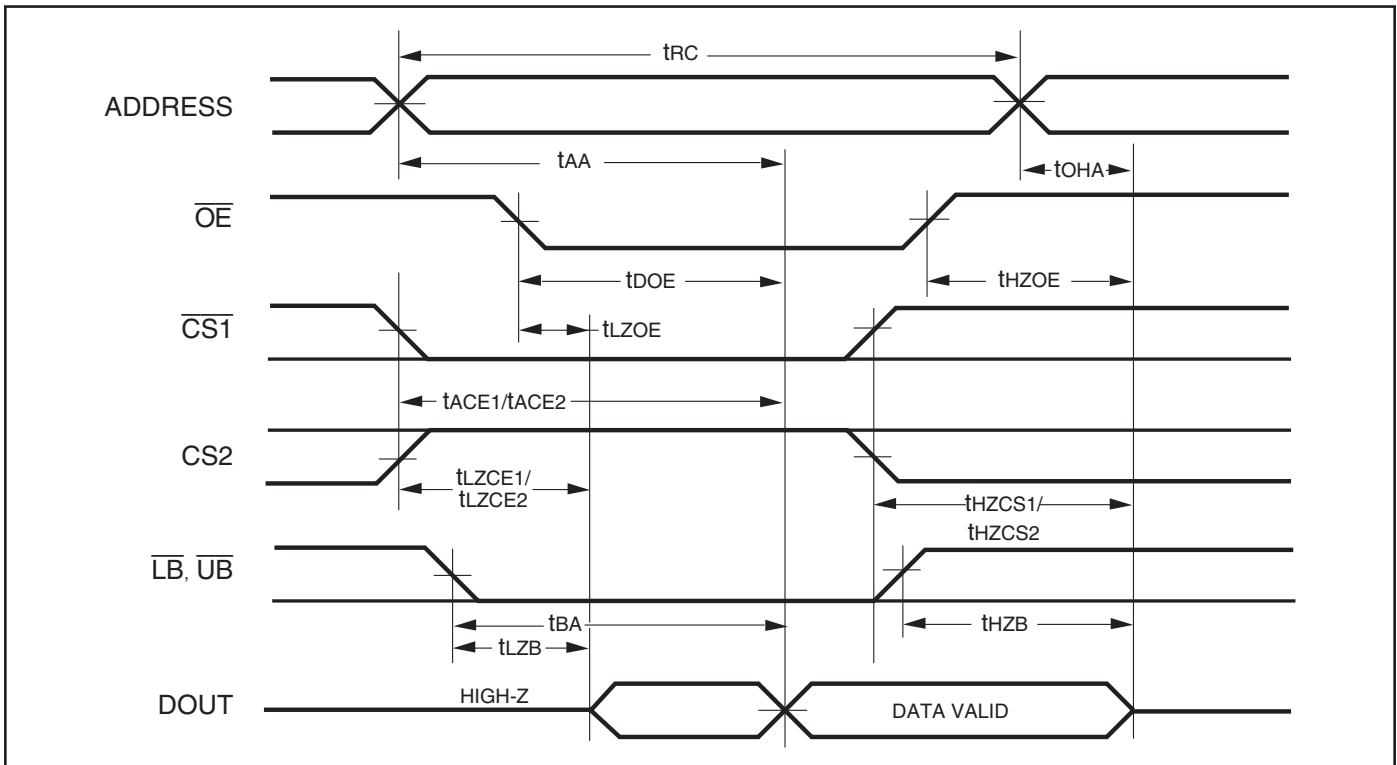
## AC WAVEFORMS

**READ CYCLE NO. 1<sup>(1,2)</sup>** (Address Controlled) ( $\overline{CS1} = \overline{OE} = V_{IL}$ ,  $CS2 = \overline{WE} = V_{IH}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ )



## AC WAVEFORMS

**READ CYCLE NO. 2<sup>(1,3)</sup>** ( $\overline{CS1}$ ,  $CS2$ ,  $\overline{OE}$ , AND  $\overline{UB}/\overline{LB}$  Controlled)



### Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CS1}$ ,  $\overline{UB}$ , or  $\overline{LB} = V_{IL}$ .  $CS2 = \overline{WE} = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CS1}$  LOW transition.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup>** (Over Operating Range)

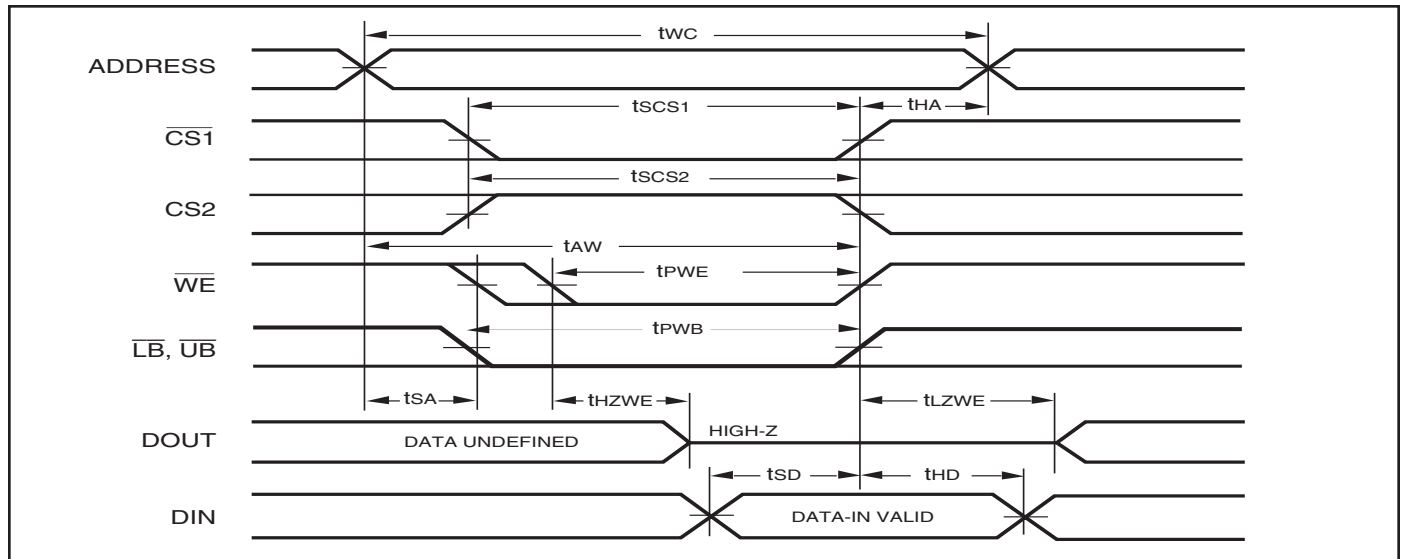
| Symbol                           | Parameter                       | 35 ns |      | 45 ns |      | 55 ns |      | Unit |
|----------------------------------|---------------------------------|-------|------|-------|------|-------|------|------|
|                                  |                                 | Min.  | Max. | Min.  | Max. | Min.  | Max. |      |
| t <sub>WC</sub>                  | Write Cycle Time                | 45    | —    | 45    | —    | 55    | —    | ns   |
| t <sub>SCS1/tSCS2</sub>          | CS1/CS2 to Write End            | 35    | —    | 35    | —    | 45    | —    | ns   |
| t <sub>AW</sub>                  | Address Setup Time to Write End | 35    | —    | 35    | —    | 45    | —    | ns   |
| t <sub>HA</sub>                  | Address Hold from Write End     | 0     | —    | 0     | —    | 0     | —    | ns   |
| t <sub>SA</sub>                  | Address Setup Time              | 0     | —    | 0     | —    | 0     | —    | ns   |
| t <sub>PWB</sub>                 | LB, UB Valid to End of Write    | 35    | —    | 35    | —    | 45    | —    | ns   |
| t <sub>PWE</sub>                 | WE Pulse Width                  | 35    | —    | 35    | —    | 40    | —    | ns   |
| t <sub>SD</sub>                  | Data Setup to Write End         | 20    | —    | 20    | —    | 25    | —    | ns   |
| t <sub>HD</sub>                  | Data Hold from Write End        | 0     | —    | 0     | —    | 0     | —    | ns   |
| t <sub>HZWE</sub> <sup>(3)</sup> | WE LOW to High-Z Output         | —     | 20   | —     | 20   | —     | 20   | ns   |
| t <sub>LZWE</sub> <sup>(3)</sup> | WE HIGH to Low-Z Output         | 5     | —    | 5     | —    | 5     | —    | ns   |

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4V to V<sub>DD</sub>-0.2V/V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of CS1 LOW, CS2 HIGH and UB or LB, and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

**AC WAVEFORMS**

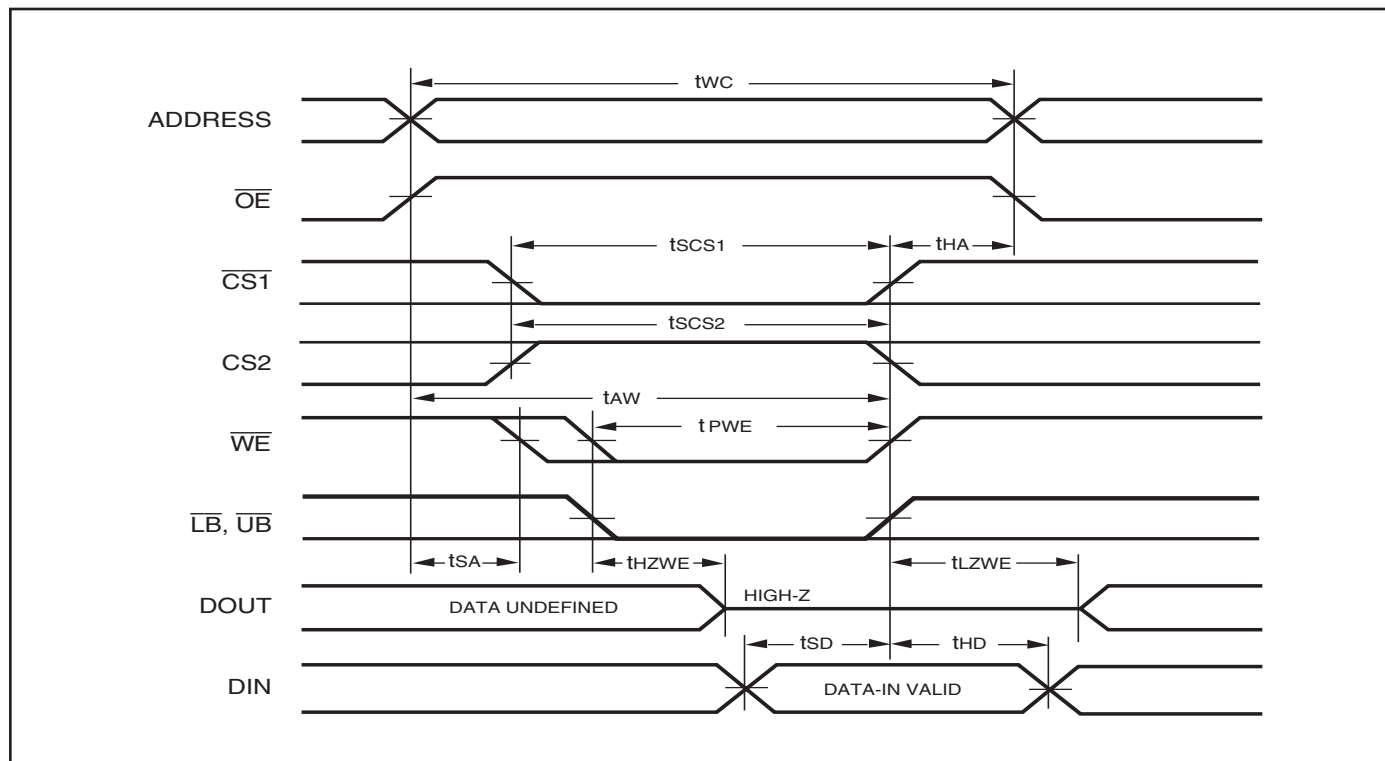
**WRITE CYCLE NO. 1<sup>(1,2)</sup>** ( $\overline{\text{CS1}}$  Controlled,  $\overline{\text{OE}}$  = HIGH or LOW)



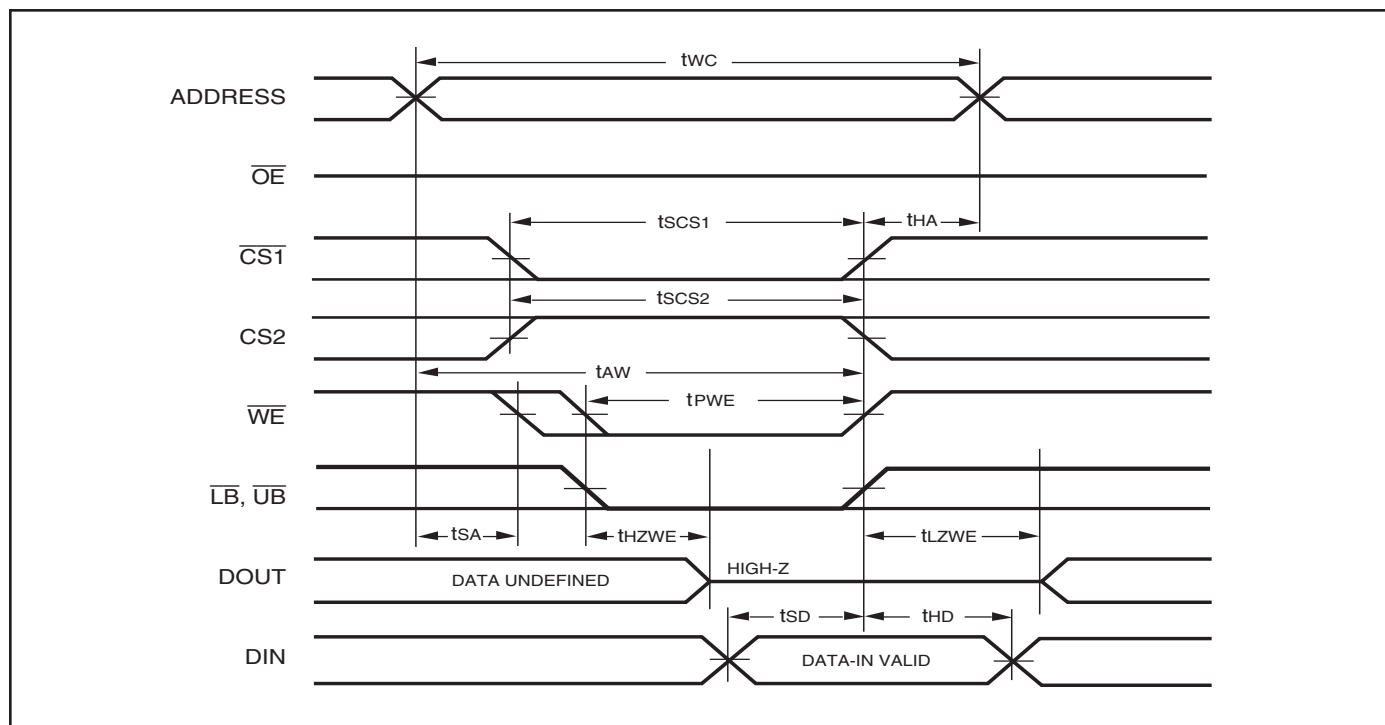
**Notes:**

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the  $\overline{\text{CS1}}$ , CS2 and  $\overline{\text{WE}}$  inputs and at least one of the LB and UB inputs being in the LOW state.
2.  $\text{WRITE} = (\overline{\text{CS1}}) [(\text{LB}) = (\text{UB})] (\overline{\text{WE}})$ .

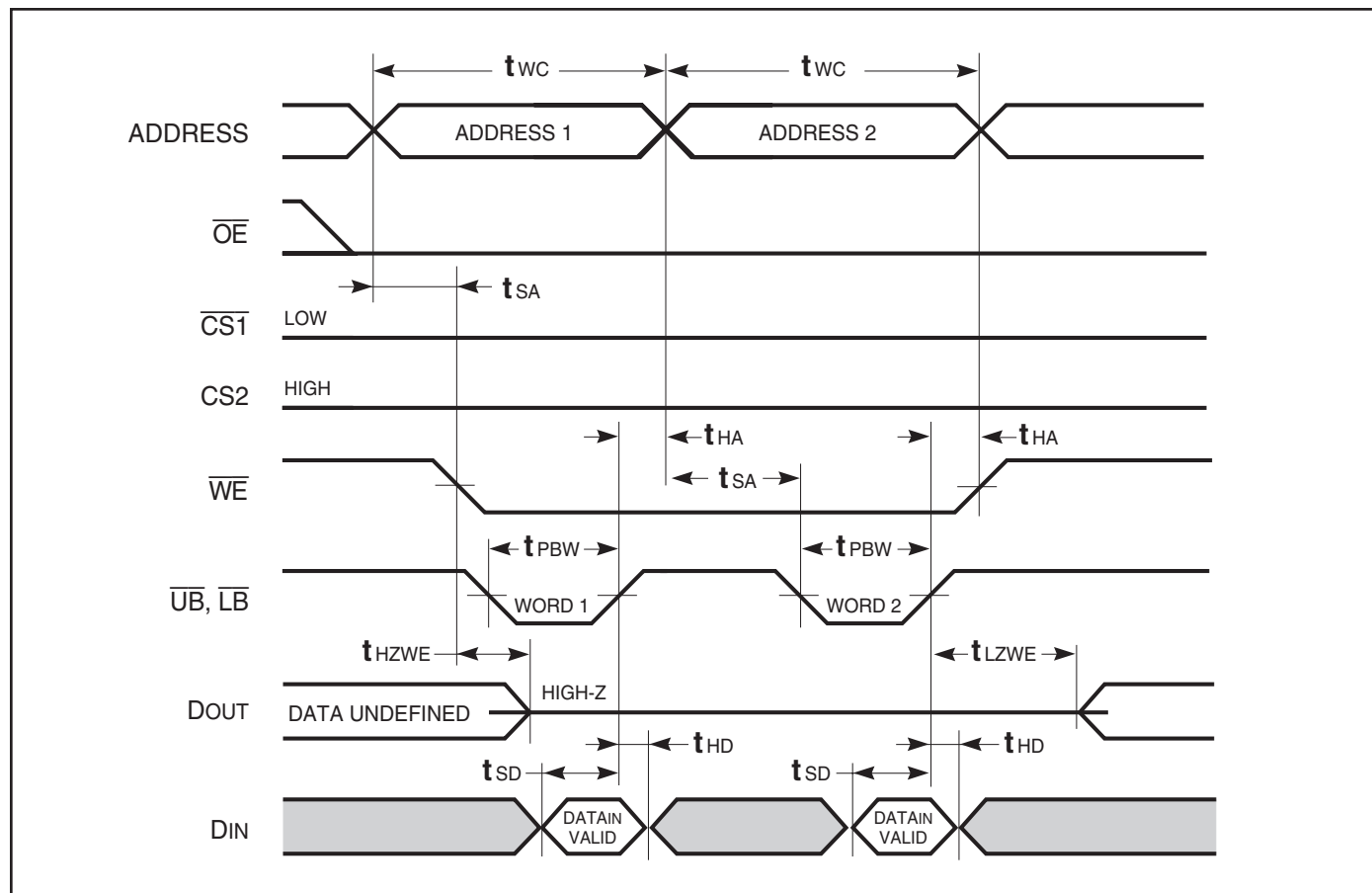
**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)



**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)



WRITE CYCLE NO. 4 ( $\overline{UB}/\overline{LB}$  Controlled)

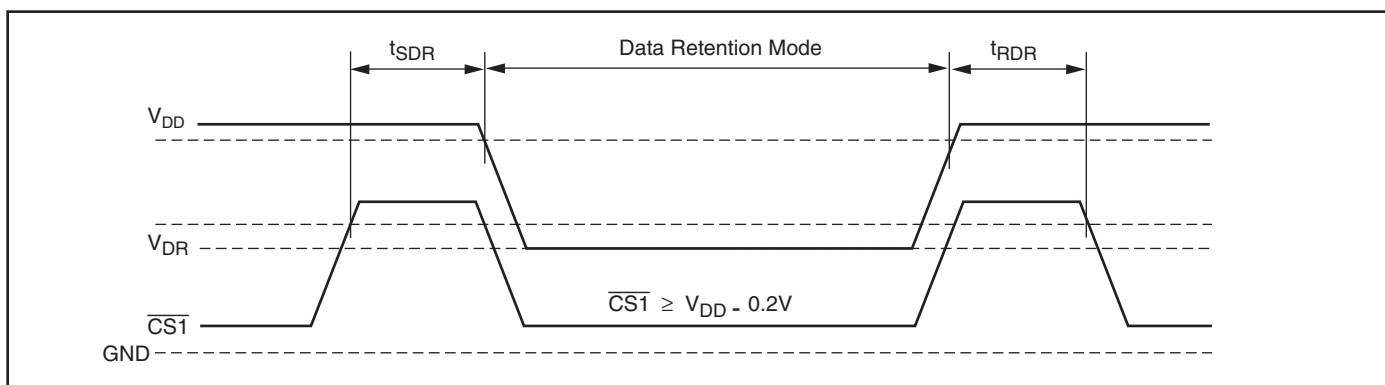


## DATA RETENTION SWITCHING CHARACTERISTICS

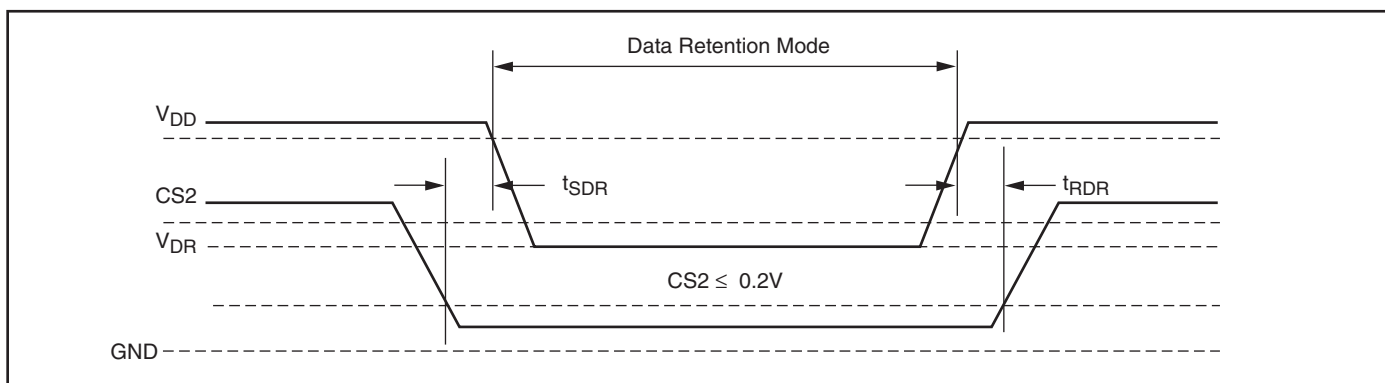
| Symbol           | Parameter                          | Test Condition                                       | Min.            | typ. <sup>(1)</sup> | Max.         | Unit |
|------------------|------------------------------------|------------------------------------------------------|-----------------|---------------------|--------------|------|
| V <sub>DR</sub>  | V <sub>DD</sub> for Data Retention | See Data Retention Waveform                          | 1.2             |                     | 3.6          | V    |
| I <sub>DR</sub>  | Data Retention Current             | V <sub>DD</sub> = 1.2V, CS1 ≥ V <sub>DD</sub> - 0.2V | —               | 0.4                 | 2<br>4<br>18 | μA   |
| t <sub>SDR</sub> | Data Retention Setup Time          | See Data Retention Waveform                          | 0               |                     | —            | ns   |
| t <sub>RDR</sub> | Recovery Time                      | See Data Retention Waveform                          | t <sub>RC</sub> |                     | —            | ns   |

Note: 1. Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

### DATA RETENTION WAVEFORM (CS1 Controlled)



### DATA RETENTION WAVEFORM (CS2 Controlled)



## ORDERING INFORMATION

### IS62WV6416DALL (1.65V - 2.2V)

**Industrial Range: -40°C to +85°C**

| Speed (ns) | Order Part No.       | Package                         |
|------------|----------------------|---------------------------------|
| 55         | IS62WV6416DALL-55BLI | mini BGA (6mm x 8mm), Lead-free |
|            | IS62WV6416DALL-55TLI | TSOP TYPE II, Lead-free         |

### IS62WV6416DBLL (2.3V-3.6V)

**Industrial Range: -40°C to +85°C**

| Speed (ns)           | Order Part No.        | Package                              |
|----------------------|-----------------------|--------------------------------------|
| 45 (35) <sup>1</sup> | IS62WV6416DBLL-45TI   | TSOP TYPE II                         |
|                      | IS62WV6416DBLL-45TLI  | TSOP TYPE II, Lead-free              |
|                      | IS62WV6416DBLL-45BI   | mini BGA (6mm x 8mm)                 |
|                      | IS62WV6416DBLL-45BLI  | mini BGA (6mm x 8mm), Lead-free      |
|                      | IS62WV6416DBLL-45B2LI | mini BGA (6mm x 8mm), 2CS, Lead-free |

Note:

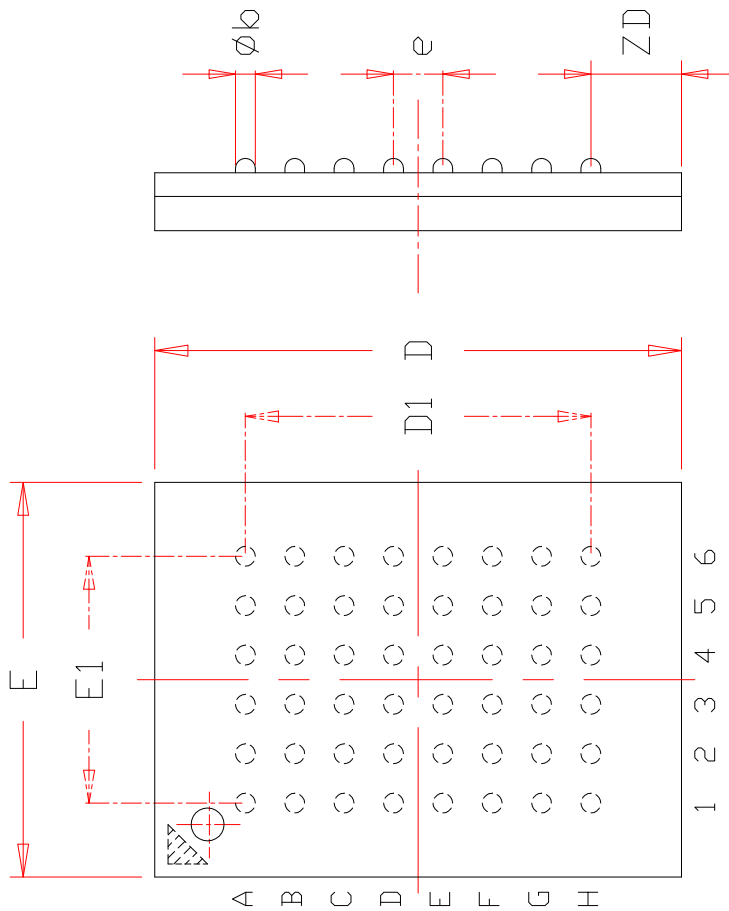
1. Speed = 35ns for  $V_{DD} = 3.3V \pm 5\%$ . Speed = 45ns for  $V_{DD} = 2.3V-3.6V$

### IS65WV6416DBLL (2.3V-3.6V)

**Automotive Range: -40°C to +125°C**

| Speed (ns) | Order Part No.         | Package                                    |
|------------|------------------------|--------------------------------------------|
| 45         | IS65WV6416DBLL-45CTLA3 | TSOP TYPE II, Lead-free, Copper Lead-frame |
|            | IS65WV6416DBLL-45BLA3  | mini BGA (6mm x 8mm), Lead-free            |

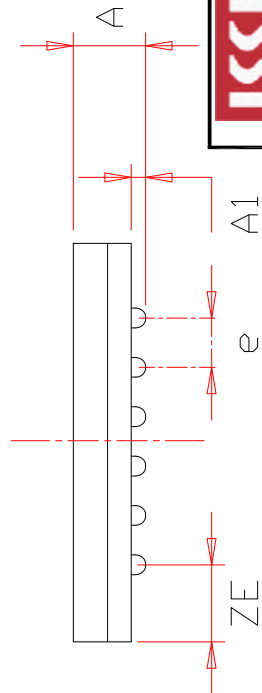
TOP VIEW



| SYMBOL   | DIMENSION IN MM |      |      | DIMENSION IN INCH |       |       |
|----------|-----------------|------|------|-------------------|-------|-------|
|          | MIN.            | NOM. | MAX. | MIN.              | NOM.  | MAX.  |
| A        |                 |      | 1.20 |                   |       | 0.047 |
| A1       | 0.20            |      | 0.30 | 0.008             |       | 0.012 |
| $\phi b$ | 0.30            | 0.35 | 0.40 | 0.012             | 0.014 | 0.016 |
| D        | 7.90            | 8.00 | 8.10 | 0.311             | 0.315 | 0.319 |
| D1       | 5.25 BSC        |      |      | 0.207 BSC         |       |       |
| E        | 5.90            | 6.00 | 6.10 | 0.232             | 0.236 | 0.240 |
| E1       | 3.75 BSC        |      |      | 0.148 BSC         |       |       |
| e        | 0.75 BSC.       |      |      | 0.030 BSC.        |       |       |
| ZD       | 1.375 REF.      |      |      | 0.054 REF.        |       |       |
| ZE       | 1.125 REF.      |      |      | 0.044 REF.        |       |       |

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207



TITLE

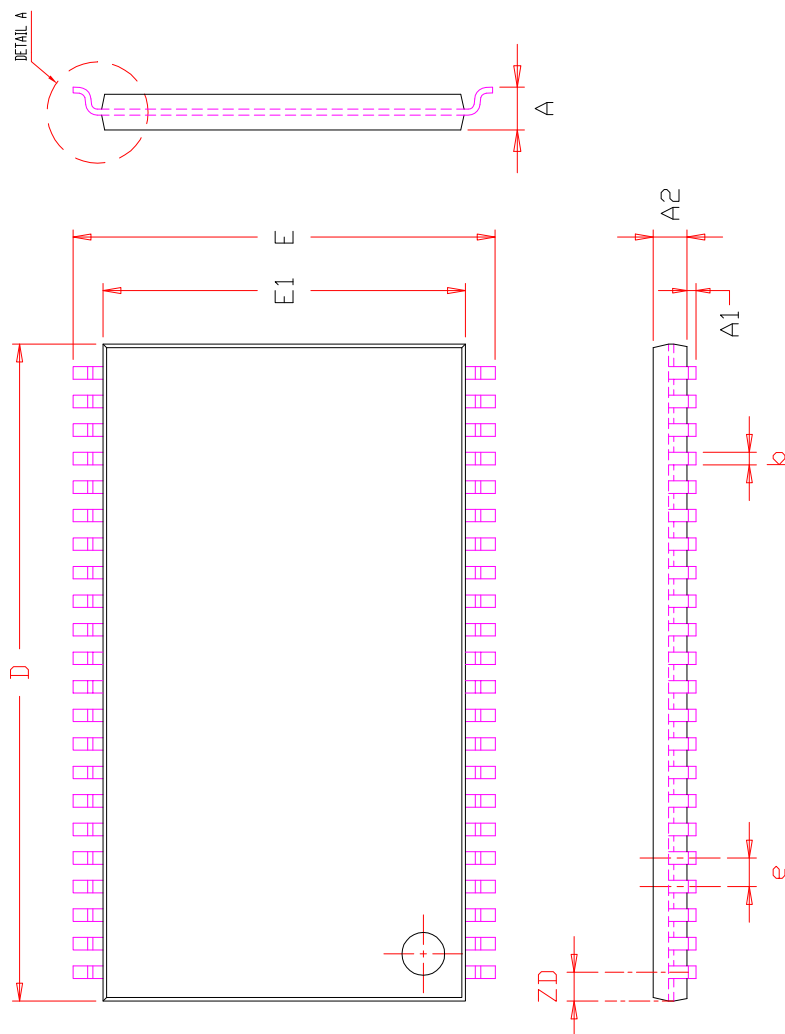
48L 6x8mm TF-BGA  
Package Outline

REV.

C

DATE

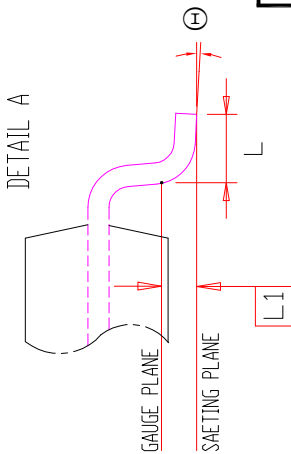
08/12/2008



| SYMBOL | DIMENSION IN MM |       |       | DIMENSION IN INCH |       |       |
|--------|-----------------|-------|-------|-------------------|-------|-------|
|        | MIN.            | NOM.  | MAX.  | MIN.              | NOM.  | MAX.  |
| A      | 1.00            |       | 1.20  | 0.039             |       | 0.047 |
| A1     | 0.05            |       | 0.15  | 0.002             |       | 0.006 |
| A2     | 0.95            | 1.00  | 1.05  | 0.037             | 0.039 | 0.041 |
| b      | 0.30            |       | 0.45  | 0.012             |       | 0.018 |
| D      | 18.28           | 18.41 | 18.54 | 0.720             | 0.725 | 0.730 |
| E      | 11.56           | 11.76 | 11.96 | 0.455             | 0.463 | 0.471 |
| E1     | 10.03           | 10.16 | 10.29 | 0.395             | 0.400 | 0.405 |
| e      |                 | 0.80  | BSC.  |                   | 0.031 | BSC.  |
| L      |                 | 0.40  |       | 0.69              | 0.016 | 0.027 |
| L1     |                 | 0.25  | BSC.  |                   | 0.010 | BSC.  |
| ZD     |                 | 0.805 | REF.  |                   | 0.032 | REF.  |
| ⊖      | 0               |       | 8°    | 0                 |       | 8°    |

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



TITLE

44L 400mil TSOP-2  
Package Outline

REV.

F

DATE

06/04/2008

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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