

100V COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET
Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(ON)}$ (Ω)max	I_D (A)max $T_A = +25^\circ\text{C}$
Q1	100V	0.230 @ $V_{GS} = 10\text{V}$	2.1
		0.300 @ $V_{GS} = 4.5\text{V}$	1.9
Q2	-100V	0.235 @ $V_{GS} = -10\text{V}$	-2.2
		0.320 @ $V_{GS} = -4.5\text{V}$	-1.9

Description

This new generation complementary dual MOSFET features low on-resistance achievable with low gate drive.

Applications

- DC Motor Control
- Backlighting

Features

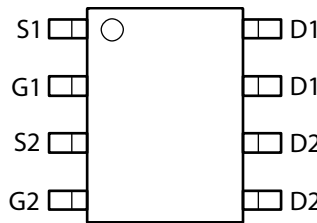
- 100V Complementary in SOIC package
- Low On-Resistance
- Fast Switching Speed
- Low Voltage ($V_{GS} = 4.5\text{V}$) gate drive
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

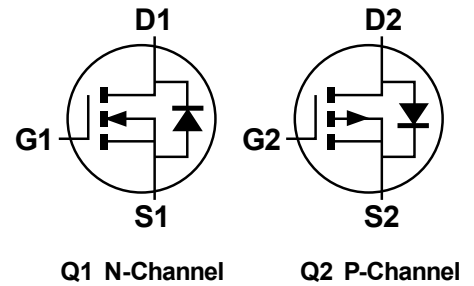
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.074 grams (approximate)



Top View



Top View

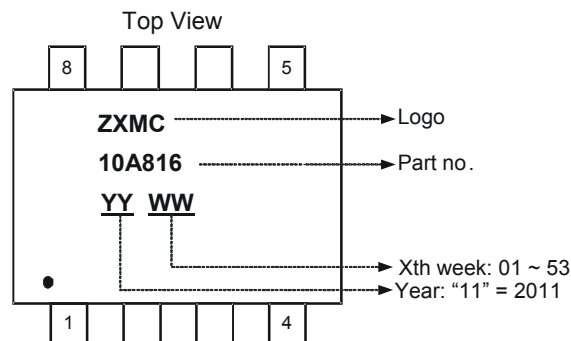


Equivalent Circuit

Ordering Information (Note 4)

Product	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMC10A816N8	13	12	2,500

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information


Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

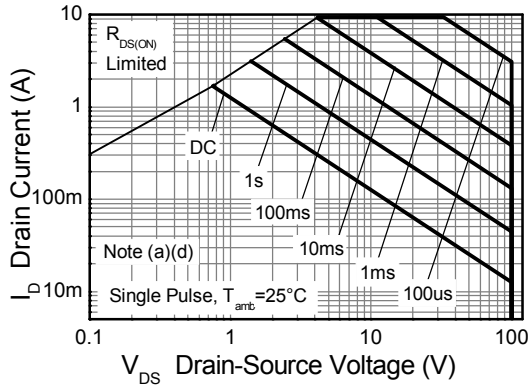
Parameter	Symbol	N-channel Q1	P-channel Q2	Unit
Drain-Source Voltage	V _{DSS}	100	-100	V
Gate-Source Voltage	V _{GS}	±20	±20	V
Continuous Drain Current @ V _{GS} = 10V; T _A = +25°C ^{(b)(d)} @ V _{GS} = 10V; T _A = +70°C ^{(b)(d)} @ V _{GS} = 10V; T _A = +25°C ^{(a)(d)} @ V _{GS} = 10V; T _A = +25°C ^{(a)(e)} @ V _{GS} = 10V; T _L = +25°C ^{(f)(d)}	I _D	2.1 1.7 1.7 2.0 2.3	-2.2 -1.8 -1.7 -2.0 -2.4	A
Pulsed Drain Current @ V _{GS} = 10V; T _A = +25°C ^{(c)(d)}	I _{DM}	9.4	-10.5	A
Continuous Source Current (Body Diode) at T _A = +25°C ^{(b)(d)}	I _S	3.0	-3.1	A
Pulsed Source Current (Body Diode) at T _A = +25°C ^{(c)(d)}	I _{SM}	9.4	-10.5	A
Avalanche Current (g) L = 0.1 mH	I _{AS}	1.2	12	A
Power Dissipation at T _A = +25°C ^{(a)(d)} Linear Derating Factor	P _D	1.3 10.0		W mW/°C
Power Dissipation at T _A = +25°C ^{(a)(e)} Linear Derating Factor	P _D	1.8 14.2		W mW/°C
Power Dissipation at T _A = +25°C ^{(b)(d)} Linear Derating Factor	P _D	2.1 16.7		W mW/°C
Power Dissipation at T _L = +25°C ^{(f)(d)} Linear Derating Factor	P _D	2.4 18.9	2.6 20.4	W mW/°C
Operating and Storage Temperature Range	T _j , T _{stg}	-55 to +150		°C

Thermal Characteristics

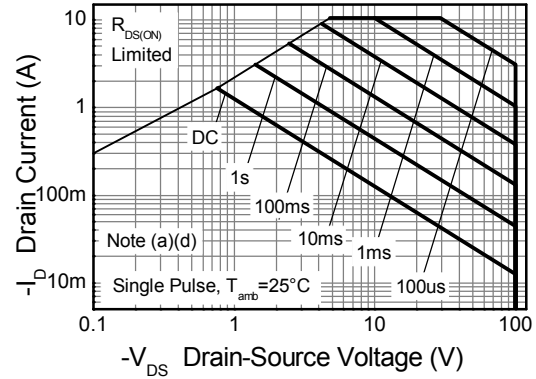
Parameter	Symbol	Value	Unit	
Junction to Ambient ^{(a)(d)}	R _{θJA}	100	°C/W	
Junction to Ambient ^{(a)(e)}	R _{θJA}	70	°C/W	
Junction to Ambient ^{(b)(d)}	R _{θJA}	60	°C/W	
Junction to Lead ^{(f)(d)}	R _{θJL}	53	49	°C/W

- Notes:
- (a) For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 - (b) Same as note (a), except the device is measured at t ≤ 10 sec.
 - (c) Same as note (a), except the device is pulsed with D= 0.02 and pulse width 300µs. The pulse current is limited by the maximum junction temperature.
 - (d) For a dual device with one active die.
 - (e) For a device with two active die running at equal power.
 - (f) Thermal resistance from junction to solder-point (at the end of the drain lead); the device is operating in a steady-state condition.
 - (g) IAS rating are based on low frequency and duty cycles to keep T_j = +25°C.

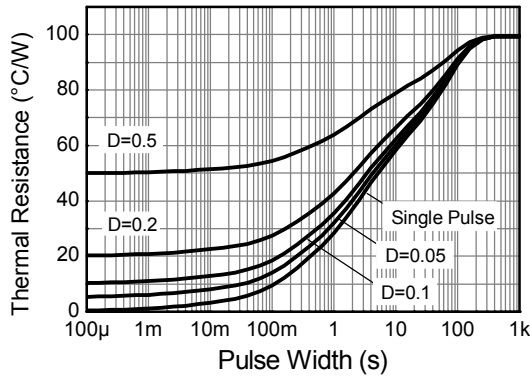
Thermal Characteristics



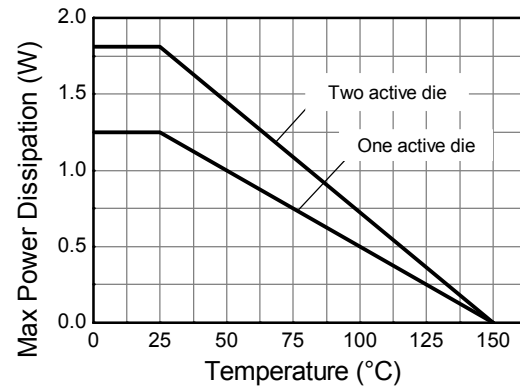
N-channel Safe Operating Area



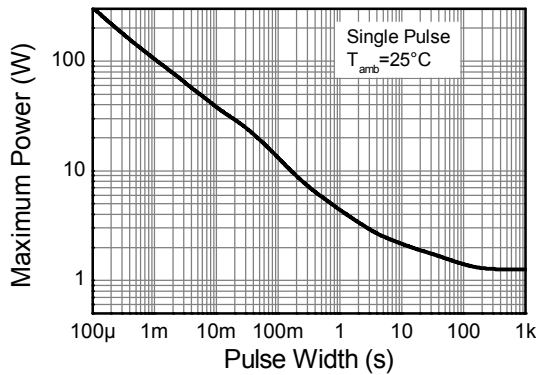
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



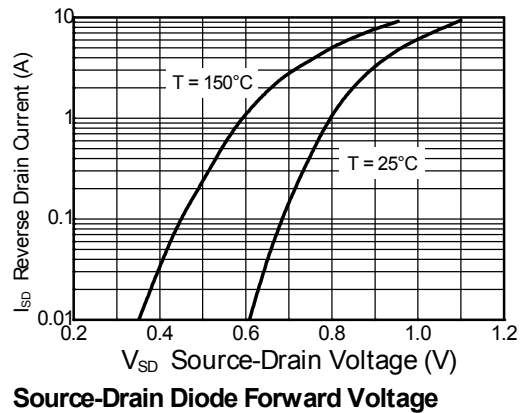
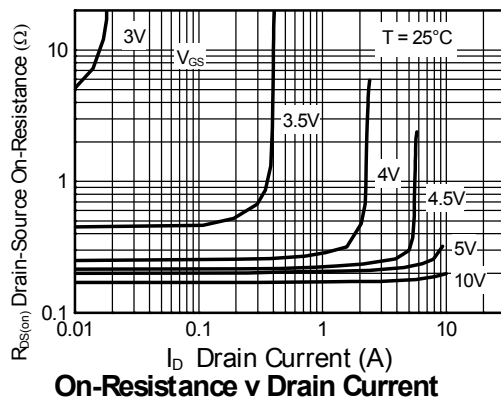
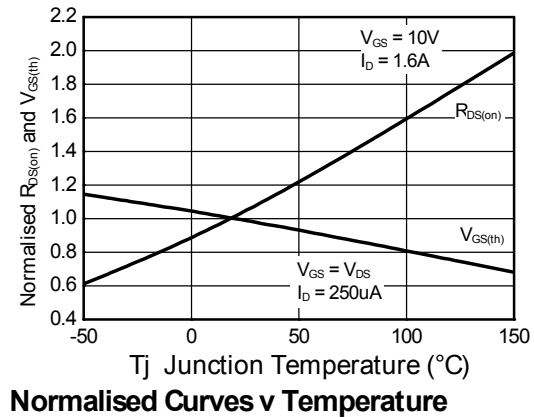
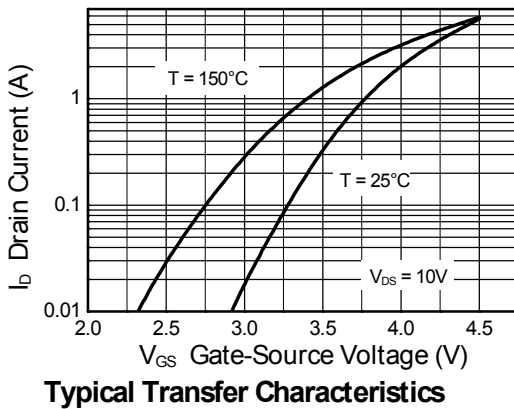
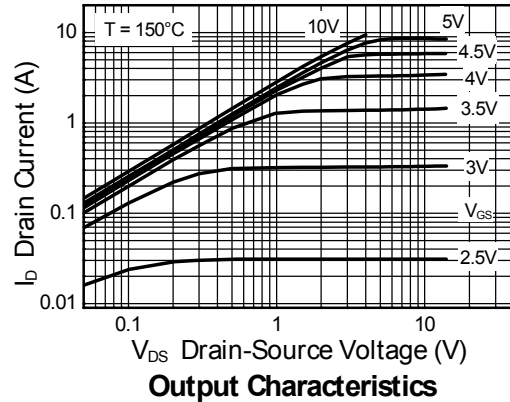
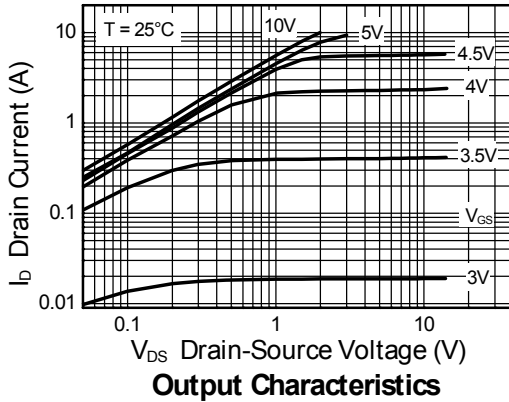
Pulse Power Dissipation

Electrical Characteristics Q1 N-Channel (@T_A = +25°C, unless otherwise specified.)

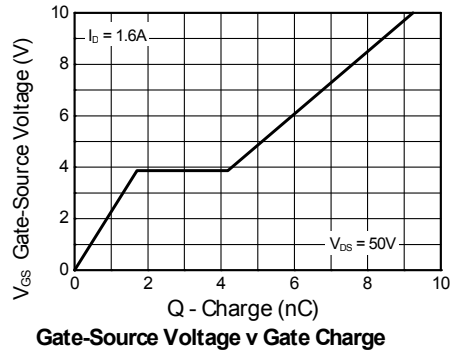
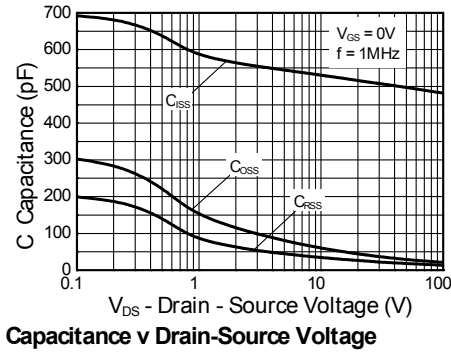
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	100	—	—	V	I _D = 250μA, V _{GS} = 0V
Zero Gate Voltage Drain Current	I _{DSS}	—	—	0.5	μA	V _{DS} = 100V, V _{GS} = 0V
Gate-Body Leakage	I _{GSS}	—	—	100	nA	V _{GS} = ±20V, V _{DS} = 0V
Gate-Source Threshold Voltage	V _{GS(th)}	1.7	—	2.4	V	I _D = 250μA, V _{DS} = V _{GS}
Static Drain-Source On-State Resistance ^(a)	R _{DS(ON)}	—	0.170 0.210	0.230 0.300	Ω	V _{GS} = 10V, I _D = 1.0A V _{GS} = 4.5V, I _D = 0.5A
Forward Transconductance ^{(a) (c)}	g _{fs}	—	4.8	—	S	V _{DS} = 15V, I _D = 1.6A
Dynamic Capacitance ^(c)						
Input Capacitance	C _{iss}	—	497	—	pF	V _{DS} = 50V, V _{GS} = 0V f = 1MHz
Output Capacitance	C _{oss}	—	29	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	18	—	pF	
Switching ^{(b) (c)}						
Turn-On-Delay Time	t _{d(ON)}	—	2.9	—	ns	V _{DD} = 50V, V _{GS} = 10V I _D = 1.0A R _G ≅ 6.0Ω,
Rise Time	t _r	—	2.1	—	ns	
Turn-Off Delay Time	t _{d(OFF)}	—	12.1	—	ns	
Fall Time	t _f	—	5.0	—	ns	
Gate Charge ^(c)						
Total Gate Charge	Q _g	—	9.2	—	nC	V _{DS} = 50V, V _{GS} = 10V I _D = 1.6A
Gate-Source Charge	Q _{gs}	—	1.7	—	nC	
Gate-Drain Charge	Q _{gd}	—	2.5	—	nC	
Source-Drain Diode						
Diode Forward Voltage ^(a)	V _{SD}	—	0.85	0.95	V	I _S = 1.7A, V _{GS} = 0V
Reverse Recovery Time ^(c)	t _{rr}	—	32	—	ns	I _S = 1.7A, di/dt = 100A/μs
Reverse Recovery Charge ^(c)	Q _{rr}	—	40	—	nC	
Gate Resistance						
Gate Resistance	R _G	0	—	3	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz

Notes: (a) Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%.
 (b) Switching characteristics are independent of operating junction temperature.
 (c) For design aid only, not subject to production testing.

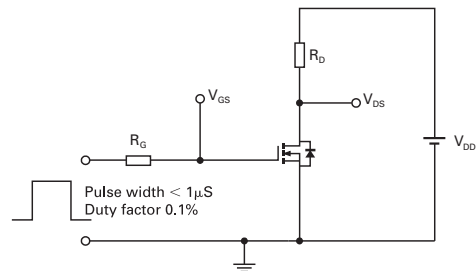
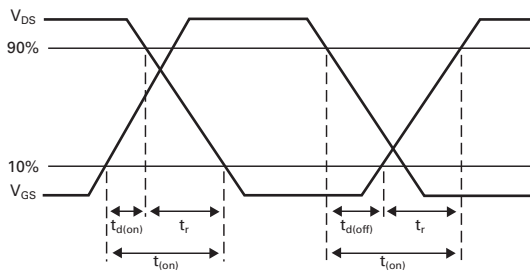
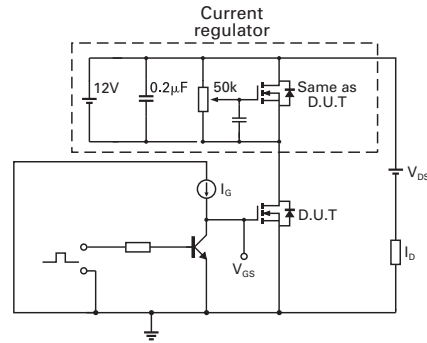
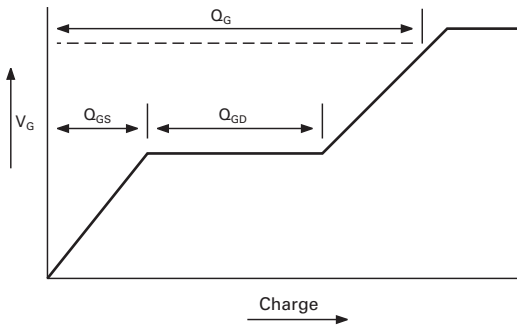
Typical Characteristics Q1 N-Channel



Typical Characteristics Q1 N-Channel (cont.)



Test Circuits

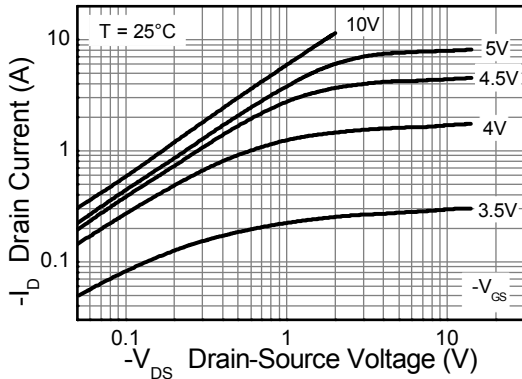


Electrical Characteristics Q2 P-Channel (@T_A = +25°C, unless otherwise specified.)

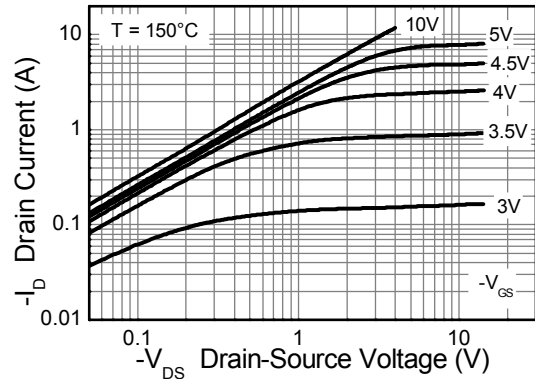
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	-100	—	—	V	I _D = -250μA, V _{GS} = 0V
Zero Gate Voltage Drain current	I _{DSS}	—	—	-0.5	μA	V _{DS} = -100V, V _{GS} = 0V
Gate-Body Leakage	I _{GSS}	—	—	100	nA	V _{GS} = ±20V, V _{DS} = 0V
Gate-Source Threshold Voltage	V _{GS(th)}	-2.0	—	-3.0	V	I _D = -250μA, V _{DS} = V _{GS}
Static Drain-Source On-State Resistance ^(a)	R _{DS(ON)}	—	0.170 0.250	0.235 0.320	Ω	V _{GS} = -10V, I _D = -1.0A V _{GS} = -4.5V, I _D = -0.5A
Forward Transconductance ^{(a)(c)}	g _{fs}	—	4.7	—	S	V _{DS} = -15V, I _D = -2.1A
Dynamic Capacitance ^(c)						
Input Capacitance	C _{iss}	—	717	—	pF	V _{DS} = -50V, V _{GS} = 0V f = 1MHz
Output Capacitance	C _{oss}	—	55	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	46	—	pF	
Switching ^{(b)(c)}						
Turn-On-Delay Time	t _{d(ON)}	—	4.3	—	ns	V _{DD} = -50V, V _{GS} = -10V I _D = -1A R _G ≅ 6.0Ω,
Rise Time	t _r	—	5.2	—	ns	
Turn-Off Delay Time	t _{d(OFF)}	—	20	—	ns	
Fall Time	t _f	—	12	—	ns	
Gate Charge ^(c)						
Total Gate Charge	Q _g	—	16.5	—	nC	V _{DS} = -50V, V _{GS} = -10V I _D = -2.1A
Gate-Source Charge	Q _{gs}	—	2.5	—	nC	
Gate-Drain Charge	Q _{gd}	—	5.4	—	nC	
Source-Drain Diode						
Diode Forward Voltage ^(a)	V _{SD}	—	-0.85	-0.95	V	I _S = -1.7A, V _{GS} = 0V
Reverse Recovery Time ^(c)	t _{rr}	—	43	—	ns	I _S = -1.7A, di/dt = 100A/μs
Reverse Recovery Charge ^(c)	Q _{rr}	—	77	—	nC	
Gate Resistance						
Gate Resistance	R _G	0	—	100	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz

- Notes: (a) Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%.
 (b) Switching characteristics are independent of operating junction temperature.
 (c) For design aid only, not subject to production testing.

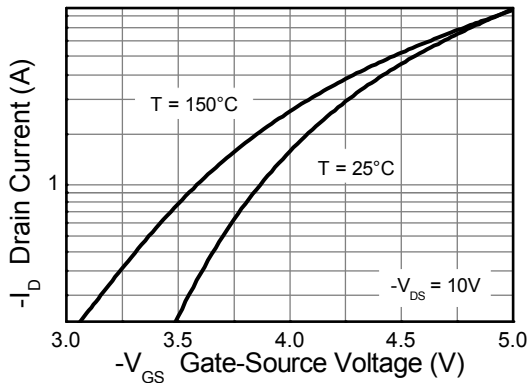
Typical Characteristics Q2 P-Channel



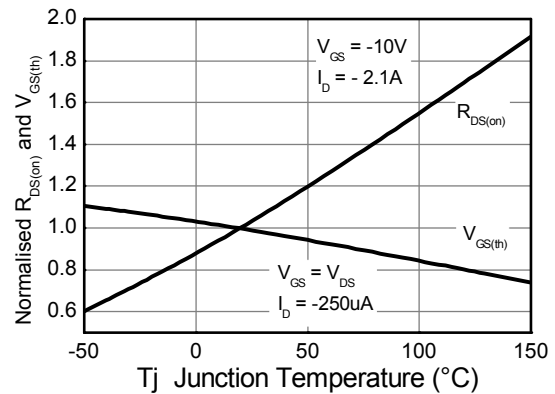
Output Characteristics



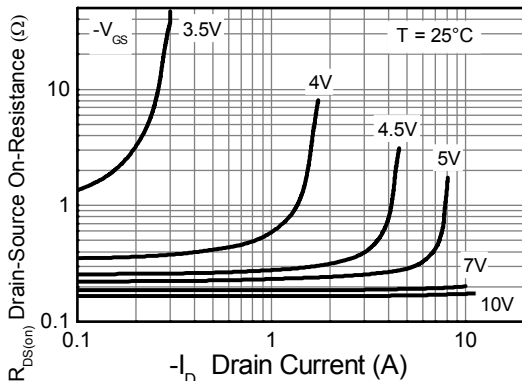
Output Characteristics



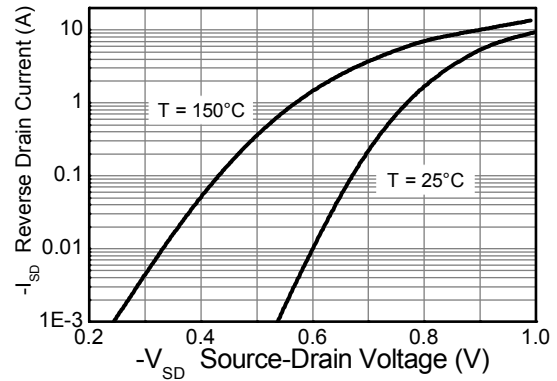
Typical Transfer Characteristics



Normalised Curves v Temperature

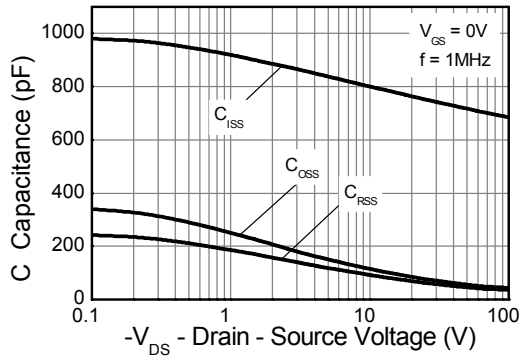


On-Resistance v Drain Current

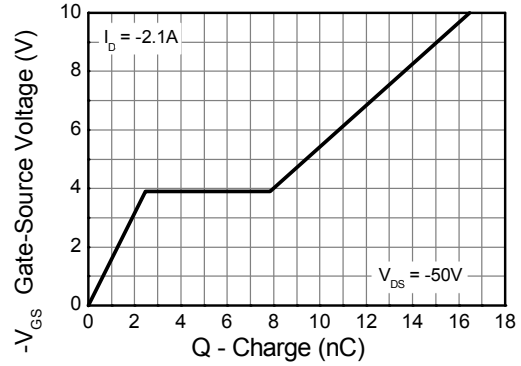


Source-Drain Diode Forward Voltage

Typical Characteristics Q2 P-Channel (cont.)

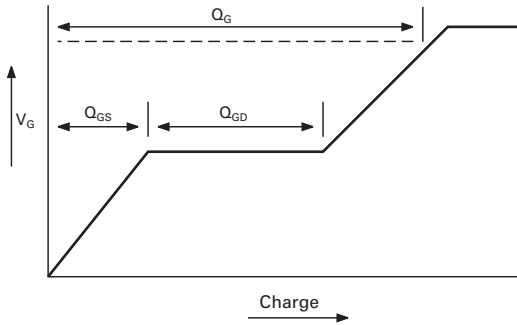


Capacitance v Drain-Source Voltage

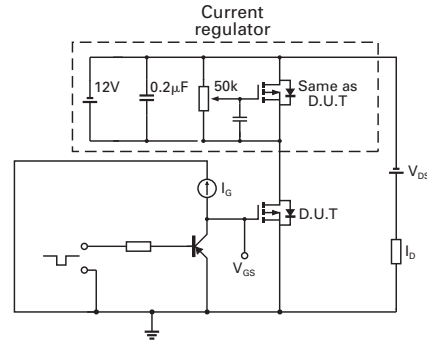


Gate-Source Voltage v Gate Charge

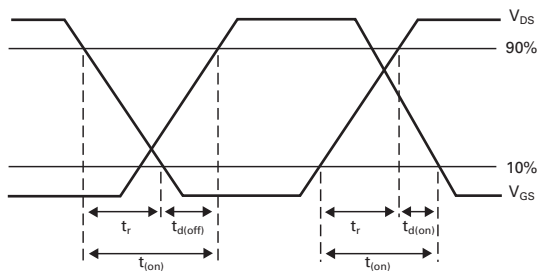
Test Circuits



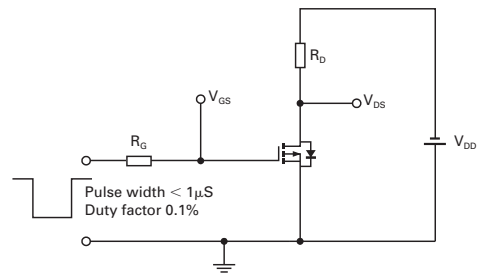
Basic gate charge waveform



Gate charge test circuit



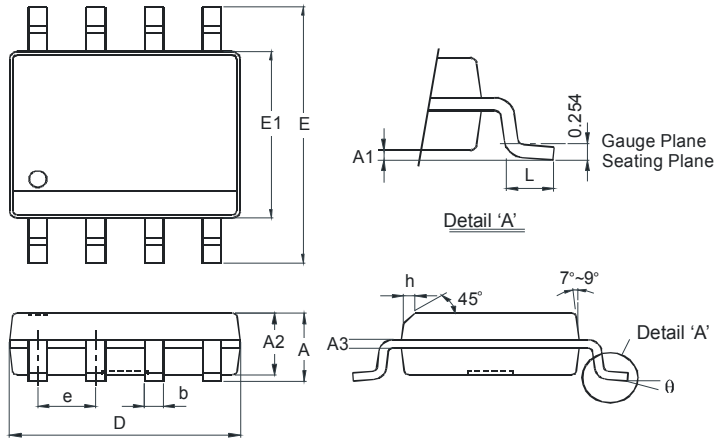
Switching time waveforms



Switching time test circuit

Package Outline Dimensions

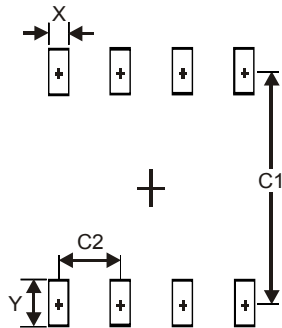
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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