

R2A20166NP/SA

8-bit 6ch D/A Converter with Buffer Amplifiers

R03DS0018EJ0100
Rev.1.00
2011.09.05

Description

The R2A20166 is an integrated circuit semiconductor of CMOS structure with 6 channels of built in D/A unnecessary and enabling configuration of a system with few component parts.

Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD.

Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink source, and can operate over the entire voltage range from almost ground to Vcc (0 to 5V), making peripheral elements unnecessary and enabling configuration of a system with few component parts.

Very small QFN package is added to lineup. It is suitable for a small mounting and reduces the mounting area.

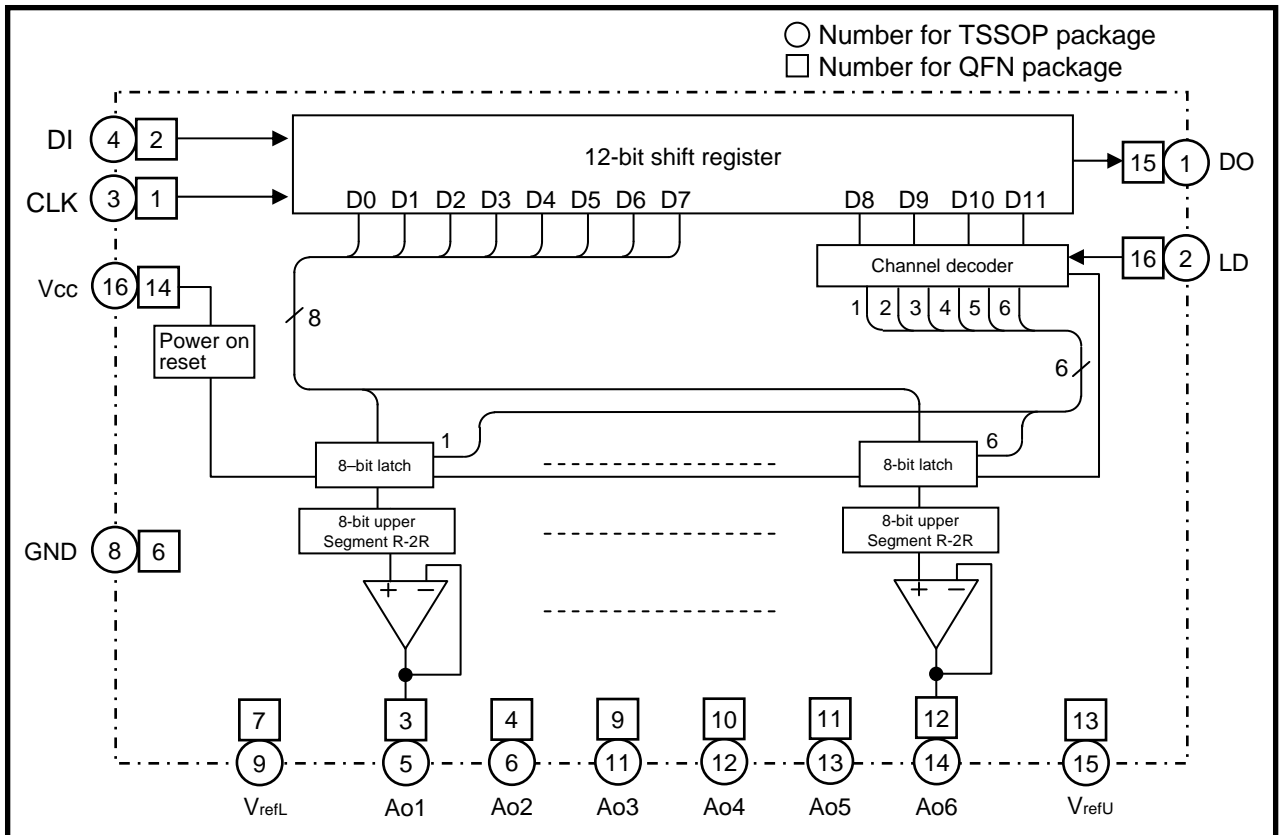
Features

- Guarantee Nonlinearity error : +/-1.0LSB, Differential nonlinearity error : +/-0.7LSB
- Data transfer format: 12-bit serial data input type by 3 wire (DI, SCK, LD)
- Output buffer op-amps: Operable over entire voltage range from almost ground to Vcc (0 to 5V)
- Very small size package line-up: QFN-16(pin pitch: 0.5mm), TSSOP-16 (pin pitch 0.65mm)

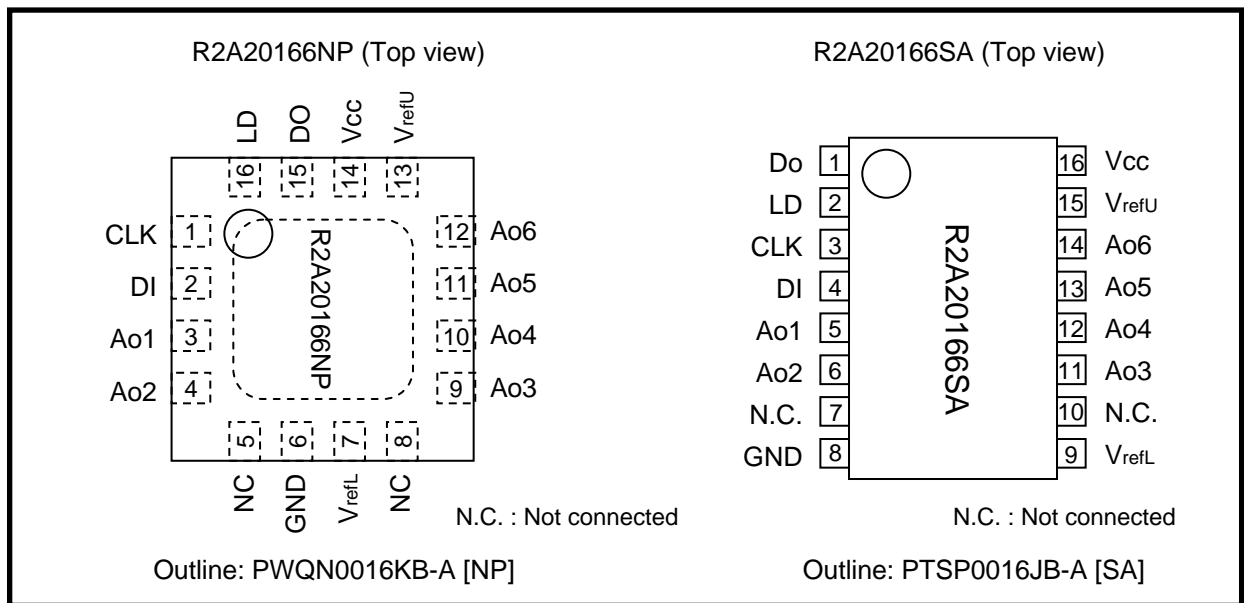
Application

- Conversion from digital data to analog control data for home-use and industrial equipment.
- Signal gain control or automatic adjustment of LCD-TV, PDP-TV or LCD display-monitor.
- Blurring correction control or various control of the interchangeable lens of digital still camera.
- Automatic adjustment by combination with microcomputer and EEPROM.
(substitution of half fixed resistance)

Block Diagram



Pin Arrangement



Pin Description

Pin No.		Symbol	Function
[QFN]	[TSSOP]		
2	4	DI	Serial data input terminal. (Input serial data with a 12-bit data length)
1	3	CLK	Serial clock input terminal (Input signal from DI terminal is input to 12-bit shift register at rise of serial clock.)
16	2	LD	Load terminal (When High level is input to LD terminal, value in 12-bit shift register is loaded into decoder and 8-bit latch.)
15	1	Do	Serial data output terminal (Data is sequentially output from the MSB bit.)
3	5	Ao1	8-bit resolution D/A converter output terminals (After power on, all channels are reset and DAC data 00h is output.)
4	6	Ao2	
9	11	Ao3	
10	12	Ao4	
11	13	Ao5	
12	14	Ao6	
14	16	Vcc	Power supply terminal
6	8	GND	GND terminal
13	15	VrefU	D/A converter upper reference voltage input terminal
7	9	VrefL	D/A converter lower reference voltage input terminal
5	7	N.C.	Not connected
8	10	N.C.	Not connected

Absolute Maximum Ratings

(Ta= +25deg unless otherwise noted)

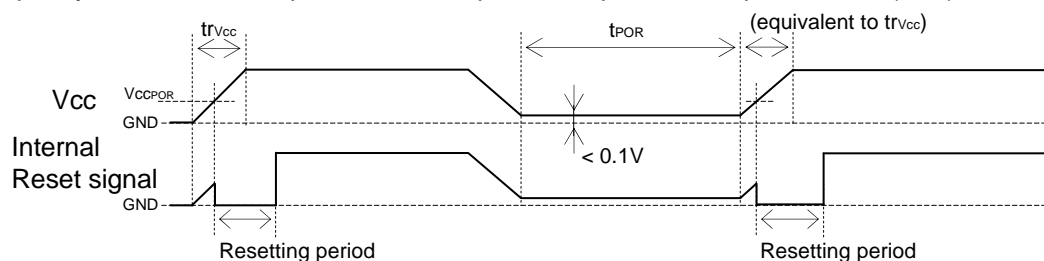
Item	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC}		-0.3 to +6.5	V
D/A converter upper reference voltage	V _{refU}		-0.3 to +6.5	V
D/A converter lower reference voltage	V _{refL}		-0.3 to +6.5	V
Buffer amplifier output current	I _{AO}	Continuous	-2.0 to +2.0	mA
Input voltage	V _{in}		-0.3 to V _{CC} +0.3 <+6.5	V
Output voltage	V _o		-0.3 to V _{CC} +0.3 <+6.5	V
Power dissipation	P _d	Ta= +85deg	290(NP) / 150(SA)	mW
Thermal derating factor	K theta	Ta> +25deg	7.25(NP) / 3.75(SA)	mW/deg
Operating temperature	T _{opr}		-30 to +85	deg
Storage temperature	T _{stg}		-40 to +125	deg

Electrical Characteristics

« Digital Part » (V_{CC}, V_{refU} = +5V +/-10%, V_{CC}>V_{refU}, GND, V_{refL} =0V, Ta= -30 to +85deg, Unless otherwise noted)

Item	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Supply voltage	V _{CC}		2.7	5.0	5.5	V
Supply current	I _{CC}	CLK = 1MHz, V _{CC} =5V, I _{AO} =0μA	-	0.35	1.1	mA
Input leak current	I _{ILK}	V _{IN} = 0 to V _{CC}	-10	-	10	μA
Input low voltage	V _{IL}		-	-	0.2V _{CC}	V
Input high voltage	V _{IH}	4.0V < V _{CC}	0.5V _{CC}	-	-	V
		V _{CC} ≤ 4.0V	0.8V _{CC}	-	-	V
Output low voltage	V _{OL}	4.0V < V _{CC} , I _{oL} = 2.0 mA	-	-	0.4	V
		V _{CC} < 4.0V, I _{oL} = 1.5 mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{oH} = -400 μA	V _{CC} - 0.4	-	-	V
Supply voltage rise time *1	t _{rVCC}	V _{CC} = 0 to 2.7V	100	-	-	μs
Internal reset operating voltage *1	V _{CCPOR}	V _{CC} = 0 to 2.7V	-	1.5	1.9	V
Power supply restart interval (Power supply OFF → ON) *1	t _{POR}	V _{CC} < 0.1V	1	-	-	ms

*1 : When power supply is turned on, internal circuit is initialized by power on reset circuit. But, if re-powered on quickly, initialize is not operate. So, keep the time period of re-powered on (t_{POR}).



« Analog Part » (V_{CC} , $V_{refU} = +5V \pm 10\%$, $V_{CC} > V_{refU}$, GND , $V_{refL} = 0V$, $T_a = -30$ to $+85$ deg, unless otherwise noted)

Item	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Current dissipation	I_{refU}	$V_{refU}=5V$, $V_{refL}=0V$, $I_{AO}=0\mu A$, Data condition: at maximum current	-	0.8	1.6	mA
D/A converter upper reference voltage range *2	V_{refU}		$0.7V_{CC}$	-	V_{CC}	V
D/A converter lower reference voltage range *2	V_{refL}		GND	-	$0.3V_{CC}$	V
Buffer amplifier output voltage range	V_{AO}	$I_{AO} = \pm 100 \mu A$	0.1	-	$V_{CC} - 0.1$	V
		$I_{AO} = \pm 500 \mu A$	0.2	-	$V_{CC} - 0.2$	V
Buffer amplifier output drive range	I_{AO}	Upper side saturation voltage = 0.3V, Lower side saturation voltage = 0.2V	-1.0	-	1.0	mA
Differential nonlinearity	SDL	$V_{refU} = 4.79V$, $V_{refL} = 0.95V$, $V_{CC} = 5.5V$ (15mV/LSB), Without load ($I_{AO} = 0\mu A$)	-0.7	-	0.7	LSB
Nonlinearity	SL		-1.0	-	1.0	LSB
Zero code error	S_{ZERO}		-2.0	-	2.0	LSB
Full scale error	S_{FULL}		-2.0	-	2.0	LSB
Output capacitive load	C_o		-	-	0.1	μF
Buffer amplifier output impedance	R_o		-	5.0	-	ohm

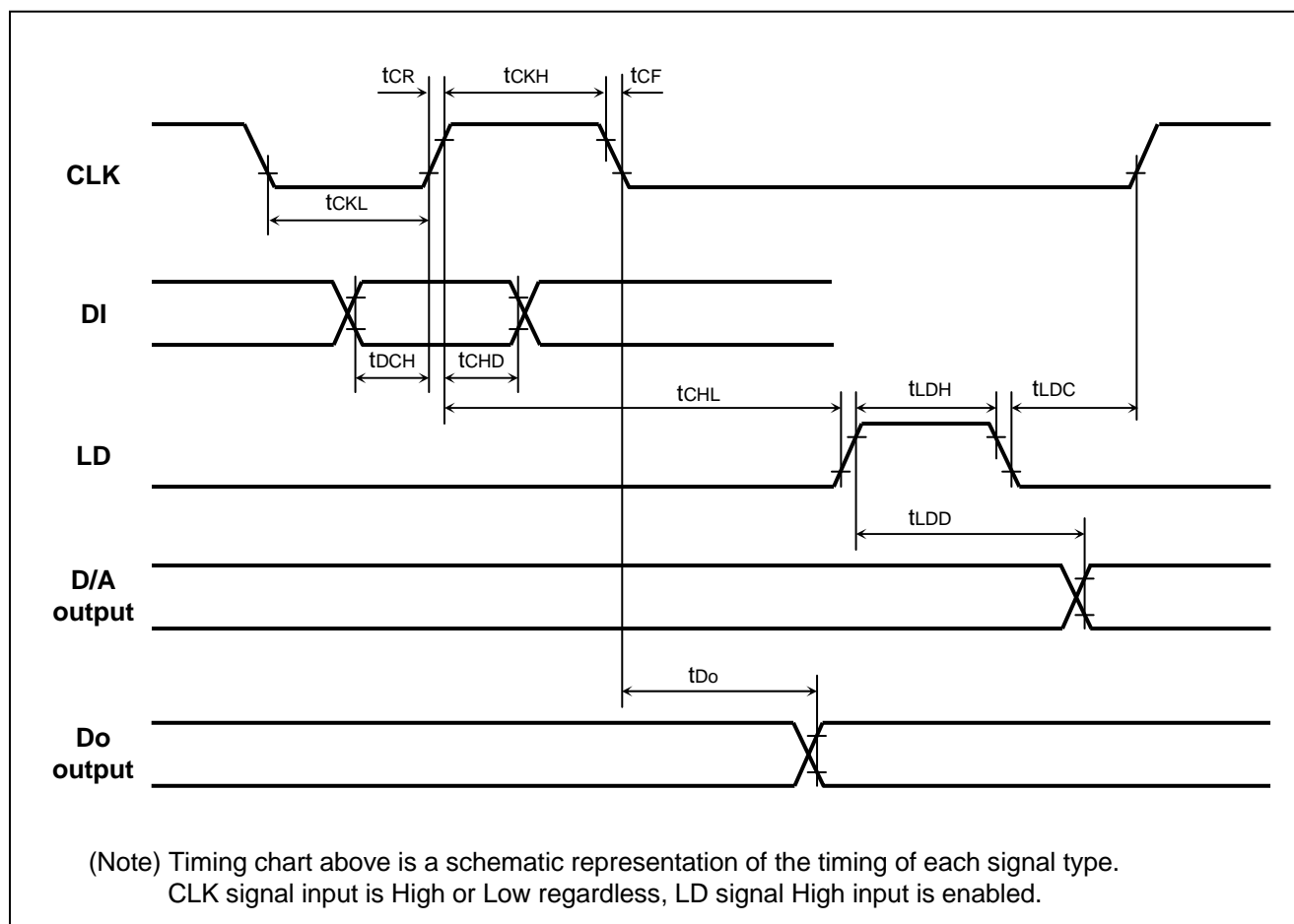
*2 : The output does not necessary be the value with the reference voltage setting range.
The output value is determined by the buffer amplifier output voltage range (V_{AO}).

AC Characteristics

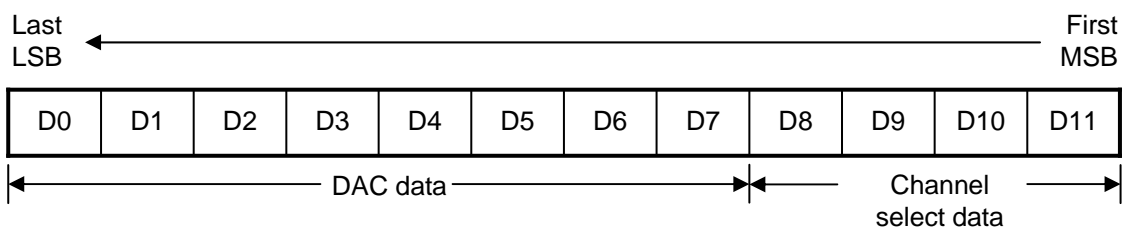
($V_{CC}, V_{refU} = +5V \pm 10\%$, $V_{CC} \geq V_{refU}$, $GND = V_{refL} = 0V$, $T_a = -30$ to $+85$ deg, unless otherwise noted)

Item	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Clock frequency	f_{CLK}		-	1.0	10	MHz
Clock low pulse width	t_{CKL}		40	-	-	ns
Clock high pulse width	t_{CKH}		40	-	-	ns
Clock rise time	t_{CR}		-	-	200	ns
Clock fall time	t_{CF}		-	-	200	ns
Data setup time	t_{DCH}		4	-	-	ns
Data hold time	t_{CHD}		30	-	-	ns
LD setup time	t_{CHL}		40	-	-	ns
LD hold time	t_{LDC}		40	-	-	ns
LD high pulse width	t_{LDH}		40	-	-	ns
Data output delay time	t_{DO}	$C_L < 100$ pF	-10	-	50	ns
D/A output settling time	t_{LDD}	$T_a = 25$ deg, $C_L < 100$ pF, $V_{AO}: 0.5 \leftrightarrow 4.5V$, The time until the output becomes the final value of 1/2 LSB.	-	-	150	μ s

Timing Chart



Digital Data Format



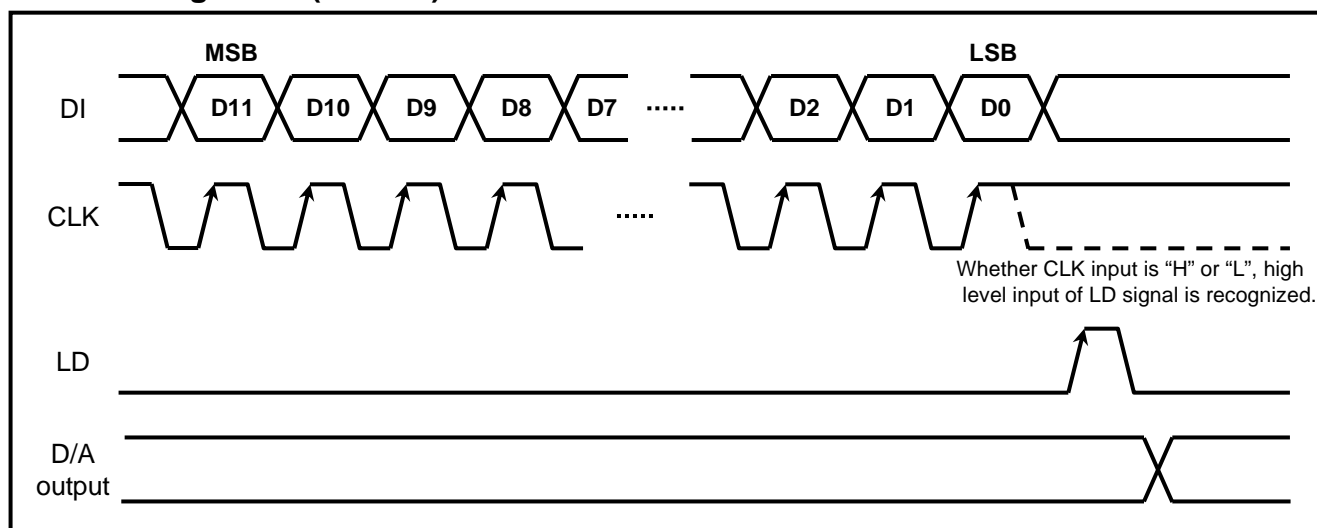
Channel select data

D8	D9	D10	D11	Chanel Selection
0	0	0	0	Don't care
0	0	0	1	Ao1 select
0	0	1	0	Ao2 select
0	0	1	1	Ao3 select
0	1	0	0	Ao4 select
0	1	0	1	Ao5 select
0	1	1	0	Ao6 select
0	1	1	1	Don't care
:	:	:	:	:
1	1	1	0	Don't care
1	1	1	1	Don't care

DAC data

D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 4 + V_{refL}$
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	$(V_{refU} - V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	V_{refU}

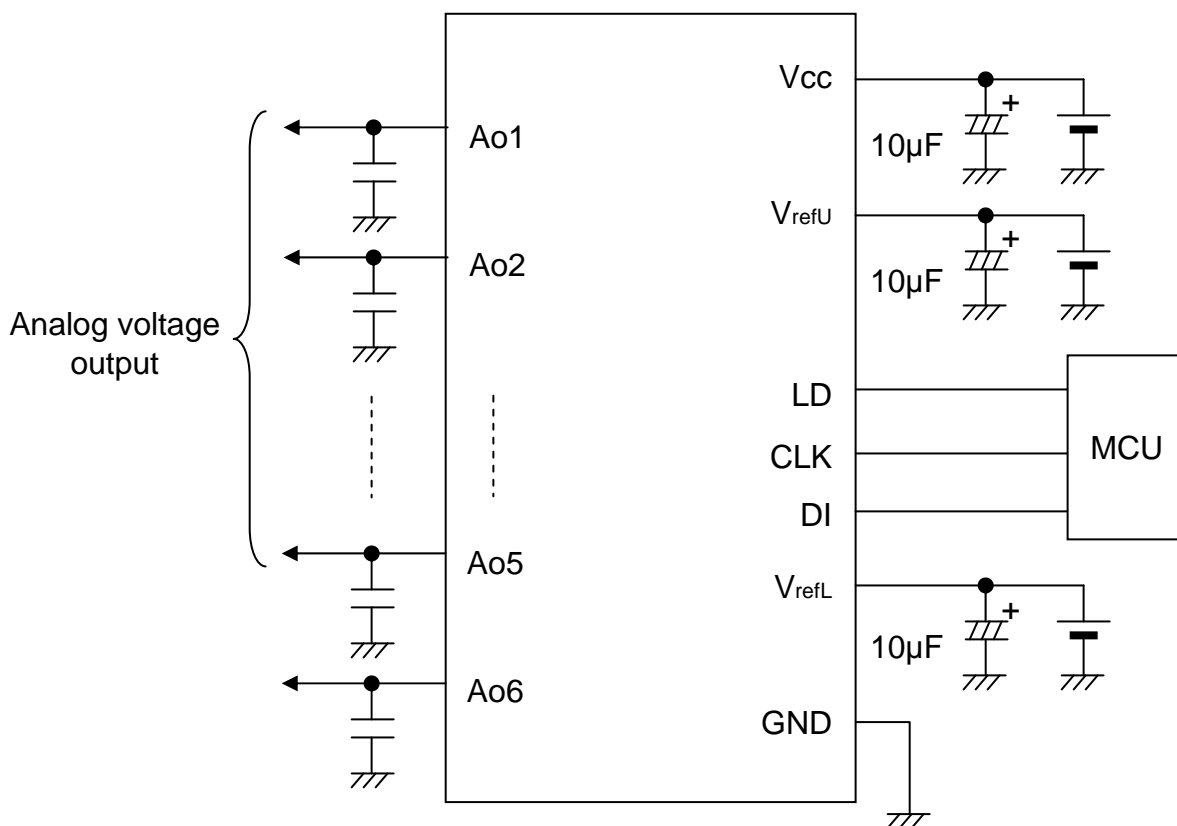
Data Timing Chart (Model)



Precaution For Use

- There are three terminals (V_{CC} , V_{refU} , V_{refL}) that should be impressed a constant voltage. When ripple or spike noise is input to this terminal, there is fear that the accuracy of D/A conversion becomes lower and this IC malfunction. So, when use this IC, please connect capacitor between these terminals (V_{CC} , V_{refU} , V_{refL}) and GND for stable D/A conversion.
- This IC's output amplifier has an advantage to capacitive load, So, it's no problem at device action when connect capacitor ($0.1\mu\text{F}$ Max) among output to GND for every noise elimination.

Standard Application Circuit

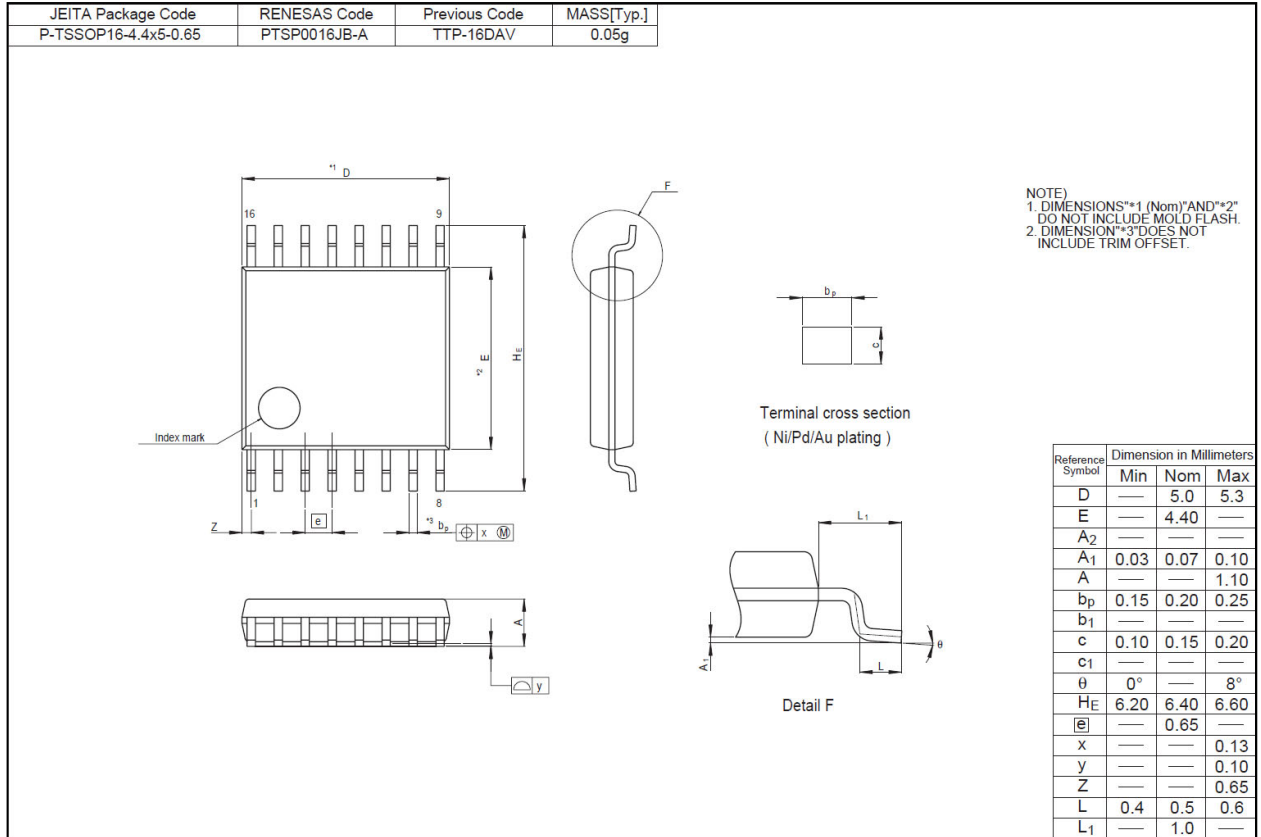


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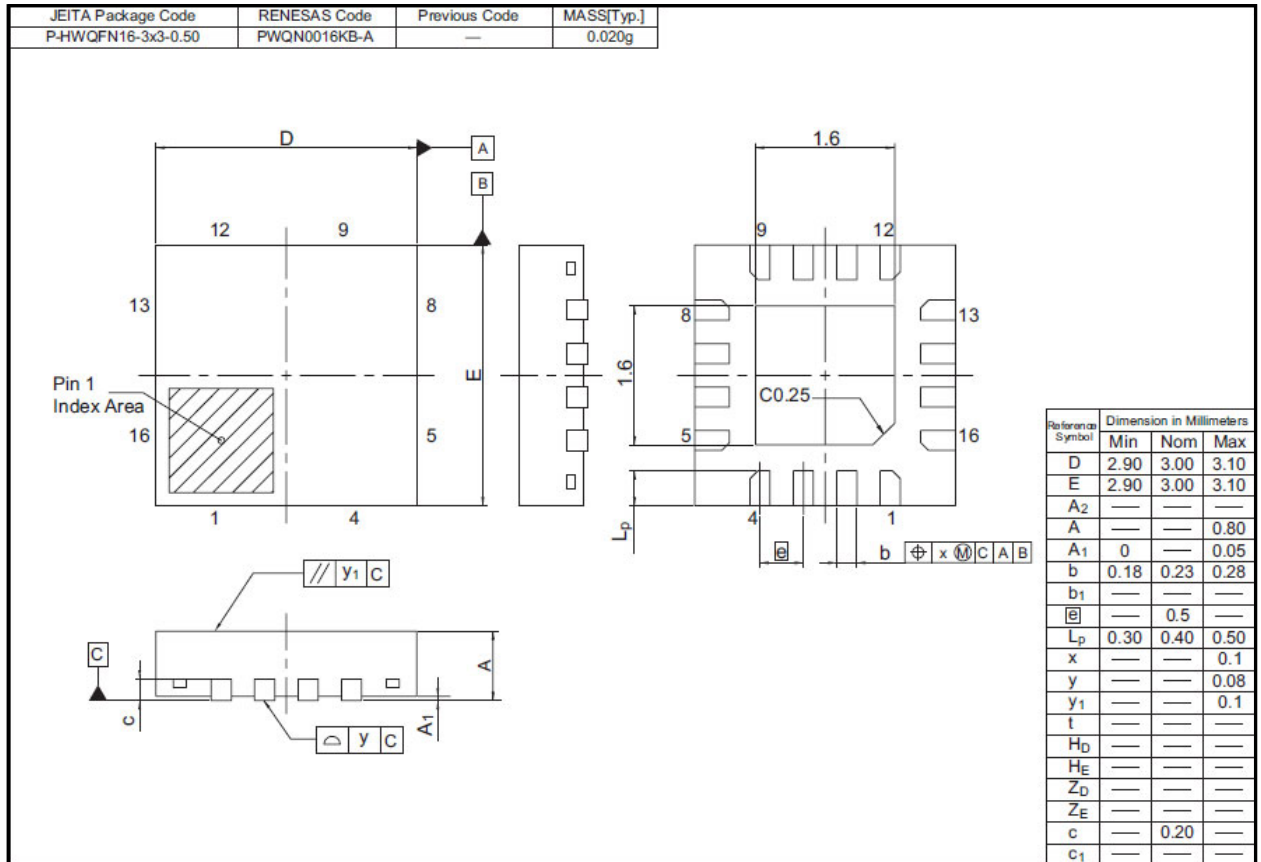
Order part No.	Package Name	Package Code	Package type No.	Packing/Quantity
R2A20166SA	TSSOP-16	RTSP0016JB-A	SA	Embossed Taping/2,000 pcs.
R2A20166NP	QFN-16	PWQN0016KB-A	NP	Embossed Taping/3,000 pcs.

Package Dimensions

PTSP0016JB-A [SA]



PWQN0016KB-A [NP]



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