Middle Power Class-D Speaker Amplifier

25W+25W
Full Digital Speaker Amplifier with built-in DSP

BM5449MWV

●General Description

BM5449MWV is a Full Digital Speaker Amplifier with built-in DSP (Digital Sound Processor) designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of 25W+25W. This IC employs state-of-the-art Bipolar, CMOS, and DMOS (BCD) process technology that eliminates turn-on resistance in the output power stage and internal loss due to line resistances up to an ultimate level. With this technology, the IC can achieve high efficiency of 90% (10W+10W output with 8Ω load). In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 40W. This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

●Features

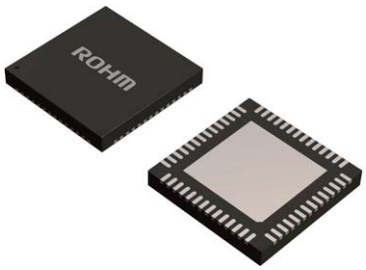
- With wide range of power supply voltage. (V_{CC}=10 to 26V)
- This IC includes the DSP (digital sound processor) for Audio signal processing for Flat TVs.
  Synchronous SRC, Surround, 8 Band EQ, 1 Band EQ (for Sub), Volume, 2 Band DRC, Delay RAM for phase revised Close Over Filter, 512 Taps FIR Filter, P^2Volume, P^2Base+, Higher Sound Complement (High Generator), Soft Clipper, Hard Clipper
- This IC has two inputs systems of digital audio interface.
  I^2S / LJ / RJ format, LRCLK: 8 to 192 kHz, BCLK: 32fs / 48fs / 64fs, SDATA: 16 / 20 / 24bits
  BCLK: 32fs / 48fs / 64fs, SDATA: 16 / 20 / 24bits
- Two Digital Audio Output for Audio DAC and headphone.
- One PWM Output for Subwoofer.
- The sound quality decrease by the power supply variation is prevented with the output feedback circuit. In addition, a low noise and a low distortion are achieved. Mass electrolytic capacitor is unnecessary because it is strong in the power supply variation.
- It contributes to miniaturizing, making to the thin type, and the power saving of the system by highly effective (10W+10W output and 8Ω on-load) 90% and low generation of heat.
- Low current at the Power down Mode.
- The pop noise at power supply on/off is prevented, and a more high-quality soft mute function is built into. Highly reliable design with built-in various protection functions.
- The component side product can be decreased because of small package (UQFN056V7070).
- The maximum output in the stereo is 25W+25W (VCC=20.5V, 8Ω load).
- The maximum output in the monaural(PBTL) is 50W(VCC=20.5V, 4Ω load)

●Key Specifications

- Supply voltage (VCC): 10V to 26V
- Speaker output power (VCC=18V, RL=8Ω): 20W+20W(Typ.)
- THD+N: 0.05 %(Typ.)

●Package

	W (Typ.) x D (Typ.) x H(Max.)
UQFN056V7070	7.00mm x 7.00mm x 1.00mm



●Applications

- Flat Panel TVs(LCD, Plasma)
- Home Audio
- Amusement equipments
- Electronic Music equipments etc.

●Typical Application Circuit

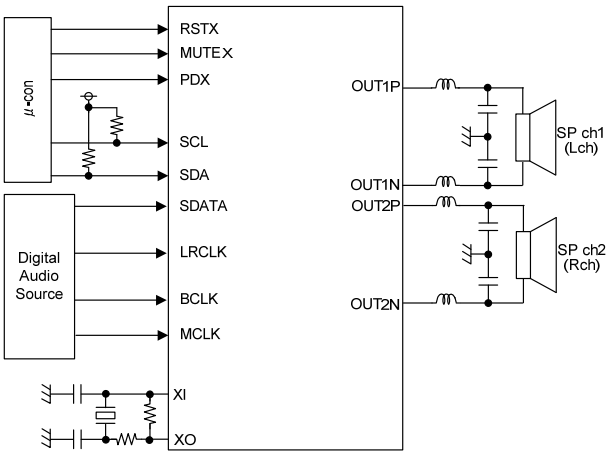


Figure 1. Typical application circuit

●Pin Configuration

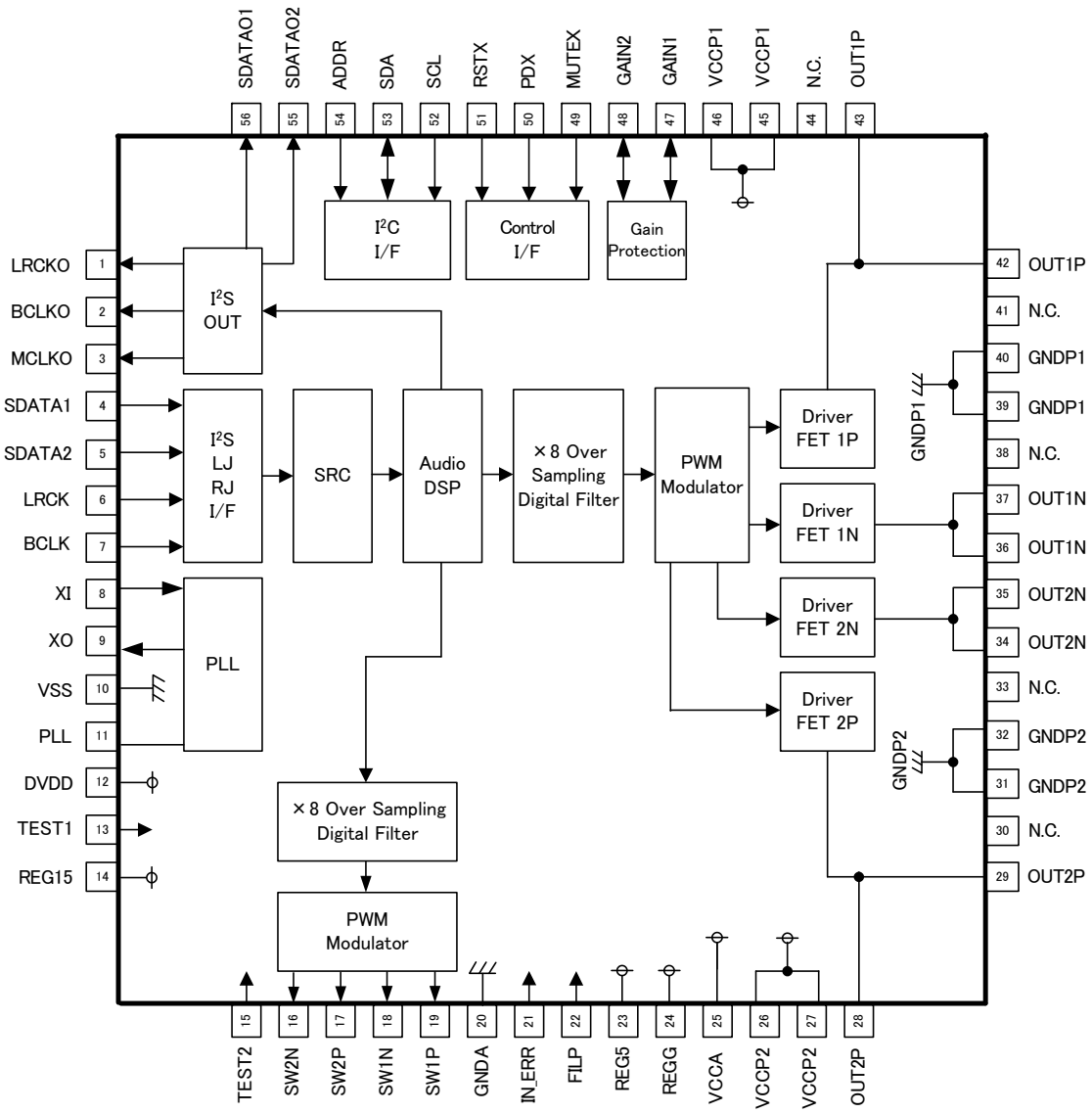


Figure 2. Pin configuration (Top View)

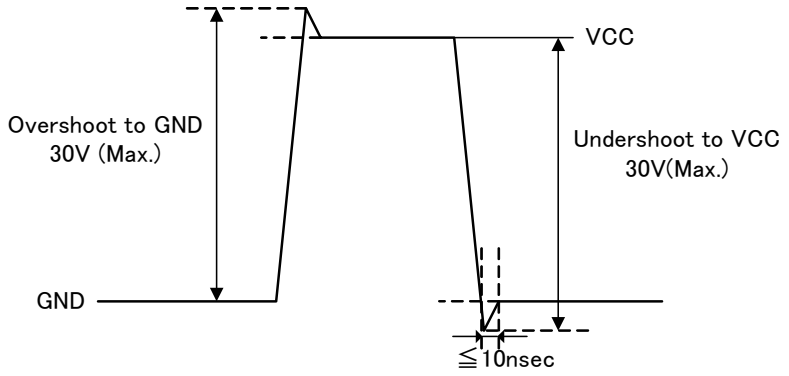
●Pin Description

No.	Name	I/O	No.	Name	I/O	No.	Name	I/O	No.	Name	I/O
1	LRCKO	I/O	15	TEST2	I	29	OUT2P	O	43	OUT1P	O
2	BCLKO	I/O	16	SW2N	O	30	N.C.	-	44	N.C.	-
3	MCLKO	I/O	17	SW2P	O	31	GNDP2	-	45	VCCP1	-
4	SDATA1	I	18	SW1N	O	32	GNDP2	-	46	VCCP1	-
5	SDATA2	I	19	SW1P	O	33	N.C.	-	47	GAIN1	I/O
6	LRCK	I	20	GNDA	-	34	OUT2N	O	48	GAIN2	I/O
7	BCLK	I	21	IN_ERR	I	35	OUT2N	O	49	MUTEX	I
8	XI	I	22	FILP	O	36	OUT1N	O	50	PDX	I
9	XO	O	23	REG5	O	37	OUT1N	O	51	RSTX	I
10	VSS	-	24	REGG	O	38	N.C.	-	52	SCL	I
11	PLL	O	25	VCCA	-	39	GNDP1	-	53	SDA	I/O
12	DVDD	-	26	VCCP2	-	40	GNDP1	-	54	ADDR	I
13	TEST1	I	27	VCCP2	-	41	N.C.	-	55	SDATAO2	I/O
14	REG15	O	28	OUT2P	O	42	OUT1P	O	56	SDATAO1	I/O

●Absolute Maximum Ratings(Ta=25℃)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	V_{CC}	-0.3 to 30	V	Pin 25, 26, 27, 45, 46 *1 *2
	V_{DD}	-0.3 to 4.5		Pin 12 *1 *2
Power dissipation	Pd	4.29	W	*3
		4.83		*4
Input voltage	V_{IN}	-0.3 to 4.5	V	Pin 4 to 8, 13, 15, 49to54 *1
Terminal voltage1	V_{PIN1}	-0.3 to 4.5	V	Pin 1 to 3, 9, 16to19, 47, 48, 55, 56 *1
Terminal voltage 2	V_{PIN2}	-0.3 to 7.0	V	Pin 22 to 24 *1
Terminal voltage 3	V_{PIN3}	-0.3 to 30	V	Pin 28, 29, 34 to 37, 42, 43 *1 *5
Operating temperature range	T_{opr}	-25 to +85	℃	
Storage temperature range	T_{stg}	-55 to +150	℃	
Maximum junction temperature	T_{jmax}	+150	℃	

*1 The voltage that can be applied reference to GND(Pin 10, 20, 31, 32, 39, 40)
*2 Do not, however exceed Pd and Tjmax=150℃.
*3 74.2mm×74.2mm×1.6mm FR4, 4-layer glass epoxy board (Top and bottom layer back copper foil size : 34.09mm^2, 2nd, 3rd layer back copper foil size:5505mm^2)
Derating in done at 34.3 mW/℃ for operating above Ta＝25℃. There are thermal via on the board.
*4 74.2mm×74.2mm×1.6mm F FR4, 4-layer glass epoxy board (Copper area 5505mm2)
Derating in done at 38.6 mW/℃ for operating above Ta＝25℃. There are thermal via on the board.
*5 It should use it below this ratings limit including the AC peak waveform (overshoot) for all conditions.
At only undershoot, it is admitted using at ≦10nse and ≦30V by the VCC reference. (Please refer following figure.)



●RecommendedOperating Ratings (Ta=25℃)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	V_{CC}	10 to 26	V	Pin 25, 26, 27, 45, 46 *1 *2
	V_{DD}	3.0 to 3.6		Pin 12 *1 *2
Minimum load impedance	R_L	3.6	Ω	Vcc≦18V, Stereo BTL mode *6
				Monaural Parallel BTL mode *6
		5.4	Ω	Vcc≦26V, Stereo BTL mode *6

*6 Do not, however exceed Pd.

●Electrical characteristics

(Unless otherwise specified Ta=25℃, Vcc=18V, V_{DD}=3.3V, fin=1kHz, R_L=8Ω, RSTX=3.3V, PDX=3.3V, MUTEX=3.3V
fs= 48kHz, GAIN=20dB, DSP : Through, Output LC filter : L=22μH, C=0.33μF, Cg=0.068μF)

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Total circuit						
Circuit current (Power down mode)	I_{CC1}	-	0.1	0.2	mA	Pin 25, 26, 27, 45, 46 No load RSTX=3.3V, PDX=0V, MUTEX=0V
	I_{DD1}	-	3.7	7.5		Pin 12, Noload RSTX=3.3V, PDX=0V, MUTEX=0V
Circuit current (mute mode)	I_{CC2}	-	7.0	25	mA	Pin 25, 26, 27, 45, 46 No load RSTX=3.3V, PDX=3.3V, MUTEX=0V
	I_{DD2}	-	25	70		Pin 12 Noload RSTX=3.3V, PDX=3.3V, MUTEX=0V
Circuit current (Normal mode)	I_{CC3}	-	50	80	mA	Pin 25, 26, 27, 45, 46 No load RSTX=3.3V, PDX=3.3V, MUTEX=3.3V
	I_{DD3}	-	30	70		Pin 12 Noload RSTX=3.3V, PDX=3.3V, MUTEX=3.3V
Regulator output voltage	V_{REG15}	1.3	1.5	1.7	V	Pin 14
	V_{REG5}	4.7	5.0	5.3		Pin 23
	V_{REGG}	4.7	5.0	5.3		Pin 24
ERROR WARNING terminal L level voltage	V_{ERR}	-	0.4	0.8	V	Pin 47, 48, I_O=0.1mA
H level input voltage	V_{IH}	V_{DD} x0.8	-	-	V	Pin 4 to 7, 13, 15, 21, 49 to 54
L level input voltage	V_{IL}	-	-	V_{DD} x0.2	V	Pin 4 to 7, 13, 15, 21, 49 to 54
Input current (Input pull-up terminal)	I_{IL}	50	100	150	μA	Pin 4 to 7, VIN = 0V
Input current(Input pull-down terminal)	I_{IH}	30	70	105	μA	Pin 49 to 51, 54, VIN = 3.3V
Input current(SCL, SDA terminal)	I_I	-	0	1	μA	Pin 52, 53, VIN = 3.3V
Input current (SCL, SDA terminal)	I_O	-1	0	-	μA	Pin 52, 53, VIN = 0V
Digital Audio Signal Output H level voltage 1	V_{OH1}	V_{DD} -0.5	-	V_{DD}	V	Pin 1 to 3,55,56, Io=1mA
PWM for Subwoofer Output H level voltage 2	V_{OH2}	V_{DD} -0.5	-	V_{DD}	V	Pin 16 to 19, Io=1mA
Digital Audio Signal Output L level voltage 1	V_{OL1}	0	-	0.5	V	Pin 1 to 3,55,56, Io=1mA
PWM for Subwoofer Output L level voltage 2	V_{OL2}	0	-	0.5	V	Pin 16 to 19, Io=1mA

Speaker output						
Maximum output	P_{O1}	-	10	-	W	Vcc=13V, THD+n=10%, Gain=20dB *7
	P_{O2}	-	20	-	W	Vcc=18V, THD+n=10%, Gain=22dB *7
	P_{O3}	-	25	-	W	Vcc=20.5V、THD+n=10%、Gain=23dB*7
Total harmonic distortion	THD	-	0.05	-	%	P_O=1W, BW=20 to 20kHz *7
Crosstalk	CT	60	80	-	dB	P_O=1W, BW=IHF-A *7
PSRR	PSRR	-	70	-	dB	Vripple=1Vrms, f=1KHz *7
Output noise voltage	V_{NO}	-	80	140	μVrms	-∞dBFS, BW=IHF-A *7
PWM sampling frequency	f_{PWM1}	-	384	-	KHz	fs=8kHz, 16kHz, 32kHz *7
	f_{PWM2}	-	352.8	-		fs=11.025kHz, 22.05kHz, 44.1kHz, 88.2kHz *7
	f_{PWM3}	-	384	-		fs=12kHz, 24kHz, 48kHz, 96kHz *7

*7 These items show the typical performance of device and depend on board layout, parts, and power supply.
The standard value is in mounting device and parts on surface of ROHM's board directly.

●Typical Performance Curves

(Ta=25℃,Vcc=18V,V_{DD}=3.3V,fin=1kHz,R_L=8Ω,RSTX=3.3V,PDX=3.3V,MUTEX=3.3V,fs= 48kHz,GAIN=23dB,DSP through)
Measured by ROHM designed 4-layer board.

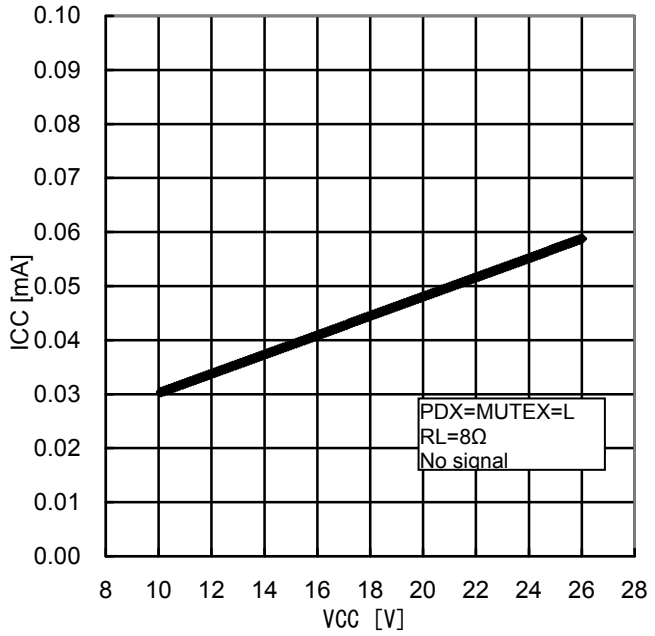


Figure 3.
. Power supply – Current consumption

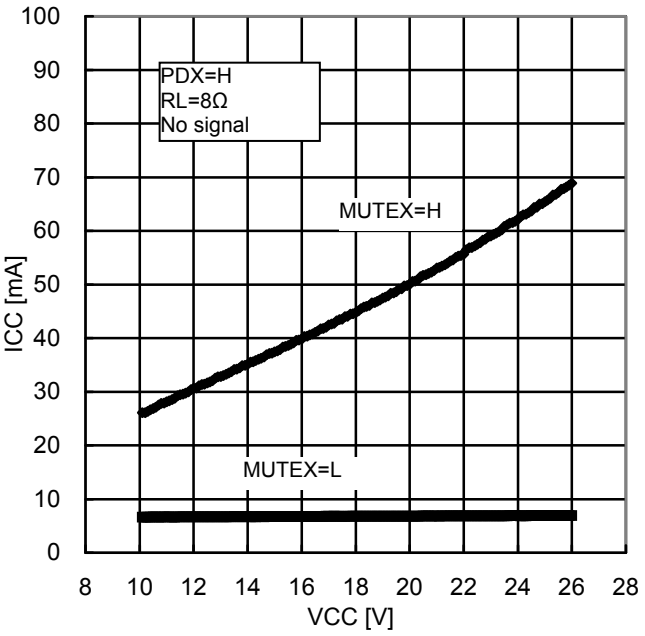


Figure 4.
. Power supply – Current consumption

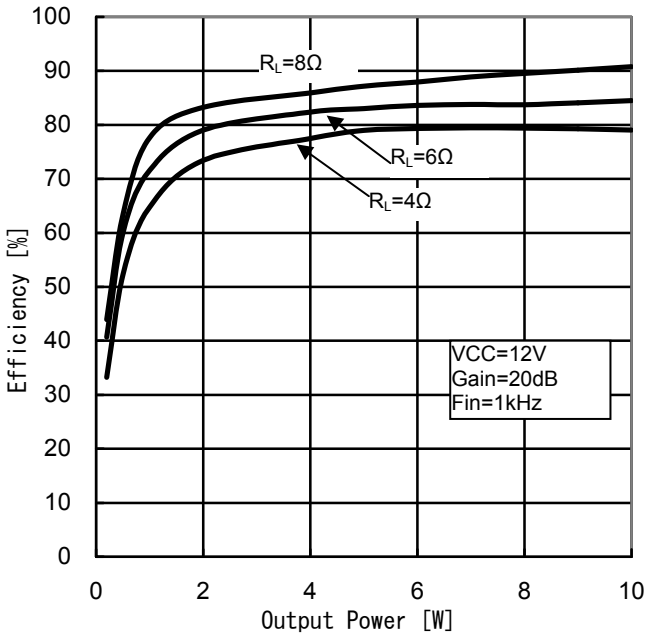


Figure 5.
. Output power – Efficiency

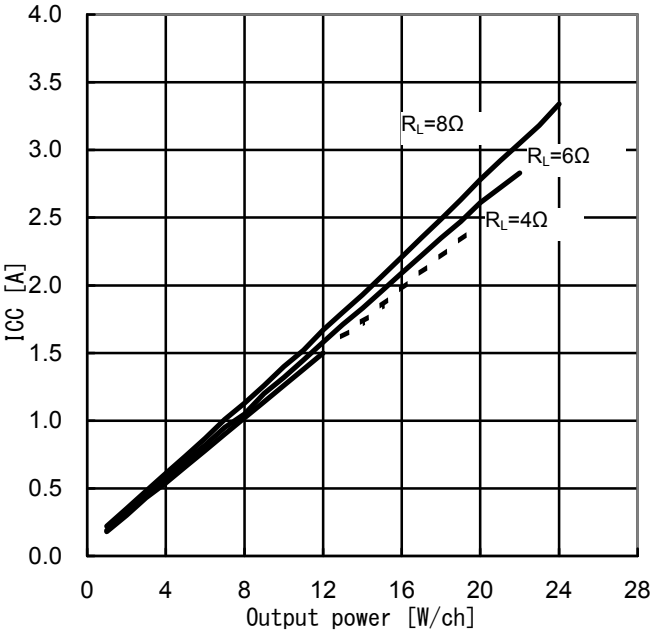


Figure 6.
. Output power – Current consumption

Continued on next page.

※Dotted line means internal dissipation is over package power.

●Typical Performance Curves (Continuation on previous page)

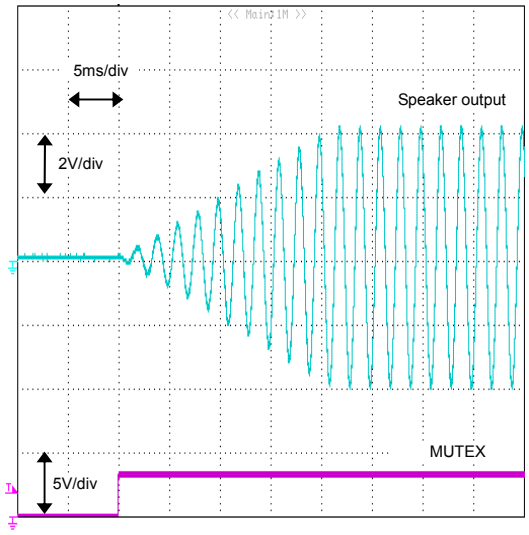


Figure 7.
Waveform at smooth start

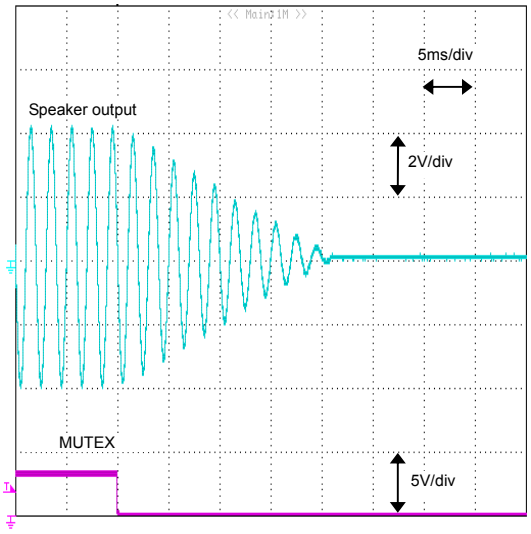


Figure 8.
Waveform at smooth mute

●Typical Performance Curves

(Ta=25℃,Vcc=18V,V_{DD}=3.3V,fin=1kHz,R_L=8Ω,RSTX=3.3V,PDX=3.3V,MUTEX=3.3V,fs= 48kHz,GAIN=23dB,DSP through)
Measured by ROHM designed 4 layer board.

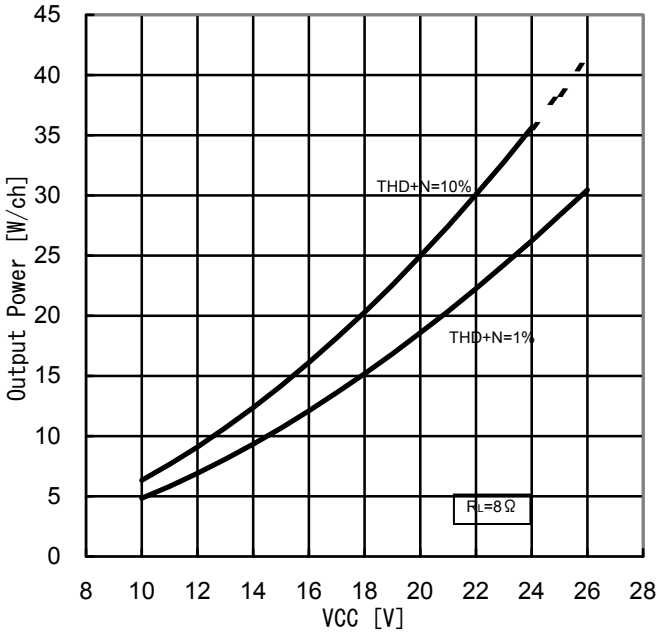


Figure 9.
Output voltage - Power voltage (R_L=8Ω).

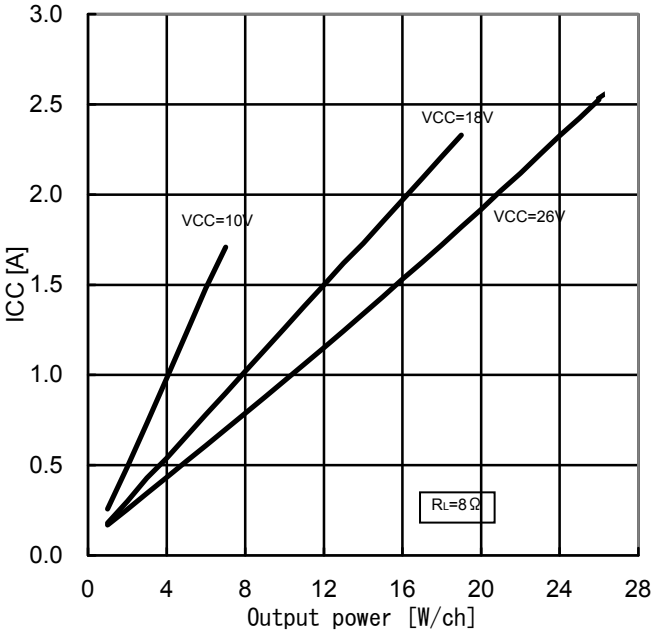


Figure 10.
Output power – Current consumption (R_L=8Ω)

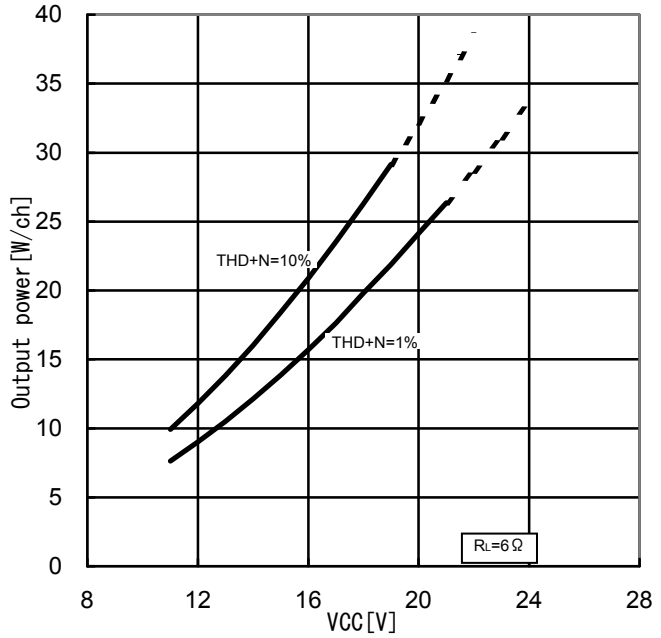


Figure 11.
Output voltage - Power voltage (R_L=6Ω).

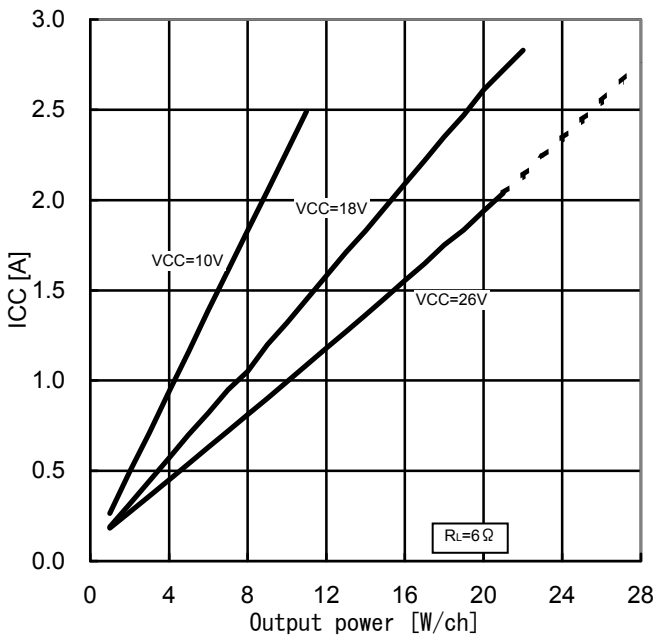


Figure 12.
Output power – Current consumption (R_L=6Ω)

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※Dotted line means internal dissipation is over package power.

●Typical Performance Curves (Continuation on previous page)

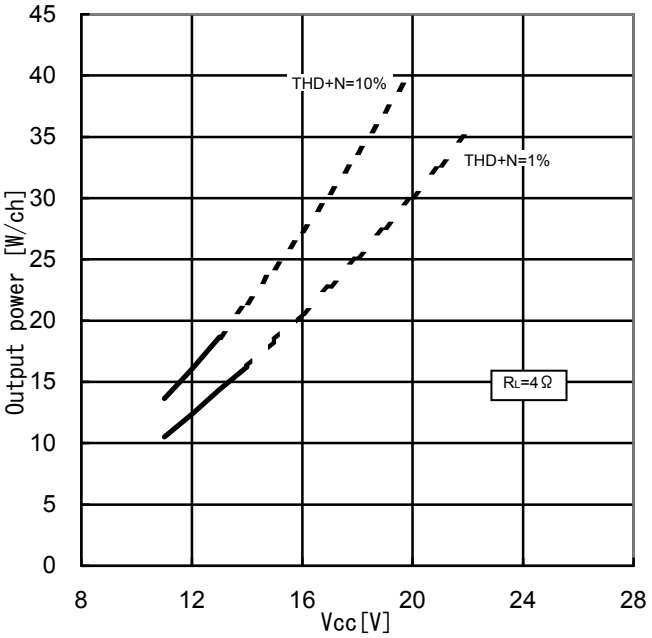

Figure 13.
Output voltage - Power voltage (R_L=4Ω).

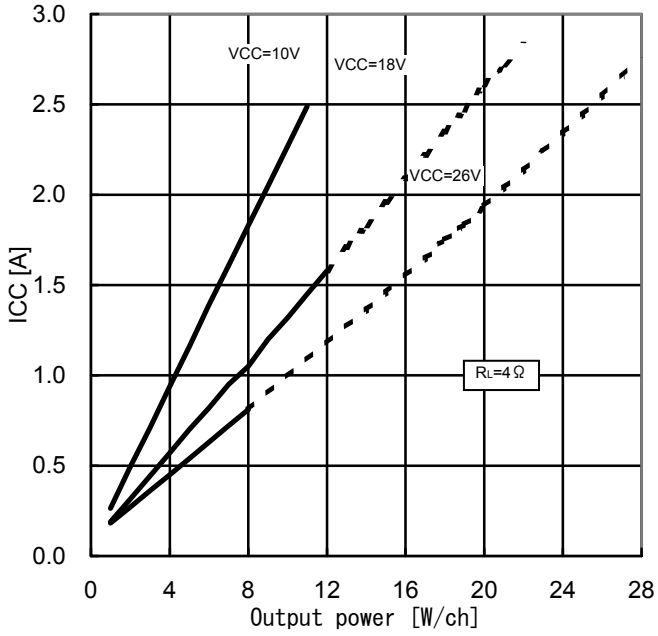

Figure 14.
Output power – Current consumption(R_L=4Ω)

●Typical Performance Curves
(Ta=25℃ ,Vcc=18V,V_{DD}=3.3V,fin=1kHz,R_L=4Ω,RSTX=3.3V,PDX=3.3V,MUTEX=3.3V,fs= 48kHz,GAIN=20dB,DSP through, Output LCfilter:L=10uH,C=0.68uF,Cg=0.15uF, Monaural Parallel BTL mode)
Measured by ROHM designed 4-layer board.

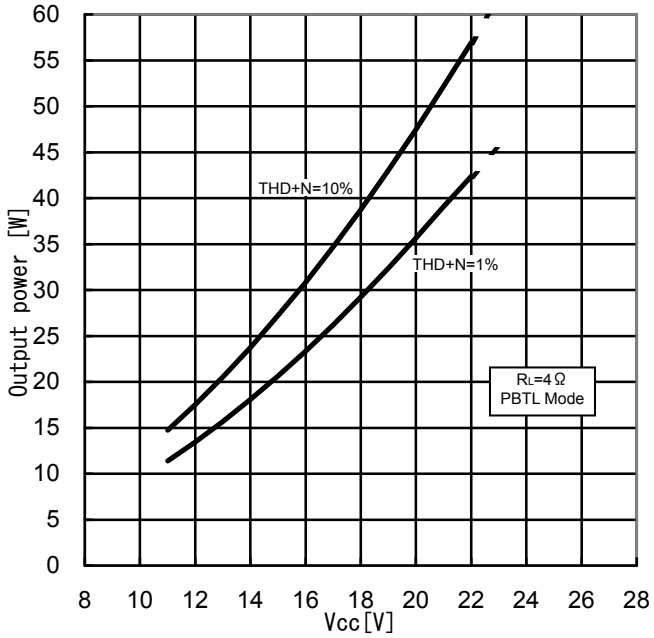

Figure 15.
Output voltage - Power voltage (R_L=4Ω, Monaural Parallel BTL mode)

※Dotted line means internal dissipation is over package power.

●Typical Performance Curves

(Ta=25℃,Vcc=18V,V_{DD}=3.3V,fin=1kHz,R_L=8Ω,RSTX=3.3V,PDX=3.3V,MUTEX=3.3V,fs= 48kHz,GAIN=20dB,DSP through, Output LCfilter:L=22uH,C=0.33uF,Cg=0.068uF)

Measured by ROHM designed 4-layer board.

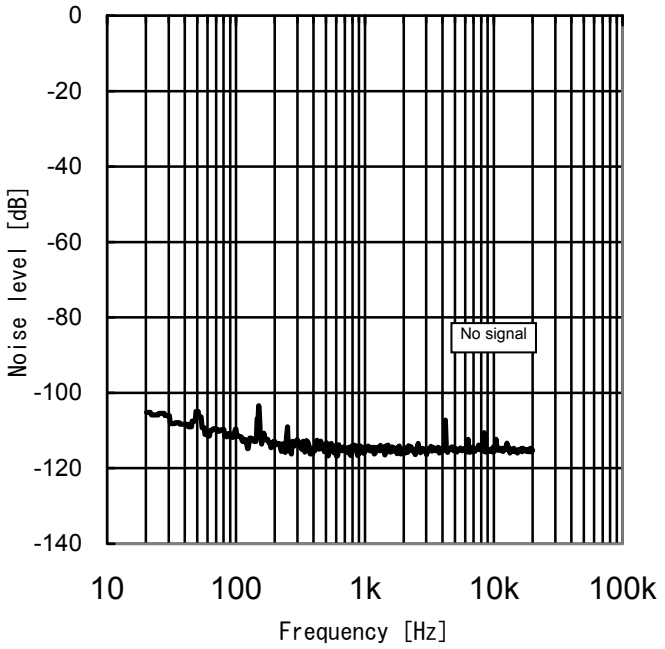

Figure 16.
FFT of output noise voltage (R_L=8Ω)

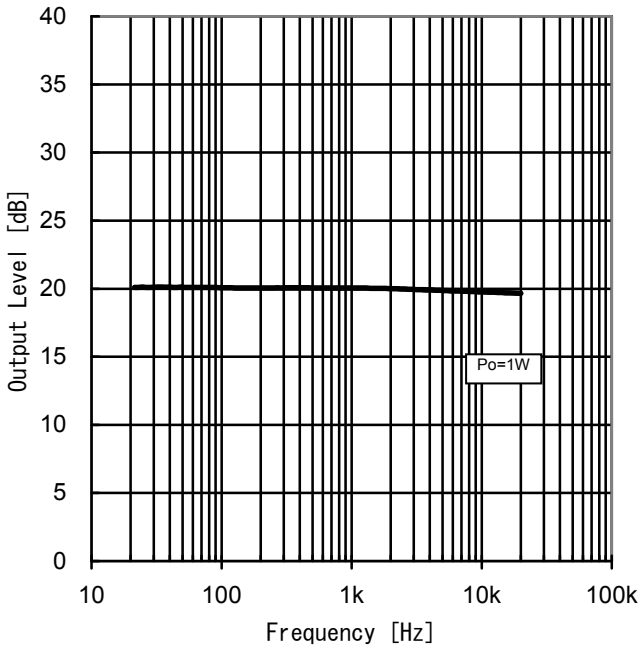

Figure 17.
Frequency – Output power (R_L=8Ω)

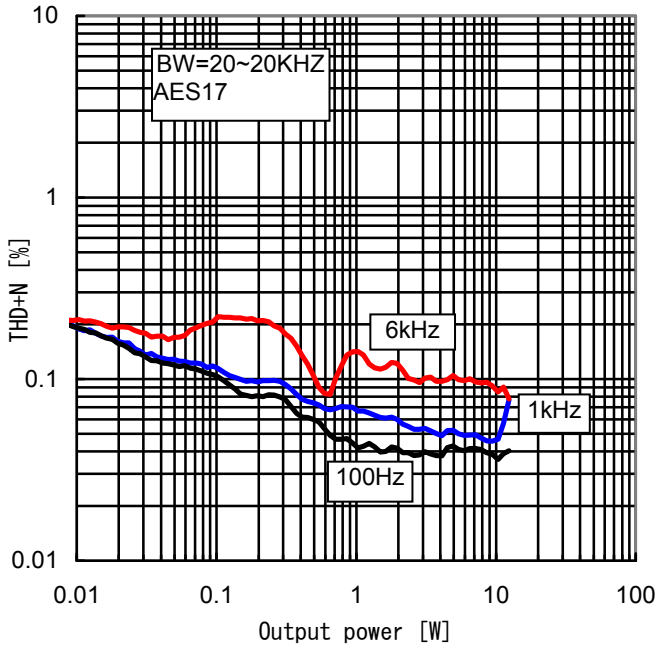

Figure 18.
Output power – THD+N (R_L=8Ω)

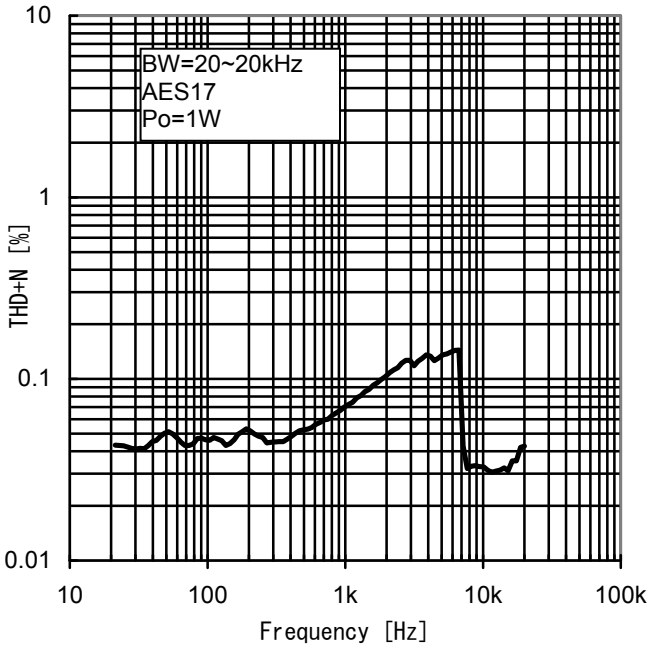

Figure 19.
Frequency – THD+N (R_L=8Ω)

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●Typical Performance Curves (Continuation on previous page)

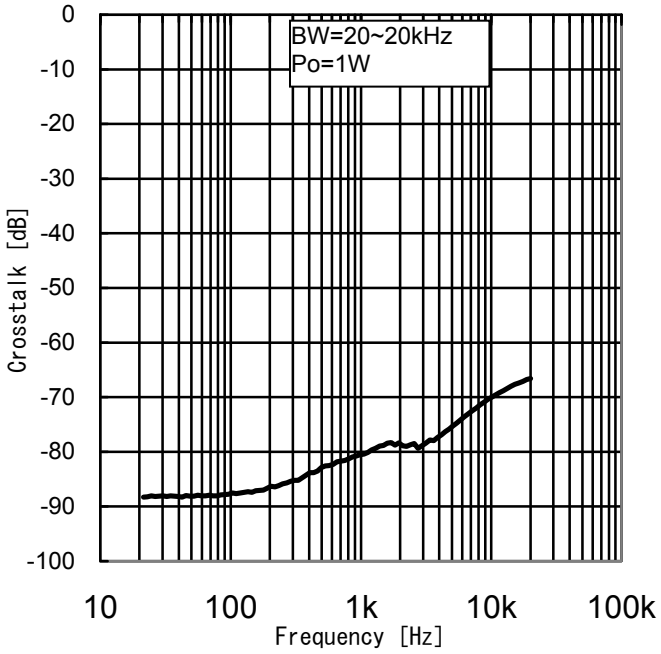

Figure 20.
Frequency – Crosstalk (R_L=8Ω)

●Typical Performance Curves

(Ta=25℃,Vcc=18V,V_{DD}=3.3V,fin=1kHz,R_L=6Ω,RSTX=3.3V,PDX=3.3V,MUTEX=3.3V,fs= 48kHz,GAIN=20dB,DSP through, Output LCfilter:L=15uH,C=0.47uF,Cg=0.1uF)
Measured by ROHM designed 4-layer board.

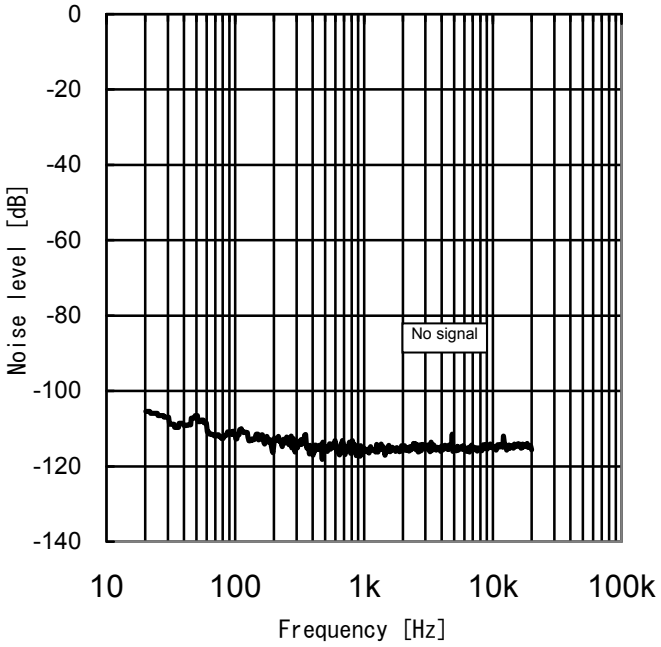

Figure 21.
FFT of output noise voltage (R_L=6Ω)

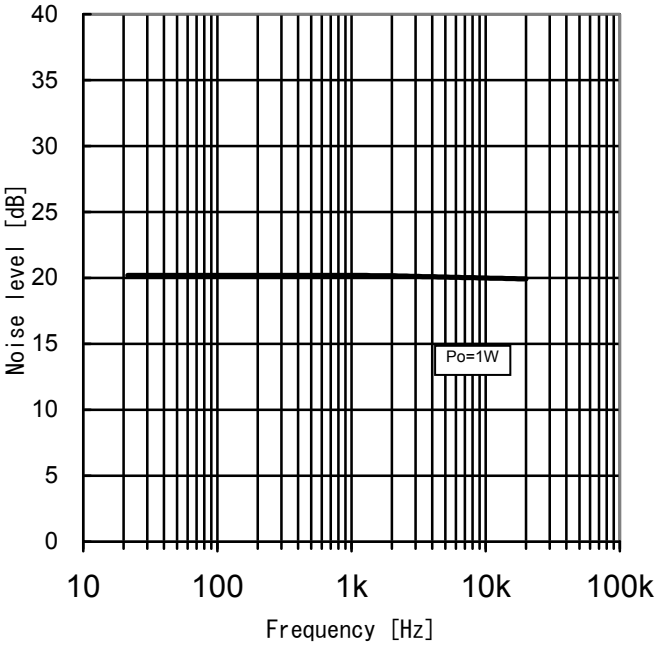

Figure 22.
Frequency – Output power (R_L=6Ω)

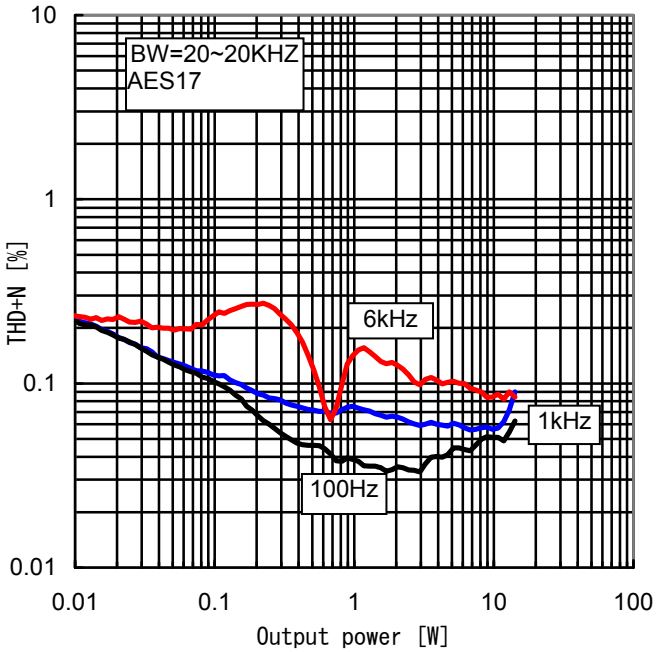

Figure 23.
Output power – THD+N (R_L=6Ω)

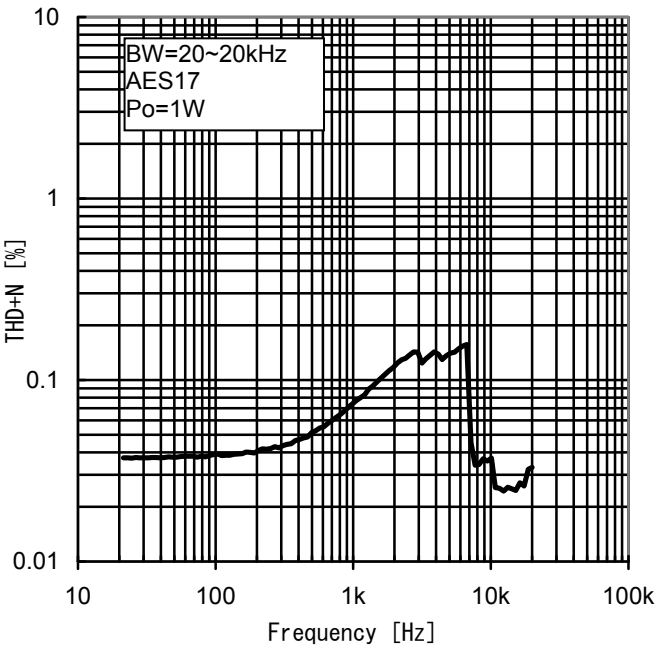

Figure 24.
Frequency – THD+N (R_L=6Ω)

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●Typical Performance Curves (Continuation on previous page)

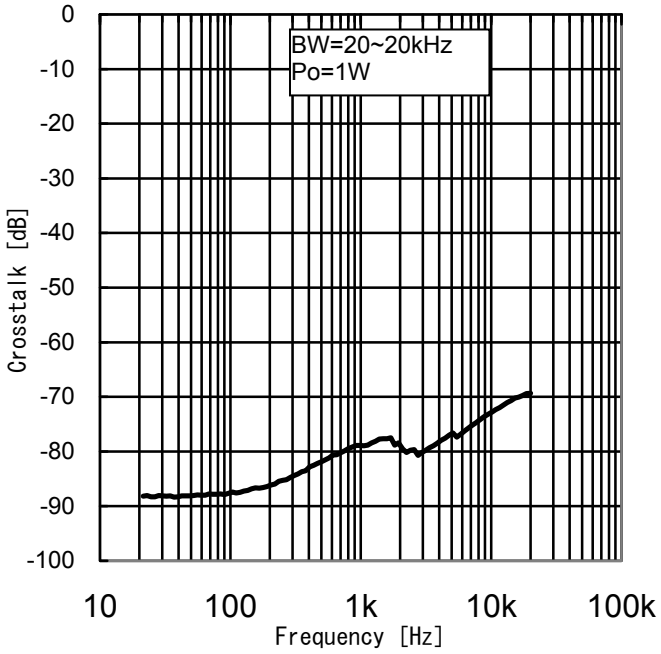


Figure 25.
Frequency – Crosstalk (R_L=6Ω)

●Typical Performance Curves

(Ta=25℃,Vcc=18V,V_{DD}=3.3V,fin=1kHz,R_L=4Ω,RSTX=3.3V,PDX=3.3V,MUTEX=3.3V,fs= 48kHz,GAIN=20dB,DSP through, Output LCfilter:L=10uH,C=0.68uF,Cg=0.15uF)
Measured by ROHM designed 4-layer board.

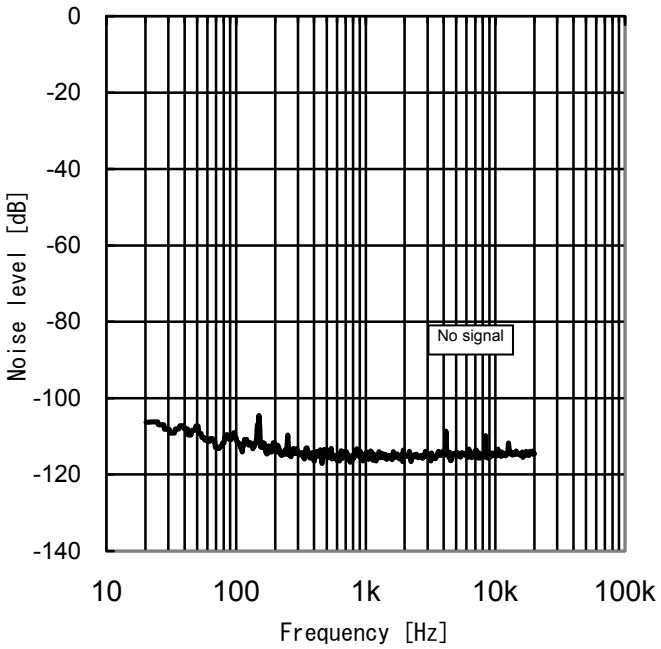


Figure 26.
FFT of output noise voltage (R_L=4Ω)

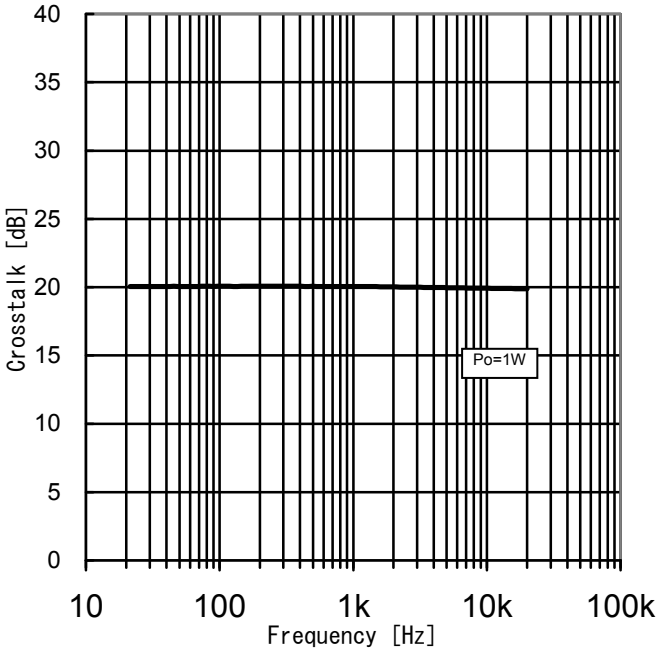


Figure 27.
Frequency – Output power (R_L=4Ω)

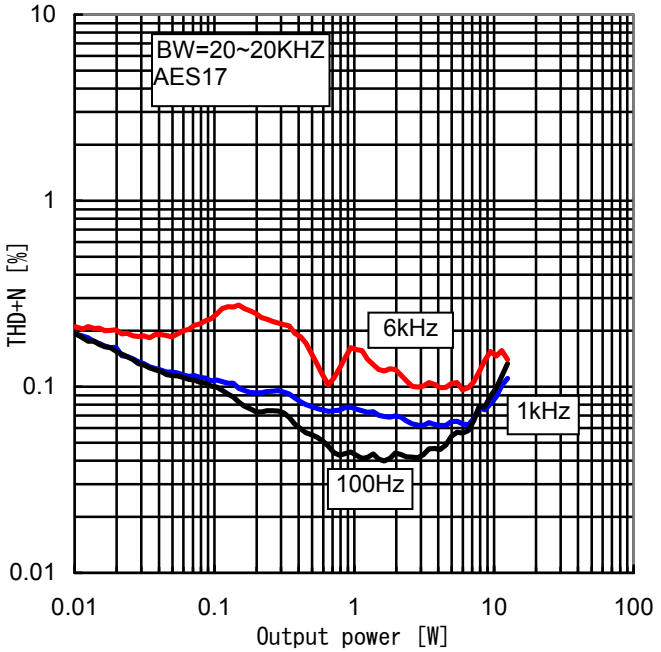


Figure 28.
Output power – THD+N (R_L=4Ω)

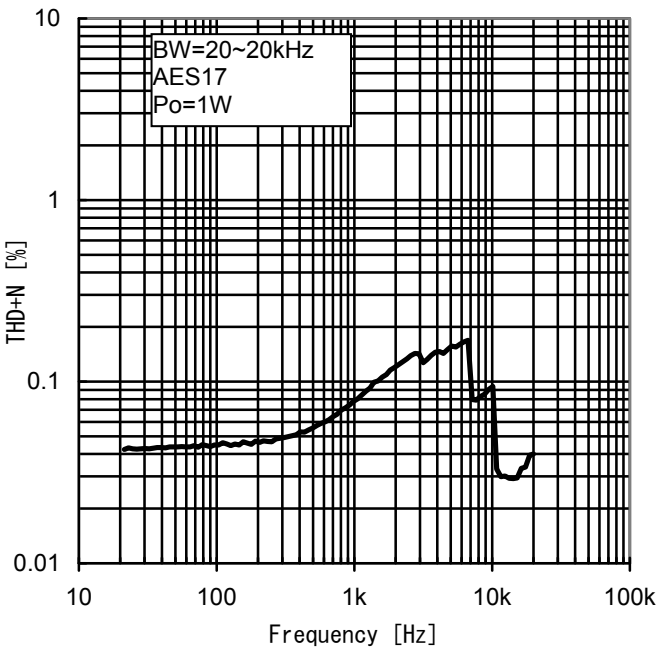


Figure 29.
Frequency – THD+N (R_L=4Ω)

Continued on next page.

●Typical Performance Curves (Continuation on previous page)

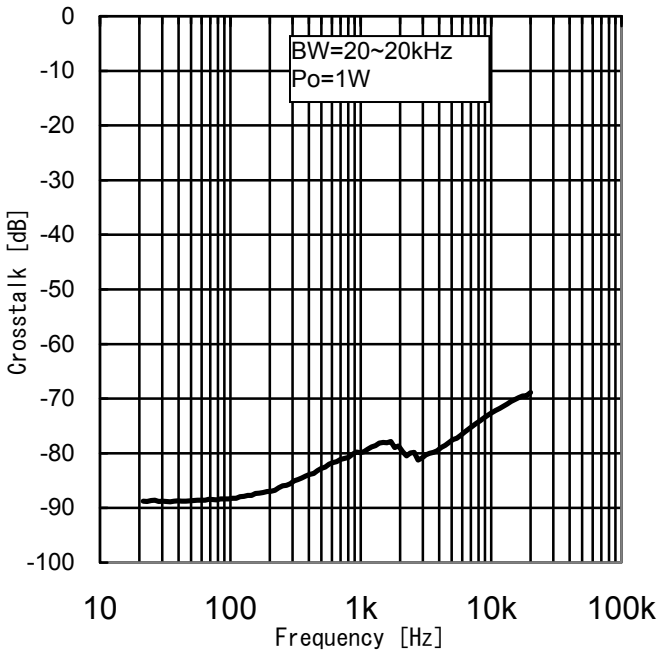


Figure 30.
Frequency – Crosstalk (R_L=4Ω)

●About external setting pin

(1) RSTX pin, PDX pin, MUTEX pin function

RSTX (51pin)	PDX (50pin)	MUTEX (49pin)	Normal state		
			PWM output (OUT1P, 1N, 2P, 2N)	ERROR output	WARNING output
L	L or H	L or H	HiZ_L (Power down mode)	H	H
H	L	L or H	HiZ_L (Power down mode)	H	H
H	H	L	HiZ_L (MUTE ON)	H	H
H	H	H	Normal (MUTE OFF)	H	H

RSTX (51pin)	PDX (50pin)	MUTEX (49pin)	ERROR detection		
			PWM output (OUT1P, 1N, 2P, 2N)	ERROR output	WARNING output
L	L or H	L or H	HiZ_L (Power down mode)	H	H
H	L	L or H	HiZ_L (Power down mode)	H	H
H	H	L	HiZ_L (MUTE ON)	H	H
H	H	H	HiZ_L (Latch)	L	H

RSTX (51pin)	PDX (50pin)	MUTEX (49pin)	WARNING detection		
			PWM output (OUT1P, 1N, 2P, 2N)	ERROR output	WARNING output
L	L or H	L or H	HiZ_L (Power down mode)	H	H
H	L	L or H	HiZ_L (Power down mode)	H	H
H	H	L	HiZ_L (MUTE ON)	H	H
H	H	H	HiZ_L	H	L

* RSTX, PDX and MUTEX pin are set Low, internal registers are initialized.

(2) ADDR pin function

ADDR (54pin)	I^2C BUS Slave address
L	80(hex)
H	82(hex)

* ADDR pin is set to low level, internal resisters are initialized

(3) GAIN pin function

GAIN2 (48pin)	GAIN1 (47pin)	Speaker output setting gain	Speaker output limitation power (*1)
L	L	13.7dB	3.3W (THD+n=1%)
L	H	18.9dB	11.0W(THD+n=1%)
H	L	15.9dB	5.5W (THD+n=1%)
H	H	20.7dB	16.5W (THD+n=1%)

*1: It provides for the limitation power in the speaker output by the speaker maximum output when RL=8Ω, DSP=0dB, 0dBFS corresponding is input. Please set it according to the speaker used. 18dB, 20dB, 22dB, and 23dB can be set by the command besides the above-mentioned, set gain.

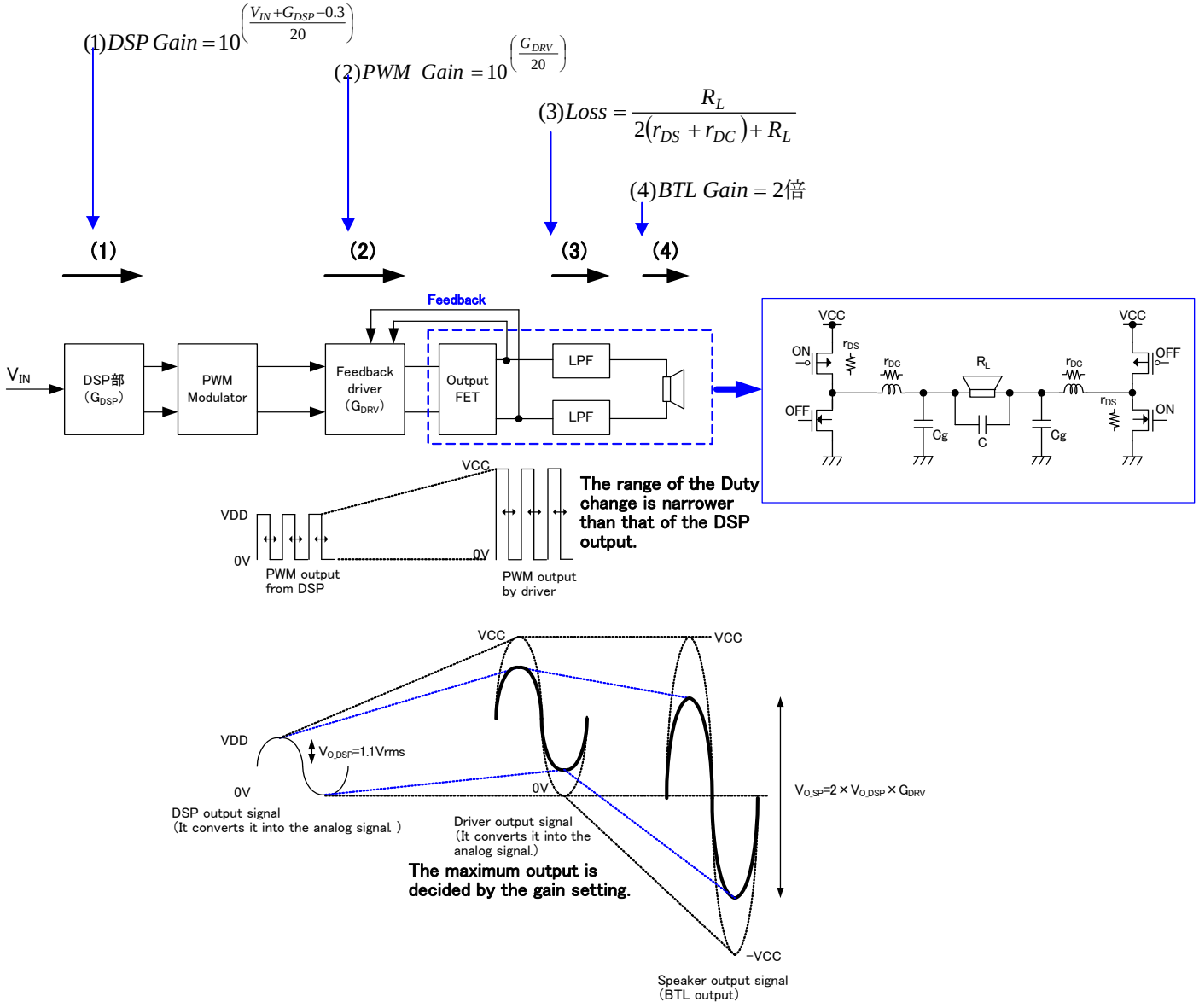
(4) Level diagram

$$(1)DSP\ Gain = 10^{\left(\frac{V_{IN}+G_{DSP}-0.3}{20}\right)}$$

$$(2)PWM\ \ Gain = 10^{\left(\frac{G_{DRV}}{20}\right)}$$

$$(3)Loss = \frac{R_L}{2(r_{DS}+r_{DC})+R_L}$$

$$(4)BTL\ Gain = 2倍$$



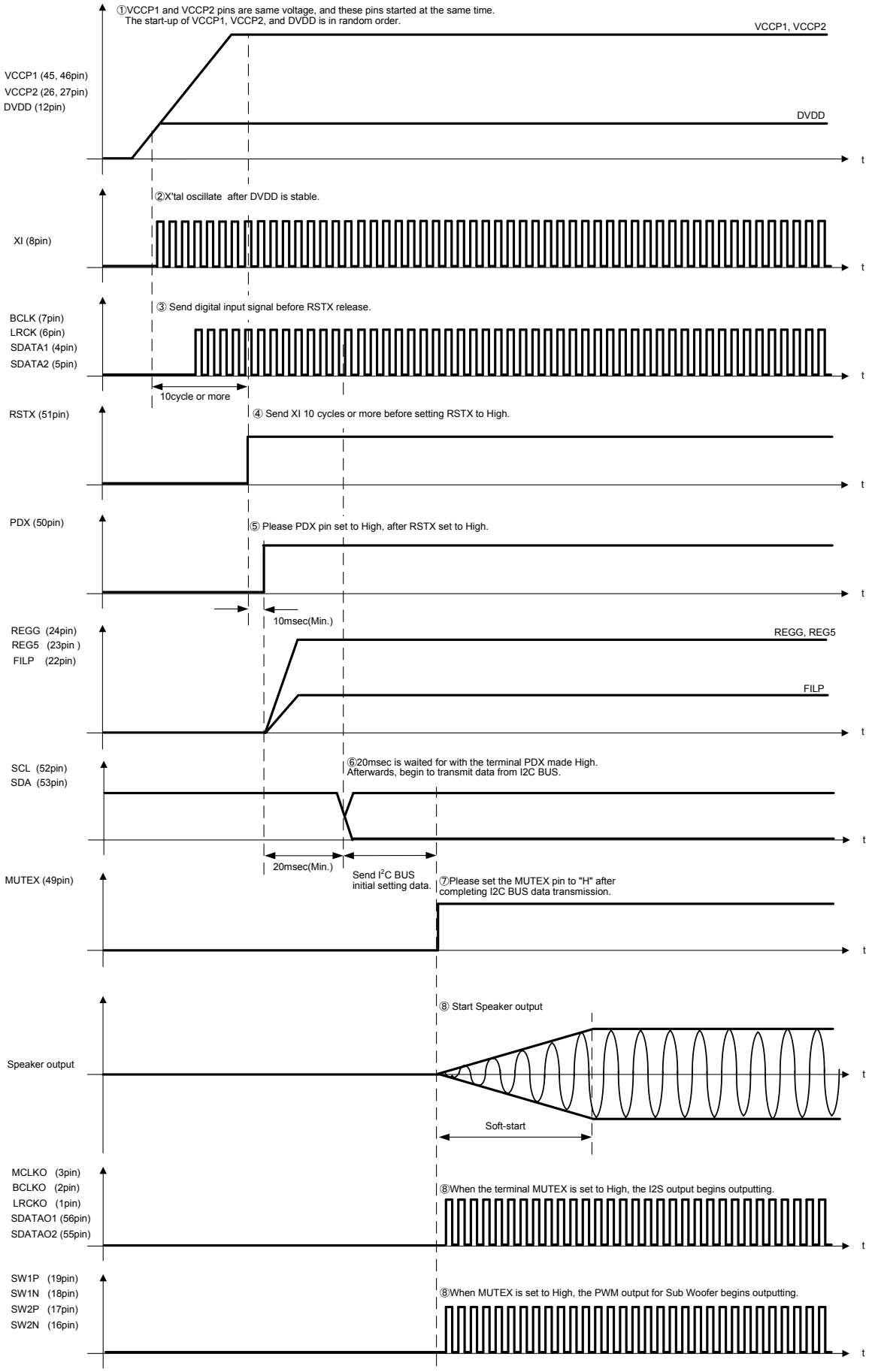
$$V_{O\_DSP} = \frac{VDD}{2\sqrt{2}}\left(10^{\frac{V_{IN}+G_{DSP}-0.3}{20}}\right) \quad [\text{Vrms}]$$

$$V_{O\_SP} = V_{O\_DSP} \times 10^{\left(\frac{G_{DRV}}{20}\right)} \times \frac{R_L}{2(r_{DS}+r_{DC})+R_L} \times 2 \quad [\text{Vrms}]$$

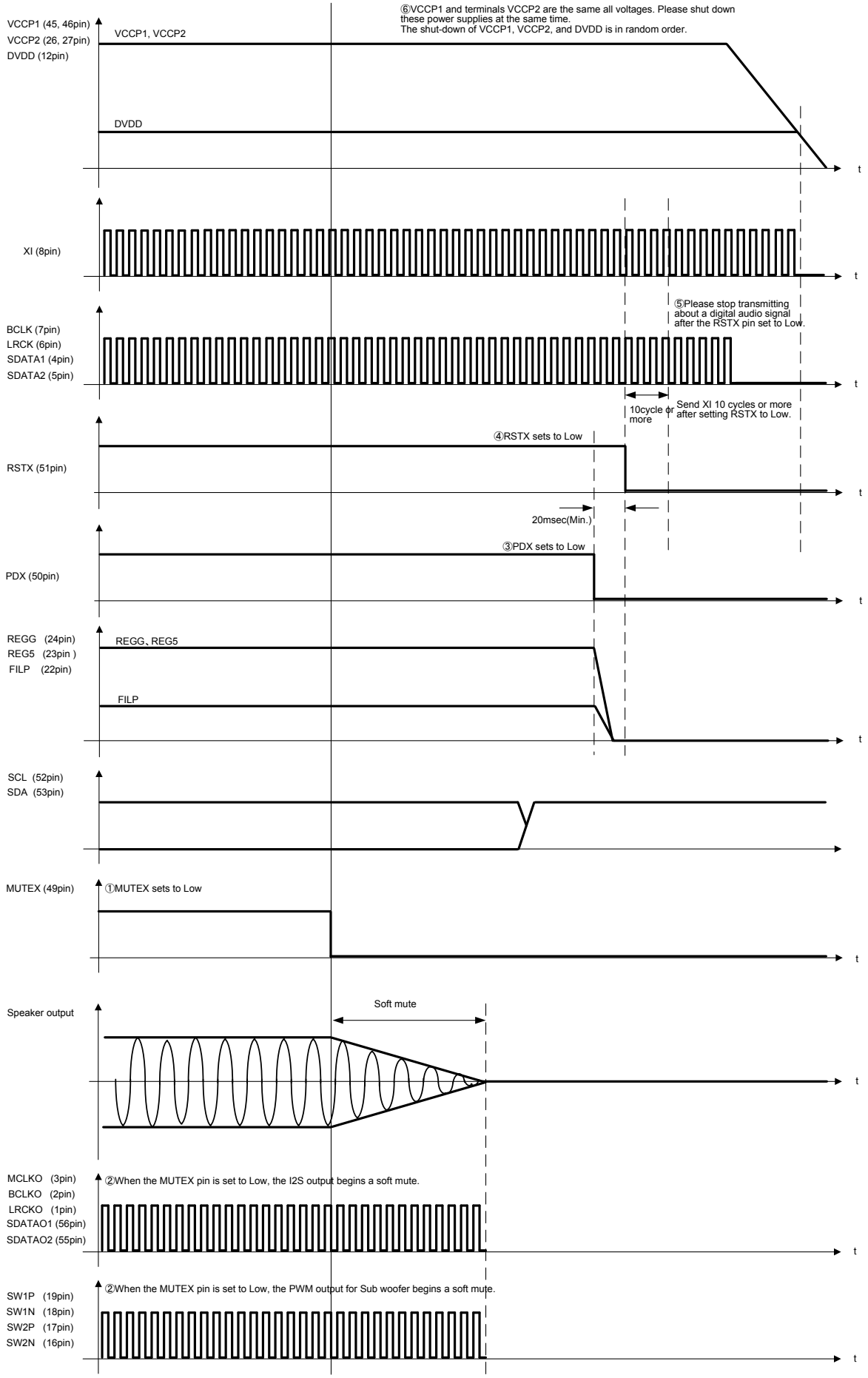
$$P_{O(THD=1\%)} = \frac{\left[\frac{VDD}{2\sqrt{2}}\left(10^{\frac{V_{IN}+G_{DSP}-0.3}{20}}\right) \times 10^{\left(\frac{G_{DRV}}{20}\right)} \times \frac{R_L}{2(r_{DS}+r_{DC})+R_L}[\text{W}] \times 2\right]^2}{R_L}$$

V_{IN} : I^2S input level [dBFS]
G_{DSP} : DSP gain [dB]
G_{DRV} : Feedback driver gain [dB]
VCC : Power supply for power amp [V]
VDD : Power supply for DSP [V]
R_L : Speaker load resistance [Ω]
r_{DS} : Output FET resistance[Ω] (TYP = 0.16Ω)
r_{DC} : Direct current resistance of coil [Ω]

●Power supply start-up sequence



●Power supply start-up sequence



●About the protection function

Protection function	Detecting & Releasing condition		Speaker PWM output	ERROR flag output	WARNING flag output
Output short protection	Detecting condition	Detecting current = 10A (TYP.)	HiZ_Low (Latch)	L	H
DC voltage protection	Detecting condition	Speaker PWM output fixes 40msec or more by Duty=0% or 100%.	HiZ_Low (Latch)	L	H
High temperature protection	Detecting condition	Chip temperature to be over 150℃ (TYP.)	HiZ_Low (Auto return)	H	L
	Releasing condition	Chip temperature to be under 120℃ (TYP.)	Normal		H
Under voltage protection	Detecting condition	Power supply voltage to be below 8V (TYP.)	HiZ_Low (Auto return)	H	L
	Releasing condition	Power supply voltage to be above 9V (TYP.)	Normal		H
Over voltage protection	Detecting condition	Power supply voltage to be above 29V (TYP.)	HiZ_Low (Auto return)	H	L
	Releasing condition	Power supply voltage to be below 28V (TYP.)	Normal		H
Clock stop protection	Detecting condition	BCLK or LRCK stops 100μsec (default) or more stops.	HiZ_Low (Auto return)	H	L
	Releasing condition	BCLK and LRCK normal input it.	Normal		H

* It doesn't return automatically even if abnormal state is released when becoming a latch state. It is possible to release it by the method of the following ①or②.
  ①After the terminal MUTEX is made Low (10 time maintained in Low = msec(Min.)) once, it returns it to High again.
  ②Please reenter the power supply after it drops to power-supply voltage Vcc<3V that the internal power-on reset circuit operates (10msec(Min.) maintenance).
* GAIN1 and GAIN2 pin can respectively be changed to the WARNING flag output pin and the ERROR flag output pin by the command.
* The stop detection time of BCLK and LRCK can respectively be changed with &h09 and &h08.

●Output selection of Stereo or Monaural on Main side.
Main side output can be set to stereo or monaural output. Initial value is set to “stereo output”.

Default = 0h

Select Address	Value	Explanation of operation	R/W
&hF0 [7]	0	Stereo output on main side. (Normal BTL Output)	R/W
	1	Monaural output on main side. (Parallel BTL Output)	

Please refer to the item of “Change of GAIN1 and GAIN2 pin “for other bits.

Default = 01h

Select Address	Value	Explanation of operation	R/W
&hF1 [7]	0	Reserved. (This bit should be set to “0”)	R/W
&hF1 [6]	0	Stereo output on main side. (Normal BTL Output)	R/W
	1	Monaural output on main side. (Parallel BT Output)	
&hF1 [5:3]	0	Reserved. (This bit should be set to “0”)	R/W
&hF1 [2:0]	1	Transmit address	R

After it sets it as follows, Channel Mixer 2 is set to set it to monaural.
(1) Write 1h to &hF0 [7] register.
(2) Write 41h to &hF1 [7:0] register.
(3) Write 01h to &hF8 [7:0] register.

When the Main side is output by the monaural output, the output of the DSP side is set to the monaural output with Channel Mixer 2. The example of setting that time is as follows.

(1) When you use L ch as a monaural output
&h26 = 19h : L out set to L in, R out set to inverse L in.

(2) When you use R ch as a monaural output
&h26 = 2Ah : L out set to R in, R out set to inverse R in.

(3) When you use L ch as a monaural output
&h26 = 3Bh : L out set to (Lch + Rch)/2, R out set to inverse (Lch + Rch)/2.

*Changing the stereo or monaural should be done after MUTEX terminal set to “L”.

Please refer to "4-11. The channel setting with the phase reversing function" for details of Channel Mixer 2.

●Output selection of Stereo or Monaural on Sub side.
The output of the Sub side can be set to the stereo or monaural as well as the Main side. An initial value is a stereo output.
If the Sub side is monaural output, it should be set to monaural output by Channel Mixer 3 of the DSP.
The example of setting that time is as follows.

(1) When you use L ch as a monaural output
&h27 = 19h : L out set to L in, R out set to inverse L in.

(2) When you use R ch as a monaural output
&h27 = 2Ah : L out set to R in, R out set to inverse R in.

(3) When you use L ch as a monaural output
&h27 = 3Bh : L out set to (Lch + Rch)/2, R out set to inverse (Lch + Rch)/2

*Changing the stereo or monaural should be done after MUTEX terminal set to “L”.

Please refer to "4-11. The channel setting with the phase reversing function" for details of Channel Mixer 3.

●Change of GAIN1 and GAIN2 pin

After address &hF0 [3] is set to 1, it is necessary to set to 1 in &hF8 [0] to change the terminal GAIN1 and the terminal GAIN2 to the WARNING flag output and the ERROR flag output terminal respectively.

Moreover, the gain value can be changed by writing 1 in &hF8 [0] after the speaker output setting gain value also similarly sets the gain value to &hF0 [6:4]. Please set &hF0 [3] to 1 when you set the gain by this command.

Restrictions on output power supply for 3W speaker

Default=00h

Select Address	Value	Explanation of operation	R/W
&hF0 [6 : 4]	0	13.7dB (Output power limitter for 3W speaker)	R/W
	1	19.0dB (Output power limitter for 10W speaker)	
	2	15.9dB (Output power limitter for 5W speaker)	
	3	20.7dB (Output power limitter for 15W speaker)	
	4	18.0dB	
	5	20.0dB	
	6	22.0dB	
	7	23.0dB	
&hF0 [3]	0	Gain setting by external pin	R/W
	1	Output flag setting for WARNING/ERROR	
&hF0 [2:0]	0	Transmit address	R

Default=0h

Select Address	Value	Explanation of operation	R/W
&hF8 [1]	0	Force stop transmission invalid	R/W
	1	Force stop transmission valid	
&hF8 [0]	0	Stop transmission	R/W
	1	Start transmission (This bit is cleared 0 by automatically)	

*The address from &hF1 to &hF7 is register for LSI test. Please don't access these register.

●Reading of ERROR and WARNING flag with I^2C

It is also possible to read it through I^2C I/F though WARNING and the ERROR flag can be output to the terminal GAIN1 and the terminal GAIN2 respectively. The reading address is as follows.

Select Address	Value	Explanation of operation	R/W
&hE8 [7]	0	ERROR state	R
	1	Normal	
&hE8 [6]	0	WARNING state	R
	1	Normal	

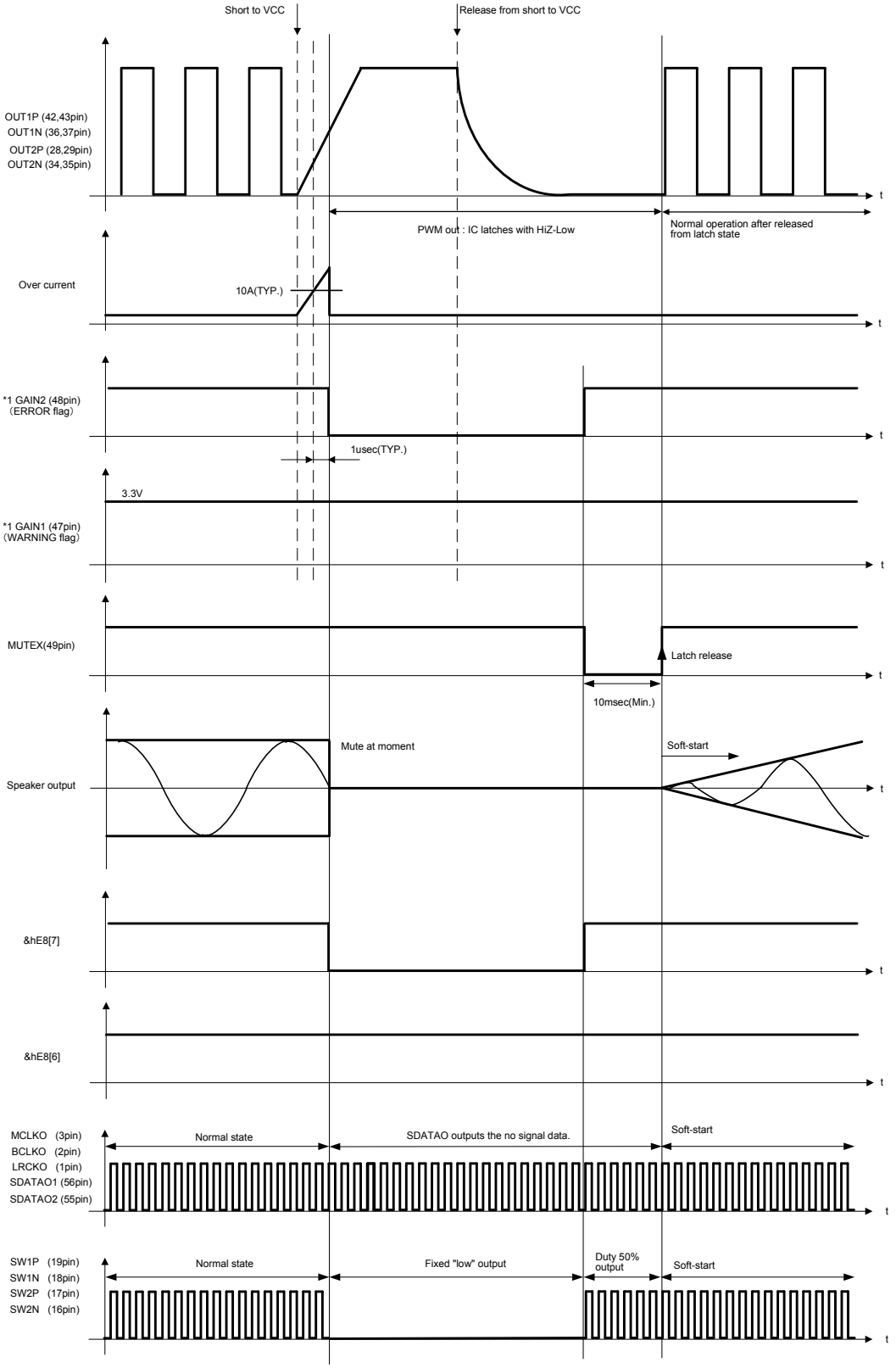
●Output short protection (Short to the power supply)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output pin becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After MUTEX pin is set Low once over the soft mute transition time(Min.:10msec), MUTEX pin is returned to High again.

②Turning on the power supply again (Vcc<3V, 10ms(min)).



(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

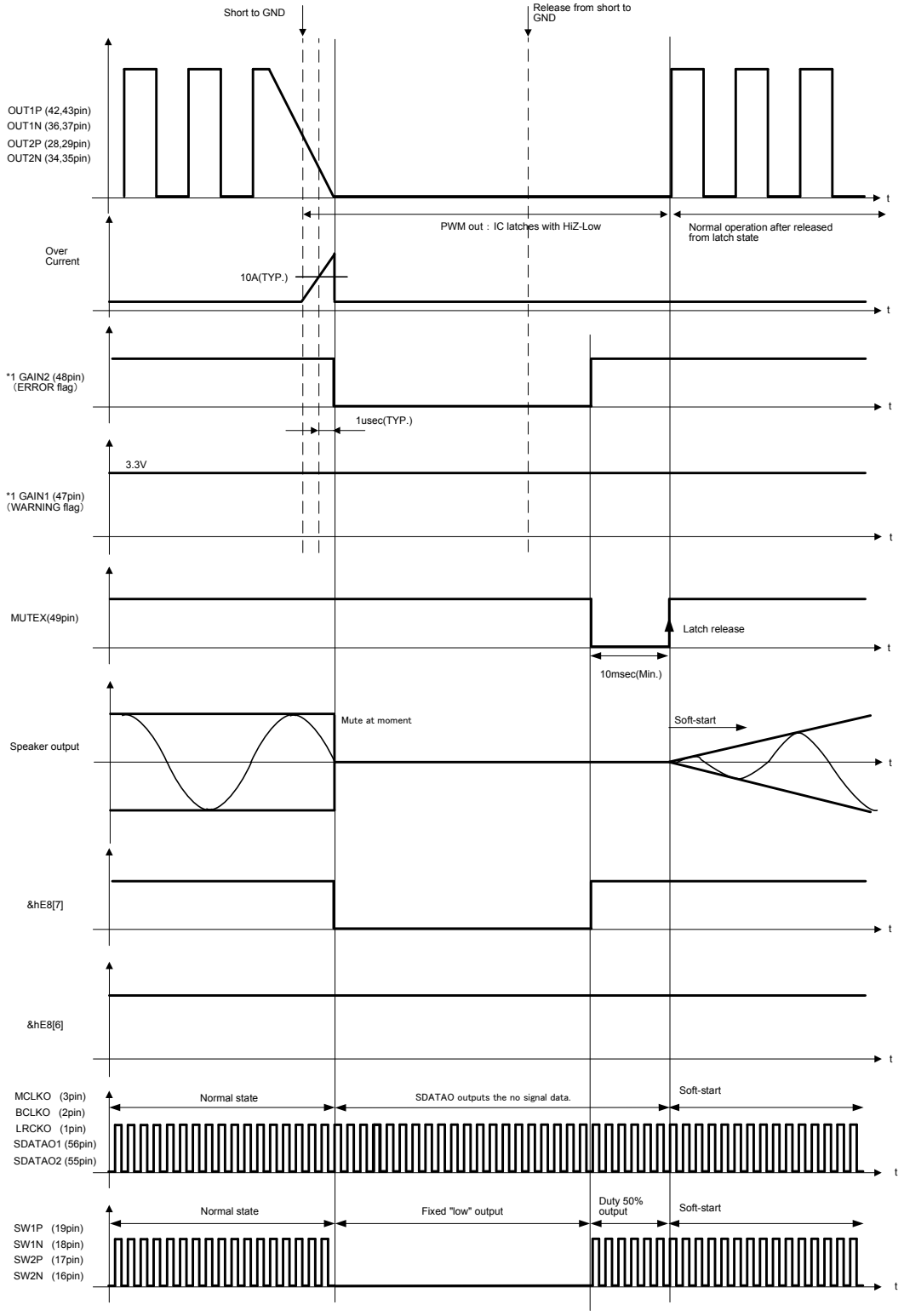
●Output short protection (Short to GND)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output terminal becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method – ①After MUTEX pin is set Low once over the soft mute transition time(10msec(Min.)), MUTEX pin is returned to High again.

②Turning on the power supply again (Vcc<3V, 10msec(Min.))



(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

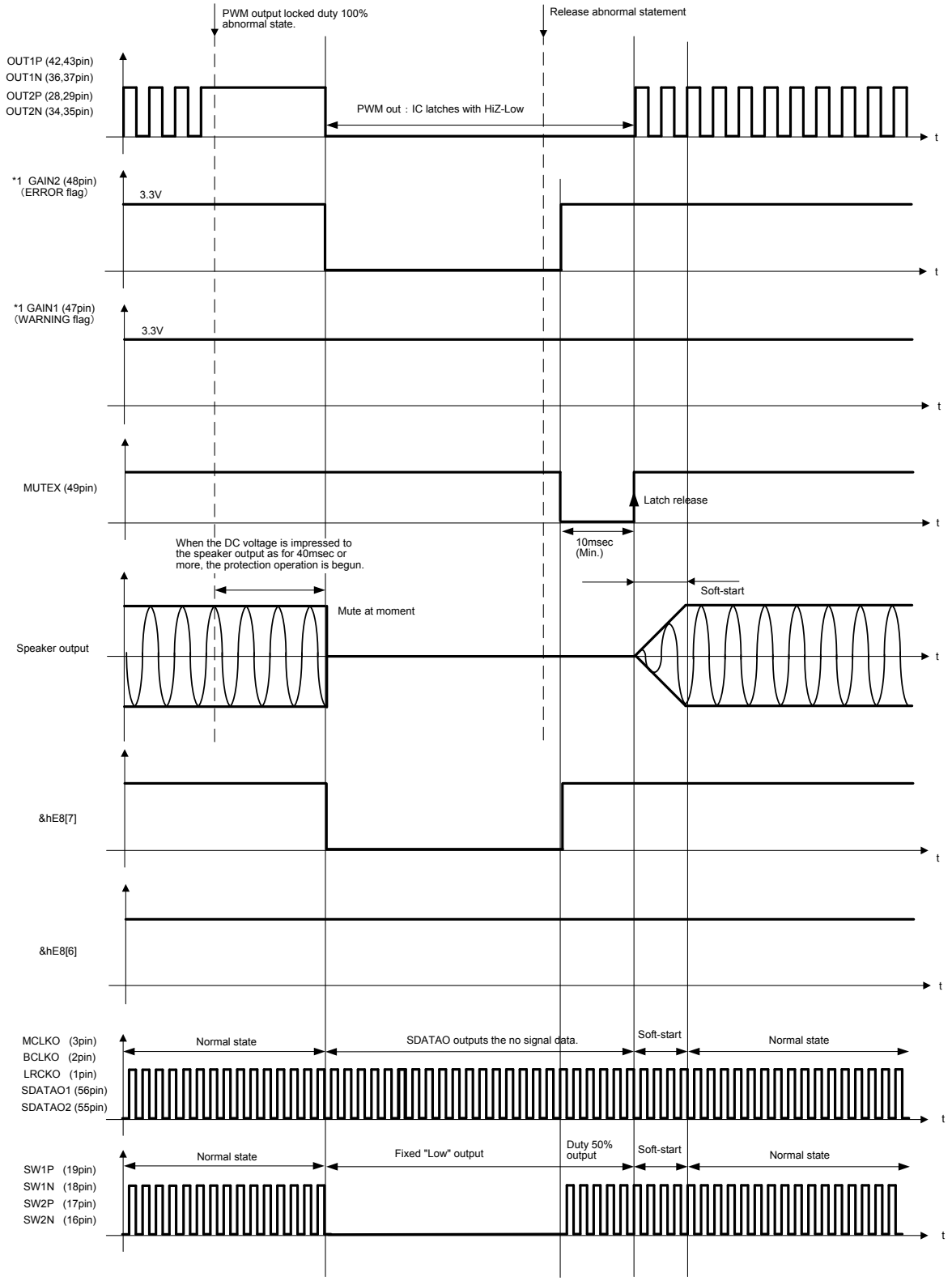
●DC voltage protection in the speaker

When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.

Detecting condition - It will detect when MUTEX pin is set High and PWM output Duty=0% or 100% over 40msec. Once detected, The PWM output instantaneously enters the state of HiZ-Low, and IC does the latch.

Releasing method – ①After MUTEX pin is set Low once over the soft mute transition time(10msec(Min.)), MUTEX pin is returned to High again.

②Turning on the power supply again (Vcc<3V, 10msec(Min)).



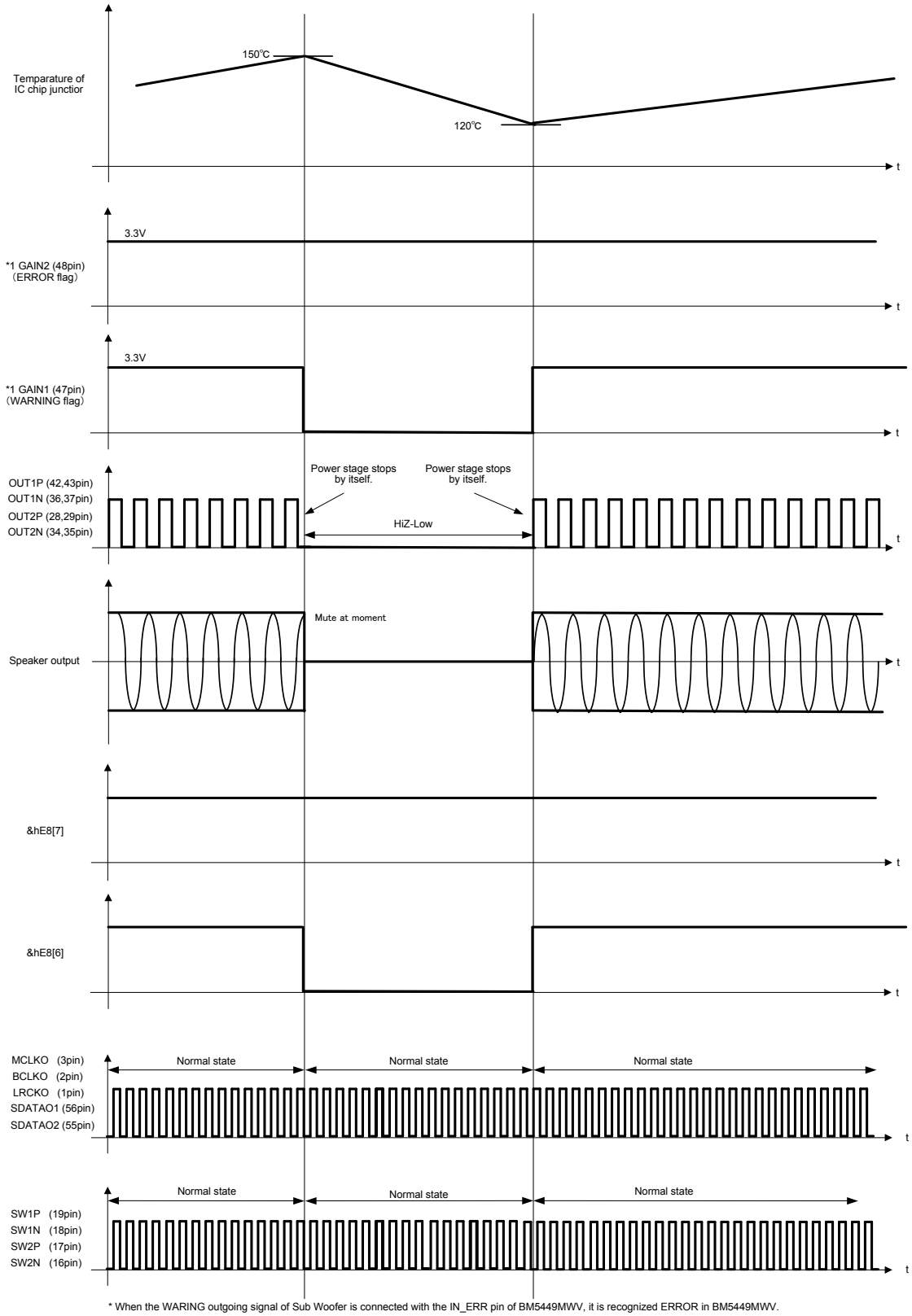
(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

●High temperature protection

This IC has the high temperature protection circuit that prevents thermal reckless driving under an abnormal state for the temperature of the chip to exceed Tjmax=150℃.

Detecting condition - It will detect when MUTEX pin is set to High and the temperature of the chip becomes 150℃(TYP.) or more. The speaker output is muted when detected.

Releasing condition - It will release when MUTEX pin is set High and the temperature of the chip becomes 120℃(TYP.) or less. The speaker output is outputted when released.



* When the WARING outgoing signal of Sub Woofer is connected with the IN_ERR pin of BM5449MWV, it is recognized ERROR in BM5449MWV.

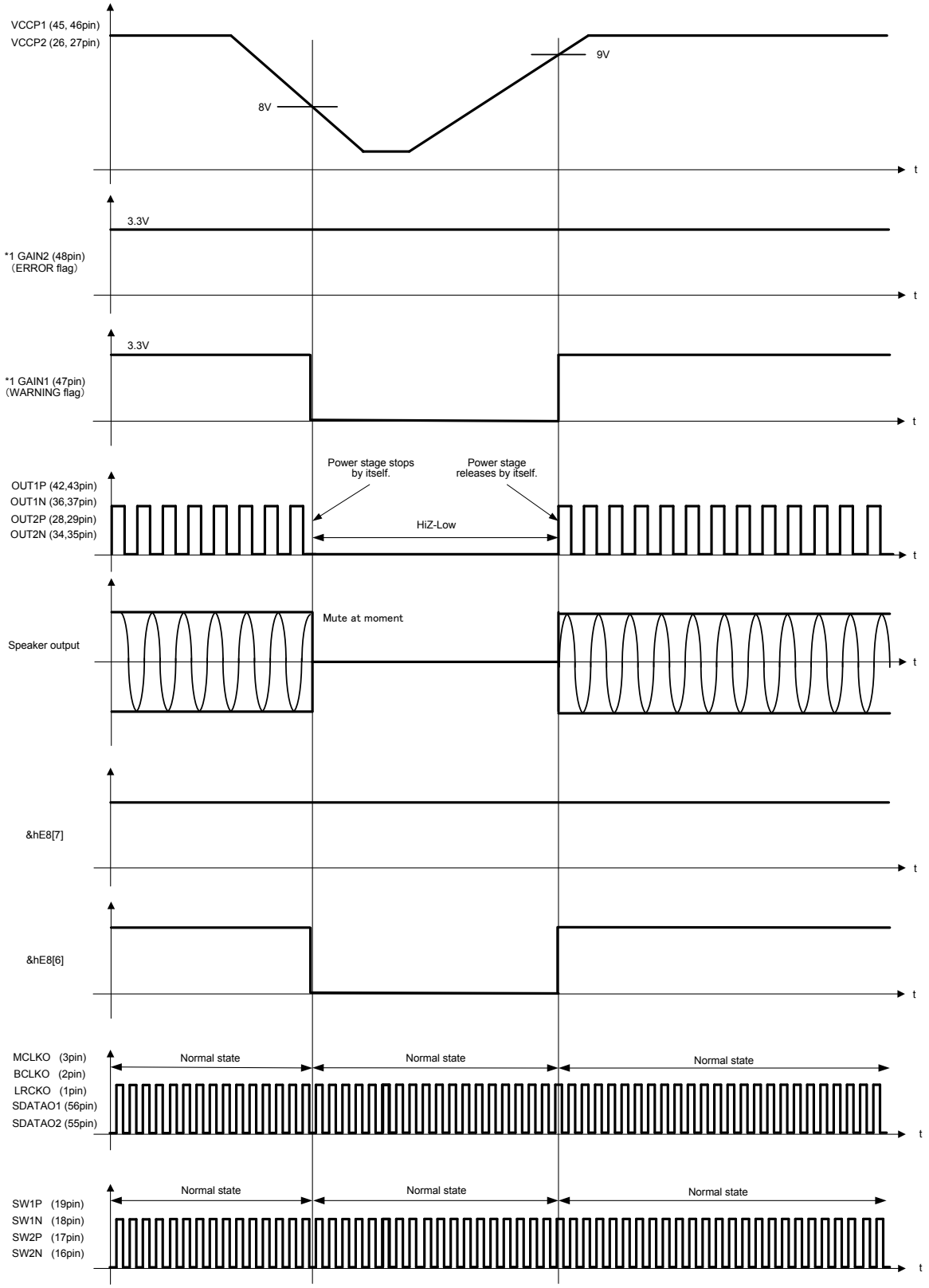
(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

●Under voltage protection

This IC has the under voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition – It will detect when MUTEX pin is set to High and the power supply voltage becomes lower than 8V. The speaker output is muted when detected.

Releasing condition – It will release when MUTEX pin is set to High and the power supply voltage becomes more than 9V. The speaker output is outputted when released



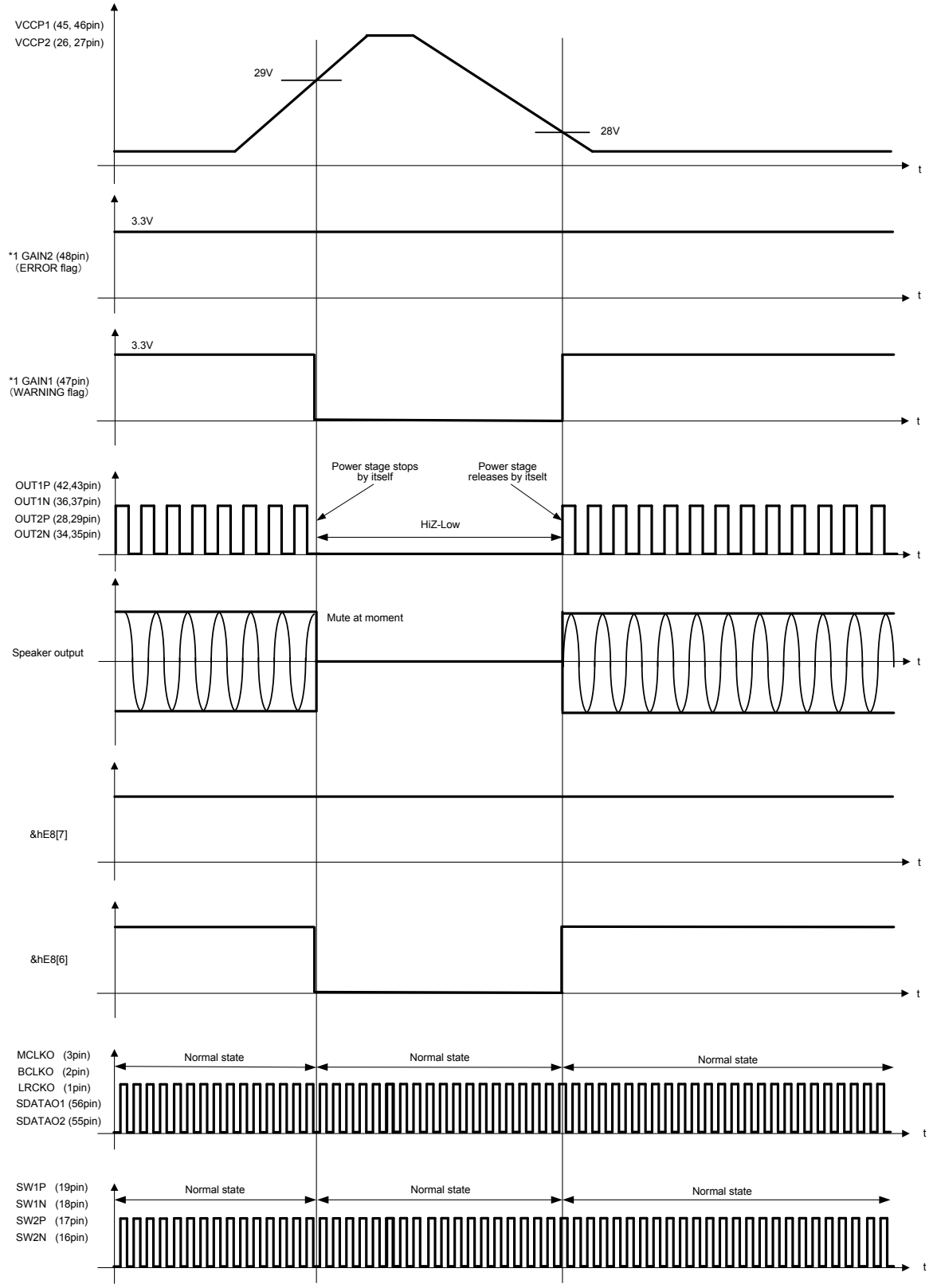
(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

●Over voltage protectione

This IC has the over voltage protection circuit that make speaker output mute once detecting extreme drop of the ower supply voltage.

Detecting condition – It will detect when MUTEX pin is set High and the power supply voltage becomes more than 29V. The speaker output is muted when detected.

Releasing condition – It will release when MUTEX pin is set High and the power supply voltage becomes less than 28V. The speaker output is outputted when released.



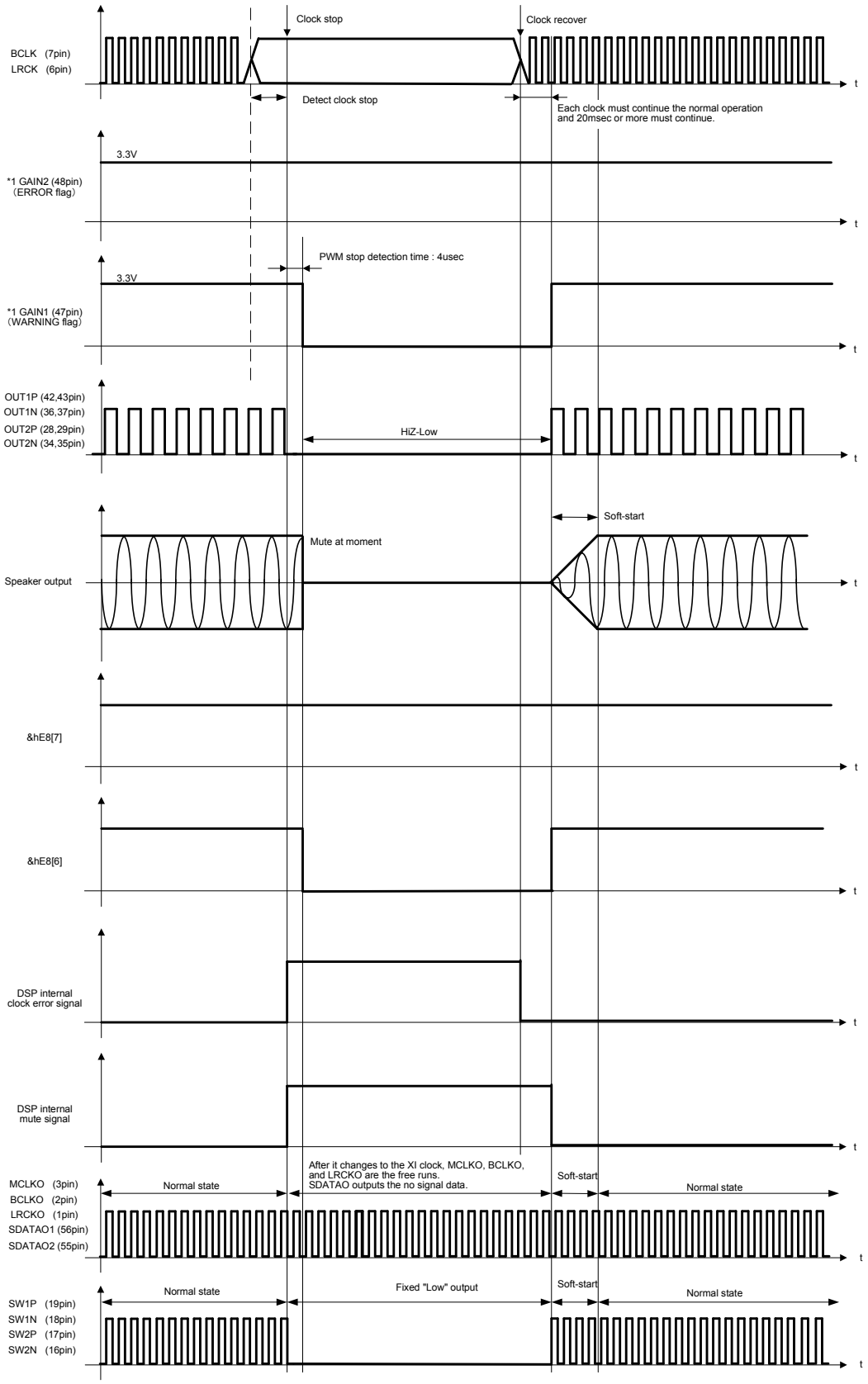
(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

● Clock stop protection

This IC has the clock stop protection circuit that make the speaker output mute when the BCLK and LRCLK frequency of the digital sound input are decreased.

Detecting condition - It enters the state of detection when BCLK or LRCK stops at 100 μsec or more when the MUTE pin is High. The speaker output instantaneously enters the state of HiZ-Low if detected.

Releasing condition - A It enters the state of release if BCLK or LRCK returns to a normal clock motion when the terminal MUTEX is High. The speaker output returns to the signal output state through a soft start when released.



(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

●DSP part Functional specification

1. Command Interface

BM5449MWV uses I^2C-bus system for the command interface with a host CPU.

The register of BM5449MWV has Write-mode and Read-mode.

BM5449MWV specifies a slave address and 1 byte of selection address, and it performs writing and read-back.

The slave mode format of I^2C bus is shown below.

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P

S: Start condition

Slave Address: After the slave address (7 bits) set up by I2CADR, bit of a read-mode (H") and a write-mode (L") is attached, and a total of 8-bit data is sent. (MSB first)

A: Acknowledge an acknowledge bit is added on to each bit of data transmitted.

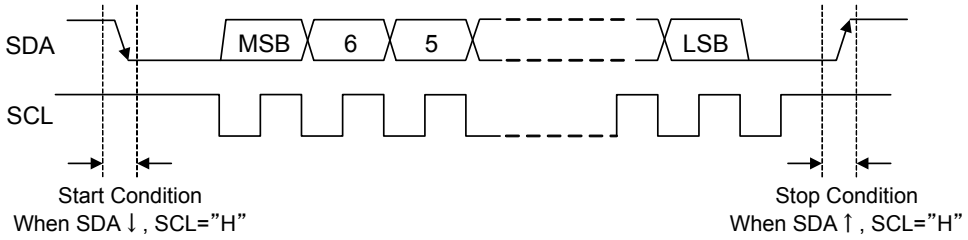
When data transmission is being done correctly, “L” is transmitted.

“H” transmission means there was no acknowledge.

Select Address: BM5449MWV uses a 1-byte select address. (MSB first)

Data: Data byte, transmitted data (MSB first)

P: Stop condition



1-1. Data Write-In

S	Slave Address	A	Select Address	A	Data	A	P

: Master to Slave Slave to Master

ADDR=0

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	0

ADDR=1

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	0

Setting of BM5449 slave address

Terminal setting	Write-mode
ADDR	Slave-address
0	80h
1	82h

S	Slave Address	A	Select Address	A	Data	A	Data	A	Data	A	P
(ex.)	80h		20h		00h		00h		00h		

: Master to Slave Slave to Master

Write-in Procedure

Step	Clock	Master	Slave(BM5449)	Note
1		Start Condition		
2	7	Slave Address		&h80 (&h82)
3	1	R/W (0)		
4	1		Acknowledge	
5	8	Select Address		Write-in target register: 8bit
6	1		Acknowledge	
7	8	Data		8bit write-in data
8	1		Acknowledge	
9		Stop Condition		

○When transmitting continuous data, the auto-increment function moves the select address up by one.
Repeat steps 7 and 8.

1-2. Data Read-Out

During read-out, the corresponding read-out address is first written into the &hD0 address register (&h20h in the example). In the following stream, the data is read out after the slave address. Do not return an acknowledge after completing the reception.

S	Slave Address	A	Req_Addr	A	Select Address	A	P
Ex.)	80h		D0h		20h		

S	Slave Address	A	Data 1	A	Data 2	A	_ _ _ _ _ _ _	A	Data N	Ā	P
Ex.)	81h		**h		**h				**h		

: Master to Slave, : Slave to Master A: With acknowledge, Ā:Without acknowledge

Read-out Procedure

Step	Clock	Master	Slave(BM5449)	Note
1		Start Condition		
2	7	Slave Address		&h80 (&h82)
3	1	R/W (0)		
4	1		Acknowledge	
5	8	Req_Addr		I^2C read-out address &hD0
6	1		Acknowledge	
7	8	Select Address		Read-out target register: 8bit
8	1		Acknowledge	
9	1	Stop Condition		
10	1	Start Condition		
11	7	Slave Address		&h81 (&h83)
12	1	R/W (1)		
13	1		Acknowledge	
14	8		Data	8bit read-out data
15	1	Acknowledge		
16		Stop Condition		

○When transmitting continuous data, the auto-increment function moves up the select address by one.
Repeat steps 14 and 15.

1-3. Control Signal Specifications

○Electrical Characteristics and Timing for Bus Line and I/O Stage

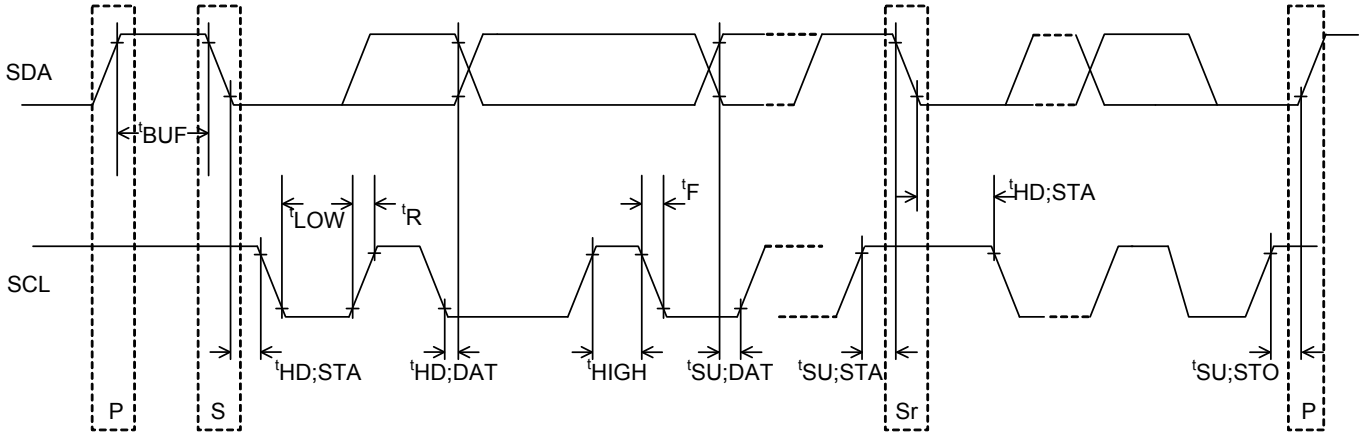


Figure 31. Timing Chart

Table 1-1: SDA and SCL Bus Line Characteristics (Ta=25℃ and DVDD=3.3V)

Parameters		Symbol	High-Speed Mode		Unit
			Min.	Max.	
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus free time between “stop” condition and “start” condition	tBUF	1.3	-	μs
3	Hold time (re-transmit) “start” condition. After this period, the first clock pulse is generated.	tHD;STA	0.6	-	μs
4	SCL clock LOW state hold time	tLOW	1.3	-	μs
5	SCL clock HIGH state hold time	tHIGH	0.6	-	μs
6	Re-transmit set-up time of “start” condition	tSU;STA	0.6	-	μs
7	Data hold time	tHD;DAT	0[1)]	-	μs
8	Data setup time	tSU;DAT	2/(XI frequency)	-	ns
9	SDA and SCL signal stand-up time	tR	20+0.1Cb	300	ns
10	SDA and SCL signal stand-down time	tF	20+0.1Cb	300	ns
11	Set-up time for “stop” condition	tSU;STO	0.6	-	μS
12	Each bus line’s capacitive load	Cb	-	400	pF

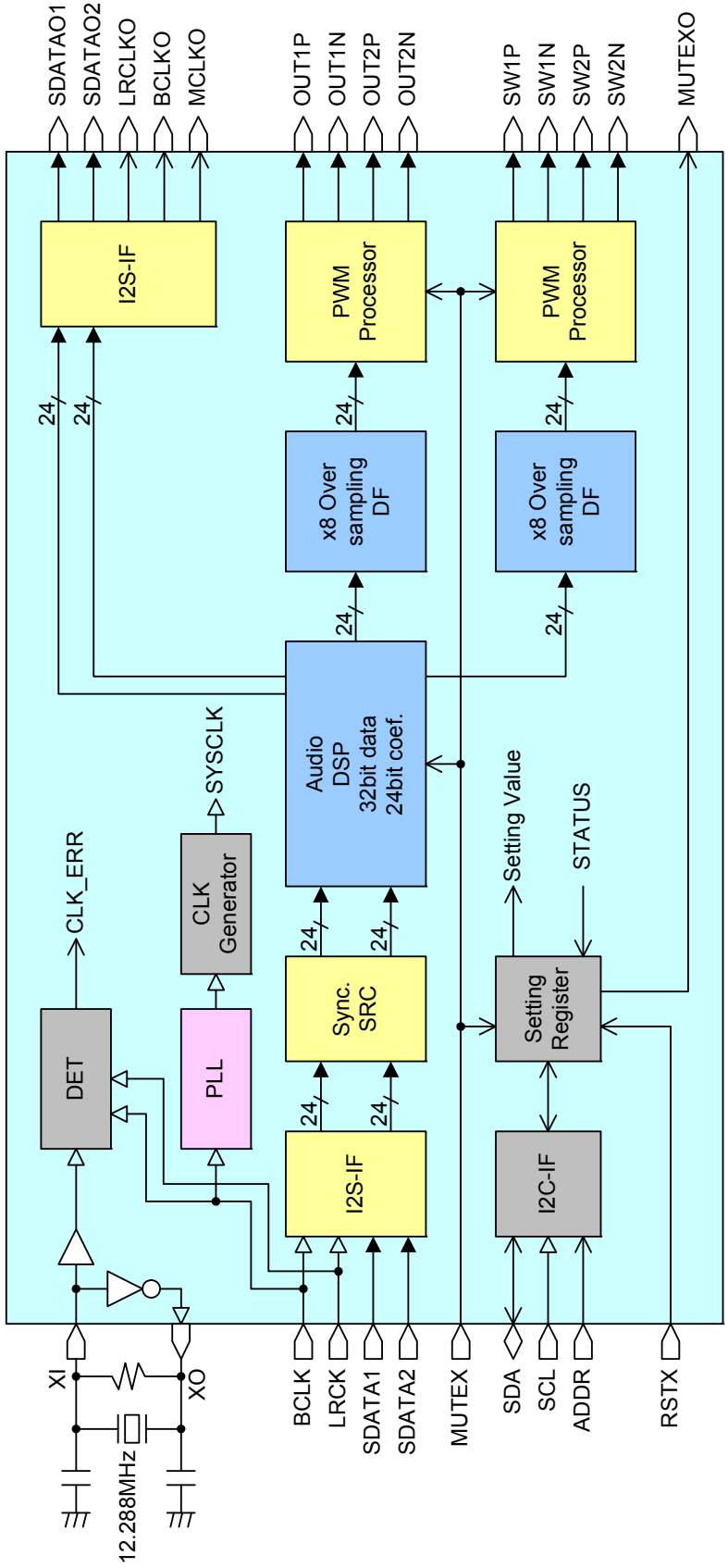
The values above correspond with $V_{IH\ min}$ and $V_{IL\ max}$ levels.

1) Because the transmission device exceeds the undefined domain of the SCL fall edge, it is necessary to internally provide a minimum
300ns hold time for the SDA signal (of $V_{IH\ min}$ of SCL signal).

The above-mentioned characteristic is a theory value in IC design and it doesn't be guaranteed by shipment inspection.
When problem occurs by any chance, we talk in good faith and correspond.
Neither terminal SCL nor terminal SDA correspond to 5V tolerant. Please use it within absolute maximum rating 4.5V.

2. Data and system clock distribution diagram

The audio input data and audio output data distribution diagram of BM5449MWV is shown below.



3. S-P conversion

In BM5449MWV, the conversion circuit from serial data to parallel data is built in.

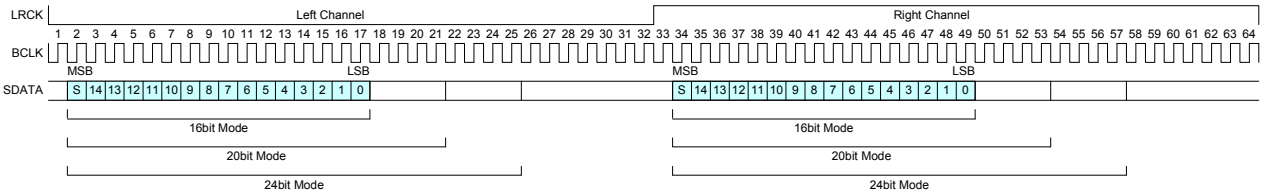
S-P conversion is blocks which receive 3-line serial input audio data from pins and convert it to parallel data.

The three input formats are IIS, left-justified and right-justified. The bit clock frequency may be selected from either 64fs or 48fs or 32fs. 16bit, 20bit and 24bit output may be selected for each format.

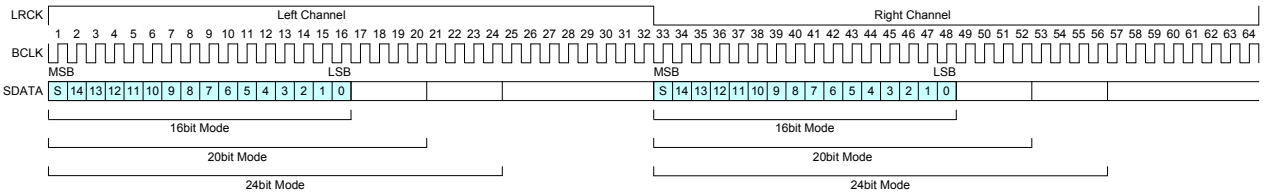
The timing chart of each transmission mode is shown in the following figure.

Bit clock frequency: 64fs form

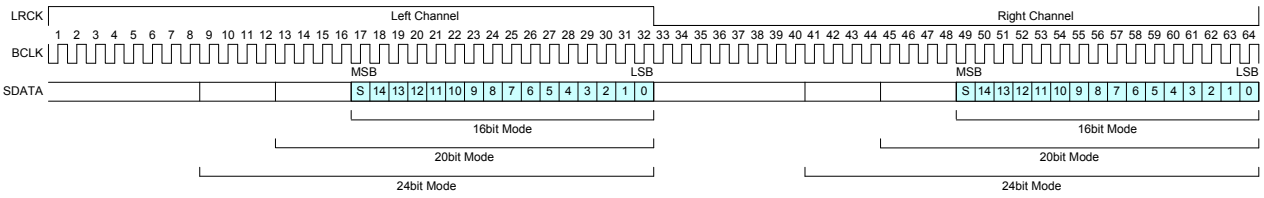
I^2S 64fs Format



Left-Justified 64fs Format

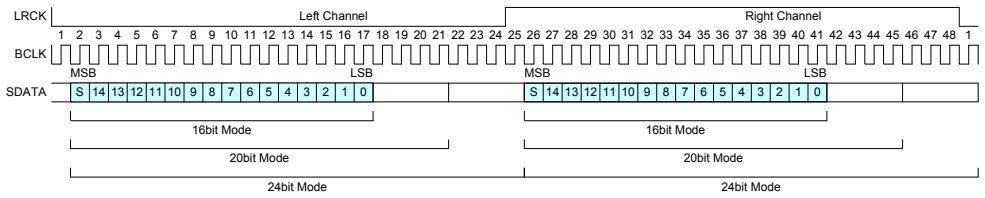


Right-Justified 64fs Format

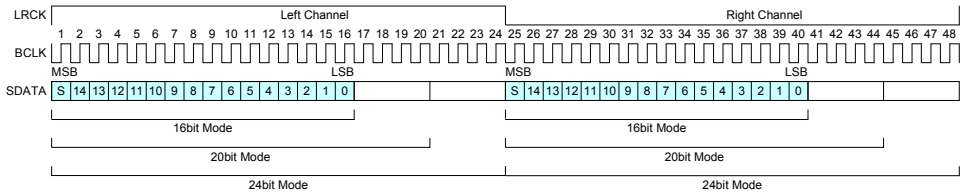


Bit clock frequency: 48fs form

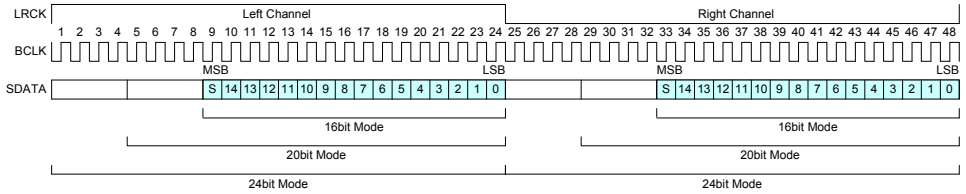
I²S 48fs Format



Left-Justified 48fs Format

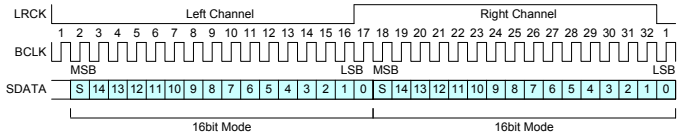


Right-Justified 48fs Format

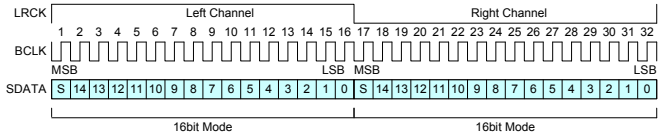


Bit clock frequency: 32fs form

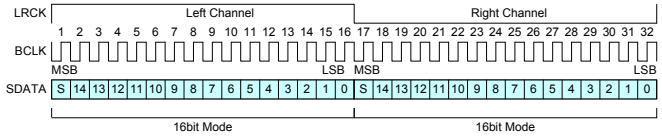
I²S 32fs Format



Left-Justified 32fs Format



Right-Justified 32fs Format



3-1. Timing reset setup of input 3-line serial data circuit

After changing into parallel data from serial data, the timing which takes in data is adjusted.

(Synchronization)

This function is used when the time of power supply starting of IC and an input sampling rate change or 3-line serial-data input format change.

When data taking-in timing shifts more than fixed, it adjusts automatically.

Default = 0

Select Address	Value	Explanation of operation
&h03 [6]	0	Auto adjustment function is invalid
	1	Auto adjustment function is valid

It resets by &h04[0] = 1 after the stability of PLLA.

This Resister is cleared automatically, after Reset function is finished.

Select Address	Value	Explanation of operation
&h04 [0]	1	Synchronous counter reset

3-2. Bit clock frequency setup of 3-line serial-data input

Default = 0

Select Address	Value	Explanation of operation
&h03 [5:4]	0	64fs form
	1	48fs form
	2	32fs form

3-3. Serial data format

Default = 0

Select Address	Value	Explanation of operation
&h03 [3:2]	0	IIS format
	1	Left-justified format
	2	Right-justified format

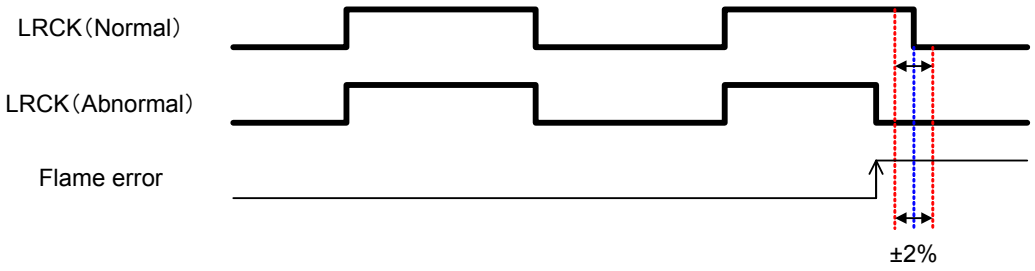
3-4. Data bit width

Default = 2

Select Address	Value	Explanation of operation
&h03 [1:0]	0	16 bit
	1	20 bit
	2	24 bit

3-5. LRCK flame error flag

When the phase of LRCK shifts by ±2% or more, the frame error becomes "H".



Setting the number of times of the conclusion of the LRCK frame error

When detecting a frame error above the number of times which was set here, &h04 [2] becomes "1".

Default = 1h

Select Address	Value	Explanation of operation
&h04 [6:4]	0	Inhibit
	1	1 time
	2	2 times
	:	:
	7	7 times

Please set to 1h or more

The flame error is read out by &h04 [2].

Select Address	Value	Explanation of operation
&h04 [2]	0	Normal
	1	Detect the LRCK flame error

It clears the LRCK frame error flag which latches in executing &h04 [1] command.

Operation is automatically cleared about the register after complete.

Default = 0

Select Address	Value	Explanation of operation
&h04 [1]	0	Normal
	1	Clear the LRCK flame error flag

3-6. Audio interface signal specification

○Electric specification and timings of BCLK,LRCK and SDATA

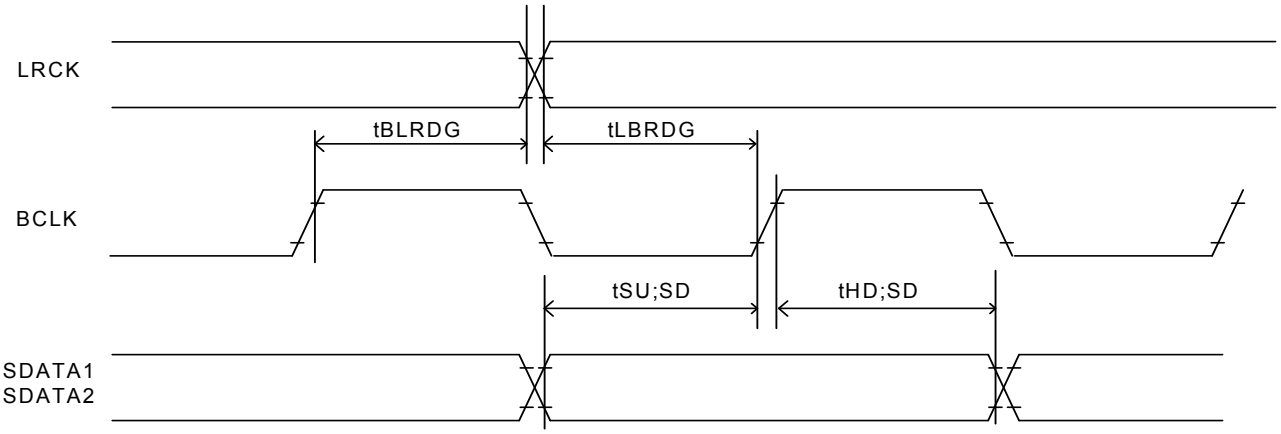


Figure 32. Audio interface timings

Parameter			Symbol	Min.	Max.	Unit
1	LRCK	Frequency	fLRCK	8	96	kHz
2		DUTY	dLRCK	40	60	%
3	BCLK	Cycle	tBCK	162.76	-	ns
4		Hi Section	tBCKH	65	-	ns
5		Low Section	tBCKL	65	-	ns
6	Time from the rising edge of BCLK to the edge of LRCK *1		tBLRDG	20	-	ns
7	Time from the edge of LRCK to the rising edge of BCLK *1		tLBRDG	20	-	ns
8	Setup time of SDATA		tSU;SD	20	-	ns
9	Hold time of SDATA		tHD;SD	20	-	ns

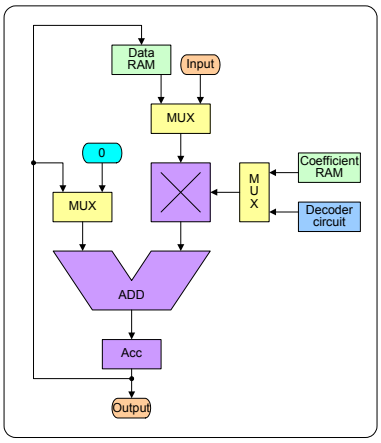
*1 This standard value has specified that the edge of LRCK and the rising edge of BCLK do not overlap.

4. Digital Sound Processing (DSP)

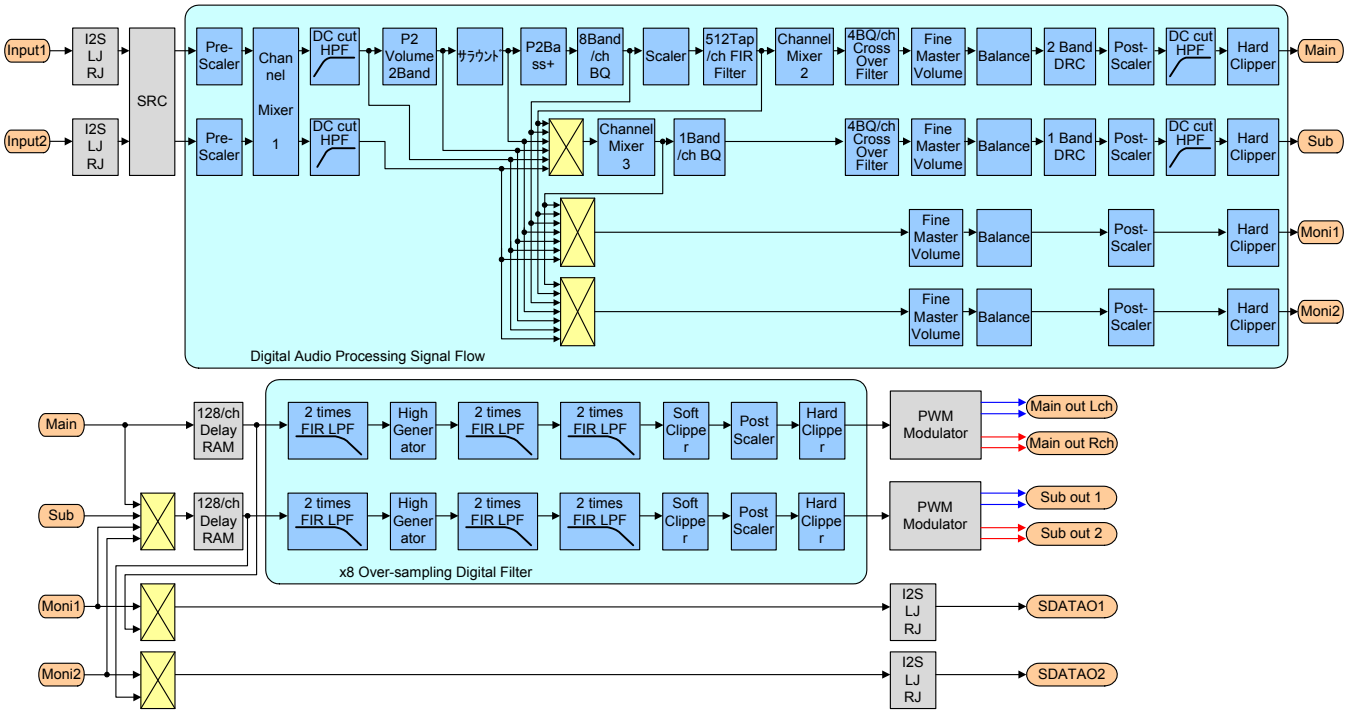
The digital sound processing (DSP) part of BM5449MWV is composed of the special hard ware which is the optimal for FPD-TV, the Mini/Micro Compo. BM5449MWV does the following processing using this special DSP.
Pre-scaler, Channel mixer, DC cut HPF, P2Volume, Surround, P2Bass+, 8 Band P-EQ, 512Tap FIR, Cross Over Filter, Fine Master Volume, Balance Volume, 2 Band DRC, Post-scaler, Hard Clipper

The outline and signal flow of the DSP part

Data width:	32 bit (DATA RAM)
Machine cycle:	20.3ns (1024fs, fs=48kHz)
Multiplier:	32×24 → 56 bit
Adder:	56+56 → 56 bit
Data RAM:	512×32 bit
Coefficient RAM:	512×24 bit
Sampling frequency :	fs=8k, 11.025k, 12k, 16k, 22.05k, 32k, 44.1k, 48k, 88.2k, 96k, 176.4k, 192kHz

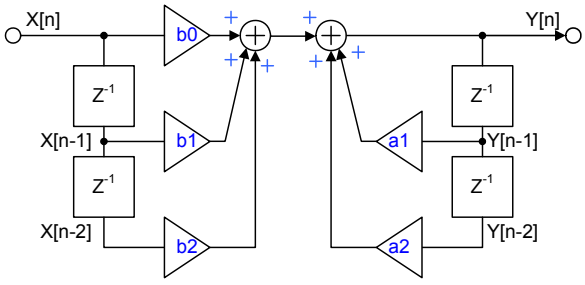


The input sampling frequency is converted into 48kHz or 44.1kHz in SRC.

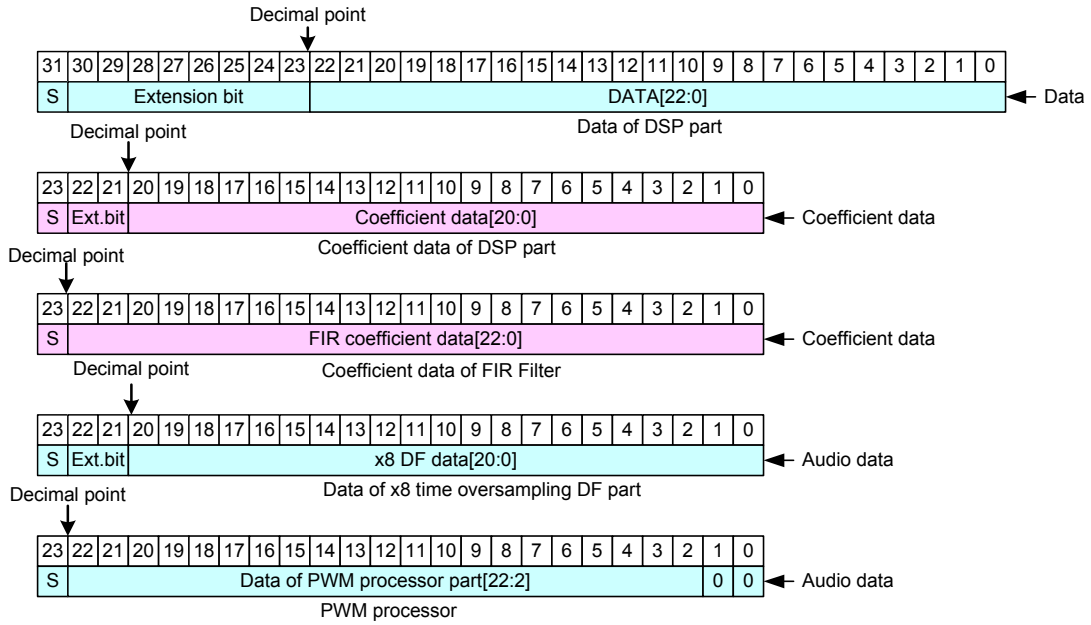


The digital signal from 16 bits to 24 bits is inputted to the DSP but extends 8bit (+42dB) as the overflow margin to the upper side. When doing the processing which exceeds this range, it processes a clip in the DSP. Incidentally, in case of the 2nd IIR-type (BQ) filter which is often used generally as the digital filter, because it consumes a lot of overflow margins, the output of the multiplier and the adder inside needs note.

The output of multipliers and the adding machine might exceed +48dB by the coefficient of a1, a2, b0, b1, and b2. In that case, data becomes saturation power. Therefore, the output of the filter cannot obtain the aimed characteristic.



The management of audio data is as follows by each block.



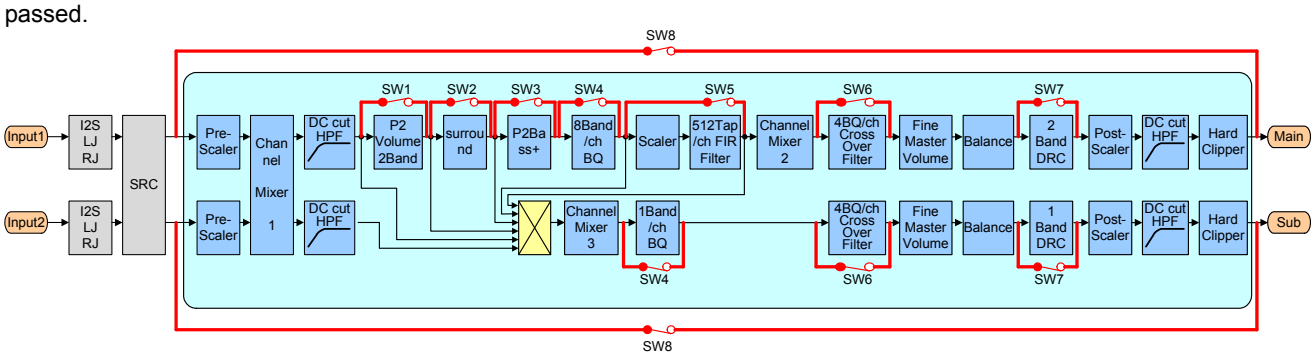
It is using 2 bits of extension of 8 times over sampling parts for the calculation by the soft clipper function.

It is 2 bits shifted to the upper side when delivering data to the PWM processor, it makes up of 0 and it delivers 0 to 2 bits of lower ranks as the 24-bit data.

4-1. Bypass

It passes in the each function of the DSP by the command. Because it left the set value of the each function can be passed in, it is possible to do the confirmation of ON/OFF of the sound effect easily.

The effect which is possible about the bypass, 1) P2Volume, 2) The surround 3) P2Bass + (The suspected low voice), 4) 8Band BQ/1Band BQ, 5) 512 Tap FIR Filter, 6) 4 BQ Cross Over Filter, 7)2Band DRC/1Band DRC and the whole DSP can be passed.



Default = 00h

Select Address	bit	Explanation of operation
&h02 [7:0]	7	Bypass of P^2Volume(SW1) 0 : Nomal, 1 : Bypass
	6	Bypass of Surround(SW2) 0 : Normal, 1: Bypass
	5	Bypass of P^2Bass+(SW3) 0 : Normal, 1 : Bypass
	4	Bypass of 8Band/1Band BQ(SW4) 0 : Normal, 1 : Bypass
	3	Bypass of Scaler and 512 Taps FIR Filter(SW5) 0 : Normal, 1 : Bypass
	2	Bypass of 4 BQ Cross Over Filter(SW6) 0 : Normal, 1 : Bypass
	1	Bypass of 2 Band/1Band DRC(SW7) 0 : Normal, 1 : Bypass
	0	Bypass of the whole DSP(SW8) 0 : Normal, 1 : Bypass

4-2. Pre-scaler

To overflow when the level sometimes is full scale entry in case of the digital signal which is inputted to the sound DSP and does surround and equalizer processing, it adjusts an entry gain with Pre-scaler. The adjustable-range can be set from +48 dB to -79 dB with the 0.5-dB step. (Lch/Rch concurrency control)

Pre-scaler doesn't have a soft transfer feature. Input1 and Input2 become an independent control.

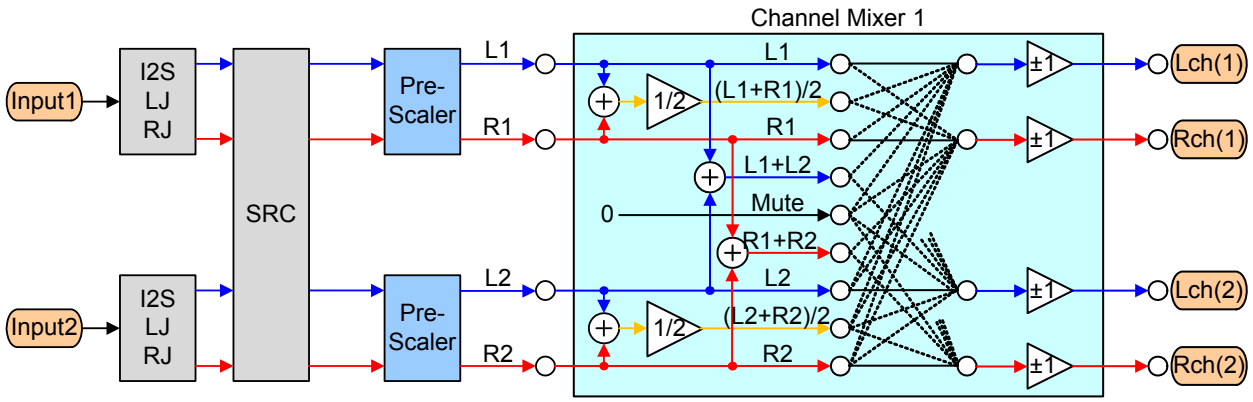
Default = 60h

Select Address	Explanation of operation
Input1 &h21 [7:0] Input2 &h22 [7:0]	

Command Value	Gain
00	+48dB
01	+47.5dB
⋮	⋮
60	0dB
61	-0.5dB
62	-1dB
⋮	⋮
FE	-79dB
FF	-∞

4-3. Channel setup with a phase inversion function (Channel Mixer 1)

It sets a mixing in the sound on the left channel and the right channel of the digital signal which was inputted to the DSP. It makes a stereo signal a monaural here. Also, the phase-inversion, the mute on each channel can be set. The sound of Input1 and Input2 can be replaced and be added, too.



DSP Input1: The data inputted into Lch (1) of DSP is inverted.

Default = 0

Select Address	Value	Explanation of operation
&h24 [7]	0	Normal
	1	Invert

DSP Input1: The data inputted into Lch (1) of DSP is mixed.

Default = 1

Select Address	Value	Explanation of operation
&h24 [6:4]	0	Mute
	1	Input Lch(1)
	2	Input Rch(1)
	3	Input (Lch(1) + Rch(1)) / 2
	4	Input Lch(2)
	5	Input Rch(2)
	6	Input (Lch(2) + Rch(2)) / 2
	7	Input Lch(1) + Lch(2)

DSP Input1: The data inputted into Rch (1) of DSP is inverted.

Default = 0

Select Address	Value	Explanation of operation
&h24 [3]	0	Normal
	1	Invert

DSP Input1: The data inputted into Rch (1) of DSP is mixed.

Default = 2

Select Address	Value	Explanation of operation
&h24 [2:0]	0	Mute
	1	Input Lch(1)
	2	Input Rch(1)
	3	Input (Lch(1) + Rch(1)) / 2
	4	Input Lch(2)
	5	Input Rch(2)
	6	Input (Lch(2) + Rch(2)) / 2
	7	Input Lch(1) + Lch(2)

DSP Input2: The data inputted into Lch (2) of DSP is inverted.

Default = 0

Select Address	Value	Explanation of operation
&h25 [7]	0	Normal
	1	Invert

DSP Input2: The data inputted into Lch (2) of DSP is mixed.

Default = 4

Select Address	Value	Explanation of operation
&h25 [6:4]	0	Mute
	1	Input Lch(1)
	2	Input Rch(1)
	3	Input (Lch(1) + Rch(1)) / 2
	4	Input Lch(2)
	5	Input Rch(2)
	6	Input (Lch(2) + Rch(2)) / 2
	7	Input Lch(1) + Lch(2)

DSP Input2: The data inputted into Rch (2) of DSP is inverted.

Default = 0

Select Address	Value	Explanation of operation
&h25 [3]	0	Normal
	1	Invert

DSP Input2: The data inputted into Rch (2) of DSP is mixed.

Default = 5

Select Address	Value	Explanation of operation
&h25 [2:0]	0	Mute
	1	Input Lch(1)
	2	Input Rch(1)
	3	Input (Lch(1) + Rch(1)) / 2
	4	Input Lch(2)
	5	Input Rch(2)
	6	Input (Lch(2) + Rch(2)) / 2
	7	Input Lch(1) + Lch(2)

4-4. 1st HPF for DC cut

It cuts the DC offset component of the digital signal which is inputted to the sound DSP with this HPF. The cut off frequency fc of HPF is using 1 Hz and the degree is using the 1st filter.

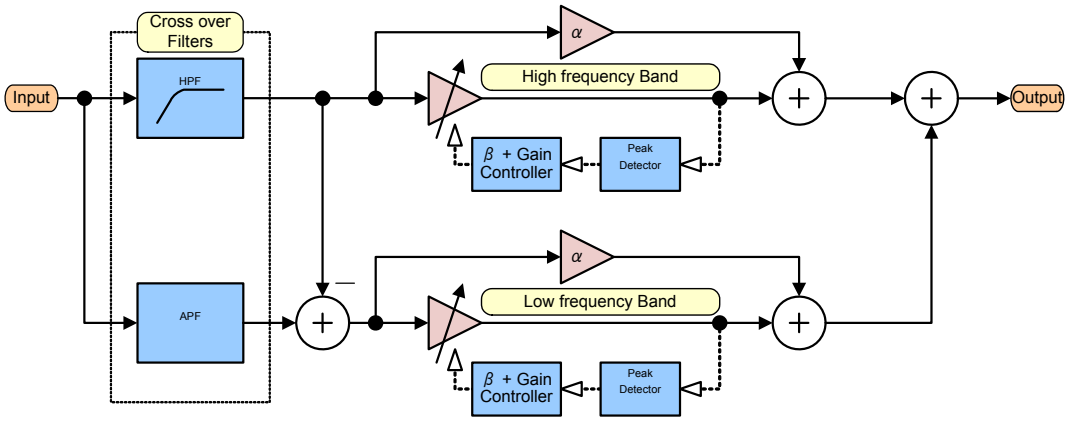
Default = 1

Select Address	Value	Explanation of operation
Input1 &h28 [3]	0	Not use DC cut HPF
Input2 &h28 [2]	1	Use DC cut HPF

4-5. 2 Band P^2Volume

When the sound suddenly grows like blasts that exist in the TV commercial and the action picture, the volume is automatically controlled. Moreover, a sound small as the serif can be caught even if the volume is squeezed in the bedroom of nighttime is enlarged, and the loud sound is suppressed. The compression can operate each two bands (the low and the high pass). Use as one band is also possible according to the command setting. Moreover, it is also possible that the sound below the set value is soft muted.

2 Band P^2Volume



It works, dividing P^2Volume feature into the area of ① and ② and ③ according to the input level.

① $V_{linf}(-\infty)$ - V_{Imin}

It prevents P^2Volume feature's generating noise.

② Input level is more than $V_{Imin,}$ and Output level is less than V_{omax}

$$V_O = V_I + \beta$$

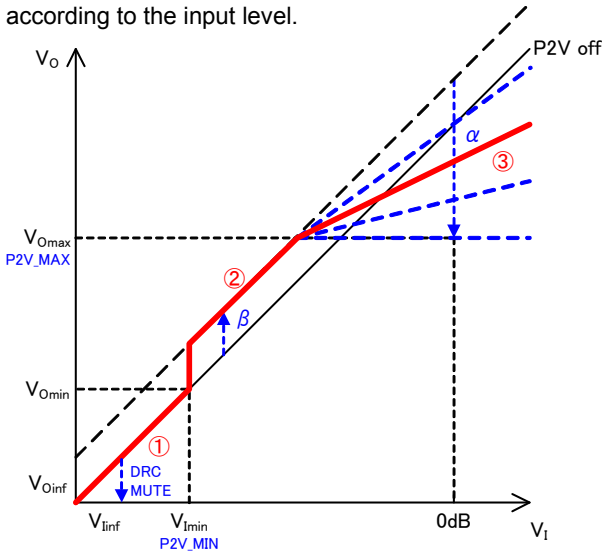
β: It lifts the whole power level for offset value beta.

③ When power level V_O exceeds V_{omax}

$$V_O = \alpha \cdot V_I + \beta$$

α: The inclination to suppress a D-range (P2V_α)

The power level can be made constant, too.



Selection of using the P^2Volume function.

Default = 0

Select Address	Value	Explanation of operation
&h02 [7]	0	Use P^2Volume function
	1	Not use P^2Volume function

Selection of using the 2 Band P^{2}Volum function for high frequency

Default = 0

Select Address	Value	Explanation of operation
&h40 [7]	0	Not use the 2 Band P^{2}Volum function for high frequency
	1	Use the 2 Band P^{2}Volum function for high frequency

Selection of using the 2 Band P^{2}Volum function for high frequency

Default = 0

Select Address	Value	Explanation of operation
&h40 [6]	0	Not use the 2 Band P^{2}Volum function for low frequency
	1	Use the 2 Band P^{2}Volum function for high frequency

[Attention] It uses it only for the high frequency when using it as 1Band P2Volume.

Selection of using soft mute when the small signal inputs in operating P^{2}Volum.

Default = 0

Select Address	Value	Explanation of operation
&h41 [2]	0	Not mute
	1	Mute

&h56 and the &h57 command adjust to the setting when attacking and releasing it.

The setting of V_{Imin}

As for P2V_MIN, to cancel that noise and so on are lifted by P2Volume, P2Volume sets a functioning minimum level.

Default = 00h

Select Address	Explanation of operation
for high freq. &h54 [4:0] for low freq. &h5C [4:0]	

Command	Gain	Command	Gain	Command	Gain	Command	Gain
00	-∞	08	-76dB	10	-60dB	18	-44dB
01	-90dB	09	-74dB	11	-58dB	19	-42dB
02	-88dB	0A	-72dB	12	-56dB	1A	-40dB
03	-86dB	0B	-70dB	13	-54dB	1B	-38dB
04	-84dB	0C	-68dB	14	-52dB	1C	-36dB
05	-82dB	0D	-66dB	15	-50dB	1D	-34dB
06	-80dB	0E	-64dB	16	-48dB	1E	-32dB
07	-78dB	0F	-62dB	17	-46dB	1F	-30dB

The setting of V_{omax}

P2V_MAX sets an output suppression level. The input level VI whenα setting “80h"

When α=80h (slope 0) is set, output power level V_{omax} at level VI=0dB input time is shown.

Default = 40h

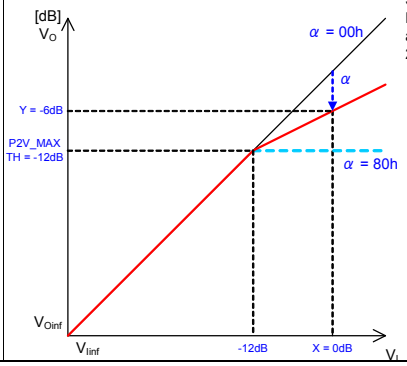
Select Address	Explanation of operation
High frequency band &h50[6:0] Low frequency band &h58[6:0]	

Command	Threshold
00	-32dB
⋮	⋮
3F	-0.5dB
40	0dB
41	+0.5dB
⋮	⋮
58	+12dB

α setting

α sets the slope of D range.

Default = 00h

Select Address	Explanation of operation
High frequency band &h51[7:0] Low frequency band &h59[7:0]	 Specify X, Y, and TH and request the slope a. Record the expression from which the slope a is requested in the following. a converts the value requested by the calculation into 8bit Hex data of the 2's complement. $\alpha = \frac{10^{\frac{Y}{20}} - 10^{\frac{TH}{20}}}{10^{\frac{X}{20}}} \times 128$ TH is P2V_MAX, X is an input level, and Y is an output power level. Ex.) Request the a at P2V_MAX=-12dB, X=0dB, and Y=-6dB. $\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{-12}{20}}}{10^{\frac{0}{20}}} \times 128$ $\alpha = 32 \rightarrow 20_H$ Set obtained 20H to &h51 and the &h59 command.

β setting

A small voice is made the offset level β easy to hear by lifting the entire output power level.

Default = 18h

Select Address	Explanation of operation
High frequency band &h55[4:0] Low frequency band &h5D[4:0]	

Command	Gain	Command	Gain	Command	Gain	Command	Gain
00	0dB	08	+8dB	10	+16dB	18	+24dB
01	+1dB	09	+9dB	11	+17dB	19	-
02	+2dB	0A	+10dB	12	+18dB	1A	-
03	+3dB	0B	+11dB	13	+19dB	1B	-
04	+4dB	0C	+12dB	14	+20dB	1C	-
05	+5dB	0D	+13dB	15	+21dB	1D	-
06	+6dB	0E	+14dB	16	+22dB	1E	-
07	+7dB	0F	+15dB	17	+23dB	1F	-

[Attention] The setting change of the offset level β should be made to &h40 [7] =0 and &h40 [6] =0 and be done.

The setting of a transition time in attack (1)

A_RATE is the transition time setting when the condition of the P^2Volume feature transfers from ② to ③.

Default = 3

Select Address	Explanation of operation
High frequency band &h52[6:4] Low frequency band &h5A[6:4]	

Command	A_RATE time	Command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

The setting of a transition time in release (1)

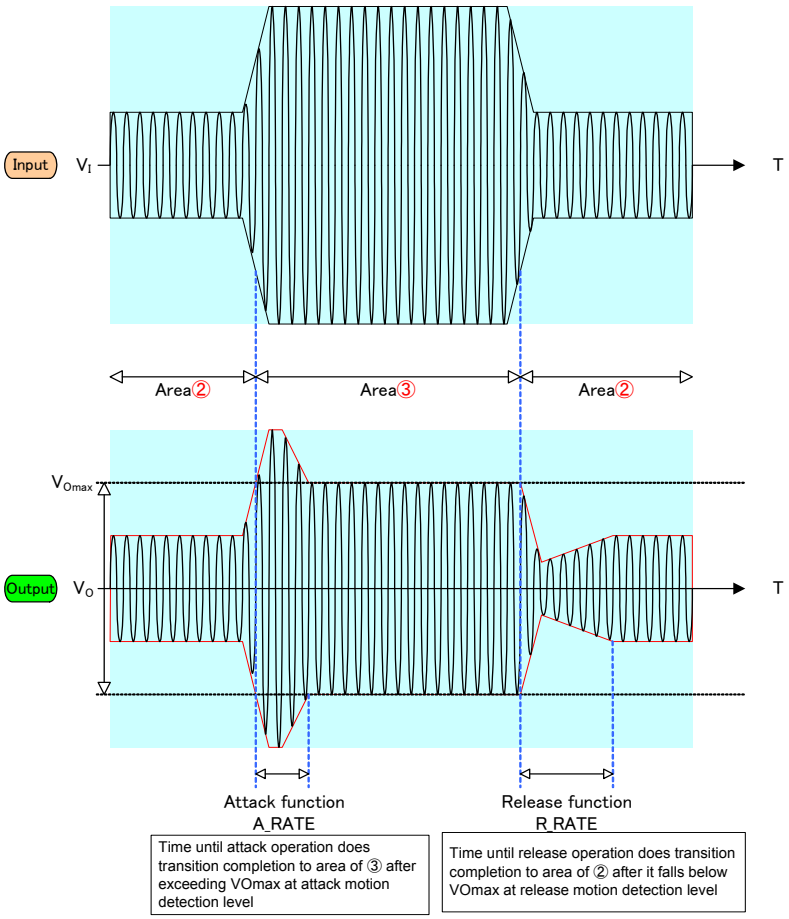
R_RATE is the transition time setting when the condition of the P^2Volume feature transfers from ③ to ②.

Default = Bh

Select Address	Explanation of operation
High frequency band &h52[3:0] Low frequency band &h5A[3:0]	

Command	R_RATE time	Command	R_RATE time
0	0.125s	8	2s
1	0.1825s	9	2.5s
2	0.25s	A	3s
3	0.5s	B	4s
4	0.75s	C	5s
5	1s	D	6s
6	1.25s	E	7s
7	1.5s	F	8s

Explanation for A_RATE andR_RATE(from ② to ③ area)



Attack detection time setup (1)

A_TIME is the transfer operation beginning setting of P2Volume feature. When the output power level when changing A_TIME time continues from ② to ③, the state transition of P2Volume is begun.

Default = 1

Select Address	Explanation of operation
High frequency band &h53[7:4] Low frequency band &h5B[7:4]	

Command	A_TIME time	Command	A_TIME time
0	0ms	8	6ms
1	0.5ms	9	7ms
2	1ms	A	8ms
3	1.5ms	B	9ms
4	2ms	C	10ms
5	3ms	D	20ms
6	4ms	E	30ms
7	5ms	F	40ms

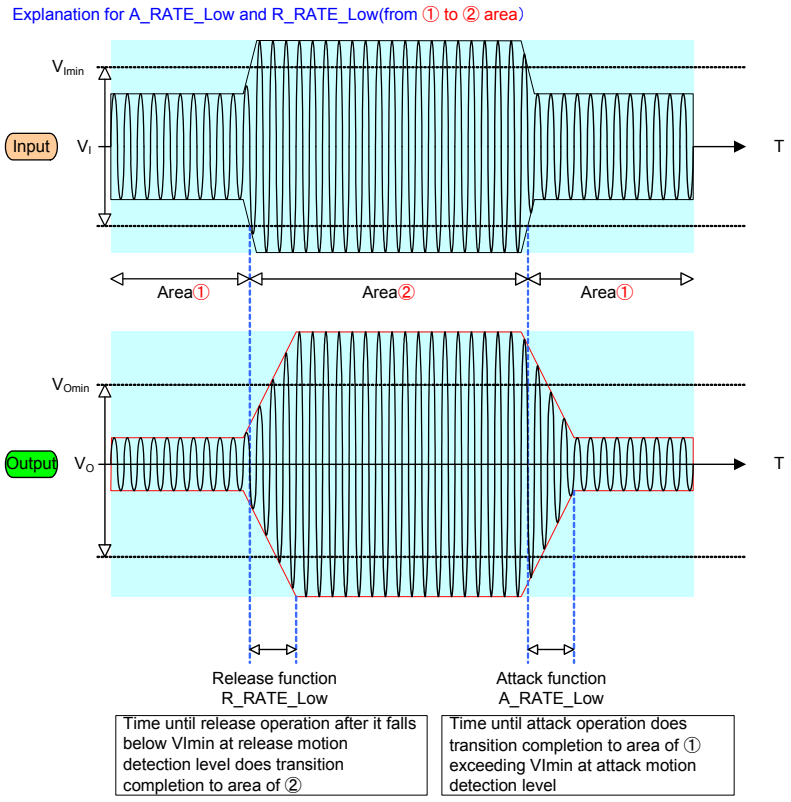
Release detection time setup (1)

R_TIME is the transfer operation beginning setting of P2Volume feature. When the output power level when changing continuous R_TIME time continues from ③ to ②, the state transition of P2Volume is begun.

Default = 3

Select Address	Explanation of operation
High frequency band &h53[2:0] Low frequency band &h5B[2:0]	

Command	R_TIME time	Command	R_TIME time
0	5ms	4	100ms
1	10ms	5	200ms
2	25ms	6	300ms
3	50ms	7	400ms



The setting of a transition time in attack (2)

A_RATE_LOW is the transition time setting when the condition of the P2Volume feature transfers from ② to ①.

Default = Bh

Select Address	Explanation of operation
High frequency band &h56 [3:0] Low frequency band &h5E [3:0]	

Command	A_RATE_LOW	Command	A_RATE_LOW
0	0.125s	8	2s
1	0.1825s	9	2.5s
2	0.25s	A	3s
3	0.5s	B	4s
4	0.75s	C	5s
5	1s	D	6s
6	1.25s	E	7s
7	1.5s	F	8s

The setting of a transition time in release (2)

R_RATE_LOW is the transition time setting when the condition of the P2Volume feature transfers from ① to ②.

Default = 3

Select Address	Explanation of operation
High frequency band &h56 [6:4] Low frequency band &h5E [6:4]	

Command	R_RATE_LOW	Command	R_RATE_LOW
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

The setting of attack detection time (2)

A_TIME_LOW is the transfer operation beginning setting of P2Volume feature. When the input level below V_{Imin} continues above continuation A_TIME_LOW at the time of ② or ③, it begins the state transition of P2Volume to the condition of ①.

Default = 3

Select Address	Explanation of operation
High frequency band &h57 [2:0] Low frequency band &h5F [2:0]	

Command	A_TIME_LOW	Command	A_TIME_LOW
0	5ms	4	100ms
1	10ms	5	200ms
2	25ms	6	300ms
3	50ms	7	400ms

The setting of release detection time (2)

R_TIME_LOW is the transfer operation beginning setting of P^2Volume feature. In case of ①, it begins the state transition of P^2Volume to the condition of ② or ③, when the input level of ② or ③ continues above R_TIME_LOW.

Default = 1h

Select Address	Explanation of operation
High frequency band &h57 [7:4] Low frequency band &h5F [7:4]	

Command	R_TIME_LOW	Command	R_TIME_LOW
0	Prohibition	8	6ms
1	0.5ms	9	7ms
2	1ms	A	8ms
3	1.5ms	B	9ms
4	2ms	C	10ms
5	3ms	D	20ms
6	4ms	E	30ms
7	5ms	F	40ms

○The scene changing detection and the high-speed recovery facility

There are some scenes in which sound suddenly becomes large like plosive sound in TV Commercial or Movie.

P^2Volume function automatically controls the volume and adjusts the output level. When a sound that pulses and is big is input, the recovery operation is done from 1/4 to 1/32 times the speed.

Use selection of scene change detection function

Default = 0

Select Address	Value	Explanation of operation
High frequency band &h41[4]	0	Not use the scene changing detection
Low frequency band &h41[3]	1	Use the scene changing detection

Setting of release time at operating time when scene change detection function is used (R_RATE)

Release time is as (R_RATE / selection at operating time when scene is detected)

Default = 0

Select Address	Explanation of operation
High frequency band &h45[5:4] Low frequency band &h45[1:0]	

Command	Time
0	4x
1	8x
2	16x
3	32x

Setting of scene change detection time

Default = 0

Select Address	Explanation of operation
High frequency band &h43[6:4] Low frequency band &h44[6:4]	

Command	Detection Time	Command	Detection Time
0	50ms	4	300ms
1	100ms	5	400ms
2	150ms	6	500ms
3	200ms	7	600ms

Behavior level setting of scene change detection function

Begin operation of the difference with the value detected now based on the value immediately before.

Default = 0

Select Address	Explanation of operation
High frequency band &h43[3:0] Low frequency band &h44[3:0]	

Command	Detection level	Command	Detection level
0	-50dB	8	-34dB
1	-48dB	9	-32dB
2	-46dB	A	-30dB
3	-44dB	B	-28dB
4	-42dB	C	-
5	-40dB	D	-
6	-38dB	E	-
7	-36dB	F	-

Selection of 2Band P2Volume composition

The standard is used with 2Band P2Volume, and use as 1Band P^2Volume is also possible.

Select HPF and APF of the crossover filter and select a through setting to compose 1Band P^2Volume.

When using it with 1Band P^2Volume, band on high frequency side is used. Therefore, please set it only for the high frequency side.

[Procedure]

1) &h91 = 12h: Select the HPF of 2Band P^2Volume
2) &h92 = 60h: Select the Filter through
3) &h96 = 01h: Please start to transfer to coefficient RAM
4) &h91 = 13h: Select the APF of 2Band P^2Volume
5) &h92 = 60h: Select the filter through
6) &h96 = 01h: Please start to transfer to coefficient RAM

Please refer to the chapter of 4-8 parametric equalizer for the setting of the crossover filter that divides a high region and a low region of 2Band P^2Volume.

4-6. Surround

Surround 1 emphasizes the stereo feeling, and is suitable for the music source.

Surround 2 is effective of a pseudostereo. Because the monaural voice is pseudomade a stereo, it is suitable for the talk show etc. of the studio recording.

Surround1 function ON/OFF

Default = 0

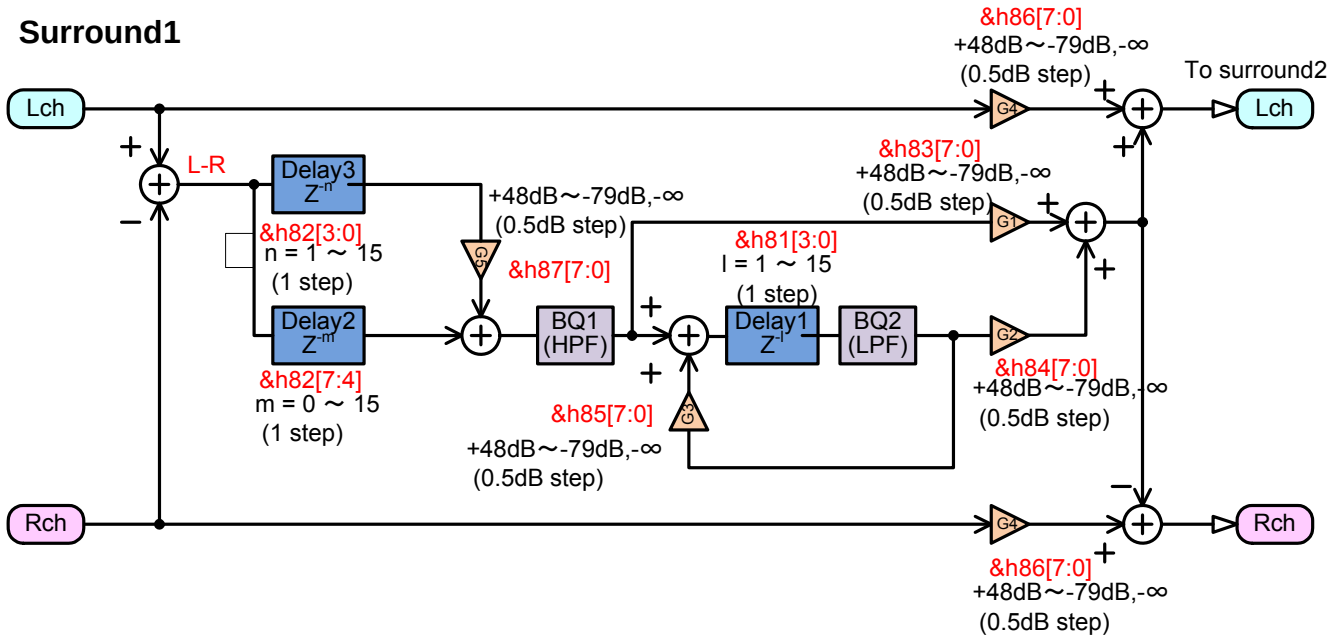
Select Address	Value	Explanation of operation
&h80 [7]	0	Surround1 OFF
	1	Surround1 ON

Surround2 function ON/OFF

Default = 0

Select Address	Value	Explanation of operation
&h80 [6]	0	Surround2 OFF
	1	Surround2 ON

Surround1



Please refer to the chapter of 4-8 parametric equalizer for the setting of BQ1 and BQ2.

BQ1 recommends the setting of High Pass Filter.

BQ2 recommends the setting of Low Pass Filter.

Delay value of feedback part setting for surround effect 1 (Delay1)

Default = 1h

Select Address	Explanation of operation
&h81 [3:0]	The command value becomes the amount of the delay. One sample delay is about 21μs. “0” is a set prohibition.

Delay value of input part setting for surround effect 1 (Delay2)

Default = 0h

Select Address	Explanation of operation
&h82 [7:4]	The command value becomes the amount of the delay. One sample delay is about 21μs.

Delay value of input part setting for surround effect 1 (Delay3)

Default = 1h

Select Address	Explanation of operation
&h82 [3:0]	The command value becomes the amount of the delay. One sample delay is about 21μs. “0” is a set prohibition.

Additive gain setting for surround effect 1 (G1, G2, G3)

Default = FFh

Select Address	Explanation of operation
G1 : &h83 [7:0] G2 : &h84 [7:0] G3 : &h85 [7:0]	Command / Gain 00 / +48dB 01 / +47.5dB ⋮ / ⋮ 60 / 0dB 61 / -0.5dB 62 / -1dB ⋮ / ⋮ FE / -79dB FF / -∞

Additive gain setting for surround effect 1 (G4)

Default = 60h

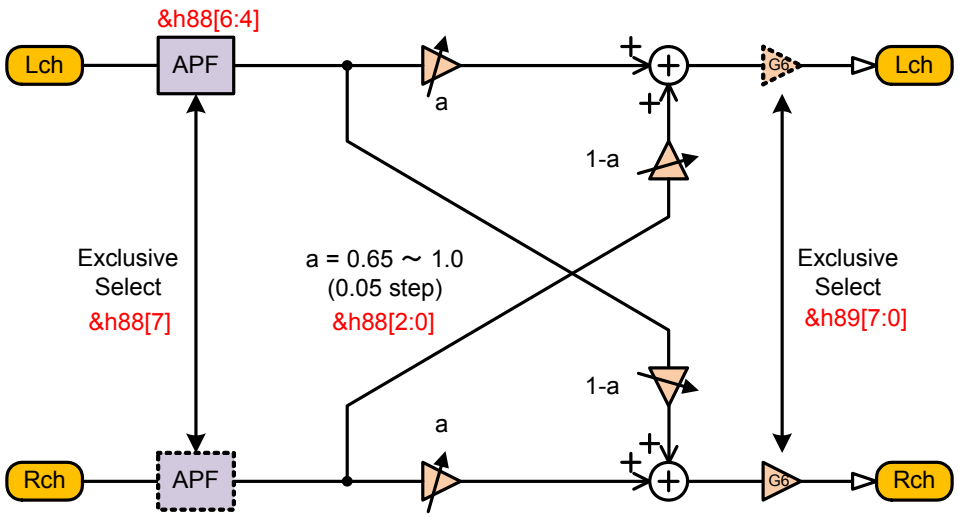
Select Address	Explanation of operation
&h86 [7:0]	Command / Gain 00 / +48dB 01 / +47.5dB ⋮ / ⋮ 60 / 0dB 61 / -0.5dB 62 / -1dB ⋮ / ⋮ FE / -79dB FF / -∞

Additive gain setting for surround effect 1 (G5)

Default = FFh

Select Address	Explanation of operation
&h87 [7:0]	Command / Gain 00 / +48dB 01 / +47.5dB ⋮ / ⋮ 60 / 0dB 61 / -0.5dB 62 / -1dB ⋮ / ⋮ FE / -79dB FF / -∞

Surround2



Select of surround effect 2 APF All Pass Filter)

Select which channel of L/Rch to insert APF.

Default = 0

Select Address	Value	Explanation of operation
&h88 [7]	0	Lch
	1	Rch

Cut off frequency of APF setting for surround effect 2

Default = 0

Select Address	Value	Explanation of operation
&h88 [6:4]	0	22Hz
	1	47Hz
	2	100Hz
	3	220Hz
	4	470Hz

LR mixing gain setting for surround effect 2

Change the LR mix gain in surround effect 2. The sound extends to the setting of about big gain.

Default = 0h

Select Address	Explanation of operation
&h88 [2:0]	

Command	Gain	Command	Gain
0	x0	4	x0.2
1	x0.05	5	x0.25
2	x0.1	6	x0.3
3	x0.15	7	x0.35

Output gain setting for surround effect 2

Change the gain of the channel opposite to the channel selected with &h88 [7].

Default = 60h

Select Address	Explanation of operation
&h89 [7:0]	

Command	Gain
00	+48dB
01	+47.5dB
⋮	⋮
60	0dB
61	-0.5dB
62	-1dB
⋮	⋮
FE	-79dB
FF	-∞

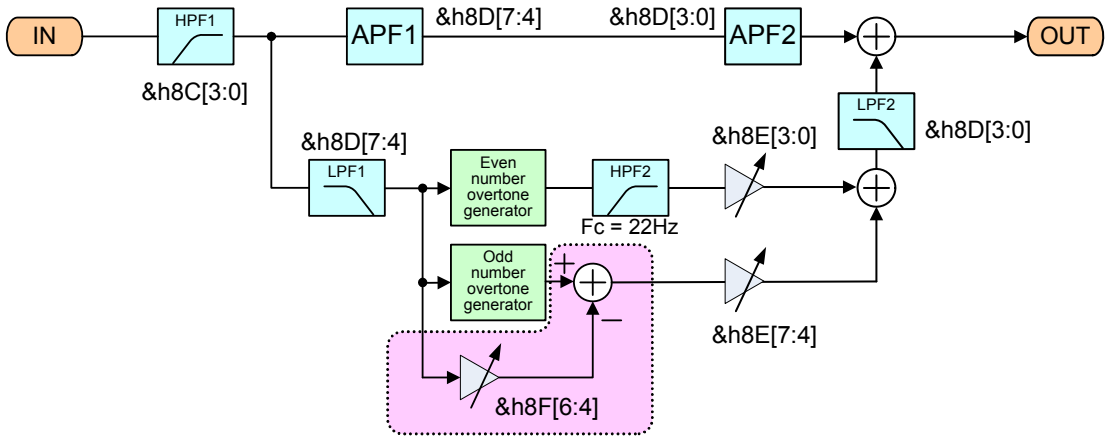
4-7. Pseudo bass (P^2Bass+)

A Pseudo bass function is a function which turns into that it is possible to emphasize low frequency sound effectively also to the low speaker of low-pass reproduction capability.

In order to be audible as the fundamental wave is sounding in false by adding 2 double sounds and 3-time sound to a fundamental wave, the reproduction capability of the band of a fundamental wave becomes possible.

Although use independently is also possible for a pseudo bass function, low-pitched sound can be emphasized more by combining with P2Bass function.

Moreover, since it is possible to change the band to emphasize, optimizing to the frequency characteristic of the speaker to be used is possible.



Pseudobass ON/OFF

The effect of the bass emphasis of a pseudobass (overtone) is used.

Default = 0

Select Address	Value	Explanation of operation
&h8C [7]	0	Not use pseudobass (overtone)
	1	Use pseudobass (overtone)

Setting of pseudo bass input HPF1 (The super-low element of the fundamental harmonic input to the overtone generator can be cut.)

Default = 0h

Select Address	Explanation of operation
&h8C [3:0]	

Command	Frequency	Command	Frequency
0	OFF	8	82Hz
1	22Hz	9	100Hz
2	27Hz	A	120Hz
3	33Hz	B	150Hz
4	39Hz	C	180Hz
5	47Hz	D	220Hz
6	56Hz	E	270Hz
7	68Hz	F	330Hz

Pseudobass input LPF1 selection. (The low element of the fundamental harmonic that the overtone generator inputs is extracted)

Default = 0h

Select Address	Explanation of operation
&h8D [7:4]	

Command	Frequency	Command	Frequency
0	68Hz	8	330Hz
1	82Hz	9	390Hz
2	100Hz	A	470Hz
3	120Hz	B	560Hz
4	150Hz	C	680Hz
5	180Hz	D	820Hz
6	220Hz	E	1000Hz
7	270Hz	F	1200Hz

LPF2 setting for 2 overtones and 3 overtones. (The harmonic content of the overtone is suppressed with this LPF)

Default = 0h

Select Address	Explanation of operation
&h8D [3:0]	

Command	Frequency	Command	Frequency
0	68Hz	8	330Hz
1	82Hz	9	390Hz
2	100Hz	A	470Hz
3	120Hz	B	560Hz
4	150Hz	C	680Hz
5	180Hz	D	820Hz
6	220Hz	E	1000Hz
7	270Hz	F	1200Hz

Additive gain setting for 3 overtones

When the input of the fundamental wave component is assumed to be 0dB, the output of the fundamental wave component from the overtone generator becomes -3dB.

(Output = Input - 3dB)

Default = 7h

Select Address	Explanation of operation
&h8E [7:4]	

Command	Gain	Command	Gain
0	-∞	8	7dB
1	0dB	9	8dB
2	1dB	A	9dB
3	2dB	B	10dB
4	3dB	C	11dB
5	4dB	D	12dB
6	5dB	E	13dB
7	6dB	F	14dB

Additive gain setting for 2 overtones

When the input of the fundamental wave component is assumed to be 0dB, the output from the overtone generator becomes -6dB.

(Output = Input - 6dB)

Default = 7h

Select Address	Explanation of operation

Command	Gain	Command	Gain
0	-∞	8	1dB
1	-6dB	9	2dB
2	-5dB	A	3dB
3	-4dB	B	4dB
4	-3dB	C	5dB
5	-2dB	D	6dB
6	-1dB	E	7dB
7	0dB	F	8dB

Subtraction gain setting for 3 overtones (recommendation value: -8dB or -6dB)

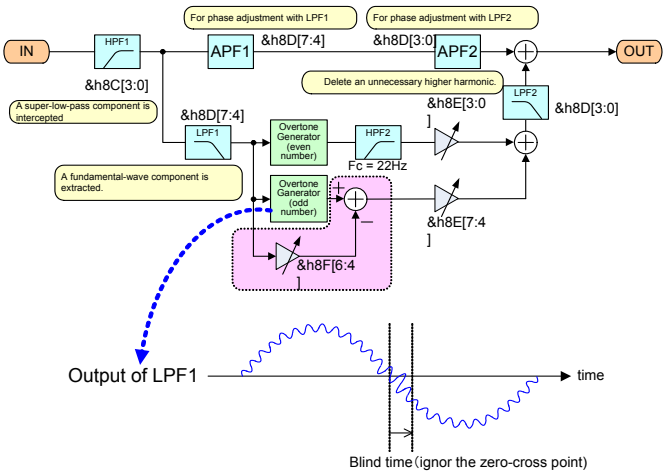
Default = 4h

Select Address	Explanation of operation

Command	Gain	Command	Gain
0	-∞	4	-6dB
1	-12dB	5	-4dB
2	-10dB	6	-2dB
3	-8dB	7	0dB

Setting at blind time of odd-order overtone generation circuit

The high frequency signal that cannot be attenuated with LPF is included in the LPF1 outgoing signal input to the overtone generation circuit. It is set the blind time to do an unnecessary zero-cross point masking.



Default = 0

Select Address	Value	Explanation of operation
&h8F [1:0]	0	1.25ms (LPF1 Fc = 47Hz to 180Hz)
	1	0.625ms (LPF1 Fc = 220Hz to 390Hz)
	2	0.3125ms (LPF1 Fc = 470Hz to 800Hz)

4-8. Parametric Equalizer

In this IC, the following block has the feature of the parametric equalizer.

Crossover filter of the P2Volume block, Two BQ (Bi-Quad Filter) of surround 1 block, 8Band BQ (Main-output), 1Band BQ (Sub-output), Four BQ of Main clossover filter block, Four BQ of Sub clossover filter, Clossover filter of 2Band DRC block and BQ of the smooth transition.

The shape is used peaking filter, low shelf filter, high shelf filter, lowpass filter, highpass filter and all path filter.

The setting is to choose F, Q, Gain, and changes into the coefficient of the digital filter in the IC and it transfers to the coefficient RAM. 8Band BQ (Main) and 1Band BQ (Sub) have the soft transfer feature. Incidentally, the detailed order of the parameter setting refer to the following PEQ setting method.

The coefficient RAM that stores a filter coefficient owns four banks and the command can choose it. The coefficient RAM for the parametric equalizer can set a coefficient to the bank-memory but the bank-memory during sound reconstruction.

Select of bank memory for coefficient RAM used to reproduce

Default = 0h

Select Address	Value	Explanation of operation
&hA1 [7:6]	0	BANK1
	1	BANK2
	2	BANK3
	3	BANK4

Select of bank memory used to set coefficient

Default = 0h

Select Address	Value	Explanation of operation
&hA1 [5:4]	0	BANK1
	1	BANK2
	2	BANK3
	3	BANK4

Sampling frequency selection of coefficient automatic calculated circuit

Default = 0h

Select Address	Value	Explanation of operation
&h90 [1:0]	0	For 48kHz
	1	For 44.1kHz
	2	For 32kHz

Select of PEQ setting
Lch and Rch are set same value.

Default = 00h

Select Address	Explanation of operation

&h91 [4:0]

Command	PEQ	Command	PEQ	Command	PEQ	Command	PEQ
00	8BandBQ(1)	08	1BandBQ	10	Sub XOVF BQ4	18	-
01	8BandBQ(2)	09	Main XOVF BQ1	11	Smooth Tran.BQ	19	-
02	8BandBQ(3)	0A	Main XOVF BQ2	12	P^2Volume HPF	1A	-
03	8BandBQ(4)	0B	Main XOVF BQ3	13	P^2Volume APF	1B	-
04	8BandBQ(5)	0C	Main XOVF BQ4	14	2BandDRC HPF	1C	-
05	8BandBQ(6)	0D	Sub XOVF BQ1	15	2BandDRC APF	1D	-
06	8BandBQ(7)	0E	Sub XOVF BQ2	16	Surround HPF	1E	-
07	8BandBQ(8)	0F	Sub XOVF BQ3	17	Surround LPF	1F	-

8Band BQ, 1Band BQ:
BQ is Bi-Quad-type digital filter.
BQ for smooth transition:
It is a filter without the switch shock sound to do as for the coefficient setting and the change of 8Band BQ and 1Band BQ.
Main/Sub XOVF (CrossOver Filter):
The crossover filter of the eighth Linkwitz-Riley type can be composed by using four BQ.
P^2Volume HPF/APF:
The crossover filter of 2Band P2Volume block should be set to high path filter and all pass filter.
2 Band DRC HPF/APF:
The crossover filter of 2Band DRC block should be set to high path filter and all pass filter.
Surround HPF/LPF:
BQ1 recommends the setting of high pass filter, and BQ2 recommends the setting of low pass filter to two BQ in the surround block.

Select of filter type

Default = 0h

Select Address	Value	Explanation of operation
&h92 [6:4]	0	Peaking Filter
	1	Low Shelf Filter
	2	High Shelf Filter
	3	Low Pass Filter
	4	High Pass Filter
	5	All Pass Filter
	6	Filter through

Select of smooth transition

Default = 0h

Select Address	Value	Explanation of operation
&h92 [2]	0	Use smooth transition
	1	Not use smooth transition

Setting of smooth transition time

Default = 0h

Select Address	Value	Explanation of operation
&h92 [1:0]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

Setting of frequency (F_0)

Default = 0Eh

Select Address	Explanation of operation
&h93 [5:0]	

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	-
06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	-
07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	-

Setting of quality factor (Q)

Default = 5h

Select Address	Explanation of operation
&h94 [4:0]	

Command	Q	Command	Q	Command	Q	Command	Q
00	0.33	08	1.2	10	5.6	18	1.932
01	0.39	09	1.5	11	6.8	19	0.51
02	0.47	0A	1.8	12	8.2	1A	0.601
03	0.56	0B	2.2	13	0.707	1B	0.9
04	0.68	0C	2.7	14	0.541	1C	2.563
05	0.75	0D	3.3	15	1.307	1D	-
06	0.82	0E	3.9	16	0.518	1E	-
07	1.0	0F	4.7	17	0.707	1F	-

Second butterworth is set to 13h. (BQx1) Fourth butterworth is set to 14h, 15h. (BQx2)
Sixth butterworth is set to 16h, 17h, 18h. (BQx1) Eighth butterworth is set to 19h, 1Ah, 1Bh, 1Ch. (BQx4)

Setting of gain (Gain)

Default = 40h

Select Address	Explanation of operation
&h95 [6:0]	

Command	Gain
1C	-18dB
⋮	⋮
38	-1dB
39	-0.5dB
40	0dB
41	+0.5dB
42	+1dB
⋮	⋮
64	+18dB

When the each coefficient (b0, b1, b2, a1, a2) exceeds ±4, it is not possible to set it.

Transfer start setting to coefficient RAM

Default = 0

Select Address	Value	Explanation of operation
&h96 [0]	0	Transfer stop
	1	Transfer start (After transferring is completed, it becomes 0 by the automatic operation.)

Setting of smooth transition start

Default = 0

Select Address	Value	Explanation of operation
&h97 [0]	0	Stop the smooth transition operation
	1	Start the smooth transition operation (After the transition is completed, it becomes 0 by the automatic operation)

* This register cannot read-out.

Read-out smooth transition status

Select Address	Explanation of operation
&h98 [0]	"1" is read while software is changing. "0" is read usually.

[Attention] The data of coefficient RAM can be read. Set values such as F, Q, and Gain cannot be read.

[Example of coefficient setting procedure 1]

Ex) Set fc=1kHz, Q=1.0, Gain=+6dB, and Filter type=Peaking Filter to 8Band BQ1 by using the soft transition function.
Sampling frequency: fs=48kHz, Smooth transition time: 21.4ms, Bank memory: BANK0

1) &hA1 [7:6] = 0h *1 : Set the BANK0
2) &hA1 [5:4] = 0h *1 : Set the BANK0
3) &h90 [1:0] = 0h : Set sampling frequency to 48 kHz
4) &h91 [4:0] = 00h : Select 8Band BQ1
5) &h92 [7:0] = 00h
   &h92 [6:4] = 0h : Select Peaking Filter
   &h92 [2] = 0h : Use smooth transition
   &h92 [1:0] = 0h : Set smooth transition time to 21.4ms
6) &h93 [5:0] = 22h : Set frequency to 1 kHz (f0)
7) &h94 [4:0] = 07h : Set quality factor to 1.0
8) &h95 [6:0] = 4Ch : Set gain level to +6dB
9) &h96 [0] = 1h : Transferring start to coefficient RAM for smooth transition
   (After transferring is completed, it is cleared automatically to 0h.)
10) Even the transferring completion waits for about 150µs.
11) &h97 [0] = 1h : Smooth transition start
   (After smooth transition is completed, it is cleared automatically to 0h.)
12) About 21.4ms stands by to the smooth transition completion. Or, it stands by until 0 is read, and command &h98 is cleared to 0h.

*1 When the clock stop automatic return function is made effective, &hA1 [5:4] is set by the automatic operation depending on the input sampling frequency. (However, the value of this register is not reflected.)
Therefore, if the coefficient is written, the setting of &hA1 [5:4] should set 0h when the input sampling frequency is 48kHz. And it should be set to 1h when sampling frequency is 44.1kHz.

[Example of coefficient setting procedure 2]

Ex) Set fc=200Hz, Q=0.707 and Filter type=Peaking Filter to 1Band BQ by using the soft transition function.

1) &hA1 [5:4] = 0h : Set BANK0
2) &h90 [1:0] = 1h : Set sampling frequency to 44.1 kHz
3) &h91 [4:0] = 08h : Select 1Band BQ
4) &h92 [7:0] = 34h
   &h92 [6:4] = 3h : Select Low Pass Filter
   &h92 [2] = 1h : Not use smooth transition
5) &h93 [5:0] = 14h : Set frequency to 200Hz (F0)
6) &h94 [4:0] = 17h : Set quality factor to 0.707 (Q)
7) &h95 [6:0] = 40h : Because Low Pass Filter was selected; the setting of the gain can be omitted.
8) &h96 [0] = 1h : Transferring start to coefficient RAM for smooth transition
   (After transferring is completed, it is cleared automatically to 0h.)
9) Even the transferring completion waits for about 150µs.

4-9. Scaler

Scaler adjusts the gain in order to prevent the overflow in DSP. Adjustable range is +24dB to -79dB and can be set by the step of 0.5dB. Scaler 1 does not incorporate the smooth transition function.

Default = 60h

<table>
<tr><th>Select Address</th><th>Explanation of operation</th></tr>
<tr><td>&h23 [7:0]</td><td>
<table>
<tr><th>Command</th><th>Gain</th></tr>
<tr><td>00</td><td>+48dB</td></tr>
<tr><td>01</td><td>+47.5dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>60</td><td>0dB</td></tr>
<tr><td>61</td><td>-0.5dB</td></tr>
<tr><td>62</td><td>-1dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>FE</td><td>-79dB</td></tr>
<tr><td>FF</td><td>-∞</td></tr>
</table>
</td></tr>
</table>

4-10. 512 Tap FIR Filter x 2ch

The FIR filter of 512 taps is used for adjusting speaker characteristics for a flat or preparing the acoustic feature of a listening room.

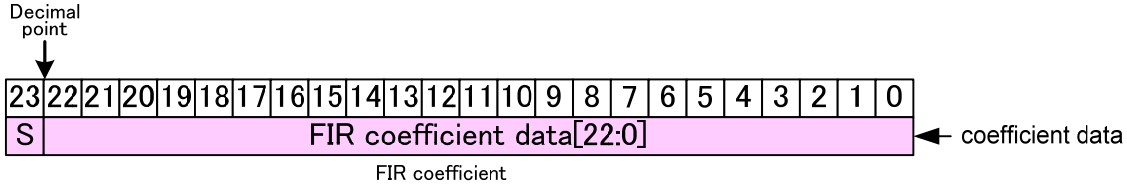
Many bands near the adjustment point influence and P-EQ of the IIR type filter mutually. Although a desirable result is obtained, the number of times of an IIR filter of trial and error may increase.

Since a FIR filter has many Tap numbers, it can be brought close to an ideal acoustic feature easily.

Moreover, when doing fine adjustment with a P-EQ filter, a “ringing noise” and a “smearing (dirt of sound) noise” may occur. With a FIR filter, it is satisfactory.

Straighten the sound characteristic of the audio all bandwidth by using 512Tap FIR Filter for the music centre of two way compositions. Afterwards, use 4BQ Crossover filter and divide into the frequency for the tweeter and for woofer. The number of taps of FIR filters becomes 512 taps or less per channel. A characteristic that three operation modes, and is different by Lch and Rch can be set.

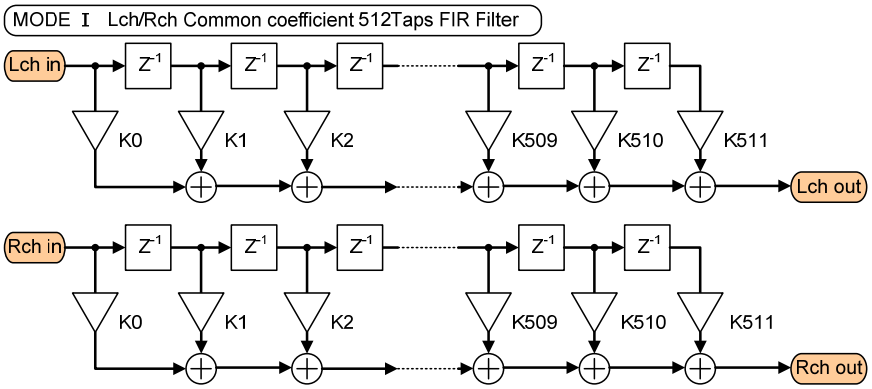
The coefficient expresses ±1 by 24bit composition.

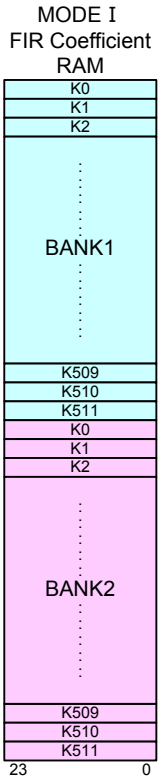


MODE Ⅰ 512 Taps mode (The coefficient of Lch/Rch is common.)

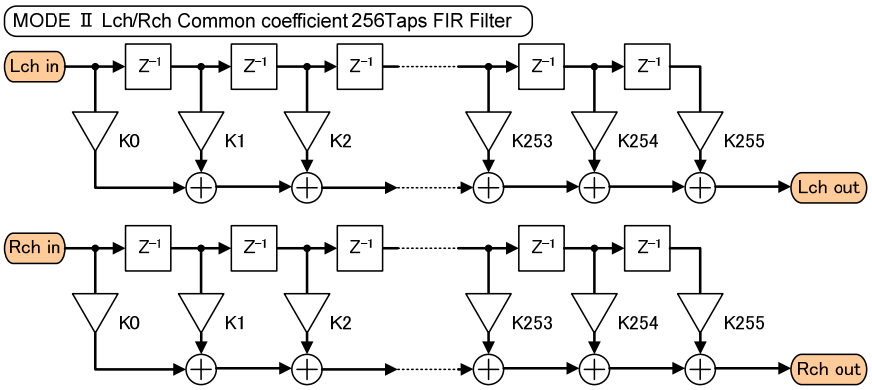
・Coefficient RAM is 2 BANK system.

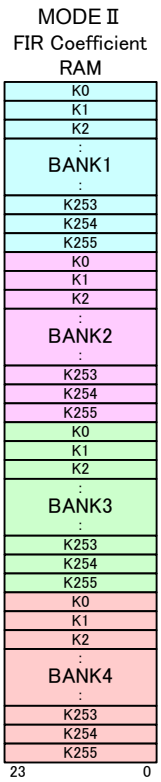
・257Taps to 512 Taps (Empty Tap is “0“)



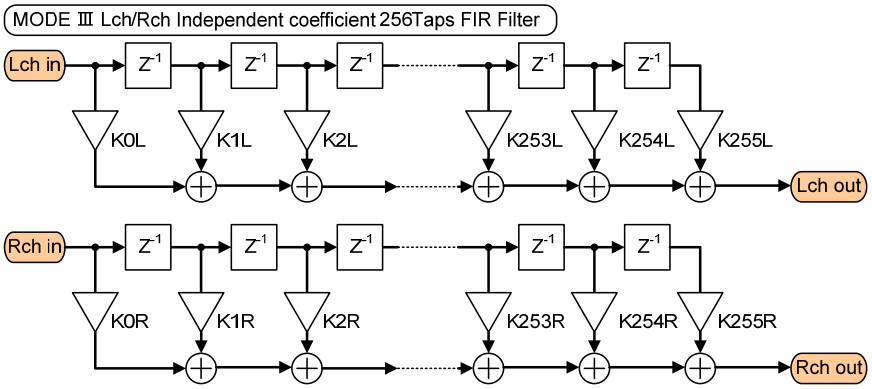


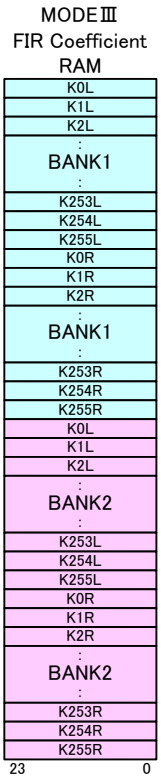
MODE Ⅱ 256 Taps mode (The coefficient of Lch/Rch is common.)
・Coefficient RAM is 4 BANK system.
・64 Taps to 256 Taps (Empty Tap is “0“)





MODE Ⅲ 256 Taps mode (The coefficient of Lch/Rch is independence.)
・Coefficient RAM is 2 BANK system.
・64 Taps to 256 Taps (Empty Tap is “0“)





FIR filter mode setting

Default = 0h

Select Address	Value	Explanation of operation
&hA0 [1:0]	0	MODE Ⅰ:512Tap to 257Tap (Lch/Rch same coefficient)
	1	MODE Ⅱ:256Tap to 64Tap (Lch/Rch same coefficient)
	2	MODE Ⅲ:256Tap to 64Tap (Lch/Rch independent coefficient)

FIR filter bank memory setting

Default = 0h

Select Address	Value	Explanation of operation
&hA1 [3:2]	0	BANK1
	1	BANK2
	2	BANK3
	3	BANK4

When MODE Ⅰ and MODE Ⅲ are used, BANK3 and 4 cannot be selected.

Memory address specification of Filter coefficient
It is used &hA2 and &hA3 commands when you write the coefficient of the FIR filter.

・MODE Ⅰ (Lch/Rch same coefficient)

24bit Coefficient Number	&hA2	&hA3
K0	00	00
K1	00	01
K2	00	02
:	:	:
K255	00	FF
K256	01	00
K257	01	01
:	:	:
K509	01	FD
K510	01	FE
K511	01	FF

・MODE Ⅱ (Lch/Rch same coefficient)

24bit Coefficient Number	&hA2	&hA3
K0	00	00
K1	00	01
K2	00	02
:	:	:
K253	00	FD
K254	00	FE
K255	00	FF

・MODEⅢ(Lch/Rch independent coefficient)

24bit Coefficient Number	&hA2	&hA3	24bit Coefficient Number	&hA2	&hA3
K0L	00	00	K0R	01	00
K1L	00	01	K1R	01	01
K2L	00	02	K2R	01	02
:	:	:	:	:	:
K253L	00	FD	K253R	01	FD
K254L	00	FE	K254R	01	FE
K255L	00	FF	K255R	01	FF

About transferring coefficient data to coefficient RAM

Transferring 24bits coefficient to coefficient RAM specified with &hA2 and &hA3.

Default = 0h

Select Address	Value	Explanation of operation
&hA7 [0]	0	Stop transferring
	1	Start transferring

After forwarding is completed, it is cleared to "0" automatically.

[Procedure 1] Writing sequence

1) &hA0 = 00h : Select MODE Ⅰ
2) &hA1 = *0h : Select BANK0
3) &hA2 = 00h : When the address of K256 or more is specified, it is assumed 01h.
4) &hA3 = 00h : Memory address specification in which coefficient is written
5) &hA4 = **h : Specify the coefficient data [23:16]
6) &hA5 = **h : Specify the coefficient data [15:7]
7) &hA6 = **h : Specify the coefficient data [7:0]
8) &hA7 = 01h : Transferring start to coefficient RAM
9) Wait for more than 100μs.

Repeat procedure from 4) to 9) when continuously writing it. (When the address of K256 or more is specified, it is set &hA2 to 01h.)

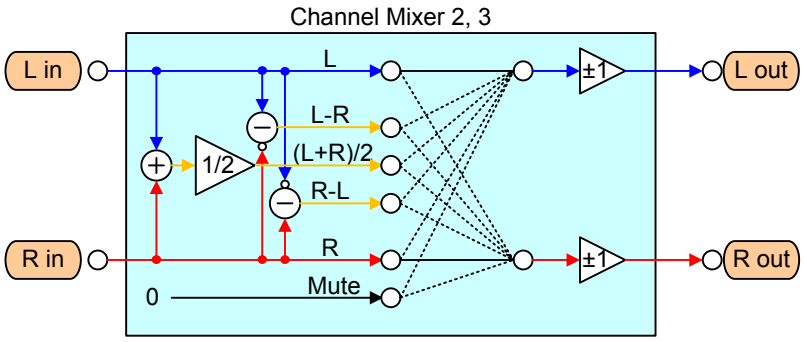
[Procedure 2] Reading sequence

1) &hA1 = *0h : Select BANK0
2) &hA2 = 00h : When the address of K256 or more is specified, it is assumed 01h.
3) &hA3 = 00h : Memory address specification in which coefficient is read
4) &hD0 = ABh : Set reading register address
5) Read upper 8bits ([23:16]) among coefficients 24bit. (&hAB[7:0])
6) Read middle 8bits ([15:8]) among coefficients 24bit. (&hAC[7:0])
7) Read lower 8bits ([7:0]) among coefficients 24bit. (&hAD[7:0])

Repeat procedure from 3) to 7) when continuously reading it. (When the address of K256 or more is specified, it is set &hA2 to 01h.)

4-11. Channel setting with phase inversion function (Channel Mixer 2, 3)

Set the mixing of the sound of a left channel and a right channel of the digital signal output from DSP. The output of making to monaural from the stereo signal can be done. The difference signal of Lch and Rch can be output. Moreover, the phase inversion and the mute of each channel can be set. Channel Mixer2 is for the Main-output. Channel Mixer3 is for the Sub-output.



Invert the output data to L out.

Default = 0

Select Address	Value	Explanation of operation
Mixer2 &h26 [7] Mixer3 &h27 [7]	0	Normal (Not invert)
	1	Invert

Select the output data to L out

Default = 1

Select Address	Value	Explanation of operation
Mixer2 &h26 [6:4] Mixer3 &h27 [6:4]	0	Mute
	1	Output the data of L in
	2	Output the data of R in
	3	Output the data of (Lch + Rch) / 2
	4	Output the data of (Lch – Rch)
	5	Output the data of (Rch – Lch)

Invert the output data to R out.

Default = 0

Select Address	Value	Explanation of operation
Mixer2 &h26 [3] Mixer3 &h27 [3]	0	Normal (Not invert)
	1	Invert

Select the output data to R out

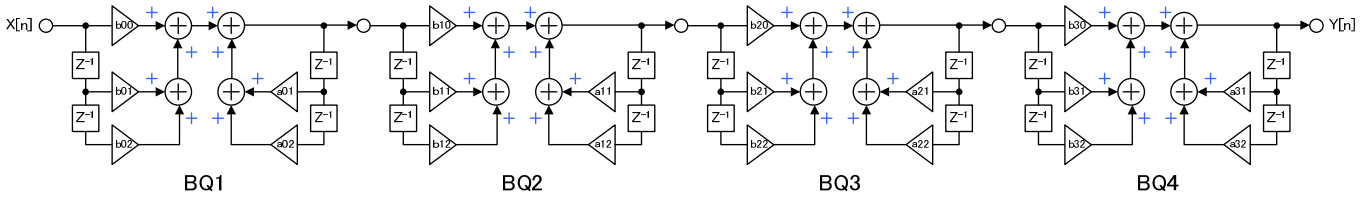
Default = 2

Select Address	Value	Explanation of operation
Mixer2 &h26 [2:0] Mixer3 &h27 [2:0]	0	Mute
	1	Output the data of L in
	2	Output the data of R in
	3	Output the data of (Lch + Rch) / 2
	4	Output the data of (Lch – Rch)
	5	Output the data of (Rch – Lch)

4-12. 4 Band BQ x 2ch for Cross Over Filter (Main, Sub)

It is 4Band Bi-Quad Filter that can be used as Linkwitz-Riley type crossover filter.

- Lch/Rch simultaneous control
- Four coefficient memory bank function
- A coefficient automatic calculating mode and a direct set mode can be used.
- The filter property can be changed by the soft transition function while reproducing.



Refer to the chapter of 4-8 parametric equalizer for the setting.

4-13. Volume

Volume is from+24dB to -103dB, and can be selected by the step of 0.25dB. At the time of switching of Volume, smooth transition is performed. Soft transition duration is optional with the command.

It becomes the following formula at the transition from AdB to BdB. C is smooth transition duration selected by &h20 [5:4] command.

$$\text{Transition time} = \left|\left(10^{\frac{A}{20}} - 10^{\frac{B}{20}}\right) * C \text{ ms}\right|$$

Setting of soft transition time

Default = 0

Select Address	Value	Explanation of operation
&h20 [5:4]	0	21.4ms
	1	42.7ms
	2	85.4ms

Setting of volume

Default = FFh

Select Address	Explanation of operation
Main &h11 [7:0] Sub &h13 [7:0] Moni1 &h15 [7:0] Moni2 &h17 [7:0]	Command / Gain 00 +24dB 01 +23.5dB ⋮ ⋮ 30 0dB 31 -0.5dB 32 -1dB ⋮ ⋮ FE -103dB FF -∞

Setting of fine volume

This command becomes effective by sending the following command after setting.

When using this command, it is possible to set a volume in 0.125dB carving.

Setting of fine volume

Default = 0h

Select Address	Value	Explanation of operation
Main &h10 [1:0]	0	0dB
Sub &h12 [1:0]	1	-0.125dB
Moni1 &h14 [1:0]	2	-0.25dB
Moni2 &h16 [1:0]	3	-0.375dB

[Note1]

It is possible to use with the 0.5-dB step in changing only &h11 [7:0] when &h10 [1:0] =0.

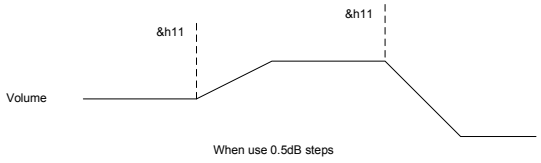
(Sub, Moni1 and Moni2 are the same)

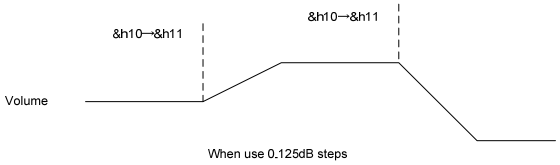
[Note2]

It is possible to use with the 0.125-dB step in setting both &h10 [1:0] and &h11 [7:0]. (Sub, Moni1 and Moni2 are the same)

In case of &h10 [1:0] =0, it becomes the set value of &h11 [7:0].
In case of &h10 [1:0] =1, it becomes the -0.125dB set value of &h11 [7:0].
In case of &h10 [1:0] =2, it becomes the -0.25dB set value of &h11 [7:0].
In case of &h10 [1:0] =3, it becomes the -0.375dB set value of &h11 [7:0].

Because it is fixed by the transfer of &h11 in any case, the soft transfer can be beforehand begun in the set value for the direct following of the purpose in setting &h11 after setting in &h10.





4-14. Balance

As for balance, it is possible to be attenuated at 1dB step width from volume setting value. The switch operation becomes a smooth transition. When the balance changes, smooth transition is done. Smooth transition duration becomes the same formula as the volume.

Setting of L/R balance

Default = 80h

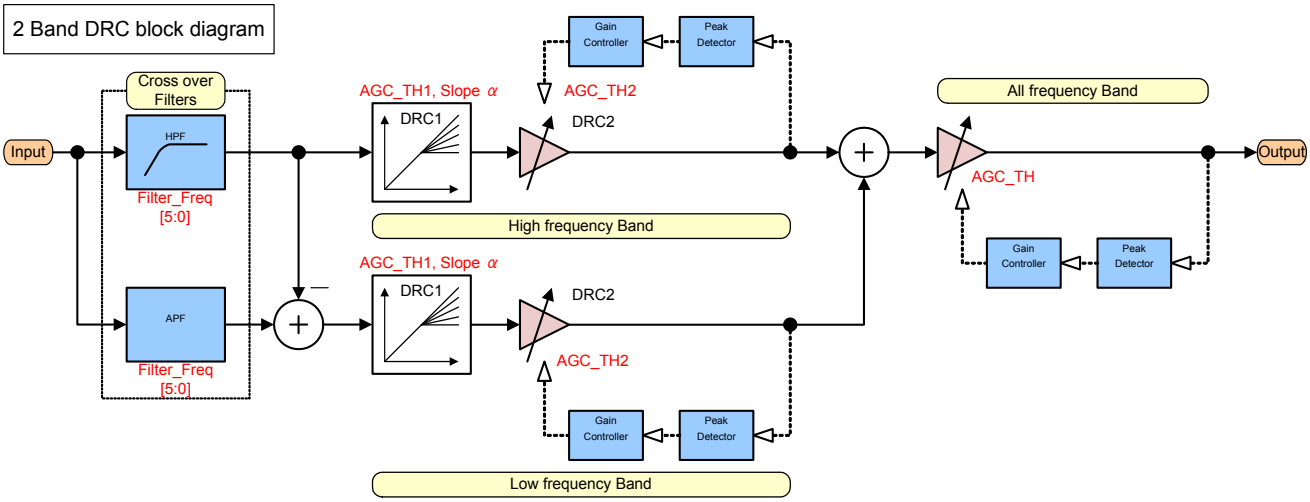
Select Address	Explanation of operation
Main &h18 [7:0] Sub &h19 [7:0] Moni1 &h1A [7:0] Moni2 &h1B [7:0]	

Command	Lch	Rch
00	0dB	-∞
01	0dB	-126dB
⋮	⋮	⋮
7E	0dB	-1dB
7F	0dB	0dB
80	0dB	0dB
81	-1dB	0dB
⋮	⋮	⋮
FE	-126dB	0dB
FF	-∞	0dB

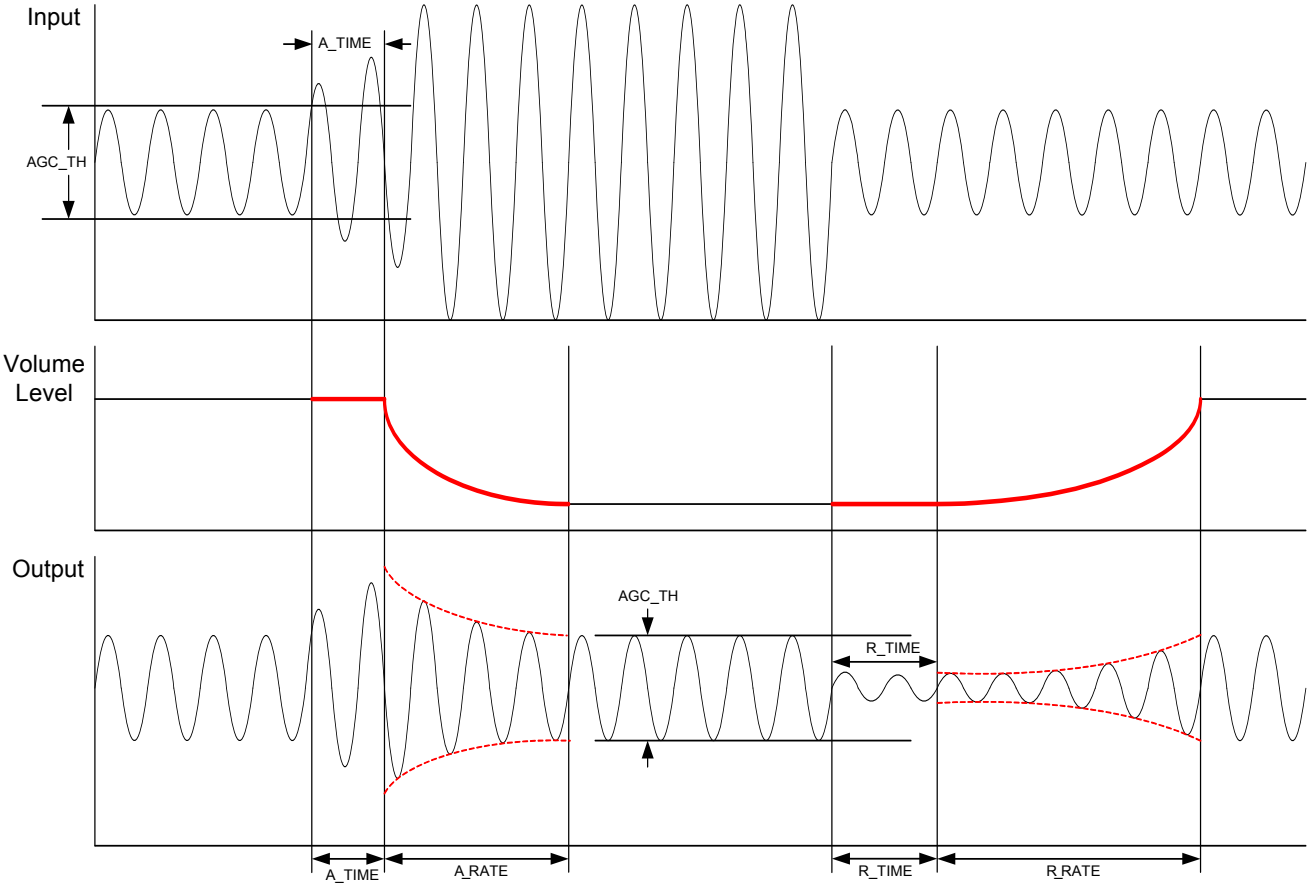
4-15. 2 band DRC (Main)

This DRC is used in order to prevent speaker protection and the clip output of a large audio signal.

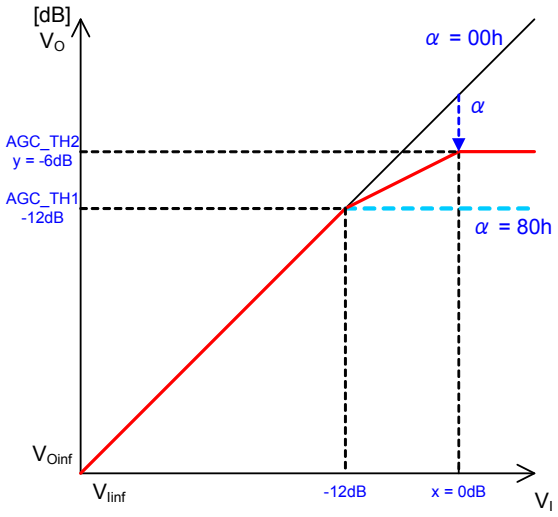
In addition to two bands of DRC for low and high frequency, there is DRC for the whole frequency in the latter part. Non-clip output is possible. DRC for low frequency band and DRC for high frequency band can set up two threshold value levels. Moreover, it is possible to also change slope.



DRC transition figure



DRC input-and-output gain characteristics



The formula which asks for Slope alpha is described below.

Alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation.

$$\alpha = \frac{10^{\frac{y}{20}} - 10^{\frac{x}{20}}}{10^{\frac{TH}{20}} - 10^{\frac{x}{20}}} \times 128$$

TH is AGC_TH1. x is input level. y is output level.

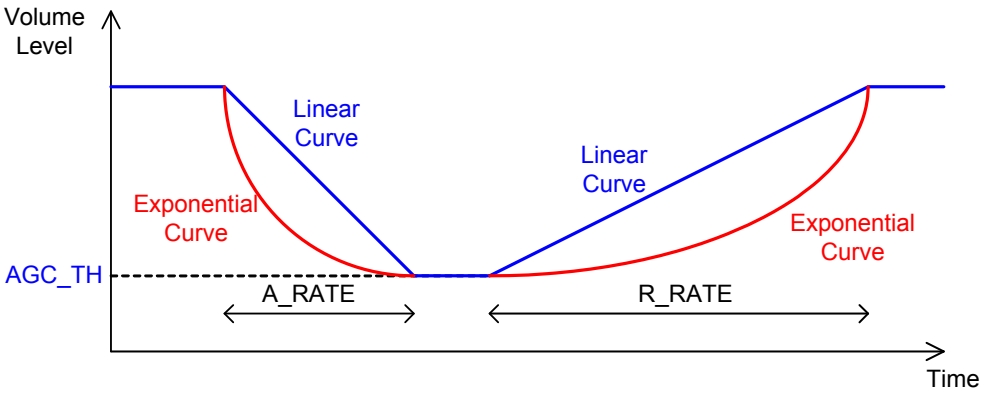
Ex) It asks for alpha at the time of AGC_TH1 = -12dB, x = 0dB y = -6dB

$$\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{0}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{0}{20}}} \times 128$$

α = 85.266 → 55_H

55_H calculated is set as &h25 or &h2A

Volume Curve



ON/OFF setting of DRC for all frequency band.

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h40[1]	0	Not use
	1	Use

ON/OFF setting of DRC1 for high frequency band. (DRC which can perform slope variable)

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h40[5]	0	Not use
	1	Use

ON/OFF setting of DRC2 for high frequency band. (Compressor)

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h40[4]	0	Not use
	1	Use

ON/OFF setting of DRC1 for low frequency band. (DRC which can perform slope variable)

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h40[3]	0	Not use
	1	Use

ON/OFF setting of DRC2 for low frequency band. (Compressor)

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h40[2]	0	Not use
	1	Use

The volume curve at the time of an attack (A_RATE) is selected.

Default = 0

Select Address	Value	Explanation of operation
&h42[7]	0	Linear curve
	1	Exponential curve

The volume curve at the time of a release (R_RATE) is selected.

Default = 0

Select Address	Value	Explanation of operation
&h42[3]	0	Linear curve
	1	Exponential curve

The choice of the DRC composition

It uses a standard in 2Band DRC but it is possible to use as 1Band DRC, too.

To make the composition of 1Band DRC, it chooses through setting in HPF and APF of the crossover filter.

[Procedure]

1) &h91 = 14h: It chooses HPF of the 2Band DRC.
2) &h92 = 60h: It chooses Filter through.
3) &h96 = 01h: It starts a transfer to the coefficient RAM.
4) &h91 = 15h: It chooses APF of 2Band DRC.
5) &h92 = 60h: It chooses Filter through.
6) &h96 = 01h: It starts a transfer to the coefficient RAM.

To set the crossover filter which divides the high frequency band and the low frequency band of 2Band DRC, therefore, it is referred to the chapter 4-8.

AGC_TH setting of DRC for all band.
When using according to either of the DRC for the high area or the DRC for the low area bigger AGC_TH setting, the distortion in the crossover point can be suppressed.

Default = 40h

Select Address	Explanation of operation
&h70[6:0]	

Command	Threshold
00	-32dB
⋮	⋮
3F	-0.5dB
40	0dB
41	+0.5dB
⋮	⋮
58	+12dB

A_RATE setting of DRC for all band. (The compression curve transition time in attack)

Default = 3h

Select Address	Explanation of operation
&h72[6:4]	

Command	A_RATE time	Command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

R_RATE setting of DRC for all band. (The expansion curve transition time in release)

Default = Bh

Select Address	Explanation of operation
&h72[3:0]	

Command	R_RATE time	Command	R_RATE time
0	0.125s	8	2s
1	0.1825s	9	2.5s
2	0.25s	A	3s
3	0.5s	B	4s
4	0.75s	C	5s
5	1s	D	6s
6	1.25s	E	7s
7	1.5s	F	8s

A_TIME setting of DRC for all band. (Setting of detection time for attack operation)

Default = 1h

Select Address	Explanation of operation
&h73 [7:4]	

Command	A_TIME time	Command	A_TIME time
0	0ms	8	6ms
1	0.5ms	9	7ms
2	1ms	A	8ms
3	1.5ms	B	9ms
4	2ms	C	10ms
5	3ms	D	20ms
6	4ms	E	30ms
7	5ms	F	40ms

R_TIME setting of DRC for all band. (Setting of detection time for release operation)

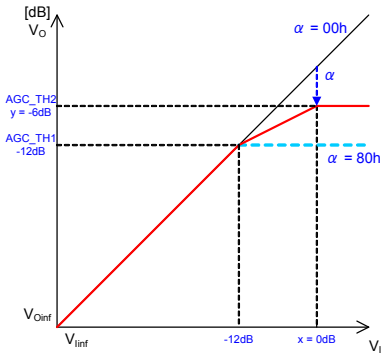
Default = 3h

Select Address	Explanation of operation
&h73 [2:0]	

Command	R_TIME time	Command	R_TIME time
0	5ms	4	100ms
1	10ms	5	200ms
2	25ms	6	300ms
3	50ms	7	400ms

Slope (α) setting of DRC1 for high frequency band

Default = 80h

Select Address	Explanation of operation
&h61 [7:0]	 The formula which asks for Slope alpha is described below. Alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation. $\alpha = \frac{10^{\frac{y}{20}} - 10^{\frac{x}{20}}}{10^{\frac{TH}{20}} - 10^{\frac{x}{20}}} \times 128$ TH is AGC_TH1. x is input level. y is output level. Ex) It asks for alpha at the time of AGC_TH1 = -12dB, x = 0dB y = -6dB $\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{0}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{0}{20}}} \times 128$ $\alpha = 85.266 \rightarrow 55_H$ 55H calculated is set as &h61 or &h69

AGC_TH1 setting of DRC1 for high frequency band

Please set below to the setting value of AGC_TH2.

Default = 40h

Select Address	Explanation of operation
&h60 [6:0]	Command / Threshold 00 / -32dB ⋮ / ⋮ 3F / -0.5dB 40 / 0dB 41 / +0.5dB ⋮ / ⋮ 58 / +12dB

AGC_TH2 setting of DRC2 for high frequency band

Default = 40h

Select Address	Explanation of operation
&h64 [6:0]	Command / Threshold 00 / -32dB ⋮ / ⋮ 3F / -0.5dB 40 / 0dB 41 / +0.5dB ⋮ / ⋮ 58 / +12dB

High frequency band A_RATE setting (It is the transition time of a compression curve at the time of an attack.)
DRC1 and DRC2 for high frequency band are individually setting.
Default = 3h

Select Address	Explanation of operation
DRC1 &h62 [6:4] DRC2 &h66 [6:4]	

Command	A_RATE time	Command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

High frequency band R_RATE setting (It is the transition time of an extension curve at the time of release.)
DRC1 and DRC2 for high frequency band are individually setting.
Default = Bh

Select Address	Explanation of operation
DRC1 &h62[3:0] DRC2 &h66[3:0]	

Command	R_RATE time	Command	R_RATE time
0	0.125s	8	2s
1	0.1825s	9	2.5s
2	0.25s	A	3s
3	0.5s	B	4s
4	0.75s	C	5s
5	1s	D	6s
6	1.25s	E	7s
7	1.5s	F	8s

A_TIME1 setting of DRC1 for high frequency band (Detection time setting of attack operation)
DRC1 and DRC2 for high frequency band are individually setting.
Default = 1h

Select Address	Explanation of operation
DRC1 &h63 [7:4] DRC2 &h67 [7:4]	

Command	A_TIME time	Command	A_TIME time
0	0ms	8	6ms
1	0.5ms	9	7ms
2	1ms	A	8ms
3	1.5ms	B	9ms
4	2ms	C	10ms
5	3ms	D	20ms
6	4ms	E	30ms
7	5ms	F	40ms

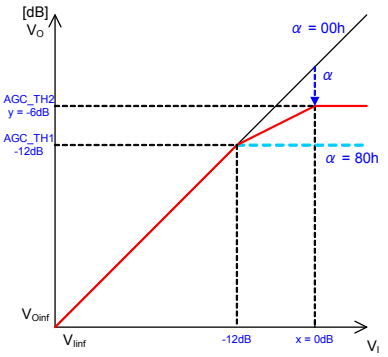
R_TIME setting of DRC for high frequency band (Detection time setting of release operation)
DRC1 and DRC2 for high frequency band are individually setting.
Default = 3h

Select Address	Explanation of operation
DRC1 &h63 [2:0] DRC2 &h67 [2:0]	

Command	R_TIME time	Command	R_TIME time
0	5ms	4	100ms
1	10ms	5	200ms
2	25ms	6	300ms
3	50ms	7	400ms

Slope (α) setting of DRC1 for low frequency band

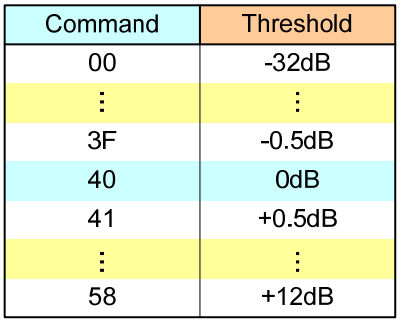
Default = 80h

Select Address	Explanation of operation
&h69 [7:0]	 The formula which asks for Slope alpha is described below. alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation. $\alpha = \frac{10^{\frac{y}{20}} - 10^{\frac{x}{20}}}{10^{\frac{TH}{20}} - 10^{\frac{x}{20}}} \times 128$ TH is AGC_TH1. x is input level. y is output level. Ex) It asks for alpha at the time of AGC_TH1 = −12dB, x = 0dB y = −6dB $\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{0}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{0}{20}}} \times 128$ $\alpha = 85.266 \rightarrow 55_H$ 55H calculated is set as &h61 or &h69

AGC_TH1 setting of DRC1 for low frequency band

Please set below to the setting value of AGC_TH2.

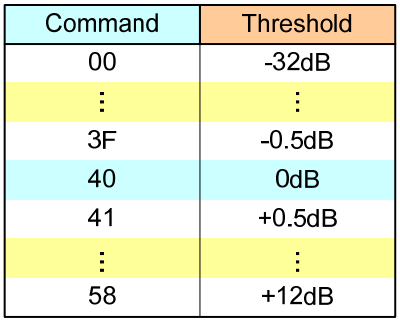
Default = 40h

Select Address	Explanation of operation
&h68 [6:0]	

Command	Threshold
00	-32dB
⋮	⋮
3F	-0.5dB
40	0dB
41	+0.5dB
⋮	⋮
58	+12dB

AGC_TH2 setting of DRC2 for low frequency band

Default = 40h

Select Address	Explanation of operation
&h6C [6:0]	

Command	Threshold
00	-32dB
⋮	⋮
3F	-0.5dB
40	0dB
41	+0.5dB
⋮	⋮
58	+12dB

Low frequency band A_RATE setting (It is the transition time of a compression curve at the time of an attack.)
DRC1 and DRC2 for low frequency band are individually setting.
Default = 3h

Select Address	Explanation of operation
DRC1 &h6A [6:4] DRC2 &h6E [6:4]	

Command	A_RATE time	Command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

Low frequency band R_RATE setting (It is the transition time of an extension curve at the time of release.)
DRC1 and DRC2 for low frequency band are individually setting.
Default = Bh

Select Address	Explanation of operation
DRC1 &h6A[3:0] DRC2 &h6E[3:0]	

Command	R_RATE time	Command	R_RATE time
0	0.125s	8	2s
1	0.1825s	9	2.5s
2	0.25s	A	3s
3	0.5s	B	4s
4	0.75s	C	5s
5	1s	D	6s
6	1.25s	E	7s
7	1.5s	F	8s

A_TIME1 setting of DRC1 for low frequency band (Detection time setting of attack operation)
DRC1 and DRC2 for low frequency band are individually setting.
Default = 1h

Select Address	Explanation of operation
DRC1 &h6B [7:4] DRC1 &h6F [7:4]	

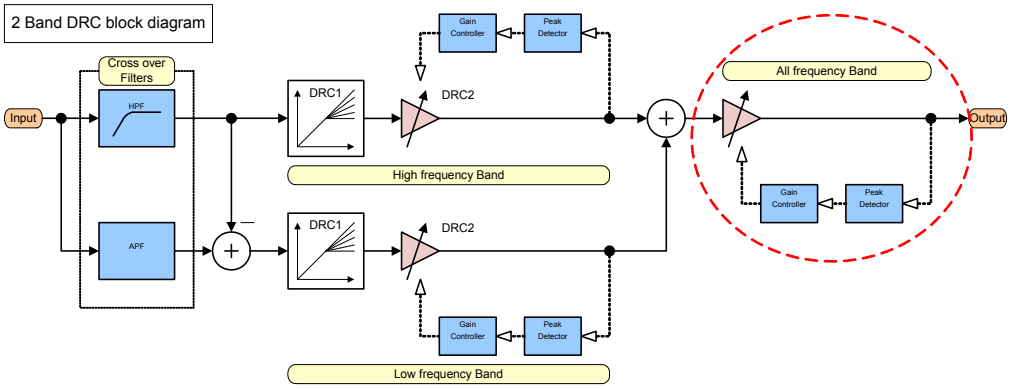
Command	A_TIME time	Command	A_TIME time
0	0ms	8	6ms
1	0.5ms	9	7ms
2	1ms	A	8ms
3	1.5ms	B	9ms
4	2ms	C	10ms
5	3ms	D	20ms
6	4ms	E	30ms
7	5ms	F	40ms

R_TIME setting of DRC for low frequency band (Detection time setting of release operation)
DRC1 and DRC2 for low frequency band are individually setting.
Default = 3h

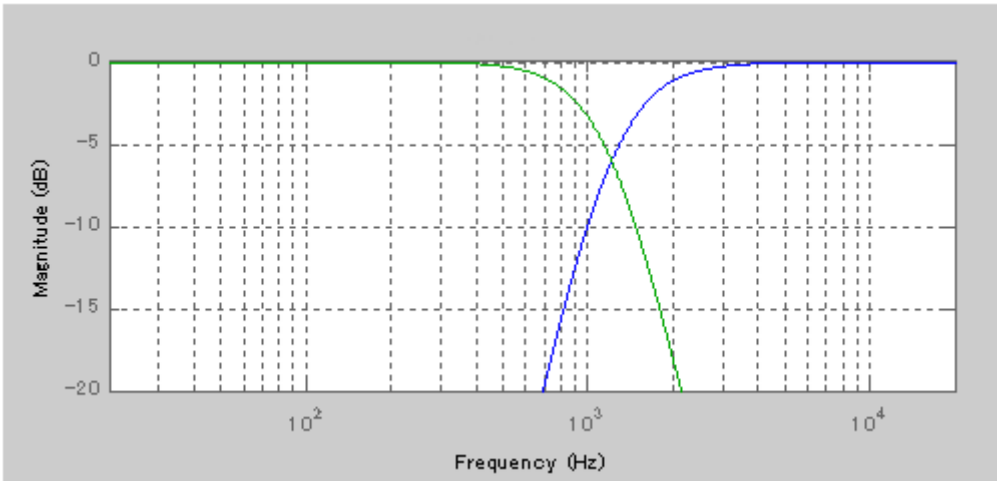
Select Address	Explanation of operation
DRC1 &h6B [2:0] DRC2 &h6F [2:0]	

Command	R_TIME time	Command	R_TIME time
0	5ms	4	100ms
1	10ms	5	200ms
2	25ms	6	300ms
3	50ms	7	400ms

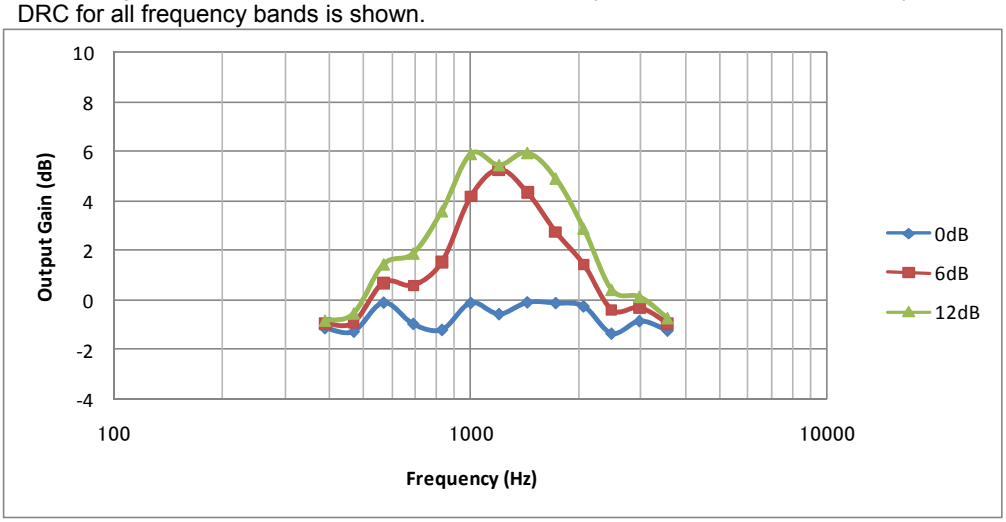
[Question]
What is the purpose of DRC for all frequency band?



[Answer]
The purpose is for keeping constant the output level in the crossover point of low frequency band and high frequency band. A frequency characteristic figure with a cross over frequency 1.2 kHz of DRC for low frequency band and DRC for high frequency band is shown below.



Next, the graph of AGC_TH=0dB, cross over frequency = 1.2kHz, and the frequency vs. output gain when not using all the DRC for all frequency bands is shown.



Input level 0dB is a flat. However, on an input level of +6dB or +12dB, it is over 0dB of a compression level near the cross over frequency.
In order to prevent this phenomenon, DRC for all frequency band is used. However, when this phenomenon does not exist in a problem, I think that it is not necessary to use DRC for all frequency band.
AGC_TH of DRC for all frequency band sets up AGC_TH2 value of the higher one, when AGC_TH2 differ by DRC for high frequency band, and DRC for low frequency band.

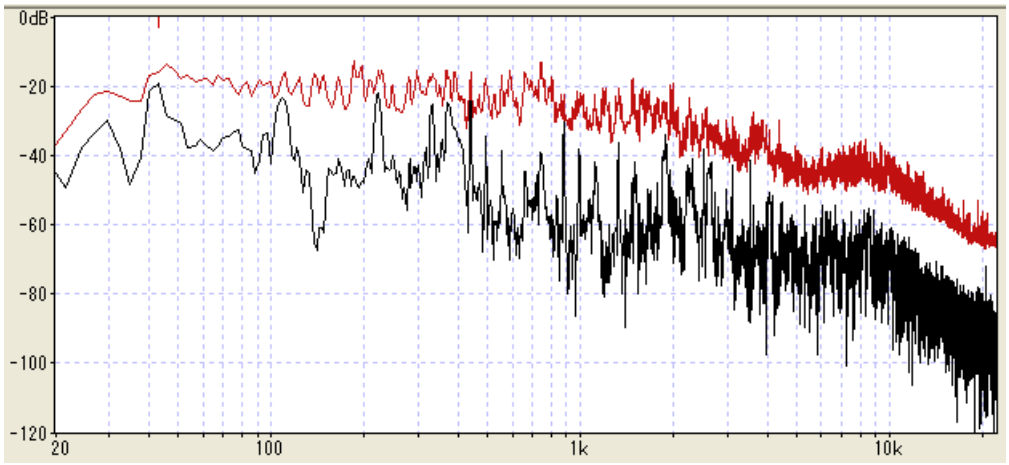
[Question]
Recommendation value setting of 2 band DRC?

[Answer]
The recommendation value of 2 band DRC was examined to speaker protection using FPD TV.
- A_RATE : 4ms
- R_RATE : 2s or more
- A_TIME : 0.5ms
- R_TIME : 50ms or more

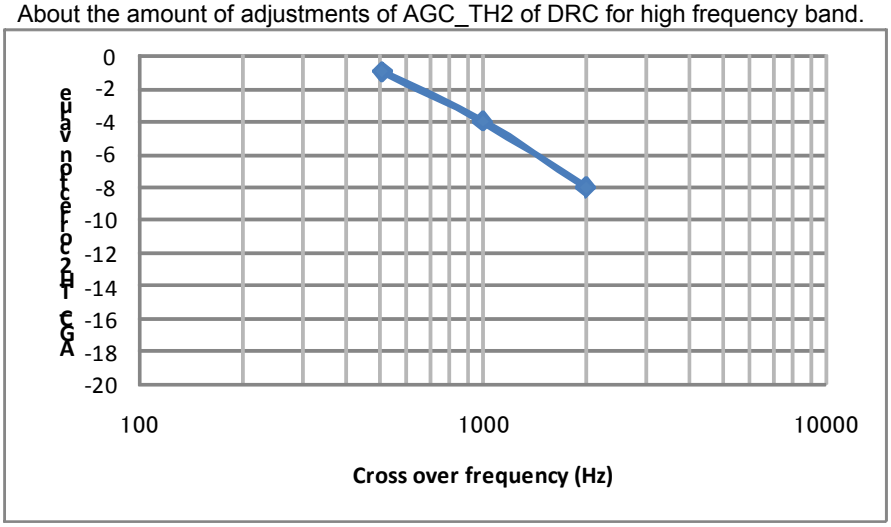
It is not uncomfortable to a music source to arrange all DRC (low frequency band, high frequency band, all frequency band) with the same value.

[Question]
When master volume is increased, why is it that only the sound of a high region becomes large?
[Answer]
It investigated about the cross over frequency and the relation of AGC_TH2 of DRC for high frequency band.
Its sound energy decreases, so that music data becomes high frequency. When a cross over frequency is set up highly, unless it lowers AGC_TH2 of DRC for high frequency band, when master volume is increased, the effect by limit cannot be heard.

The red line shows the Peak level.



About the amount of adjustments of AGC_TH2 of DRC for high frequency band.

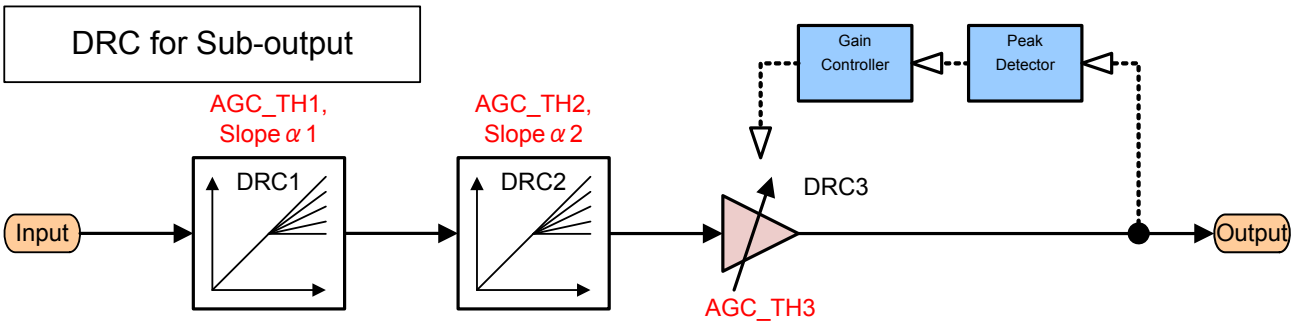


Please use as a standard of the adjustment value from AGC_TH2 value of DRC for low frequency band.
Moreover, the amount of adjustments decreases by setting up a cross over frequency lowness.

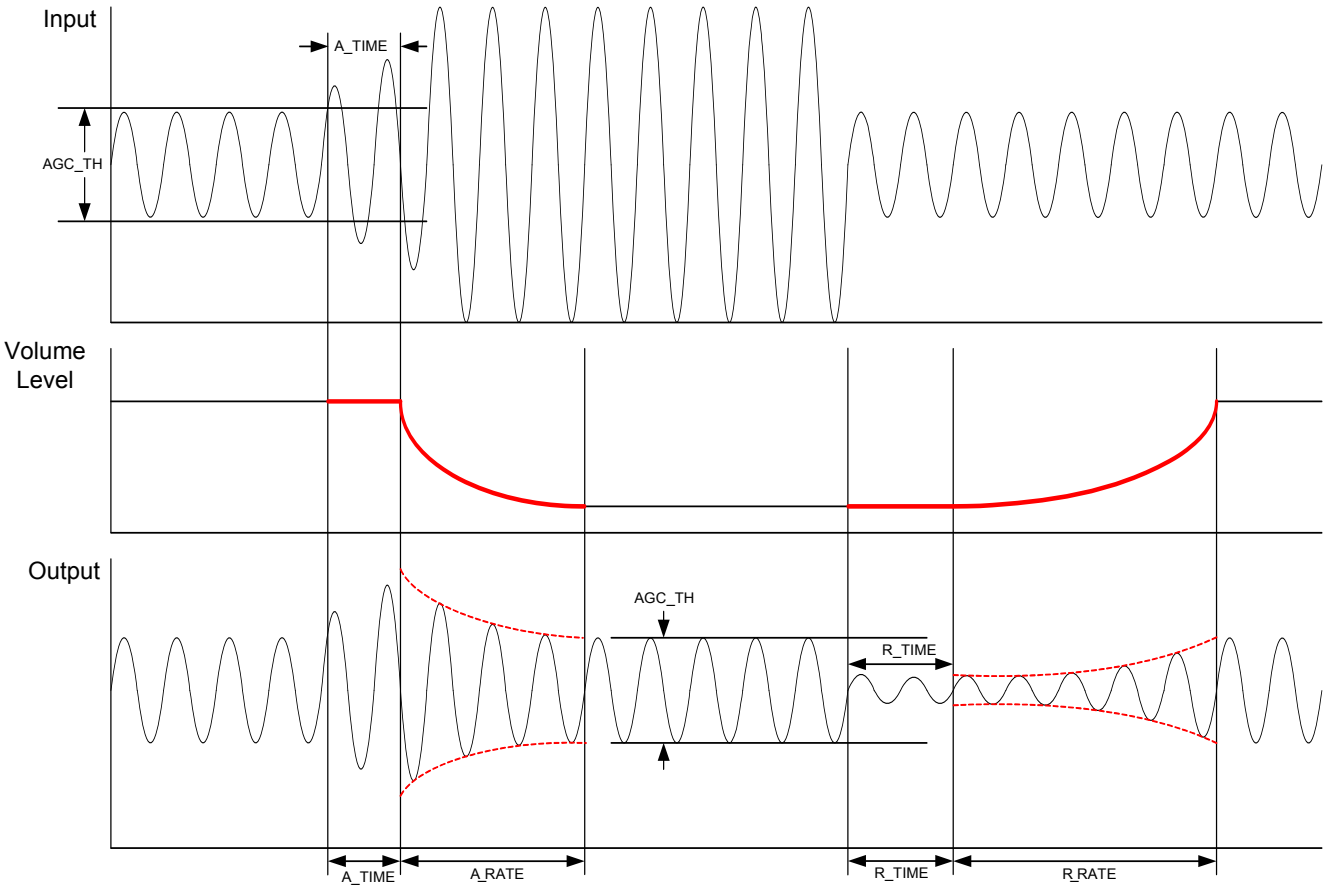
4-16. DRC for Sub-output

This DRC is used in order to prevent speaker protection and the clip output of a large audio signal.

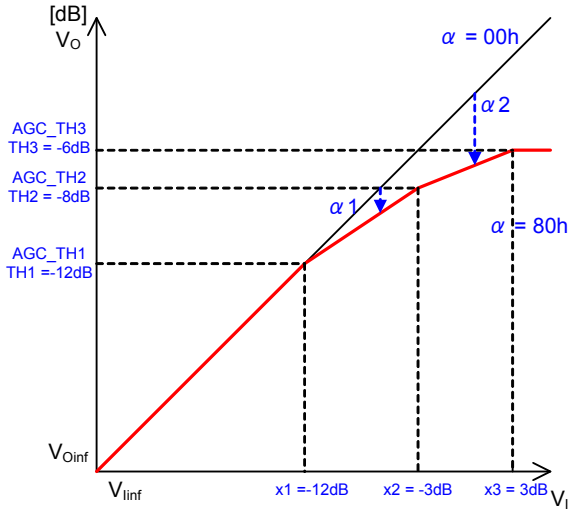
In to set three threshold levels, it is possible to do compression and expansion more smoothly in the sound.



DRC transition figure



DRC input-and-output gain characteristics



The formula which asks for Slope alpha1 and alpha2 is described below.
Alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation.

$$\alpha 1 = \frac{10^{\frac{TH2}{20}} - 10^{\frac{x2}{20}}}{10^{\frac{TH1}{20}} - 10^{\frac{x2}{20}}} \times 128 , \quad \alpha 2 = \frac{10^{\frac{TH3}{20}} - (10^{\frac{TH1}{20}} - 10^{\frac{x3}{20}}) \cdot \alpha 1 - 10^{\frac{x3}{20}}}{10^{\frac{TH2}{20}} - (10^{\frac{TH1}{20}} - 10^{\frac{x3}{20}}) \cdot \alpha 1 - 10^{\frac{x3}{20}}} \times 128$$

x is input level, AGC_TH is output level.

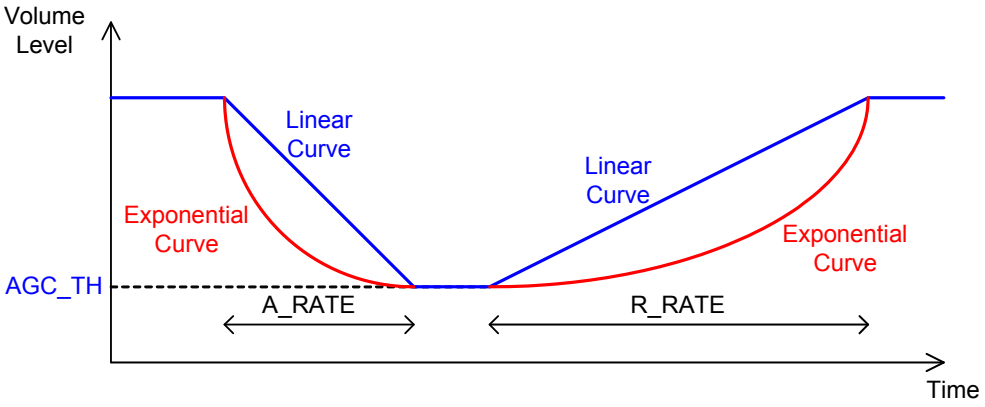
Ex) x1 = -12dB, x2 = -3dB, x3 = +3dB, TH1 = -12dB, TH2 = -8dB, TH3 = -6dB

$$\alpha 1 = \frac{10^{\frac{-8}{20}} - 10^{\frac{-3}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{-3}{20}}} \times 128 , \quad \alpha 2 = \frac{10^{\frac{-12}{20}} - (10^{\frac{-6}{20}} - 10^{\frac{3}{20}}) \cdot \alpha 1 - 10^{\frac{3}{20}}}{10^{\frac{-8}{20}} - (10^{\frac{-12}{20}} - 10^{\frac{3}{20}}) \cdot \alpha 1 - 10^{\frac{3}{20}}} \times 128$$

$\alpha 1 = 86.828 \rightarrow 56_H$ $\alpha 2 = 82.051 \rightarrow 52_H$

Calculated $\alpha 1 = 56_H$ is set as &h75, calculated $\alpha 2 = 52_H$ is set as &h79.

Volume Curve



ON/OFF setting of DRC1 for Sub-output.

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h41 [7]	0	Not use
	1	Use

ON/OFF setting of DRC2 for Sub-output.

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h41 [6]	0	Not use
	1	Use

ON/OFF setting of DRC2 for Sub-output.(Compressor)

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h41 [5]	0	Not use
	1	Use

The volume curve at the time of an attack (A_RATE) is selected.

Default = 0

Select Address	Value	Explanation of operation
&h42 [6]	0	Linear curve
	1	Exponential curve

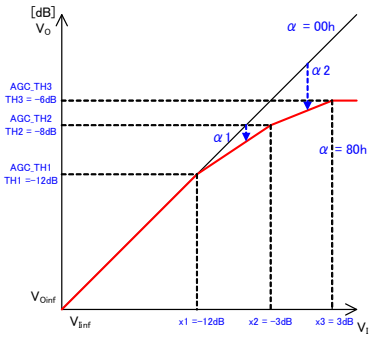
The volume curve at the time of a release (R_RATE) is selected.

Default = 0

Select Address	Value	Explanation of operation
&h42 [2]	0	Linear curve
	1	Exponential curve

Slope (α) setting of DRC1 and DRC2 for Sub-output

Default = 80h

Select Address	Explanation of operation
DRC1(α1) &h75 [7:0] DRC2(α2) &h79 [7:0]	 The formula which asks for Slope alpha1 and alpha2 is described below. Alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation. $\alpha 1 = \frac{10^{\frac{TH2}{20}} - 10^{\frac{x2}{20}}}{10^{\frac{TH1}{20}} - 10^{\frac{x2}{20}}} \times 128$, $\alpha 2 = \frac{10^{\frac{TH3}{20}} - (10^{\frac{TH1}{20}} - 10^{\frac{x3}{20}}) \cdot \alpha 1 - 10^{\frac{x3}{20}}}{10^{\frac{TH2}{20}} - (10^{\frac{TH1}{20}} - 10^{\frac{x3}{20}}) \cdot \alpha 1 - 10^{\frac{x3}{20}}} \times 128$ x is input level, AGC_TH is output level. Ex) x1 = −12dB, x2 = −3dB, x3 = +3dB, TH1 = −12dB, TH2 = −8dB, TH3 = −6dB $\alpha 1 = \frac{10^{\frac{-8}{20}} - 10^{\frac{-3}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{-3}{20}}} \times 128$, $\alpha 2 = \frac{10^{\frac{-12}{20}} - (10^{\frac{-6}{20}} - 10^{\frac{3}{20}}) \cdot \alpha 1 - 10^{\frac{3}{20}}}{10^{\frac{-8}{20}} - (10^{\frac{-12}{20}} - 10^{\frac{3}{20}}) \cdot \alpha 1 - 10^{\frac{3}{20}}} \times 128$ $\alpha 1 = 86.828 \rightarrow 56_H$ $\alpha 2 = 82.051 \rightarrow 52_H$ Calculated $\alpha 1 = 56_H$ is set as &h75, calculated $\alpha 2 = 52_H$ is set as &h79.

AGC_TH1, AGC_TH2 and AGC_TH3 setting of DRC for Sub-output

Please set to the value as below.

AGC_TH3 > AGC_TH2 > AGC_TH1

Default = 40h

Select Address	Explanation of operation
AGC_TH1 &h74 [6:0] AGC_TH2 &h78 [6:0] AGC_TH3 &h7C [6:0]	

Command	Threshold
00	-32dB
⋮	⋮
3F	-0.5dB
40	0dB
41	+0.5dB
⋮	⋮
58	+12dB

A_RATE setting of DRC for Sub-output(It is the transition time of a compression curve at the time of an attack.)

Default = 3h

Select Address	Explanation of operation
DRC1 &h76 [6:4] DRC2 &h7A [6:4] DRC3 &h7E [6:4]	

Command	A_RATE time	Command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

R_RATE setting of DRC for Sub-output (It is the transition time of an extension curve at the time of release.)

Default = Bh

Select Address	Explanation of operation
DRC1 &h76[3:0] DRC2 &h7A[3:0] DRC3 &h7E[3:0]	

Command	R_RATE time	Command	R_RATE time
0	0.125s	8	2s
1	0.1825s	9	2.5s
2	0.25s	A	3s
3	0.5s	B	4s
4	0.75s	C	5s
5	1s	D	6s
6	1.25s	E	7s
7	1.5s	F	8s

A_TIME setting of DRC for Sub-output (Detection time setting of attack operation.)

Default = 1h

Select Address	Explanation of operation
DRC1 &h77 [7:4] DRC2 &h7B [7:4] DRC3 &h7F [7:4]	

Command	A_TIME time	Command	A_TIME time
0	0ms	8	6ms
1	0.5ms	9	7ms
2	1ms	A	8ms
3	1.5ms	B	9ms
4	2ms	C	10ms
5	3ms	D	20ms
6	4ms	E	30ms
7	5ms	F	40ms

R_TIME setting of DRC for Sub-output (Detection time setting of release operation.)

Default = 3h

Select Address	Explanation of operation
DRC1 &h77 [2:0] DRC2 &h7B [2:0] DRC3 &h7F [2:0]	

Command	R_TIME time	Command	R_TIME time
0	5ms	4	100ms
1	10ms	5	200ms
2	25ms	6	300ms
3	50ms	7	400ms

4-17. Post-scaler (DSP part)

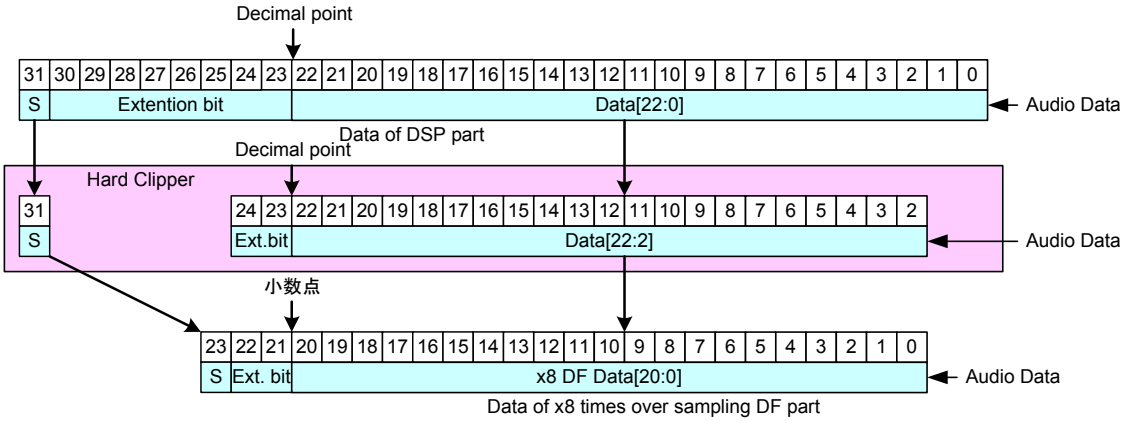
To prevent from an overflow in the DSP, it adjusts a gain with the scaler. An adjustable range can be set up at a 0.5dB step from +48dB to -79dB. Post-scaler does not have a smooth transition function.

Default = 60h

Select Address	Explanation of operation
Main &h1C [7:0] Sub &h1D [7:0] Moni1 &h1E [7:0] Moni2 &h1F [7:0]	Command / Gain 00 / +48dB 01 / +47.5dB ⋮ / ⋮ 60 / 0dB 61 / -0.5dB 62 / -1dB ⋮ / ⋮ FE / -79dB FF / -∞

4-18. Hard Clipper (DSP part)

Signed 24bit data that cuts upper 6bits and lower 2bit of 32bit DSP is output to eight times over sampling digital filter part. It becomes saturation output for data that exceeds ±12dB.

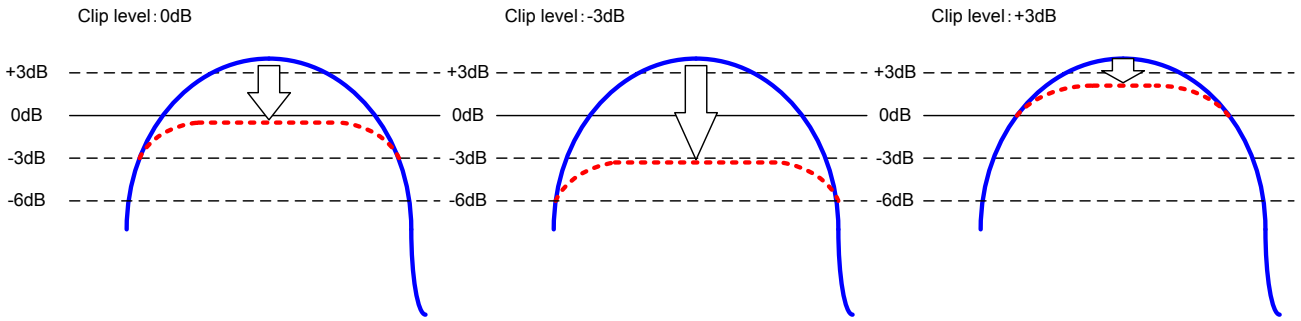


4-19. Soft clipper

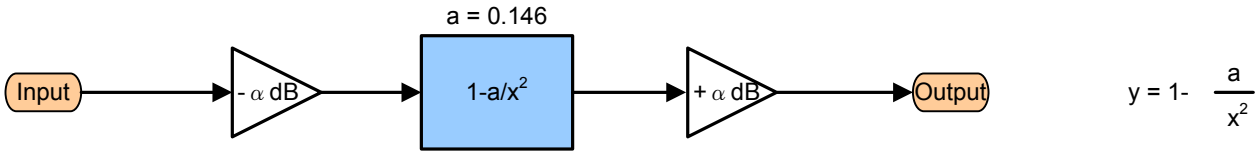
When measuring the rated output of the television, THD+N measures in 10%. It can be made to clip with any output amplitude by using a clipper function. For example, the rated output of 10W or 5W can be gained using the amplifier of 15W output.

Selection of a soft clip or a hard clip can be performed by this IC.

Soft clip



The block diagram of a soft clipper circuit



$y = 1 - \frac{a}{x^2}$

Clipper Level
In case of -3dB, it multiplies by +3dB.
In case of +3dB,
it multiplies -3dB.

The function which begins to curve from -3dB and becomes a clip output at 0dB

Clipper Level
In case of -3dB, it multiplies by -3dB.
In case of +3dB,
it multiplies +3dB.

[Question]

Why does the soft clipper output lower than in the set clip level?

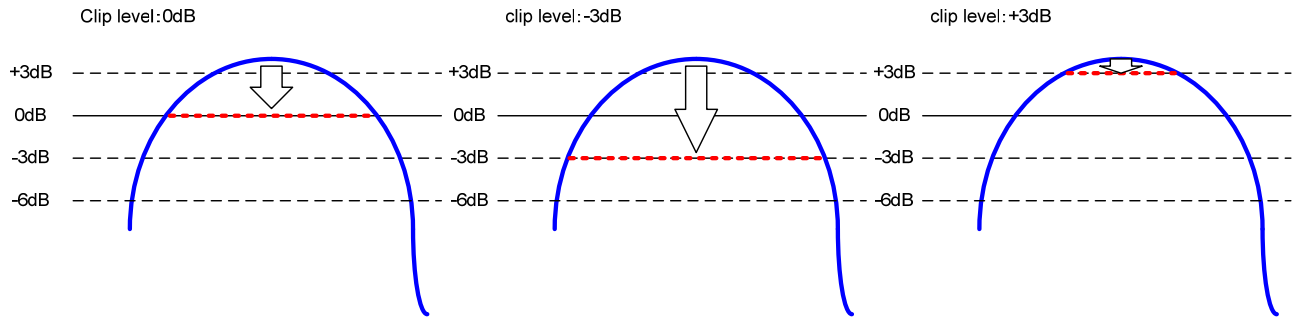
[Answer]

For example, when clipper level is set to 0dB, it is as follows.

0dB input : 20*log(1-0.146/10^((0/20)*2)) = -1.37dB.

6dB input : 20*log(1-0.146/10^((6/20)*2)) = -0.32dB.

Hard clip



Clipper setting

Default = 0

Select Address	Value	Explanation of operation
Main &h35 [5:4] Sub &h35 [1:0]	0	Clipper function is not used.
	1	Soft clipper function is used.
	2	Hard clipper function is used.

Clip level selection

Default = E1h

Select Address	Explanation of operation
Main &h36 [7:0] Sub &h37 [7:0]	Command / Gain: 00 / -22.5dB; ⋮ / ⋮; E0 / -0.1dB; E1 / 0dB; E2 / +0.1dB; ⋮ / ⋮; FF / +3dB

4-20. Post-scaler (x8 Over sampling Digital Filter part)

Level adjustment in x8 over sampling DF block. An adjustable range can be set up at a 0.1dB step from +12dB to -32dB. Lch/Rch is independently controllable.

&h38[0], &h3A[0], &h3C[0] and &h3E[0] is MSB, and &h3B[7:0], &h3D[7:0], &h3F[7:0] is LSB.

Post-scaler does not have a smooth transition function.

Default = 0D2h

Select Address	Explanation of operation
Main Lch &h38[0] Main Lch &h39[7:0] Main Rch &h3A[0] Main Rch &h3B[7:0] Sub Lch &h3C[0] Sub Lch &h3D[7:0] Sub Rch &h3E[0] Sub Rch &h3F[7:0]	Command / Gain 000 / -32dB ⋮ / ⋮ 13F / -0.1dB 140 / 0dB 141 / +0.1dB ⋮ / ⋮ 1B8 / +12dB (Initial value:0D2h → -11dB)

4-21. DC cut HPF (Latter part of DSP processing part)

DC offset element of the digital signal outputted from audio DSP is cut by this HPF.

The cutoff frequency fc of HPF uses the 1Hz filter, and the degree uses the first-order filter.

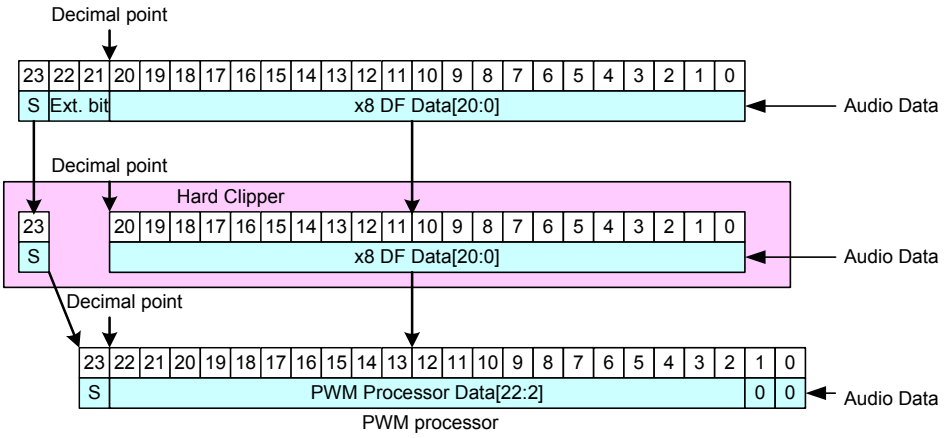
Default = 1

Select Address	Value	Explanation of operation
Main &h28 [1]	0	Not use
Sub &h28 [0]	1	Use

4-22. Hard Clipper (x8 Over Sampling Digital Filter part)

The audio data is changed from <S1.22> to <S0.23> format. It is outputted to PWM Modulator.

As for insufficient subordinate position 1bit, "0" data is inserted. It becomes saturation output when overflowing.

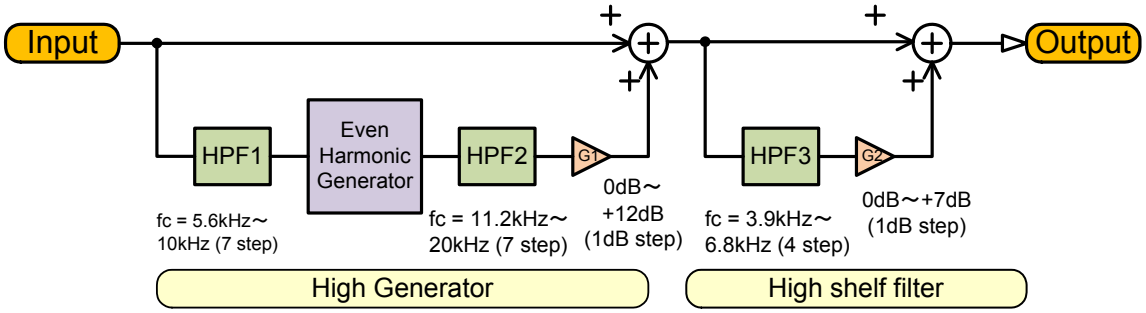


4-23. Higher sound complement (High Generator)

The higher frequency sound deleted when it encoded in MP3 form is complemented in pseudo.

This circuit consists of High Generator circuit and high shelf filter.

The High shelf filter part is used to make the effect of the high frequency band.



High generator setting for Main-output

Default = 0

Select Address	Value	Explanation of operation
&hB4 [7]	0	Not use High Generator
	1	Use High Generator

High generator setting for Sub-output

Default = 0

Select Address	Value	Explanation of operation
&hB4 [6]	0	Not use High Generator
	1	Use High Generator

Mute mode setting

Only the complemented sound can listen by this register setting.

Default = 0

Select Address	Value	Explanation of operation
&hB4 [5]	0	Mute OFF
	1	Mute ON

Please set to 0 at normally use.

High generator high shelf filter f_0 setting

It makes up the ON/OFF sense of the high generator function by this register.

Default = 0

Select Address	Value	Explanation of operation
&hB4 [1:0]	0	3.9kHz
	1	4.7kHz
	2	5.6kHz
	3	6.8kHz

High generator HPF1 cut off frequency setting

Cut an unnecessary inside low element from the sound input to the high generator function.

Default = 0

Select Address	Value	Explanation of operation
&hB5 [6:4]	0	5.6kHz
	1	6.2kHz
	2	6.8kHz
	3	7.5kHz
	4	8.2kHz
	5	9.1kHz
	6	10kHz

High generator HPF2 cut off frequency setting

Cut the high pass element that became unnecessary after the generating harmonic of the even-ordered.

Default = 0

Select Address	Value	Explanation of operation
&hB5 [2:0]	0	11.2kHz
	1	12.4kHz
	2	13.6kHz
	3	15kHz
	4	16.4kHz
	5	18.2kHz
	6	20kHz

High generator additional gain setting

Default = 0h

Select Address	Explanation of operation
Main &hB6 [7:4] Sub &hB7 [7:4]	

Command	Gain	Command	Gain
0	-∞	8	7dB
1	0dB	9	8dB
2	1dB	A	9dB
3	2dB	B	10dB
4	3dB	C	11dB
5	4dB	D	12dB
6	5dB	E	-
7	6dB	F	-

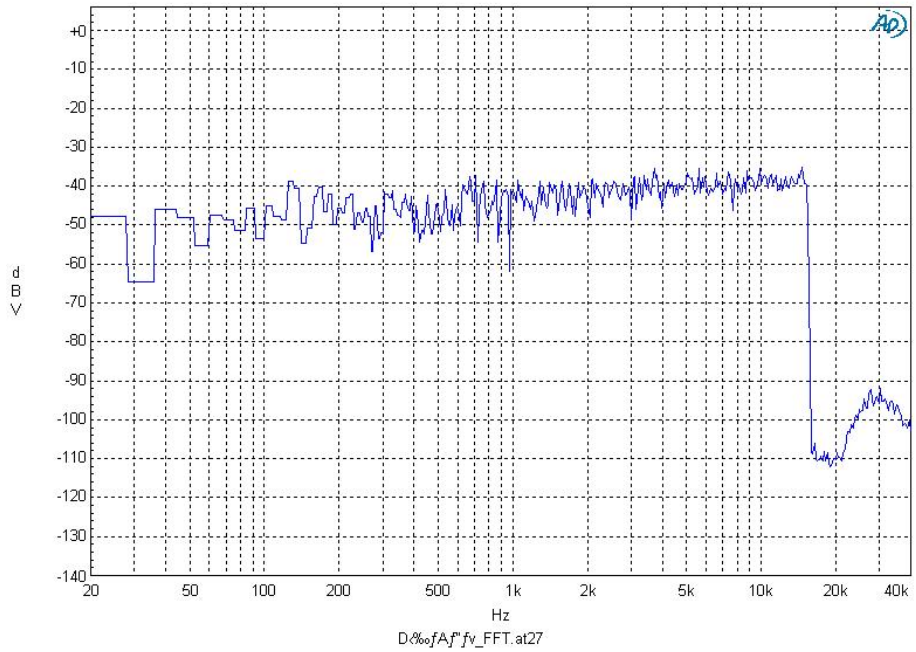
High shelf filter boost gain setting

Default = 0

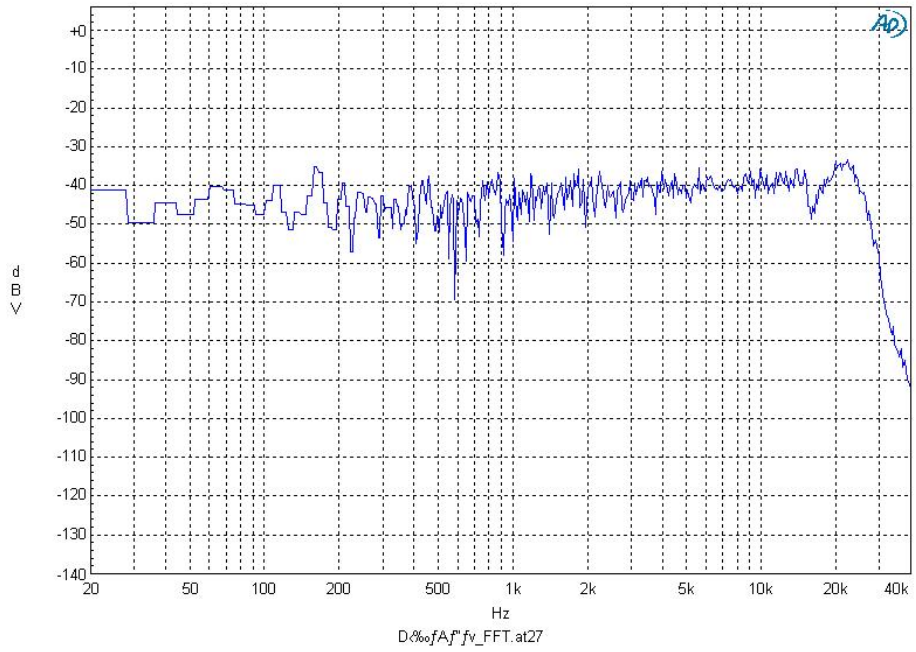
Select Address	Value	Explanation of operation
Main &hB6 [2:0] Sub &hB7 [2:0]	0	0dB
	1	1dB
	2	2dB
	3	3dB
	4	4dB
	5	5dB
	6	6dB
	7	7dB

The graph of frequency characteristic of ON/OFF of the high generator function is shown.
Input data is a white noise made the MP3 of 128kbps by sampling 44.1 kHz.

High generator OFF
Input source : White noise
Frequency : 20 to 40kHz



High generator ON
HPF cut off : 5.6kHz
Additional gain : +3dB



4-24. RAM clear

The data RAM of DSP and SRC, coefficient RAM, and NS register inside PWM processor block are cleared.

40μs or more is required until all the data is cleared.

Clear of the data RAM and SRC

Default = 1

Select Address	Value	Explanation of operation
&h01 [7]	0	Normal
	1	Clear operation

Clear of coefficient RAM (BANK1, BANK2)

Default = 1

Select Address	Value	Explanation of operation
&h01 [6]	0	Normal
	1	Clear operation

Clear of PWM NS register inside PWM processor block

Default = 1

Select Address	Value	Explanation of operation
&h01 [5]	0	Normal
	1	Clear operation

4-25. Audio Output Level Meter

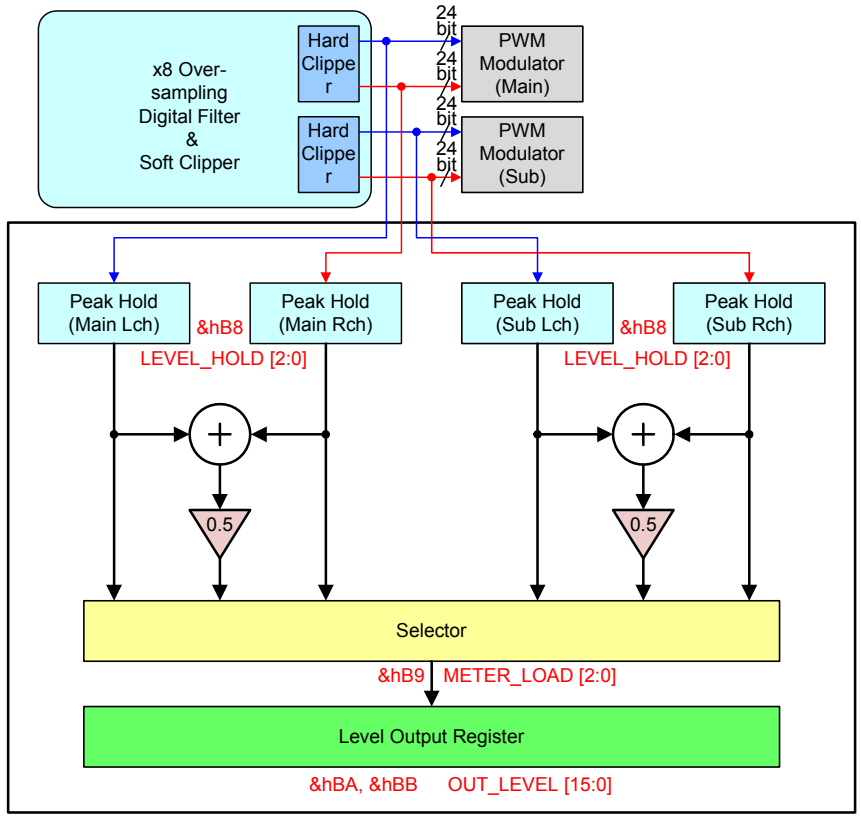
It is possible to output the peak level of the PCM data inputted into a PWM processor.

A peak value can be read using an I^2C command interface as 16 bit data of an absolute value.

The interval holding a peak value can be selected from 6 steps (50ms step) from 50ms to 300ms.

A peak hold result can be selected from L channel, R channel, and a monophonic channel {(Lch+Rch) /2}.

Audio Output Level Meter block diagram



Setting of the peak level hold time interval of Audio Output Level Meter

Default = 00h

Select Address	Explanation of operation
&hB8[2:0]	See table below

Command	Hold time
0	50ms
1	100ms
2	150ms
3	200ms
4	250ms
5	300ms

The signal of Audio Level Meter read-back is selected.
A value will be taken into a read-only register if a setting value is written in.
In order to update this register value, it is necessary to write in a setting value again.

Default = 0

Select Address	Value	Explanation of operation
&hB9 [2:0]	0	The peak level of Main-output L channel
	1	The peak level of Main-output R channel
	2	The peak level of Main-output monophonic channel {(Lch+Rch) /2}
	3	The peak level of Sub-output L channel
	4	The peak level of Sub-output R channel
	5	The peak level of Sub-output monophonic channel {(Lch+Rch) /2}

Read-back of Audio Output Level

&hBA (upper 8 bits) and a &hBB (lower 8 bits) commands are read for the maximum within the period appointed by the command &hB8 using an I2C interface.

(Example)

When FFFFh is read, mean 1.0 (0dBFs).

When 8000h is read, mean 0.5 (-6dBFs).

4-26. Audio Signal Selector Setting

It selects the audio signal of the SUB output, the MONI1 output, the MONI2 output inside the DSP.

Output select of SDATA1 and SDATA2

Default = 0

Select Address	Value	Explanation of operation
&h2A [6]	0	MONI1/MONI2
	1	Main/Sub (output of 128/ch Delay RAM)

Sub-output select

The selector which is between the DSP part and x8 over sampling filter parts

Default = 0

Select Address	Value	Explanation of operation
&h2A [5:4]	0	DSP Sub output
	1	DSP Main output
	2	DSP MONI1 output
	3	DSP MONI2 output

Input select for Sub calculation of audio DSP part

Default = 5

Select Address	Value	Explanation of operation
&h2A [2:0]	0	Input2-HPF
	1	Input1-HPF
	2	P^2Volume
	3	Surround
	4	8 Band-BQ
	5	FIR Filter

The DSP part MONI1 channel selection
Default = 1

Select Address	Value	Explanation of operation
&h2B [6:4]	0	Input2-HPF
	1	Input1-HPF
	2	P^2Volume
	3	Surround
	4	8 Band-BQ
	5	FIR Filter
	6	Channel Mixer 3

The DSP part MONI2 channel selection
Default = 1

Select Address	Value	Explanation of operation
&h2B [2:0]	0	Input2-HPF
	1	Input1-HPF
	2	P^2Volume
	3	Surround
	4	8 Band-BQ
	5	FIR Filter
	6	Channel Mixer 3

DAIF output selection for IC evaluation
It outputs audio output from the DSP part for the monitor in the DAIF.
Default = 0

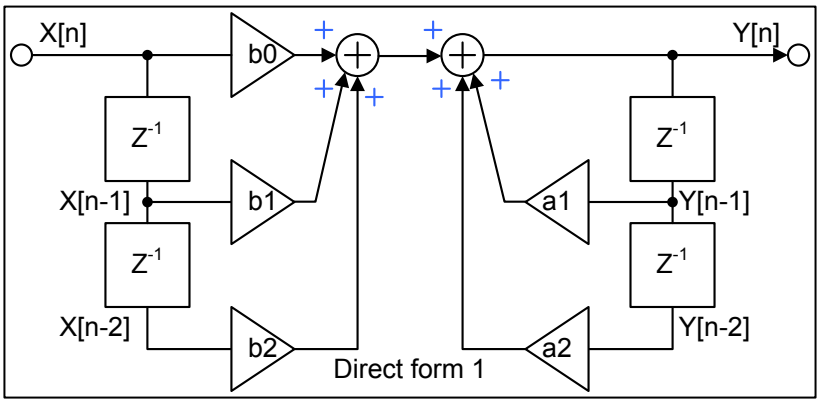
Select Address	Value	Explanation of operation
&h2C [1:0]	0	Main output (128/ch Delay RAM)
	1	Sub output (128/ch Delay RAM)
	2	MONI1
	3	MONI2

5. Setting and reading method of parametric equalizer

It explains a detailed sequence of the setting method and the reading method of the parametric equalizer separately for usage. Please read while referring to Chapter 4-4.

5-1 PEQ coefficient setting

The parametric equalizer consists of Bi-quad filter as follows. Each coeffiect of Bi-quad filter can be written directly. It is S2.21 format, and setting range is -4≦ x ＜+4.
Moreover, the coefficient address is shown in Table 1.



5-1-1 Writing sequence (It sets up in number order)

1. BANK1 to 4 is appointed. (&hA1[5:4])
2. Address setting (&hA3) (*1) Table 1 is referred to.
3. 24bit coefficient Upper[23:16]bit setting (&hA4[7:0])
4. 24bit coefficient Middle[15:8]bit setting (&hA5[7:0])
5. 24bit coefficient Lower [7:0]bit setting (&hA6[7:0])
6. The writing of coefficients are performed.(&hA7[1:0] = 2) (*2)

(*2) After a writing complete of coefficients is cleared automatically. It is not necessary to transmit h34[0] =L. Coefficient writing takes about 100μsec.100μsec should not change an address setup and several 24-bit setup after coefficient write-in execution.

(ex) When 0x3DEDE7 is written in BANK1, Lch, 8band(1) b0

1. &hA1 = 0*h (BANK1 is appointed.)
2. &hA3 = 00h (8band (1) b0 is appointed)
3. &hA4 = 3Dh (Upper [23:16] is setting)
4. &hA5 = EDh (Middle [15:8] is setting)
5. &hA6 = E7h (Lower [7:0] is setting)
6. &hA7 = 02h (Coefficient transfer) (*3)

(*3) After a writing complete of coefficients is cleared automatically.

7. 100μsec or more μsec wait

The writing of other coefficients is performed.

5-1-2 Read-back sequence (It sets up in number order)

1. BANK1 to 4 is appointed. (&hA1 [0])
2. Address setting (&hA3) (*4) Table 1 is referred to.
3. Setting of a read-back register address (&hD0)
4. Read-back of the 24bit coefficient Upper [23:16] bit (&hA8 [7:0])
5. Read-back of the 24bit coefficient Middle [15:8] bit (&hA9 [7:0])
6. Read-back of the 24bit coefficient Lower [7:0] bit (&hAA [7:0])

Table1. Specified coefficient

&hA3	Specified coefficient	&hA3	Specified coefficient	&hA3	Specified coefficient	&hA3	Specified coefficient
00	8BandBQ1 b0	23	8BandBQ8 b0	46	SubXOV2 b0	69	DRC_APF b0
01	8BandBQ1 b1	24	8BandBQ8 b1	47	SubXOV2 b1	6A	DRC_APF b1
02	8BandBQ1 b2	25	8BandBQ8 b2	48	SubXOV2 b2	6B	DRC_APF b2
03	8BandBQ1 a1	26	8BandBQ8 a1	49	SubXOV2 a1	6C	DRC_APF a1
04	8BandBQ1 a2	27	8BandBQ8 a2	4A	SubXOV2 a2	6D	DRC_APF a2
05	8BandBQ2 b0	28	1BandBQ b0	4B	SubXOV3 b0	6E	SRND_BQ1 b0
06	8BandBQ2 b1	29	1BandBQ b1	4C	SubXOV3 b1	6F	SRND_BQ1 b1
07	8BandBQ2 b2	2A	1BandBQ b2	4D	SubXOV3 b2	70	SRND_BQ1 b2
08	8BandBQ2 a1	2B	1BandBQ a1	4E	SubXOV3 a1	71	SRND_BQ1 a1
09	8BandBQ2 a2	2C	1BandBQ a2	4F	SubXOV3 a2	72	SRND_BQ1 a2
0A	8BandBQ3 b0	2D	MainXOV1 b0	50	SubXOV4 b0	73	SRND_BQ2 b0
0B	8BandBQ3 b1	2E	MainXOV1 b1	51	SubXOV4 b1	74	SRND_BQ2 b1
0C	8BandBQ3 b2	2F	MainXOV1 b2	52	SubXOV4 b2	75	SRND_BQ2 b2
0D	8BandBQ3 a1	30	MainXOV1 a1	53	SubXOV4 a1	76	SRND_BQ2 a1
0E	8BandBQ3 a2	31	MainXOV1 a2	54	SubXOV4 a2	77	SRND_BQ2 a2
0F	8BandBQ4 b0	32	MainXOV2 b0	55	Smooth BQ b0		
10	8BandBQ4 b1	33	MainXOV2 b1	56	Smooth BQ b1		
11	8BandBQ4 b2	34	MainXOV2 b2	57	Smooth BQ b2		
12	8BandBQ4 a1	35	MainXOV2 a1	58	Smooth BQ a1		
13	8BandBQ4 a2	36	MainXOV2 a2	59	Smooth BQ a2		
14	8BandBQ5 b0	37	MainXOV3 b0	5A	P2V_HPF b0		
15	8BandBQ5 b1	38	MainXOV3 b1	5B	P2V_HPF b1		
16	8BandBQ5 b2	39	MainXOV3 b2	5C	P2V_HPF b2		
17	8BandBQ5 a1	3A	MainXOV3 a1	5D	P2V_HPF a1		
18	8BandBQ5 a2	3B	MainXOV3 a2	5E	P2V_HPF a2		
19	8BandBQ6 b0	3C	MainXOV4 b0	5F	P2V_APF b0		
1A	8BandBQ6 b1	3D	MainXOV4 b1	60	P2V_APF b1		
1B	8BandBQ6 b2	3E	MainXOV4 b2	61	P2V_APF b2		
1C	8BandBQ6 a1	3F	MainXOV4 a1	62	P2V_APF a1		
1D	8BandBQ6 a2	40	MainXOV4 a2	63	P2V_APF a2		
1E	8BandBQ7 b0	41	SubXOV1 b0	64	DRC_HPF b0		
1F	8BandBQ7 b1	42	SubXOV1 b1	65	DRC_HPF b1		
20	8BandBQ7 b2	43	SubXOV1 b2	66	DRC_HPF b2		
21	8BandBQ7 a1	44	SubXOV1 a1	67	DRC_HPF a1		
22	8BandBQ7 a2	45	SubXOV1 a2	68	DRC_HPF a2		

6. P-S conversion

Two parallel serial conversion circuits are built in BM5449.

P-S conversion 1 convert the Main output of DSP from SDATAO1, LRCKO, and BCKO into three line serial data and output the data. P-S conversion 2 convert the sub output of DSP from SDATAO1, LRCKO, and BCKO into three line serial data and output the data. Output audio data can be selected by &h2A and &h2B command.

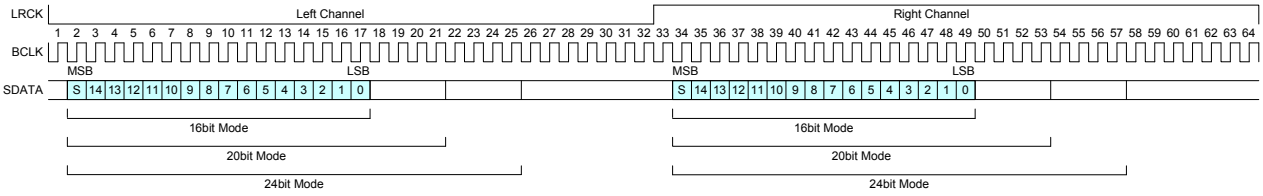
Sampling frequency of output audio data is same as synchronous SRC. <32kHz／44.1kHz／48kHz>

Transfer clock form is fixed 64fs.

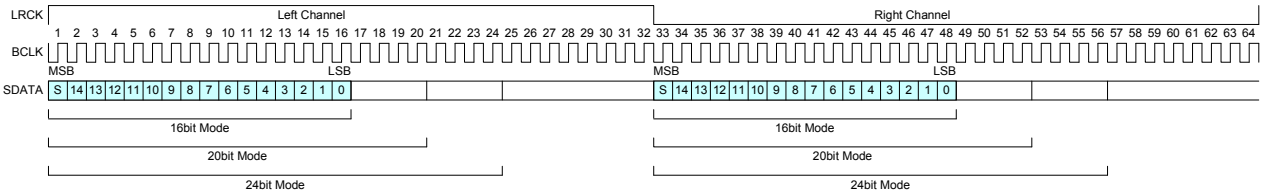
Output format has the IIS mode, left-align mode, and right-align mode. 16 each bit, 20bit, and 24bit output can also be selected. The figure below shows the timing chart of each transmission mode.

Bit clock frequency : 64fs

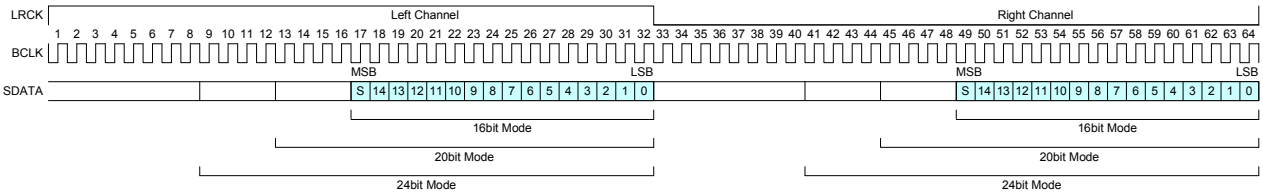
I^2S 64fs Format



Left-Justified 64fs Format



Right-Justified 64fs Format



6-1. Format setting of three line serial output

Default = 0

Select Address	Value	Explanation of operation
&h05 [3:2]	0	IIS mode
	1	left-align mode
	2	right-align mode

6-2. Setting data bit width of three line serial output

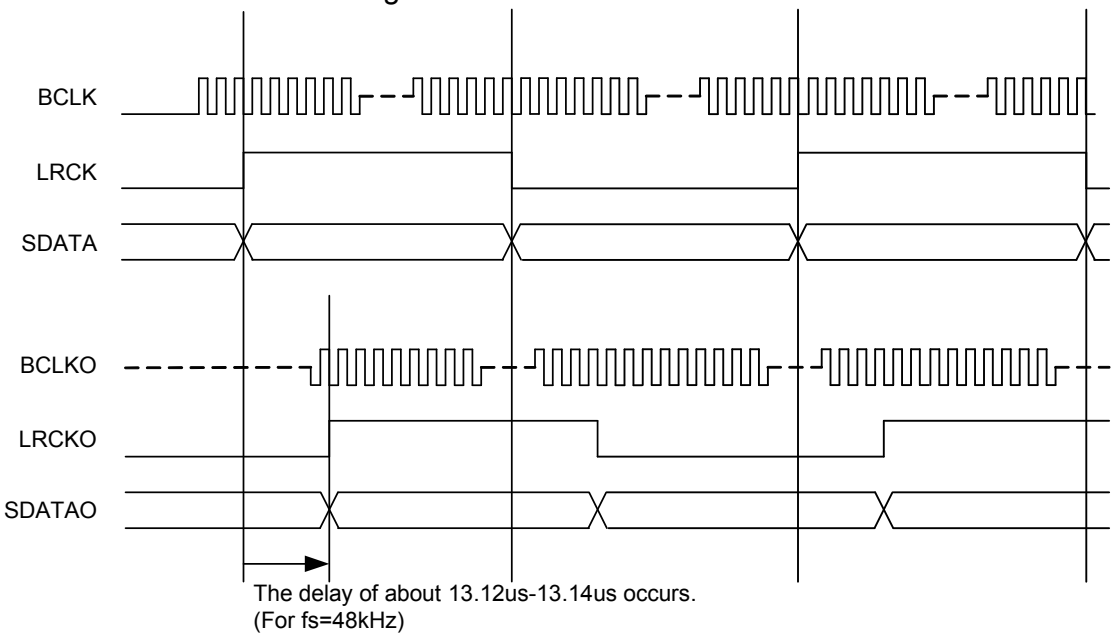
Default = 2

Select Address	Value	Explanation of operation
&h05 [1:0]	0	16 bits
	1	20 bits
	2	24 bits

6-3. About the I/O timing of the cereal audio data

LRCKO and the BCLKO signal output from BM5449MWV generate the internal clock from the BCLK signal.
The clock is divided frequency and output. Therefore, the LRCKO signal output becomes an output of the LRCK input signal and the asynchronous system.

Related chart of I/O timing of cereal audio data



It is output delaying 645 clocks or 646 clocks when the delay of LRCKO is expressed with internal clock (1024 x fs).

7. The mute function by a terminal

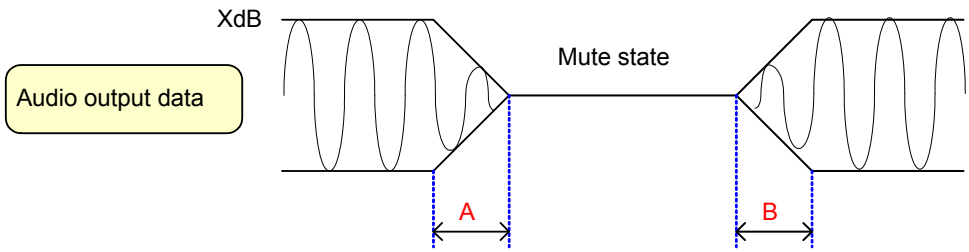
BM5449MWV has a mute function of audio DSP by a terminal.
It is possible to perform mute of the output from Audio DSP by setting a MUTEX terminal to "L."

Transition time setting at the time of mute is as follows.
Smooth transition mute time setting

The transition time when changing to a mute state is selected.
The soft transition time at the time of mute release is 10.7ms fixed.
Default = 0

Select Address	Value	Explanation of operation
&h20 [1:0]	0	85.4ms
	1	42.7ms
	2	21.4ms
	3	10.7ms

&h20[1:0] Mute time setting
It is only operated by mute terminal.



&h20[1:0] setting

Command	A	B
0	85.4ms	10.7ms
1	42.7ms	10.7ms
2	21.4ms	10.7ms
3	10.7ms	10.7ms

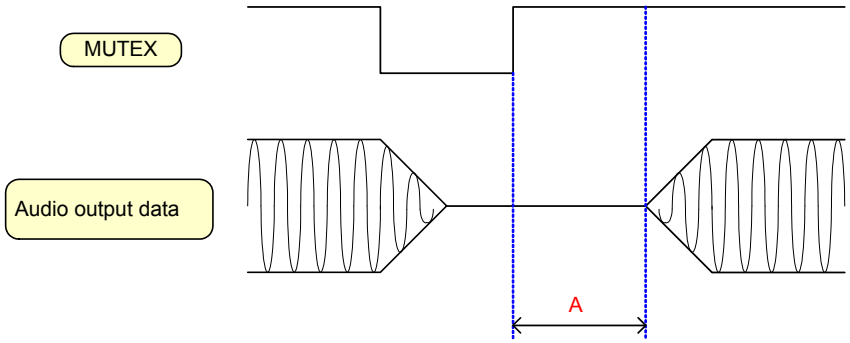
Smooth transition mute release time setting

Time after detecting mute release until it actually begins mute release operation is set up.

Default = 0

Select Address	Value	Explanation of operation
&h20 [3:4]	0	0ms
	1	100ms
	2	200ms
	3	300ms

Operation of mute delay &h20[3:2]



Command	A
0	0ms
1	100ms
2	200ms
3	300ms

[Question]

When mute release is performed, what happens during mute operation?

Moreover, when there is release delay time, what happens?

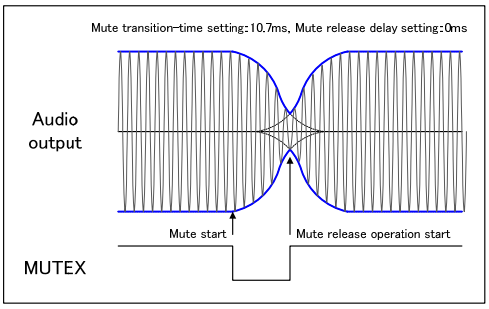
[Answer]

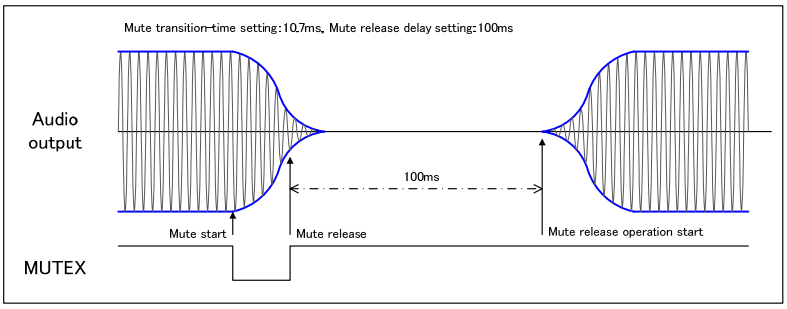
When mute release is performed during mute operation, mute release operation is started in an instant.

(When delay setting is 0)　Return time at this time becomes shorter than mute release time (for example, 10ms).

Next, when there is setting of release delay time, a delay timer starts a count from the time of performing mute release, and mute release operation is started after delay time completing.

When mute release time setting is set to 10ms, it is designing so that a mute release curve may draw f curve.





8. The notes at the time of reset

Since the state of IC is not stable at the time of the power supply ON, please perform IC reset action. [RSTX = “L”]

The input of the reset signal of BM5449MWV is performing noise removal using a clock signal.

Therefore, in order for IC reset to become valid, 10 times or more of clocks need to be inputted from a XI terminal in the state of RSTX=L.

9. The cautions at the time of starting

Please be sure to send the following command after the IC reset release containing the power supply ON.

9-1. When you do not use the clock stop automatic operation return function (Chapter 16-3)

0. Power supply turn on

↓

○Please input a clock from XI terminal. When the clock is not inputted, reset does not start normally.

↓

1. Reset release (RSTX = H)

Please input serial digital audio data.(LRCLK, BCLK, SDATA) If the input of serial audio data is while it is so far from a power supply injection, it is never satisfactory.

↓

2. Release power down mode(PDX = H)

○Please wait for about 20ms until PLL is stabilized.

↓

3. &h0A [2:0] = 7h : Input clock disappearance flag is cleared.

↓

4. &hE9 [7:0] = 34h : The system clock inside IC is set up.

↓

5. &h03 [5:0] = *h : 3-line serial audio input format is set up. Refer to Chapter 3 for a setting value.

↓

6. &h04 [0] = 1 : Adjust the input data incorporation position.

↓

○Wait for about 1ms until the adjustment of the incorporation position is completed.

↓

7. &h04 [1] = 1 : Clear LRCK frame error flag.

↓

8. &h07 [0] = 1 : Clear LRCK-synchronous error signal.

↓

9. &h01[7:5] = 0h : RAM clear OFF

↓

10. &hC8[7:0] = 05h : Main PWM set up.

↓

11. &hC9[7:0] = 01h : Main PWM set up.

↓

12. &hCA[7:0] = 0Fh : Main PWM set up.

↓

13. &hCB[7:0] = 0Bh : Main PWM set up.

↓

14. &hCC[7:0] = 06h : Sub PWM set up.

↓

15. &hCD[7:0] = 01h : Sub PWM set up.

↓

16. &hCE[7:0] = 0Fh : Sub PWM set up.

↓

17. &hCF[7:0] = 09h : Sub PWM set up.

↓

18. Set other register

Ex) &h10 [1:0] = 0h : Set master fine volume for main output

&h11 [7:0] = 30h : Release mute of master volume for main output (In case of 030h = 0dB)

↓

19. Release mute terminal (MUTEX =”H”)

9-2. When you use the clock stop automatic operation return function (Chapter 16-3)

0. Power supply turn on

↓

○Please input a clock from XI terminal. When the clock is not inputted, reset does not start normally.

↓

1. Reset release (RSTX = H)

Please input serial digital audio data. (LRCLK, BCLK, SDATA) If the input of serial audio data is while it is so far from a power supply injection, it is never satisfactory.

↓

2. Release power down mode (PDX = H)

○Please wait for about 20ms until PLL is stabilized.

↓

3. &hE9 [7:0] = 34h : The system clock inside IC is set up.

↓

4. &h03 [5:0] = *h : 3-line serial audio input format is set up. Refer to Chapter 3 for a setting value.

↓

5. &h01 [7:0] = 00h : RAM clear OFF

↓

6. &hC8[7:0] = 05h : Main PWM set up.

↓

7. &hC9[7:0] = 01h : Main PWM set up.

↓

8. &hCA[7:0] = 0Fh : Main PWM set up.

↓

9. &hCB[7:0] = 0Bh : Main PWM set up.

↓

10. &hCC[7:0] = 06h : Sub PWM set up.

↓

11. &hCD[7:0] = 01h : Sub PWM set up.

↓

12. &hCE[7:0] = 0Fh : Sub PWM set up.

↓

13. &hCF[7:0] = 09h : Sub PWM set up.

↓

14. Set other register

Ex) &h10 [1:0] = 0h : Set master fine volume for main output

&h11 [7:0] = 30h : Release mute of master volume for main output (In case of 030h = 0dB)

↓

15. Release mute terminal (MUTEX =”H”)

10. Power Down Mode

There is a down of power mode in this IC. PLL and the internal clock stop when changing to this mode, and power consumption can be lowered. A set value of the register and the data of RAM are maintained even if it sets it to this mode. Please execute the following procedure to set it to this mode.

10-1. When you do not use the clock stop automatic operation return function (Chapter 16-3)

10-1-1.Shift to power down mode

1. Mute with terminal (MUTEX ="L")
   ○X ms or more is waited for until MUTE hangs completely.
   X = (Mute transition duration setting) + 50ms
   ↓
2. &h01 [4] = 1 : The PWM output is made "L" fixed output.
   ↓
3. &hE1 [7] = 1 : The output of the serial digital audio data is stopped.
   ↓
4. &hE9 [7:0] = 35h : The clock supply by PLL is stopped.
   ↓
5. Power down with terminal (PDX = "L")
   ↓
6. Serial digital audio data input is stopped.

10-1-2.Return from power down mode

1. Please input the serial digital audio data.
   ↓
2. Power down release with terminal (PDX ="H")
   ↓
3. &h0A [2:0] = 7h : The input clock disappearance flag is cleared.
   ○Please wait for about 20ms(Min.) until PLL is stabilized.
   ↓
4. &hE9 [7:0] = 34h : The clock supply by PLL is started.
   ↓
5. &hE1 [7] = 0 : The serial digital audio data output starts.
   ↓
6. &h01 [7:5] = 7h : RAM clear is executed.
   ○It makes to &h01[4]=0, and PWM is put into the state of normal output at the same time.
   ↓
7. &h03[5:0] = *h :3-line serial audio input format is set up. Refer to Chapter 3 for a setting value.
   ↓
8. &h04[0] = 1 :Adjust the input data incorporation position.
   ○It is about 1ms wait until the adjustment of the incorporation position is completed.
   ↓
9. &h04[1] = 1 :Clear LRCK frame error flag.
   ↓
10. &h07[0] = 1 :Clear LRCK-synchronous error signal.
   ↓
11. &h01[7:0] = 00h :RAM clear OFF
   ↓
12. Release mute terminal (MUTEX ="H")

10-2. When you use the clock stop automatic operation return function (Chapter 16-3)

10-2-1.Shift to power down mode

1. Mute with terminal (MUTEX =”L”)
   ○X ms or more is waited for until MUTE hangs completely.
   X = (Mute transition duration setting) + 50ms
   ↓
2. &h01 [4] = 1 : The PWM output is made "L" fixed output.
   ↓
3. &hE1 [7] = 1 : The output of the serial digital audio data is stopped.
   ↓
4. &hE9 [7:0] = 35h : The clock supply by PLL is stopped.
   ↓
5. Power down with terminal (PDX = “L”)
   ↓
6. Serial digital audio data input is stopped.

10-2-2. Return from power down mode

1. Please input the serial digital audio data.
   ↓
2. Power down release with terminal (PDX =“H”)
   ○Please wait for about 20ms(Min.) until PLL is stabilized.
   ↓
3. &hE9 [7:0] = 34h : The clock supply by PLL is started.
   ↓
4. &hE1 [7] = 0 : The serial digital audio data output starts.
   ↓
5. &h01 [7:5] = 7h : RAM clear is executed.
   ○It makes to &h01[4]=0, and PWM is put into the state of normal output at the same time.
   ↓
6. &h03[5:0] = *h : 3-line serial audio input format is set up. Refer to Chapter 3 for a setting value.
   ↓
7. &h01 [7:0] = 00h : RAM clear OFF
   ↓
8. Release mute terminal (MUTEX =”H”)

11. Sampling Rate and Clock Change

Please transmit the following command when you change of the serial audio data format, the sampling rate and the clock. Please execute this procedure when you do not use the clock stop automatic operation return function (Chapter 16-3).

1. Mute with terminal (MUTEX ="L")
↓
Please change serial digital audio data.(LRCLK, BCLK, SDATA)
↓
2. &h0A [2:0] = 7h : The input clock disappearance flag is cleared.
↓
○Please wait for about 20ms(Min.) until PLL is stabilized.
↓
3. &hE9 [7:0] = 34h : The system clock in IC is set.
↓
4. &h01 [7:0] = F0h : Execute RAM clear
↓
5. &h03[5:0] = *h : 3-line serial audio input format is set up. Refer to Chapter 3 for a setting value.
↓
6. &h04 [0] = 1 : Adjust the input data incorporation position.
↓
○It is about 1ms wait until the adjustment of the incorporation position is completed.
↓
7. &h04 [1] = 1 : Clear LRCK frame error flag.
↓
8. &h07 [1] = 1 : Clear LRCK-synchronous error signal.
↓
9. &h01 [7:0] = 00h : RAM clear OFF
↓
10. Set other register
↓
11. Release mute terminal (MUTEX ="H")

12. Setting of sampling rate and PLL

12-1. Sampling frequency setting

This IC does the settings such as sampling rates and PLL by the automatic operation in using X 'tal (12.288MHz). In this case, please set only the bit clock frequency of audio serial input data. Please follow the following tables about the setting.

・Table for sampling rate

Input sampling frequency [kHz]	Bit clock frequency (&h03[5:4])		
	32fs	48fs	64fs
8.000	-	-	○
11.025	-	-	○
12.000	-	-	○
16.000	○	-	○
22.050	○	-	○
24.000	○	-	○
32.000	○	○	○
44.100	○	○	○
48.000	○	○	○
88.200	○	○	○
96.000	○	○	○
176.400	○	○	○
192.000	○	○	○

Moreover, it is also possible to change the setting of the sampling frequency with the manual.

Input sampling frequency change setting

Default = 1

Select Address	Value	Explanation of operation
&h0B [5]	0	Manually setting
	1	Automatically setting (Initial)

SRC output setting

Default = 0

Select Address	Value	Explanation of operation
&h0B [4]	0	48kHz (Setting, except for Fs=8k, 16k, and 32kHz)
	1	32kHz (Setting in case of Fs=8k, 16k, and 32kHz)

Input sampling rate setting

Default = 8h

Select Address	Explanation of operation		
&h0B [3:0]	0 : 8kHz 1 : 11.025kHz 2 : 12kHz 3 : 16kHz	4 : 22.05kHz 5 : 24kHz 6 : 32kHz 7 : 44.1kHz 8 : 48kHz (Initial)	9 : 88.2kHz A : 96kHz B : 176.4kHz C : 192kHz Other : Inhibit

Automatic change setting of clock of BCLK dividing frequency

Default = 1

Select Address	Value	Explanation of operation
&h0D [1]	0	Manually setting
	1	Automatically setting

BCLK dividing setting

Default = 0

Select Address	Value	Explanation of operation
&h0D [0]	0	192 (Initial)
	1	128

*The following refer to details.

【Reference】

・Ratio of dividing frequency selection to PLLA when ratio of BCLK dividing frequency setting is made manual operation

Input sampling frequency	8kHz	11.025kHz / 12kHz	16kHz	22.05kHz / 24kHz	32kHz	44.1kHz / 48kHz	88.2kHz / 96kHz	176.4kHz / 192kHz
&h0D[0] Initial:0h	0h (192)	1h (128)	0h (192)	1h (128)	0h (192)	1h (128)	1h (128)	1h (128)

When &h0D [1] is made "0" (manual setting), it becomes effective. Initial value of &h0D [1] is "1" (automatic setting)

12-2. PLL setting when PWM sampling frequency is changed

To avoid the interference with the AM Radio Frequency belt, BM5449MWV can change the PWM sampling frequency (PWM hopping function). To change the PWM sampling frequency, &h30, &hE9, and &hEC register are set. The relation of the PWM career frequency to the setting of this register is as follows.

Relation of PWM sampling frequency to input sampling frequency

Input sampling frequency [kHz]	&h30[3:2]	&hE9	&hEC	PWM career frequency [kHz]
8, 12, 16, 24, 32 48, 96, 192	0h	34h	XXh	384
	2h	70h	00h	288
	1h		10h	336
11.025, 22.05, 44.1 88.2, 176.4	0h	34h	XXh	352.8
	2h	70h	00h	264.6
	1h		10h	308.7

*XXh means “Don’t care”

PWM hopping setting

Default = 0

Select Address	Value	Explanation of operation
&h30 [3:2]	0	8fs
	1	7fs
	2	6fs

PLL7 clock setting when PWM hopping function is used.

Default = 0

Select Address	Value	Explanation of operation
&hE9 [6]	0	Use X’tal clock (When PWM hopping function is not used)
	1	Use PLL7 clock (When PWM hopping function is used)

PLL7 operation setting 1 when PWM hopping function is used.

Default = 0

Select Address	Value	Explanation of operation
&hEC [4]	0	6 times multiply clocks (When you choose 6fs by the PWM hopping setting)
	1	7 times multiply clocks (When you choose 7fs by the PWM hopping setting)

PLL7 operation setting 2 when PWM hopping function is used.

Default = 1

Select Address	Value	Explanation of operation
&hEC [0]	0	PLL7 is activated.
	1	PLL7 is deactivated.

Please go according to the following procedure when you change the PWM sampling frequency.

1. Mute with terminal (MUTEX = “L”)
   ○X msec or more is waited for until MUTE hangs completely.
   X = (Mute transition duration setting) + 50msec

↓

2. &hEC[0] = 0h : PLL7 is activated (Normaly, it is deactivated)

↓

3. &hEC[4] = *h : Setting of PLL7 multiplier (“0” : 6 times multiply, “1” : 7 times multiply).

↓

4. &h30 [3:2] = *h : Setting for PWM hopping (“0” : 8 times multiply, “1” : 7 times multiply, “2” : 6 times multiply)

↓

5. &hE9[7:0] = 70h : The system clock inside IC is set up.

↓

○Please wait for about 20ms until PLL7 is stabilized.

↓

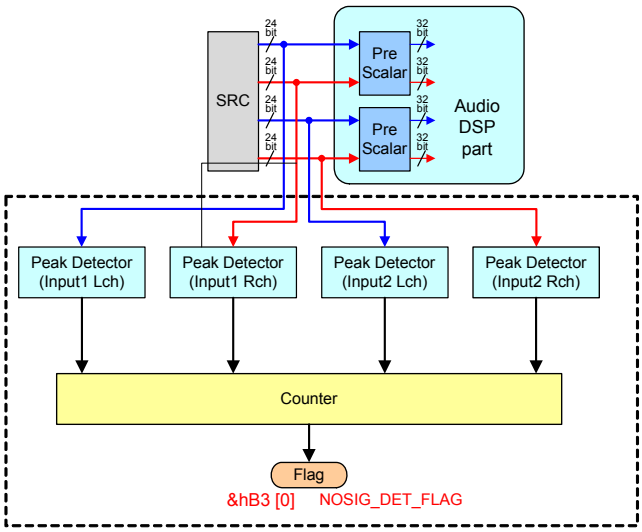
6. Release mute terminal (MUTEX = “H”)

13. Small signal input detection function

There is a function which detects the audio data input of a non-signal or a small signal. This function is used in order to reduce the standby power consumption of an audio set. Setting of a detection level and detection time can be performed.

If the signal below a setting detection level continues in both L channel and R channel, a small signal detection flag will become "H". A detection result can be read from command &hB3 [2:0]. The point which acts as a monitor of the small signal becomes input data of audio DSP block.

Block diagram



Mask setting for INPUT1 and INPUT2

Default = 0

Select Address	Value	Explanation of operation
INPUT1 &hB0 [7] INPUT2 &hB0 [6]	0	Not mask input signal
	1	Mask input signal

Detection level setting

Default = 00h

Select Address	Explanation of operation
&hB0 [4:0]	

Command	Level	Command	Level	Command	Level
00	-∞	08	-77dB	10	-69dB
01	-96dB	09	-76dB	11	-68dB
02	-92dB	0A	-75dB	12	-67dB
03	-88dB	0B	-74dB	13	-66dB
04	-84dB	0C	-73dB	14	-65dB
05	-80dB	0D	-72dB	15	-64dB
06	-79dB	0E	-71dB	16	-62dB
07	-78dB	0F	-70dB	17	-60dB

Detection time setting

Default = 0

Select Address	Value	Explanation of operation
&hB2 [5:4]	0	42.7ms
	1	85.3ms
	2	170.7ms
	3	341.3ms

* Sampling frequency is value of Fs = 48 kHz. In the case of Fs = 44.1 kHz, it will be about 1.09 times the setting value.

Detection flag read-back (Read Only)

Select Address	Value	Explanation of operation
&hB3 [0]	0	Un-detecting.
	1	Detecting

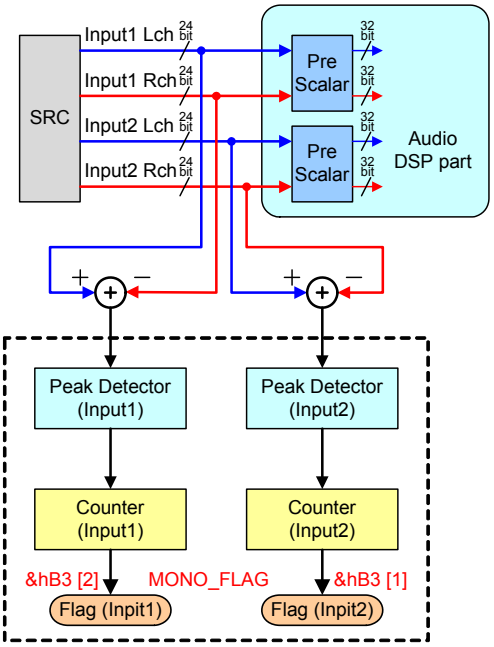
14. Monaural / Stereo detection

This block judges whether the input signal is monaural or stereo, and outputs the flag.

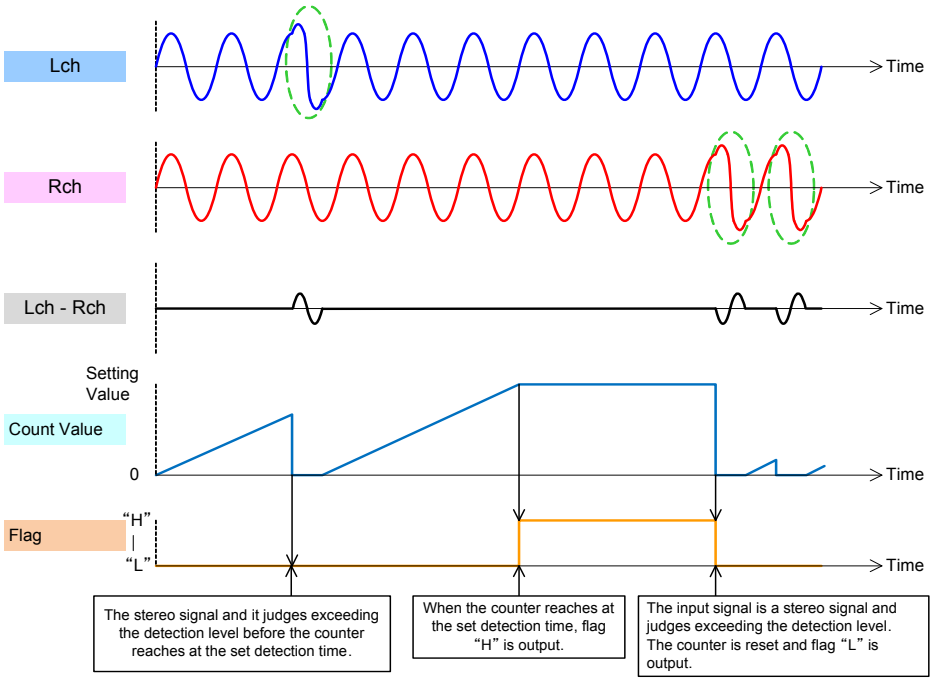
When the peak value of the difference between Lch and Rch of the input signal is detected, and the signal below the set value is consecutive, it is judged monaural. Afterwards, the flag of the register reading outputs H.

However, judge monaural for a no input signal and the signal taken with an AD convertor together with the small signal detecting function in Chapter 11. (It is judged monaural and the flag outputs H to the no sound part between tunes. Have the same meaning as the no sound part of the stereo signal because the small signal detection flag also outputs H in this case.)

The detection result can be read from command &hB3 [2:1]. The place that monitors signals becomes an entrance in the DSP block.



Explanation of monaural/stereo detection block



Detection time setting

Default = 0

Select Address	Value	Explanation of operation
&hB2 [1:0]	0	42.7ms
	1	85.3ms
	2	170.7ms
	3	341.3ms

*It is a value at sampling frequency Fs=48 kHz time. In case of Fs=44.1kHz, increases to about 1.09 times that of the set value.

LR difference detection level setting

Default = 0h

Select Address	Explanation of operation
&hB1 [2:0]	

Command	Detection level
0	-∞dB
1	Under -96dB
2	Under -90dB
3	Under -84dB
4	Under -78dB
5	Under -72dB
6	Under -66dB
7	Under -60dB

Detection flag reading (Read Only)

Select Address	Value	Explanation of operation
Input1 &hB3 [2]	0	Not detect
Input2 &hB3 [1]	1	Detect

15. Channel delay memory

In the main output and the sub output, there are delay memories for the phase correction for 128 samples or less.

Delay mode setting

Default = 0

Select Address	Value	Explanation of operation
&h30 [1:0]	0	All of 4ch is possible the delay.
	1	Only Main Lch and Main Rch are possible the delay.
	2	Only Sub Lch and Sub Rch are possible the delay.

Method of setting delay memory

・Delay Value = 0d{Command Value} / Fs [s]

Ex)

Sampling frequency Fs = 48 kHz

Setting value = 33h → Converts 33h into the decimal number 0d51.

Delay value = 51 / 48000

= 1.0625ms

It corresponds to the delay of about 37cm when assuming speed of sound 346m/s.

Lch delay setting command for Main output: &h31 [6:0]

Rch delay setting command for Main output: &h32 [6:0]

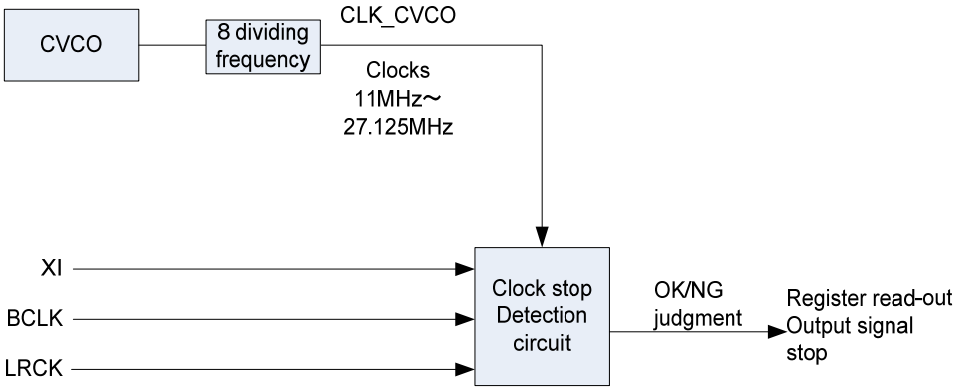
Lch delay setting command for Sub output: &h33 [6:0]

Rch delay setting command for Sub output: &h34 [6:0]

16. Clock stop detection and synchronous blank detection

16-1 Clock stop detection

A necessary clock for the audio processing is generated by supplying two or more clocks in this IC, and using these clocks. The clock for the audio processing might stop, too, when the clock supplied from the outside stops and the detector to evade these is needed. The detected clock has detected the state with XI, BCLK, and LRCK with internal CVCO clock.



When the clock stops at the time set depending on the command, the stop detection condition of each clock is detected. As for the detection result, reading from the register is possible. As a result of the judgment as the stop once, it is not cleared until a clear command is transmitted even if the state of the clock returns normally.

XI, LRCK, BCLK stop detection time setting
Default = 0h

Select Address	Value	Explanation of operation
XI &h08 [6:4] LRCK &h08 [2:0] BCLK &h09 [6:4]	0	About 100μs
	1	About 200μs
	2	About 300μs
	3	About 400μs
	4	About 500μs
	5	About 600μs
	6	About 700μs
	7	About 800μs

*The above-mentioned detection time reaches the value when the clock stop decision circuit operates by 27.125MHz.

Clock stop flag reading register (Read Only)

Select Address	Value	Explanation of operation
&h0A [6]	0	Normal
	1	XI clock stop detect
&h0A [5]	0	Normal
	1	LRCK clock stop detect
&h0A [4]	0	Normal
	1	BCLK clock stop detect

Clock stop flag clear (Write Only)

Select Address	Explanation of operation
&h0A [2]	When "1" is written, the XI stop flag is cleared.
&h0A [1]	When "1" is written, the LRCK stop flag is cleared.
&h0A [0]	When "1" is written, the BCLK stop flag is cleared.

*When the clock stop automatic return function (Chapter 16-3) is used, these flags are cleared by the automatic operation.

16-2 Synchronous blank detection

As for synchronous blank detecting function, it detects as synchronous blank error when it counts between the rising edges of LRCK with internal clock (49.152MHz), and it shifts more than the definite value, and whether PLL is normally locked is judged.

Input sampling frequency	8kHz	12kHz	16kHz	24kHz	32kHz	48kHz	96kHz	192kHz
Count value (Start of counting from 0)	6143	4095	3071	2047	1535	1023	511	255

As for the detection result, reading from the register is possible. As a result of the judgment as synchronous blank once, it is not cleared until a clear command is transmitted even if the state of the clock returns normally. Moreover, the setting of the detection approval frequency is also possible, and if the error more than the predetermined number is detected, the flag (&h07 [1]) becomes "1" by the command.

Synchronous blank flag reading register (Read Only)

Select Address	Value	Explanation of operation
&h07 [1]	0	Normal
	1	Synchronous blank detect

Synchronous blank flag clear register (Write Only)

Select Address	Explanation of operation
&h07 [0]	When "1" is written, the synchronous blank flag is cleared.

*When the clock stop automatic return function (Chapter 16-3) is used, these flags are cleared by the automatic operation.

Synchronous blank count setting

Default = 1h

Select Address	Explanation of operation
&h07 [6:4]	1 or more is set. (It should be set from 1 to 7) If synchronous blank more than the set number of count is detected, & h07 [1] becomes "1".

16-3 Clock stop automatic return function

When the clock stop, the synchronous blank, and the frame error are detected, DSP stops the PWM output. Moreover, the serial audio output outputs the no signal data to SDATAO and does the free run. When the clock returns, the function to restart the DSP processing by the automatic operation is built into. The automatic return function is effective to initial value. Each error flag (&h0A [5:4], &h07 [1], and &h04 [2]) returns to 0 when returning automatically. Moreover, the register to confirm whether the error occurred separately is prepared, and the state of the error can be monitored in that.

Clock stop automatic return function selection register
Default = 2h

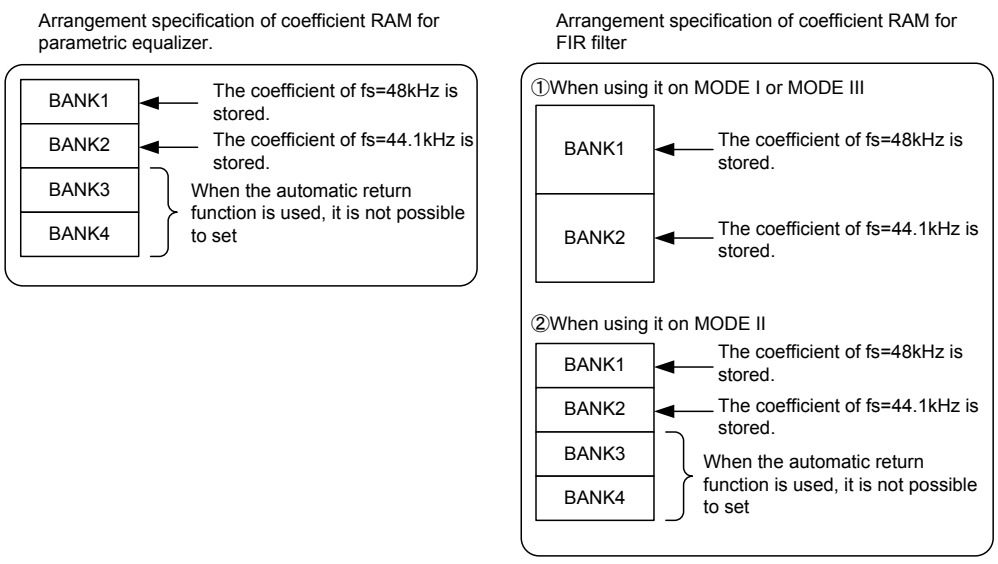
Select Address	Value	Explanation of operation
&h0E [1]	0	It decides it with &hA1 [3:2]. (manual change)
	1	It changes automatically by input fs.
&h0E [0]	0	Automatic return function ON
	1	Automatic return function OFF

Clock stop, frame, and synchronous error detection monitor register
Default = 0h

Select Address	Value	Explanation of operation
&h0F [7]	0	Normal. When 0 is written, the flag of this bit is cleared.
	1	Flame error flag detection monitor.
&h0F [6]	0	Normal. When 0 is written, the flag of this bit is cleared.
	1	Synchronous error flag detection monitor.
&h0F [5]	0	Normal. When 0 is written, the flag of this bit is cleared.
	1	XI clock stop flag detection monitor.
&h0F [4]	0	Normal. When 0 is written, the flag of this bit is cleared.
	1	LRCK clock stop flag detection monitor.
&h0F [3]	0	Normal. When 0 is written, the flag of this bit is cleared.
	1	BCLK clock stop flag detection monitor.
&h0F [2:0]	-	Monitor for IC test, Read Only

When the automatic return function is made effective, the limitation is generated in the usage of coefficient RAM used with the parametric equalizer and coefficient RAM and used with the FIR filter.
The coefficient for the parametric equalizer stores the coefficient for 48 kHz in BANK1, and stores the coefficient for 44.1 kHz in BANK2. BANK3 and BANK4 cannot be used (It is disregarded even if it sets it).
The method of the setting to each BANK according to the operation mode changes into the coefficient for the FIR filter. Store the coefficient for 48kHz in BANK1 when using it by MODE I and Ⅲ, and store the coefficient for 44.1kHz in BANK2. Store the coefficient for 48kHz in BANK1 when using it with MODE Ⅱ, and store the coefficient for 44.1kHz in BANK2. BANK3 and BANK4 cannot be used (It is disregarded even if it sets it).

About the restriction matter of the automatic return function from the clock error



17. Software reset function

In this IC, the software reset by the command setting can be done. Execute the software reset after effectively setting the software reset. &hFB 0 shows "1" while executing the software reset. When the reset processing is completed, it is cleared automatically.

Software reset effective setting

Default = 0

Select Address	Value	Explanation of operation
&hFA [7]	0	Software reset is invalid.
	1	Software reset is valid.

Software reset execution setting

Default = 0

Select Address	Value	Explanation of operation
&hFB [0]	0	Release software reset.
	1	Execute software reset. (After the softreset is completed, it is cleared automatically.)

*When the softreset is executed, it is not executed if &FA 7 is not set to "1".

●Application Example (Stereo BTL output, RL=8Ω)

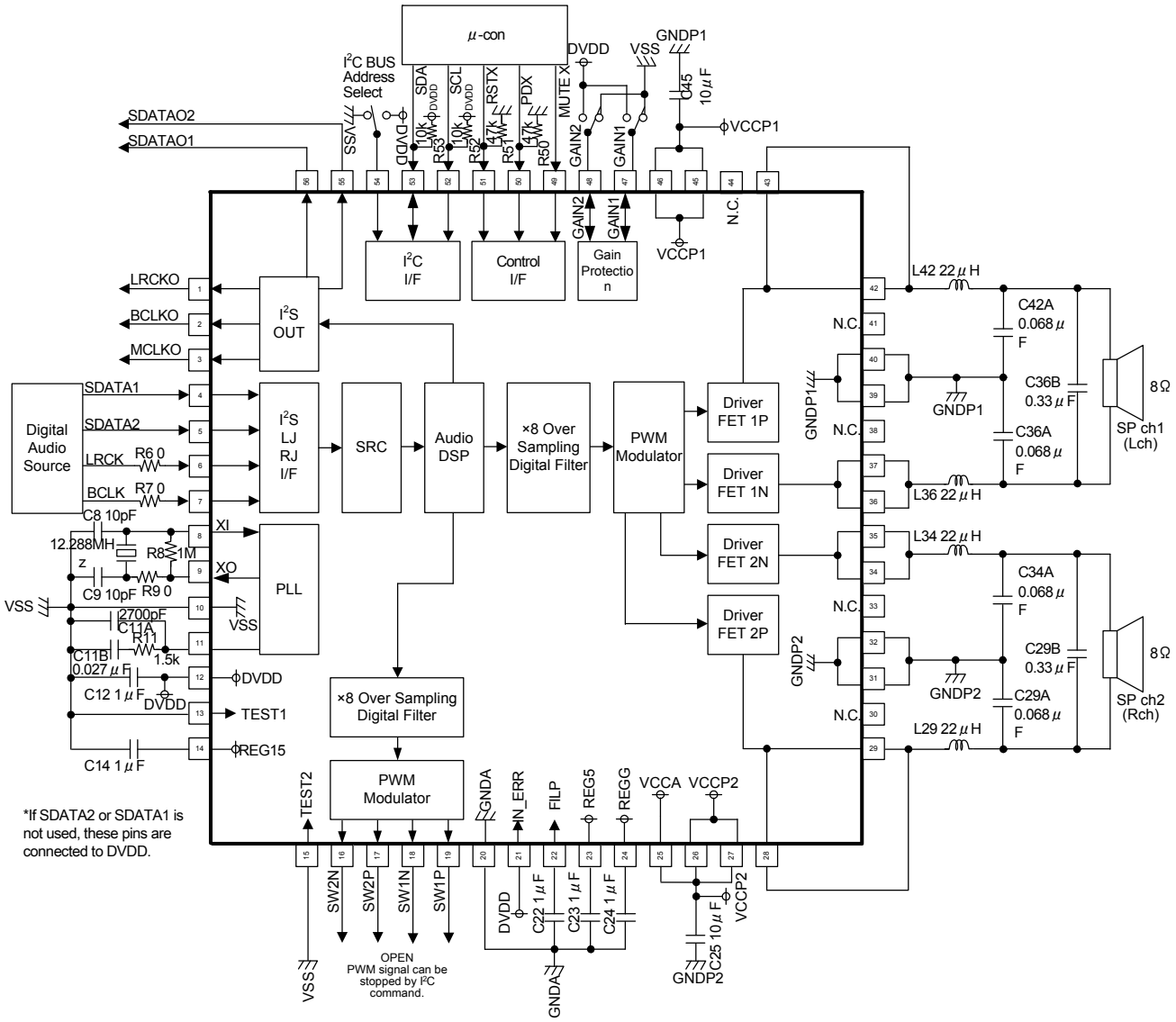


Figure 33. Application Example (Stereo BTL output, RL=8Ω)

●Application Example (Monaural PBTL output, RL=4Ω)

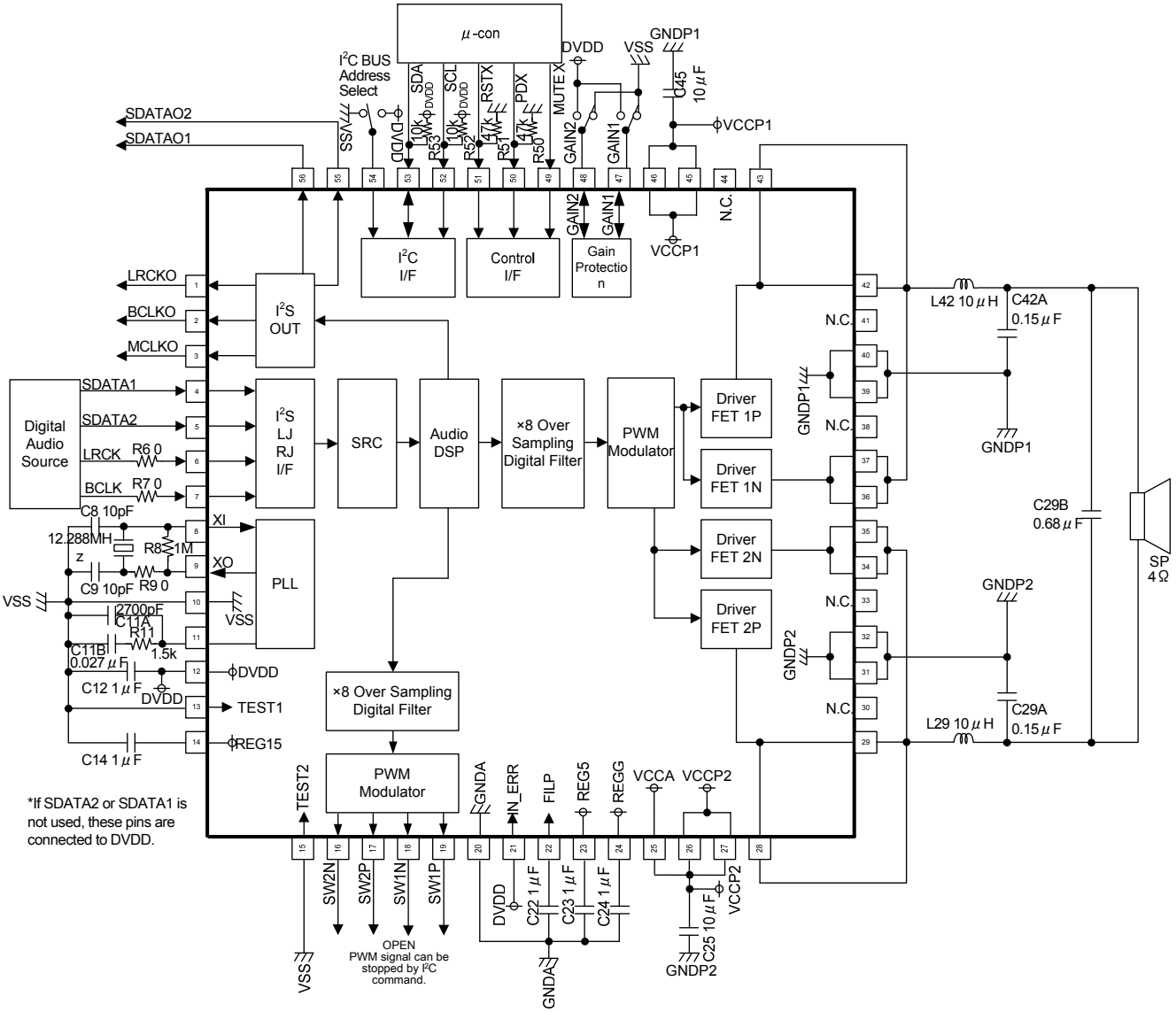


Figure 34. Application Example (Monaural PBTL output, RL=4Ω)

● Application Example (2.2ch application, RL=8Ω)

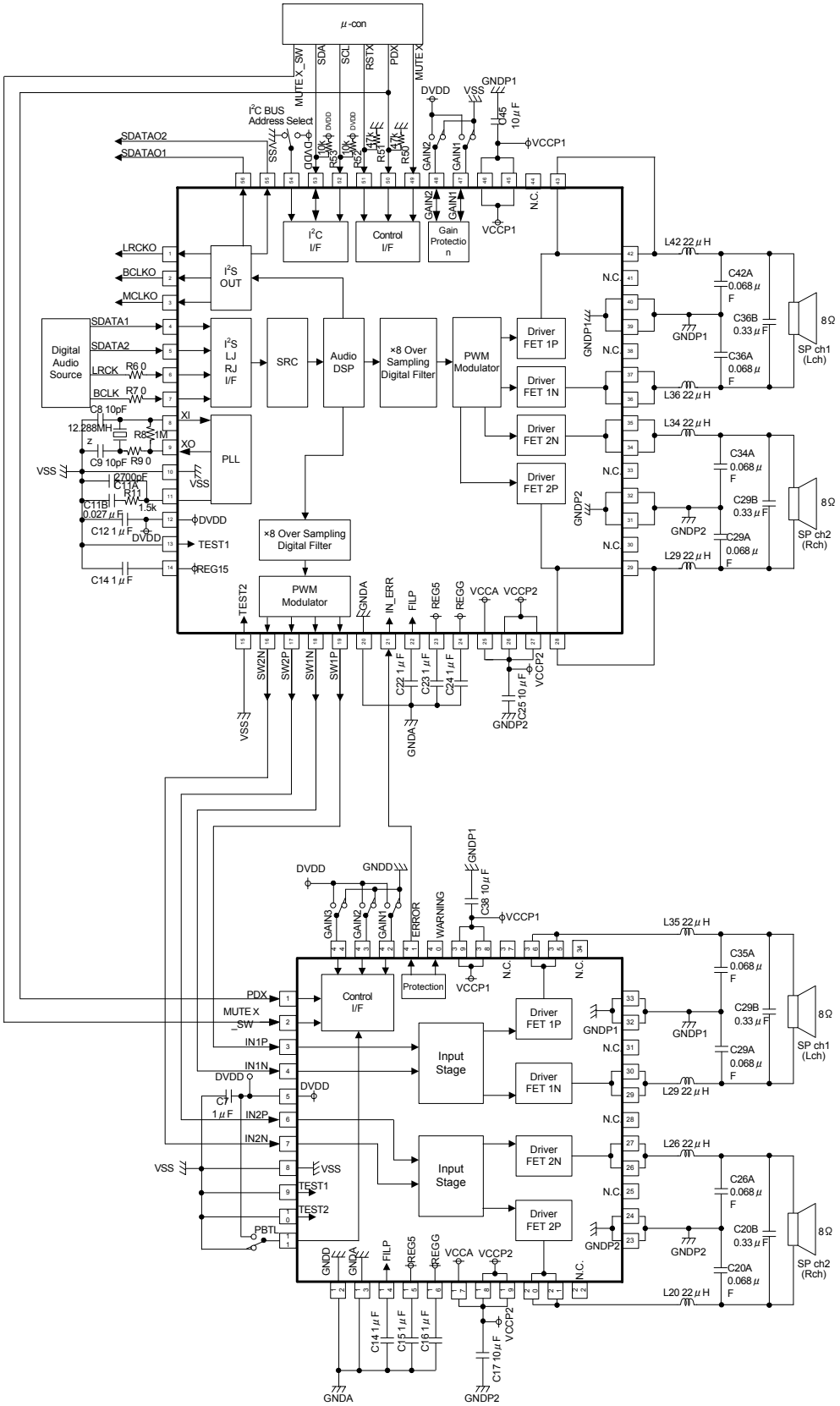


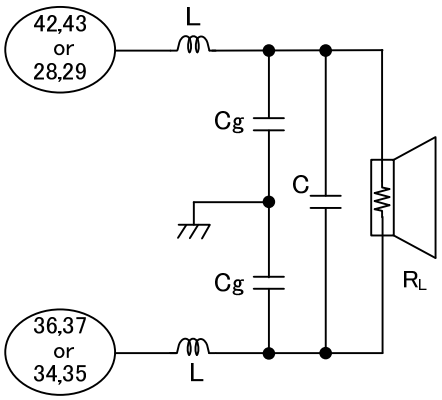
Figure 35. Application Example (2.2ch application, RL=8Ω)

●Selection of Components Externally Connected

(1)Output LC Filter Circuit

An output filter is required to eliminate radio-frequency components exceeding the audio-frequency region supplied to a load (speaker). Because this IC uses sampling clock frequencies from 256 kHz to 384 kHz in the output PWM signals, the high-frequency components must be appropriately removed.

This section takes an example of an LC type LPF shown in Figure 12. , in which coil L and capacitor C compose a differential filter with an attenuation property of -12dB/oct. A large part of switching currents flow to capacitor C, and only a small part of the currents flow to speaker R_L. This filter reduces unwanted emission this way. In addition, coil L and capacitor Cg compose a filter against in-phase components, reducing unwanted emission further.



Following presents output LC filter constants with typical load impedances.

R_L	L	Cg	C_{BTL}
4Ω	10μH	0.15μF	0.68μF
6Ω	15μH	0.1μF	0.47μF
8Ω	22μH	0.068μF	0.33μF

Use coils with a low direct-current resistance and with a sufficient margin of allowable currents. A high direct-current resistance causes power losses. In addition, select a closed magnetic circuit type product in normal cases to prevent unwanted emission.

Use capacitors with a low equivalent series resistance, and good impedance characteristics at high frequency ranges (100 kHz or higher). Also, select an item with sufficient withstand voltage because flowing massive amount of high-frequency currents is expected.

(2)BOM list (Stereo BTL output, R_L=8Ω)

Parts	Parts No.	Value	Company	Product No.	Rated Voltage	Tolerance
IC	U1	-	ROHM	BM5449MWV	-	-
Inductor	L29, L34, L36, L42	22μH	TOKO	B1047AS-220M	-	(±20%)
Resistor	R9	1.5k ohm	ROHM	MCR03EZPJ152	1/10W	J(±5%)
	R8	1M ohm		MCR03EZPJ105	1/10W	J(±5%)
	R11	1.5k ohm		MCR03EZPF1501	1/16W	F(±1%)
	R52, R53	100k ohm		MCR03EZPJ104	1/10W	J(±5%)
Capacitor	C25, C45	10μF	MURATA	GRM31CB11H106KA75L	50V	B(±10%)
	C29B, C36B	0.33μF		GRM219B31H334KA87	50V	B(±10%)
	C29A, C34A, C36A, C42A	0.068μF		GRM21BB11H683KA01	50V	B(±10%)
	C12, C14, C22 C23, C24	1μF		GRM185B31C105KE43	16V	B(±10%)
	C11B	0.027μF		GRM033B10J273KE01	6.3V	B(±10%)
	C11A	2700pF		GRM033B10J272KA01	6.3V	B(±10%)
	C8, C9	10pF		GRM188B11E100KA01	25V	B(±10%)
Oscillation unit	X8	12.288MHz	NIHON DENPA KOGYO	NX5032GA	-	-

The CERALOCK can be used instead of the X'tal. The constant is as follows.
However, the frequency accuracy worsens compared with the crystal oscillation. The gap might be caused in the sampling frequency detection result.

Parts	Parts No.	Value	Company	Product No.	Rated Voltage	Tolerance
Resistor	R9	220 ohm	ROHM	MCR03EZPJ221	1/10W	J (±5%)
	R8	1M ohm	ROHM	MCR03EZPJ105	1/10W	J (±5%)
Capacitor	C8, C9	33pF	ROHM	It is built into the oscillation unit (CSTCE12M2G55-R0)	-	-
Oscillation unit	X8	12.288MHz	MURATA	CSTCE12M2G55-R0	-	-

As return of current regenerated by back EMF of output coil happens, take steps such as putting capacitor between power supply and GND as an electric pathway for the regenerated current. Be sure that there is no problem with each property such as emptied capacity at lower temperature regarding electrolytic capacitor to decide capacity value. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

(3) The settlement of the snubber

When over/undershoot of the output PWM exceeds rating, it must insert the snubber circuit shown below.

① Measure the spike resonance frequency f1 of the PWM output wave shape (When it stands up.) by using FET probe in the OUT terminal. (Figure 79) The FET probe is to monitor very near pin and shorten ground lead at the time of that.
② Measure resonance frequency f2 of the spike as a snubber circuit fixed number R=0Ω（Only with the condenser C, to connect GND） At this time, the value of the condenser C is adjusted until it becomes half of the frequency (2f2=f1) of the resonance frequency f1 of ①. The value of C which it could get here is three times of the parasitic capacity Cp that a spike is formed. (C=3Cp)
③ Parasitic inductance Lp is looked for at the next formula.

$$L_p = \frac{1}{(2\pi f_1)^2 C_p}$$

④ The character impedance Z of resonance is looked for from the parasitic capacity Cp and the parasitism inductance Lp at the next formula.

$$Z = \sqrt{\frac{L_p}{C_p}}$$

⑤ A snubber circuit fixed number R is set up in the value which is the same as the character impedance Z. A snubber circuit fixed number C is set up in the value of 4-10 times of the parasitic capacity Cp. (C=4Cp～10Cp) Decide it with trade-off with the character because switching electric currents increase when the value of C is enlarged too much.

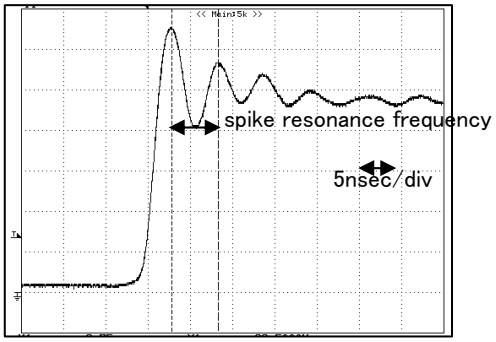


Figure 36. PWM Output waveform
（measure of spike resonance frequency

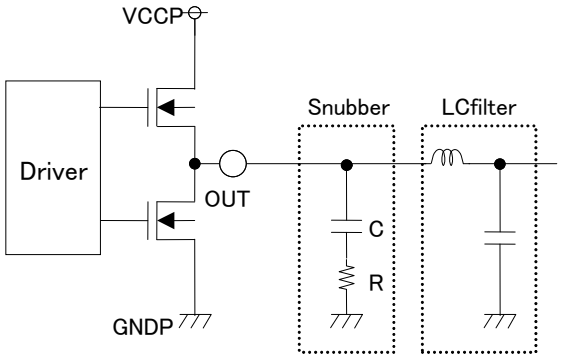


Figure 37.Snubber schematic

●About circuit board layout

Be careful of the following order of priority, and design a circuit board layout.

①C25・C45(10uF)・C12(1uF) put shortest compared with VCC and GND.
②The thermal pattern on the back connected with the GND.
③C14・C22・C23・C24(1uF) put shortest compared with each pin and GND.
④Each GND line connected by one point without common impedance.
⑤Each power supply and each GND are divided
⑥GND pattern of both side connected with the a lot of VIA electric contacts to lower the impedance of GND.
⑦GND area of the heat radiation area widen to improve the heat radiation ability.

Reference：ROHM designed 4 layer board

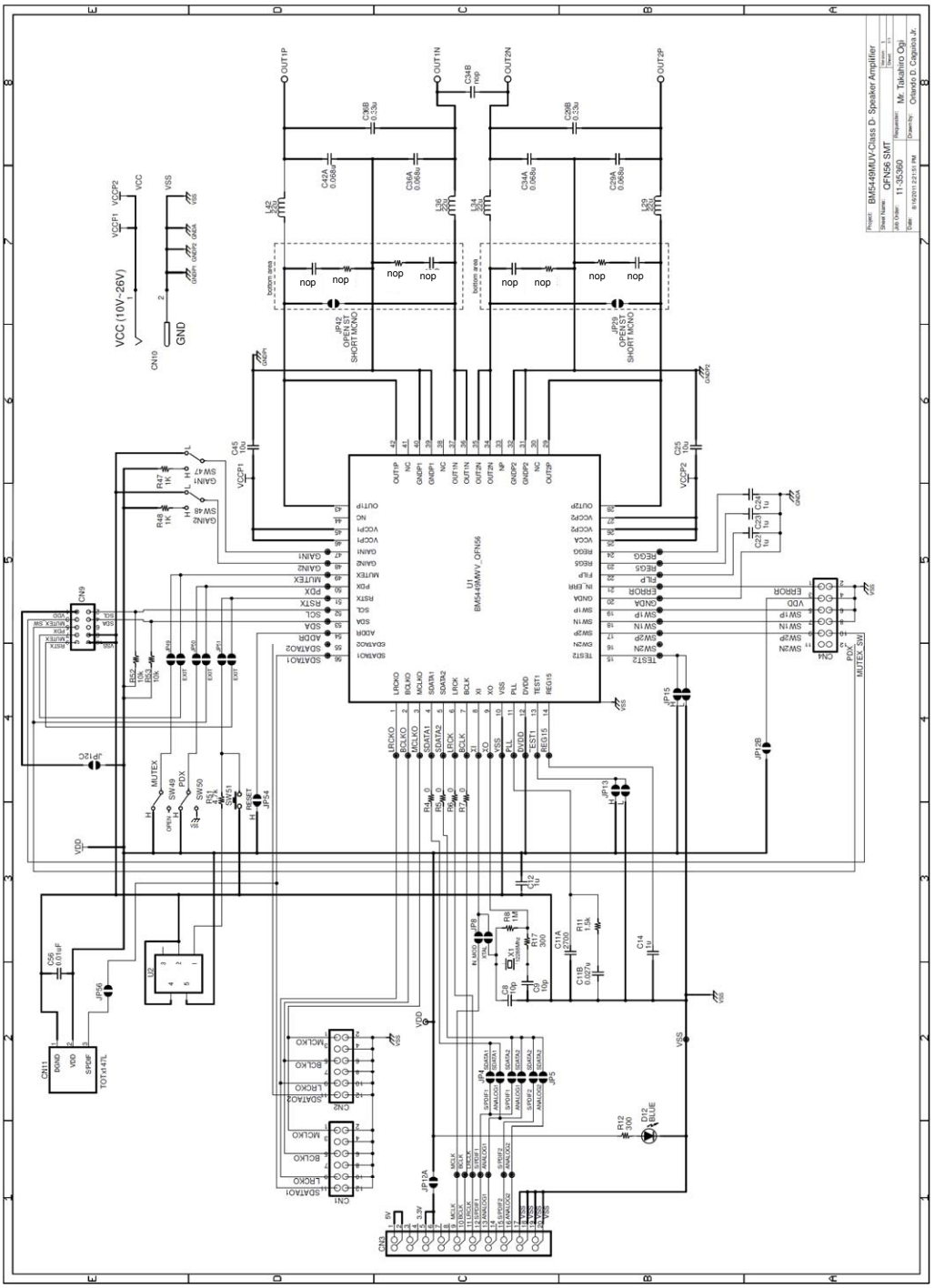


Figure 38. ROHM designed 4layer board

参考：ROHM designed 4 layer board SilkScreen

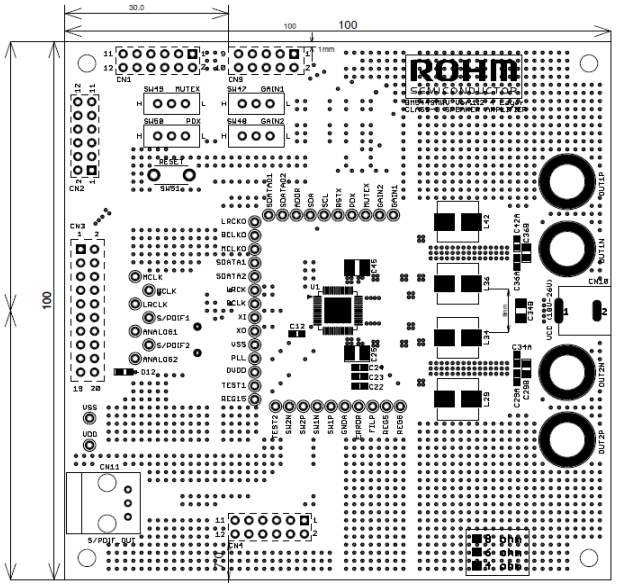


Figure 39. Top Layer Silk Screen (Top View)

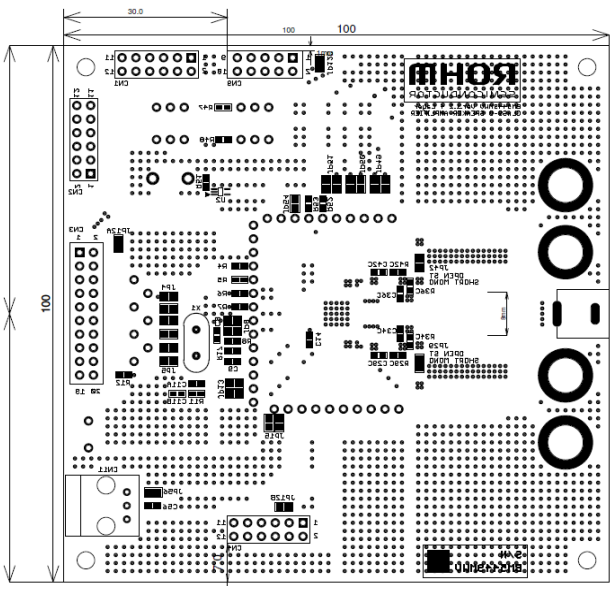


Figure 40. Bottom Layer Silk Screen (Top View)

ROHM designed 4-layer board Copper Layer

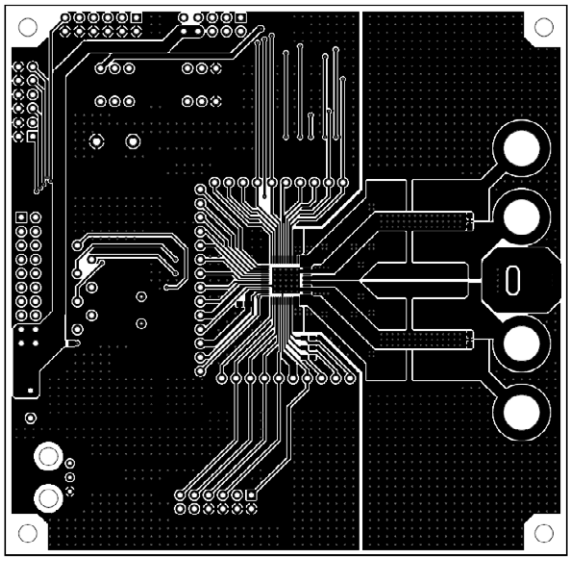


Figure 41. Top Copper Layer (Top View)

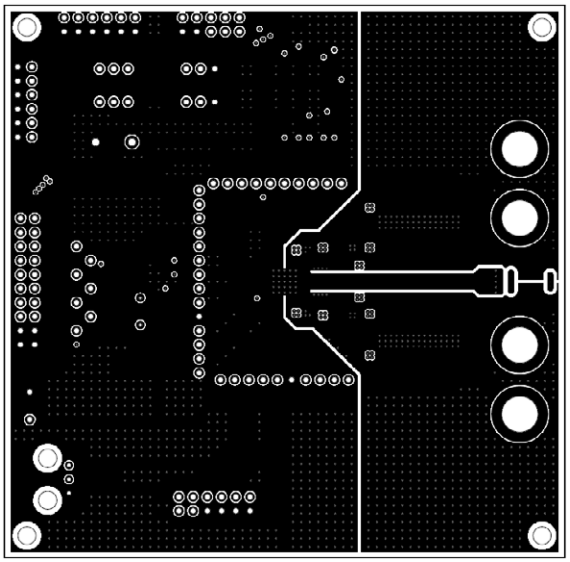


Figure 42. Mid Copper Layer1 (Top View)

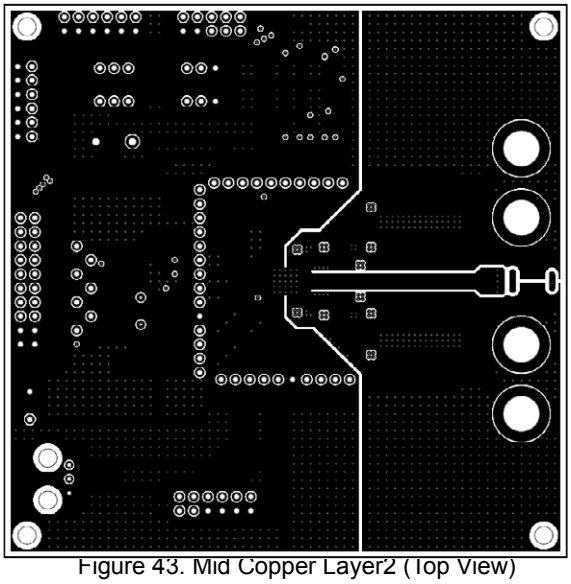


Figure 43. Mid Copper Layer2 (Top View)

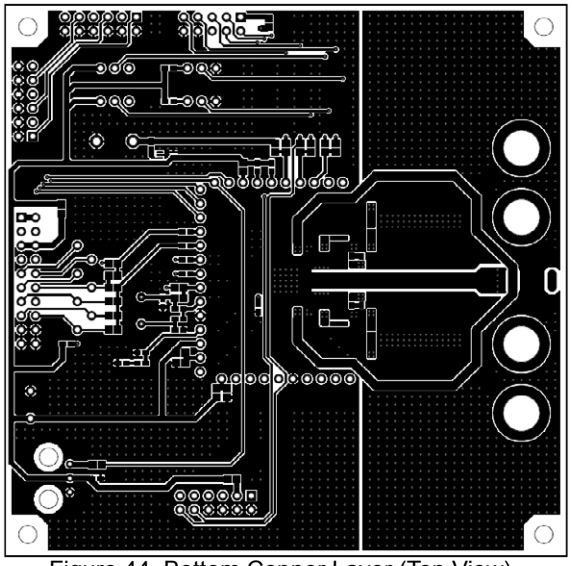
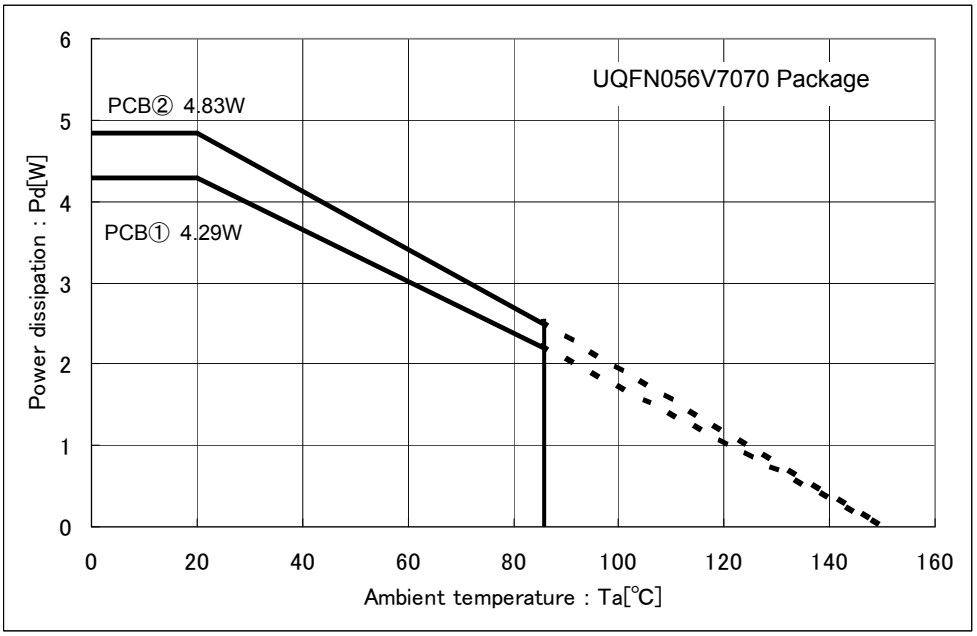


Figure 44. Bottom Copper Layer (Top View)

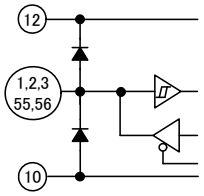
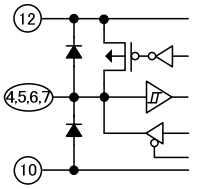
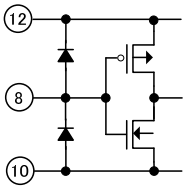
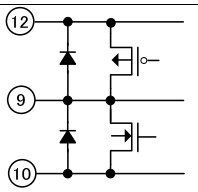
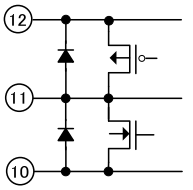
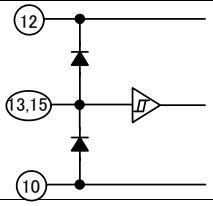
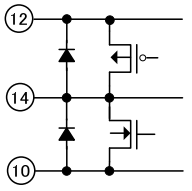
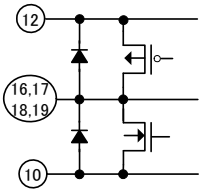
●Power Dissipation



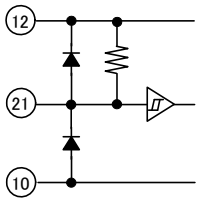
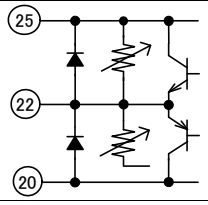
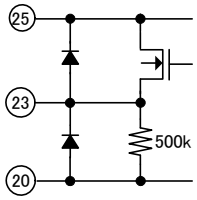
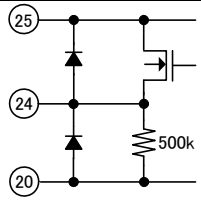
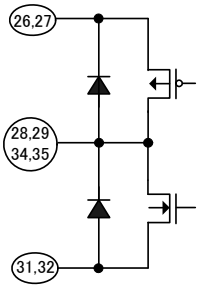
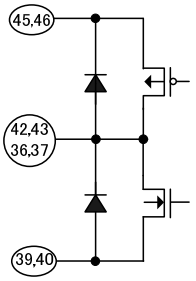
Measuring instrument:TH-156(Shibukawa Kuwano Electrical Instruments Co., Ltd.)
Measuring conditions: Installation on ROHM's board
Board size : 74.2mm x 74.2mm x 1.6mm (with thermal via on board)
Material : FR4
・The board and exposed heat sink on the back of package are connected by soldering.

PCB①:4-layer board (Top and bottom layer back copper foil size:34.09mm^2
2nd, 3rd layer back copper foil size:5505mm^2), θja＝29.1℃/W
PCB②:4-layer board (back copper foil size:5505mm^2), θja＝25.9℃/W

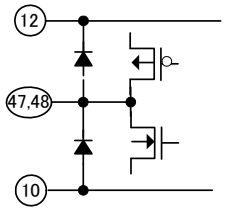
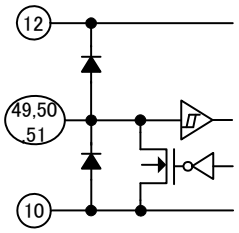
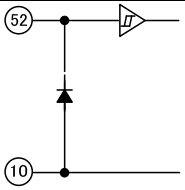
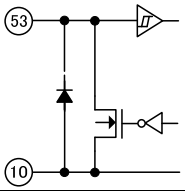
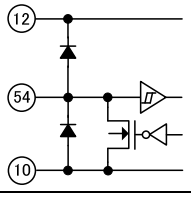
●I/O equivalence circuit (Provided pin voltages are typ. Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
55 56 1 2 3	SDATAO2 SDATAO1 LRCKO BCLKO MCLKO	V_{DD} to 0V	Digital Audio signal output pin	
4 5 6 7	SDATA1 SDATA2 LRCK BCLK	3.3V	Digital Audio signal input pin	
8	XI	-	X'tal input pin	
9	XO		X'tal output pin	
10	VSS	0V	GND pin for Digital block	-
11	PLL		PLL's filter pin	
12	DVDD	3.3V	Power supply pin for Digital I/O Please connect the capacitor	-
13 15	TEST1 TEST2	-	Test pin Please connect to VSS.	
14	REG15	1.5V	Internal power supply pin for Digital circuit Please connect the capacitor	
16 17 18 19	SW2N SW2P SW1N SW1P	V_{DD} to 0V	PWM Ouput for Subwoofer	

●I/O equivalence circuit (Provided pin voltages are typ. Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
20	GNDA	0V	GND pin for analog signal	-
21	IN_ERR	5V	Error flag input pin H: Normal state L: Error detect	
22	FILP		Standard pin for power stage Please connect the capacitor	
23	REG5	5V	Internal power supply pin for Power Stage Please connect the capacitor	
24	REGG	5V	Internal power supply pin for Gate Driver Please connect the capacitor	
25	VCCA	Vcc	Power supply pin for analog block Please connect the capacitor	-
26,27	VCCP2	Vcc	Power supply pin for ch2 PWM signal Please connect the capacitor	
28,29	OUT2P	Vcc to 0V	Output pin of ch2 positive PWM Please connect to Output LPF.	
31,32	GNDP2	0V	GND pin for ch2 PWM signal	
34,35	OUT2N	Vcc to 0V	Output pin of ch2 negative PWM Please connect to Output LPF.	
36,37	OUT1N	Vcc to 0V	Output pin of ch1 negative PWM Please connect to Output LPF.	
39,40	GNDP1	0V	GND pin for ch1 PWM signal	
42,43	OUT1P	Vcc to 0V	Output pin of ch1 positive PWM Please connect to Output LPF.	
45,46	VCCP1	-	Power supply pin for ch1 PWM signal Please connect the capacitor	

●I/O equivalence circuit (Provided pin voltages are typ. Values)

NO.	Pin Name	Pin voltage	Pin explanation	Internal equivalence circuit
30,33 38,41 44	N.C.	-	Non connection pin	-
47	GAIN1	0V	Gain setting pin for restriction on output power consumption This pin can be changed WARNING flag by command. [Set for WARNING flag] This pin is configured as an open-drain output. Please attach 100kohm pull-up resistance to 3.3V. H: Normal L: Indication of WARNING	
48	GAIN2	0V	Gain setting pin for restriction on output power consumption This pin can be changed ERROR flag by command. 【Set for ERROR flag】 This pin is configured as an open-drain output. Please attach 100kohm pull-up resistance to 3.3V. H: Normal L: Indication of ERROR	
49	MUTEX	0V	Speaker output mute control pin H: Mute OFF L: Mute ON	
50	PDX	0V	Power down control pin H: Power down OFF L: Power down ON	
51	RSTX	0V	Reset pin for internal logic circuit H: Reset OFF L: Reset ON	
52	SCL	-	I^2C transmit clock input pin *The SCL pin doesn't correspond to 5V tolerant. Please use it within 4.5V of the absolute maximum rating.	
53	SDA	-	I^2C data input/output pin *The SDA pin doesn't correspond to 5V tolerant. Please use it within 4.5V of the absolute maximum rating.	
54	ADDR	0V	I^2C slave address select pin	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

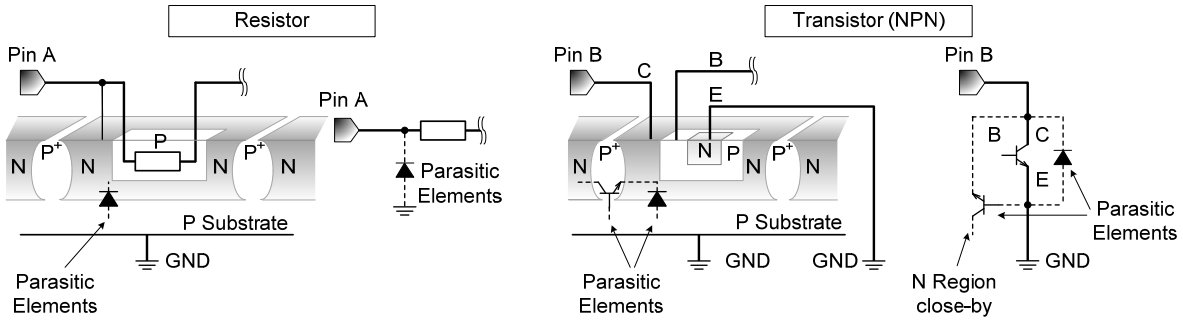


Figure xx. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

17. Power supply on/off (Pin 25, 26, 27, 45, 46)

In case power supply is started up, RSTX (Pin 51), PDX (Pin 50) and MUTEX (Pin 49) always should be set Low. And in case power supply is shut down, it should be set Low likewise. Then it is possible to eliminate pop noise when power supply is turned on/off. And also, all power supply terminals should start up and shut down together.

18. ERROR terminal (Pin 48), WARNING terminal(Pin 47)

The ERROR flag is outputted when Output short protection or DC voltage protection. And the WARNING flag is outputted when high temperature protection, under voltage protection or over voltage protection. This flag is the function which the condition of this product is shown in.

19. N.C.terminal (Pin 30, 33, 38, 41, 44)

N.C. terminal (Non Connection Pin) does not connect to the inside circuit. Therefore, possible to use open.

20. TESTterminal(Pin 13, 15)

TEST terminal connects with ground to prevent the malfunction by external noise.

Operational Notes – continued

21. Precautions for Speaker-setting

If the impedance characteristics of the speakers at high-frequency range while increase rapidly, the IC might not have stable-operation in the resonance frequency range of the LC-filter. Therefore, consider adding damping-circuit, etc., depending on the impedance of the speaker.

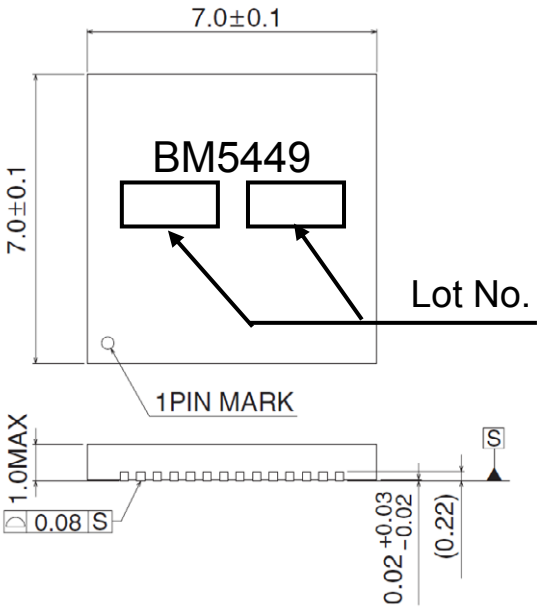
●Ordering Information

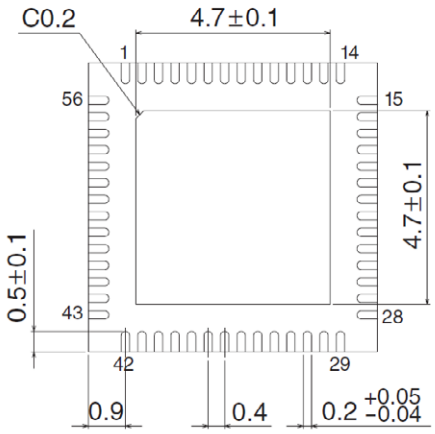
B	M	5	4	4	9	M	W	V	-	E2

Package
MWV:
UQFN056V7070

Packaging and forming specification
E2: Embossed tape and reel

●Marking Diagram

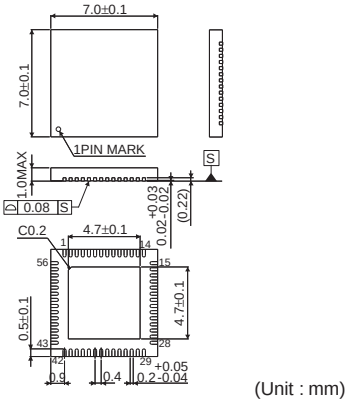




(UNIT: mm)
PKG: UQFN056V7070
Drawing No: EX465-5001-1

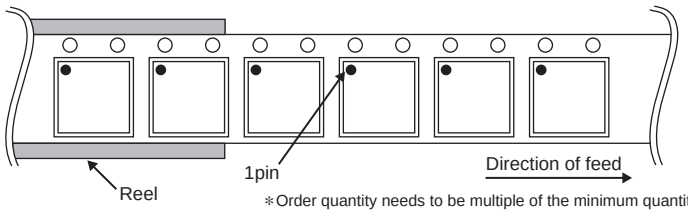
●Physical Dimensions Tape and Reel Information

UQFN056V7070



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Revision History

Date	Revision	Changes
18.Sep. 2012	001	New Release
15.Oct. 2012	002	P102,103 Add PWM setting. P129 pin47,48 1.Change equivalence circuit. 2.Change Pin explanation.
7.FEB.2013	003	P30 revise BM5443 to BM5449
5.JAN.2015	004	Modify P118-P120 application circuit Modify Operation notes

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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