DS3923

High-Speed Current Mirror with Sample/Hold Output

General Description

The DS3923 high-speed current mirror integrates high-voltage devices necessary for monitoring the burst-mode receive power signal in avalanche photodiode (APD) biasing and optical line terminal (OLT) applications. It provides small and large gain current mirror outputs to monitor the APD current. A sample/hold circuit with automatic gain selection captures the sampled signal so that an external ADC can accurately measure the signal. An adjustable current clamp limits current through the APD. The clamp also features an external shutdown. An integrated FET is also provided which can be used to quickly clamp the high-voltage bias to ground in the case of high optical input power.

The DS3923 is available in a 24-pin TQFN package and operates over an extended temperature range of -40°C to +95°C.

Applications

- APD Monitoring
- GPON OLT
- 10GPON OLT

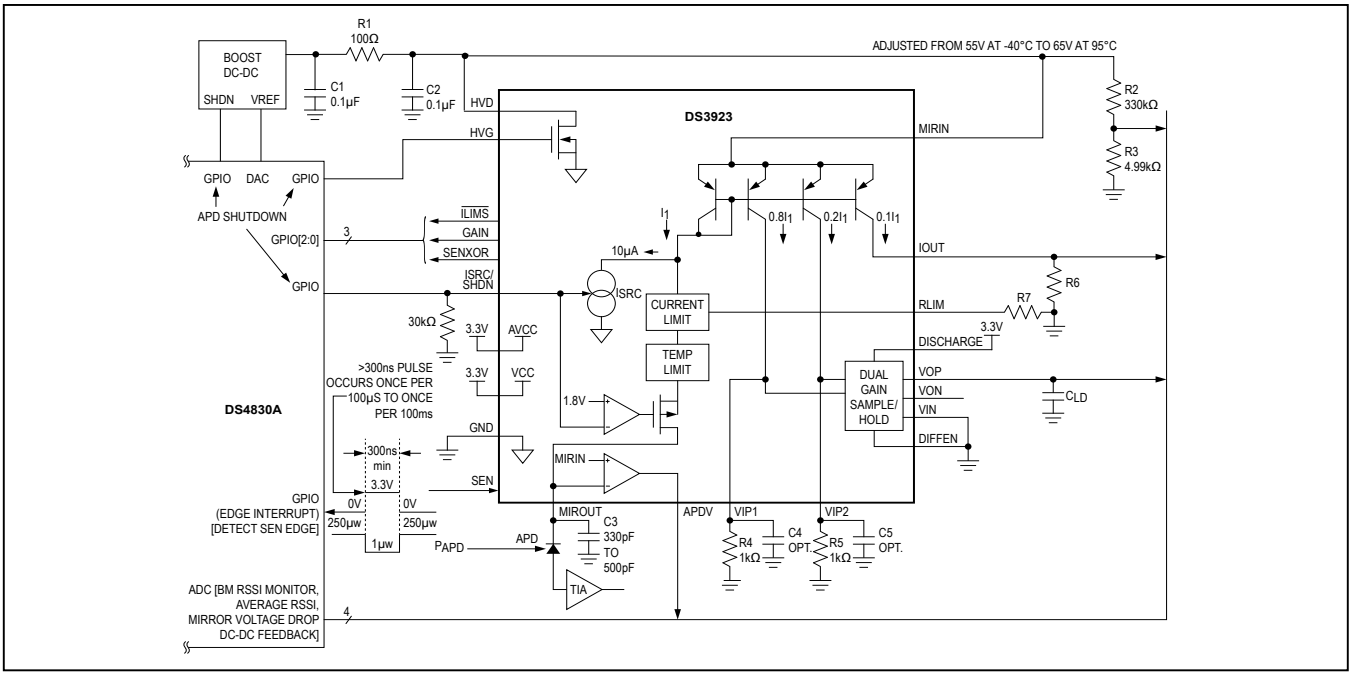
***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Accurate Burst-Mode RSSI Measurement with Two Current Mirror Outputs Improves Dynamic Range
  - -32dBm to -5dBm Optical Input Range
  - ±0.5dB Accuracy
  - Sampling Period as Short as 300ns
  - Pin Discharge Option
- Low-Noise APD Bias with Shutdown Options Reduces Receiver Sensitivity
  - 15V to 76V APD Bias
  - External Capacitor Connection for Controlled RC Time Constant of APD Voltage Filter
  - Current Clamp with Adjustable Limit and External Shutdown with Limit Status
  - High-Voltage Switch FET for APD Fast Shutdown
- Small Package Reduces Total Solution Size and Cost
  - 3.5mm x 3.5mm, 24-Pin TQFN Package with Exposed Pad

For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/DS3923.related**.

Typical Application Circuit



maxim integrated™

Absolute Maximum Ratings

Voltage on HVD, MIRIN, MIRCAP, and MIROUT Relative to HVGND .....-0.3V to +79V
Voltage on V_{CC} and AVCC to GND .....-0.3V to + 4.3V
Voltage on All Other Pins Relative to GND.....-0.3V to (V_{CC} + 0.3V) Not to Exceed +4V

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 15.4mW/°C above +70°C).....1228.9mW
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{MIRIN} = 15V to 76V, V_{CC} = 2.85V to 3.63V, T_A = -40°C to +95°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low Voltage Supply	V_{CC}			2.85		3.63	V
Low Voltage Current	I_{CC}	(Note 2)			8	16	mA
MIRIN Quiescent Current	I_{MIRIN}	V_{MIRIN} = 60V, ISRC/SHDN = 30kΩ to GND	I_{MIROUT} = 0µA		1	2	mA
			I_{MIROUT} = 1mA		3.2	4	
MIRIN Voltage	V_{MIRIN}			15		76	V
HV FET On-Resistance	R_{DSONHV}	V_{GS} = 3.0V, I_D = 170mA			0.85	2	Ω
HVG Voltage	V_{GSHV}			0		V_{CC} + 0.3	V
HVD Voltage	V_{DHV}					76	V
HVD Leakage	I_{LHV}			-1		+1	µA
Logic-Input Thresholds (DIFFEN, DISCHARGE, GAIN, HVG, SEN, SENXOR)	V_{IL}					0.3 x V_{CC}	V
	V_{IH}			0.7 x V_{CC}			
ISRC/SHDN Threshold	V_{IL_SHDN}					1.4	V
	V_{IH_SHDN}			V_{CC} - 0.2			
ISRC/SHDN Resistor	R_{ISRC}	(Note 3		29.7	30	30.3	kΩ
Maximum MIROUT Current	I_{CLAMP}	ISRC/SHDN = low	R_{LIM} = 40.2kΩ	1.4	2	2.8	mA
			R_{LIM} = 24.9kΩ	2.5	3.2	4.1	
		ISRC/SHDN = high				0.01	
MIROUT Capacitive Load	C_{MIROUT}	Total capacitance on MIROUT to achieve accuracy specification		330		500	pF
Logic Output Levels ($\overline{ILIMS}$)	V_{OL_ILIMS}	$I_{\overline{ILIMS}}$ = -2mA				0.45	V
	V_{OH_ILIMS}	$I_{\overline{ILIMS}}$ = +2mA		V_{CC} -0.45			

Electrical Characteristics (continued)

(V_{MIRIN} = 15V to 76V, V_{CC} = 2.85V to 3.63V, T_A = -40°C to +95°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Output Levels (GAIN Has 3.5kΩ Internal Nominal Impedance)	V_{OL}	I_{GAIN} = -30µA			0.4	V
	V_{OH}	I_{GAIN} = +30µA	V_{CC} - 0.4			
$\overline{ILIMS}$ Output Time	$t_{\overline{ILIMS}}$	(Note 4)		1		µs
IOUT to MIROUT Ratio	K_{IOUT}	I_{MIROUT} = 1mA	0.090	0.100	0.110	A/A
VIP1 to MIROUT Ratio	K_{VIP1}	I_{MIROUT} = 1mA	0.720	0.800	0.880	A/A
VIP2 to MIROUT Ratio	K_{VIP2}	I_{MIROUT} = 1mA	0.180	0.200	0.220	A/A
K_{VIP1}, K_{VIP2}, and K_{IOUT} Voltage Variation	K_{VAR}	V_{MIRIN} = 40V ± 10%		±0.3	±2.5	%
Mirror Voltage Drop Monitor Load Capacitance	$V_{APDV:CAP}$	External capacitance required on APDV	50		250	pF
Mirror Voltage Drop	V_{MIRIN} - V_{MIROUT}	Current limit not exceeded, V_{SHDN} = Hi-Z, I_{MIRIN} = 1mA		4		V
Shutdown Temperature	T_{SHDN}			150		°C
Shutdown Temperature Hysteresis	T_{HYS}			20		°C
VIP1 Offset Current	$I_{VIP1OFF}$	R_{ISRC} = 30kΩ		20	40	µA
VIP2 Offset Current	$I_{VIP2OFF}$	R_{ISRC} = 30kΩ		19	30	µA
IOUT Offset Current	I_{OUTOFF}	R_{ISRC} = 30kΩ		18	25	µA

Sample and Hold Parameters

(V_{MIRIN} = 15V to 76V, V_{CC} = 2.85V to 3.63V, T_A = -40°C to +95°C, R_{ISRC} = 30kΩ, DISCHARGE = high, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Error (Total Error from All Sources)	V_{ERR}	I_{MIROUT} from 600µA to 60uA (Note 5)		±5.5		%
		I_{MIROUT} from 20µA to 500µA (Note 5)	-9.0		+9.0	
Output Voltage	V_{OUT}	$V_{OUT} = V_{VOP} - V_{VON}$, 100kΩ output load	0		2.5	V
Output Voltage Common Mode	V_{OUTCM}	V_{DIFFEN} = High		1.4		V
Output Impedance	R_{OUT}				1	kΩ
VOP Output Capacitive Load	C_{LD}	Capacitance for stable operation			50	pF
Gain Selection Threshold	V_{GTHR}		320	400	460	mV
GAIN Impedance	R_G	(Note 6)	2.1	3.5	4.9	kΩ
Sample Time	t_S	1kΩ resistors connected to VIP1 and VIP2 (Note 7)	300			ns
Delay Time	t_{DEL}	(Note 7)	10			ns
Output Valid Time	t_{O_VAL}	Less than 1% change from the time the output is valid, C_{LD} = 50pF (Notes 7 and 8)	9		109	µs

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage rating are guaranteed by design and characterization.

Note 2: ISRC/SHDN is not connected; HV FET is driven by a 100Ω source at 250kHz with a 2.97V square wave; HVD is connected to GND.

Note 3: External resistor connected to GND. This value guarantees accuracy of DS3923. $I_{ISRC} = (6/R_{ISRC})$ ±6%.

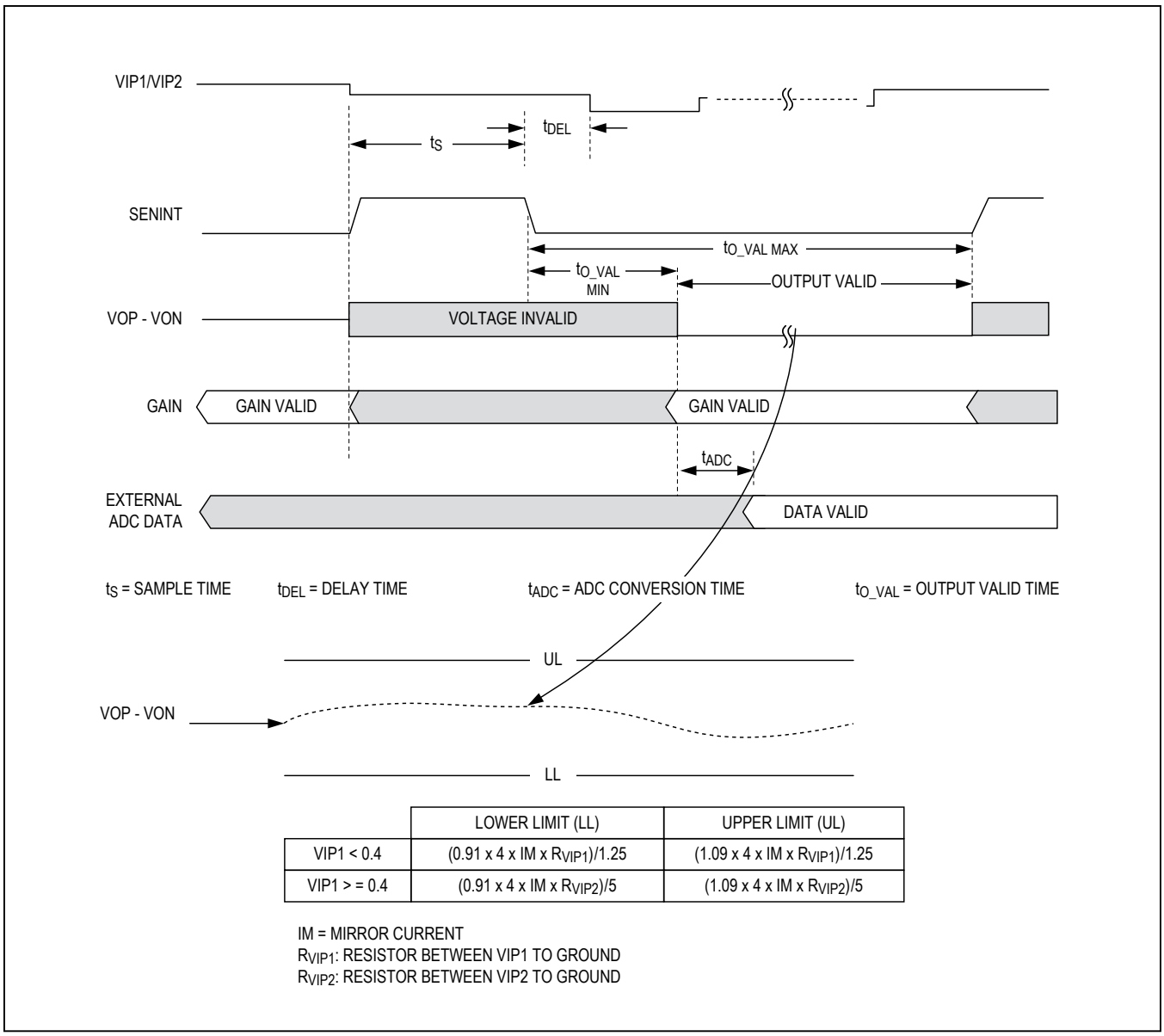
Note 4: Resistor connected to RLIM for 1mA clamp limit. I_{MIROUT} step from 10µA to 10mA. Time measured from I_{MIROUT} step to I_{MIROUT} < 1.1mA (see the *Typical Application Circuit*). C3 = 47pF, C1 = C2 = 0.1µF, V_{VC1} = 30V; R1 = 100Ω.

Note 5: Output Error = VOP – 4 x (VIP1 or VIP2) and sampled at t_{OUT}. Measured at +25°C with offset removed.

Note 6: To change internal gain selection, external driver must be capable of meeting the GAIN input logic level with the GAIN impedance connected to either V_{CC} or GND.

Note 7: See Figure 1 for more detail on timing.

Note 8: Time referenced to SENINT falling edge when output is valid at VOP - VON if DIFFEN = High or VOP if DIFFEN = Low.

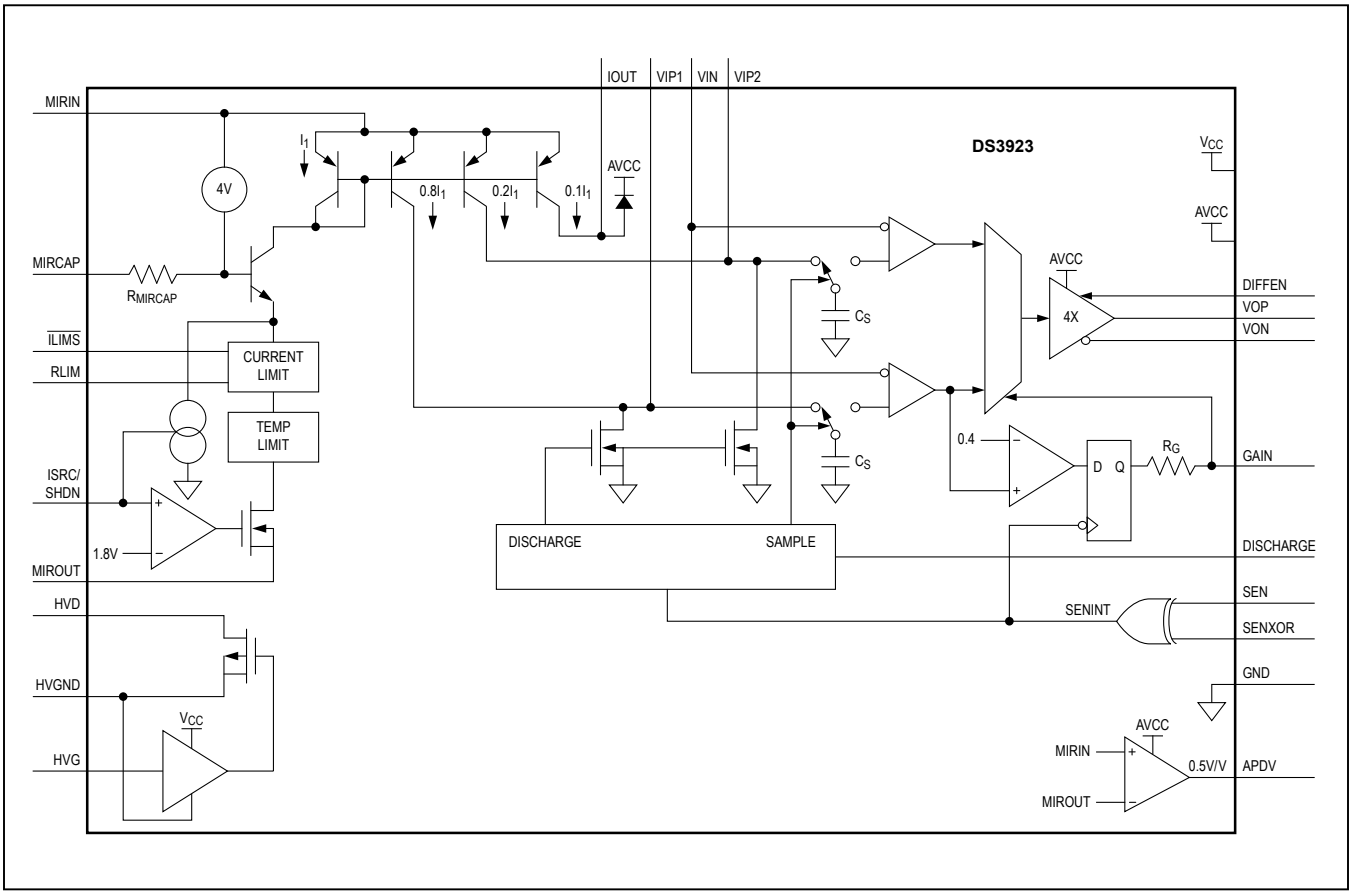


	LOWER LIMIT (LL)	UPPER LIMIT (UL)
VIP1 < 0.4	(0.91 x 4 x IM x R_{VIP1})/1.25	(1.09 x 4 x IM x R_{VIP1})/1.25
VIP1 > = 0.4	(0.91 x 4 x IM x R_{VIP2})/5	(1.09 x 4 x IM x R_{VIP2})/5

IM = MIRROR CURRENT
R_{VIP1}: RESISTOR BETWEEN VIP1 TO GROUND
R_{VIP2}: RESISTOR BETWEEN VIP2 TO GROUND

Figure 1. DS3923 Sample/Hold Timing Diagram

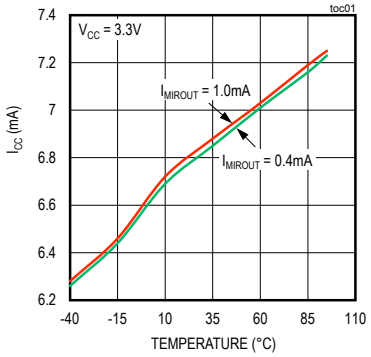
Block Diagram



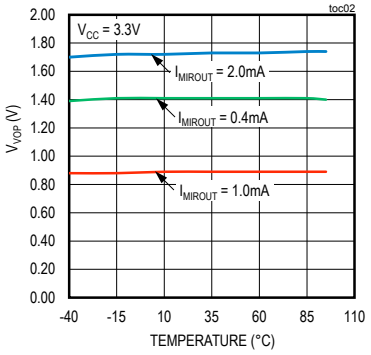
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

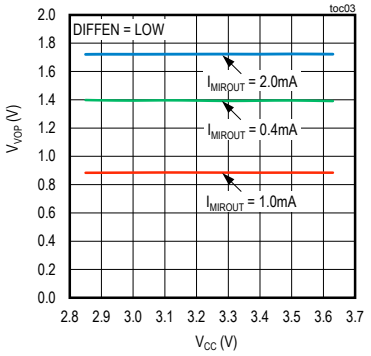
I_{CC} vs. TEMPERATURE



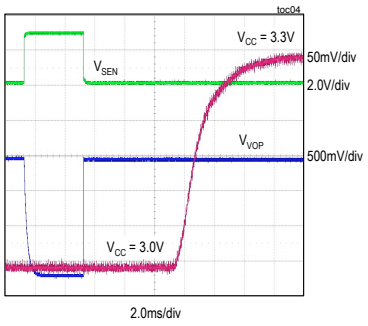
V_{VOP} vs. TEMPERATURE



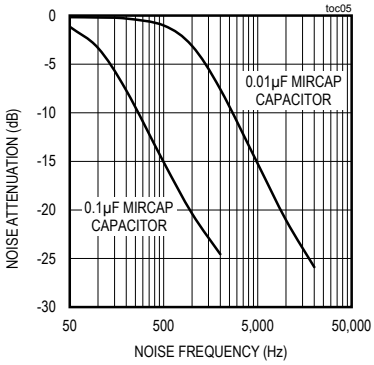
V_{VOP} vs. V_{CC}



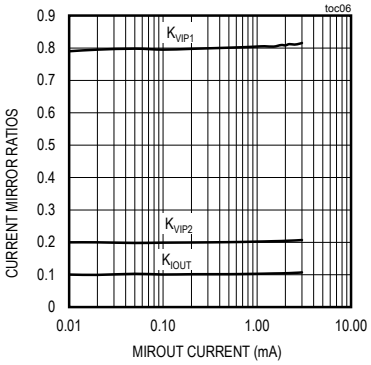
SINGLE-ENDED OUTPUT, TRANSIENT WITH 10% V_{CC} STEP



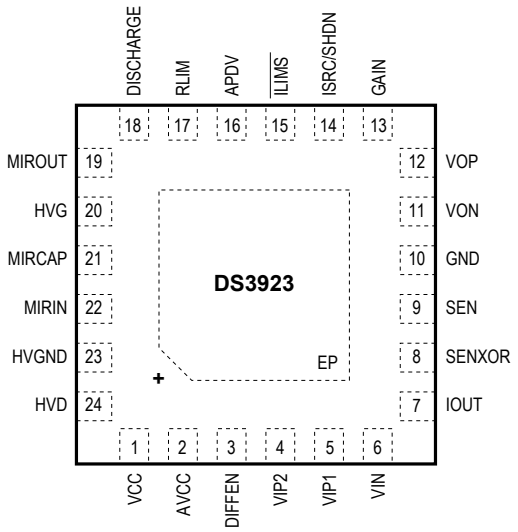
CURRENT MIRROR FILTER FREQUENCY RESPONSE



CURRENT MIRROR RATIO vs. MIROUT CURRENT



Pin Configuration



24-LEAD TQFN
(3.5mm x 3.5mm x 0.8mm)

Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Digital 3.3V (Nominal) Supply
2	AVCC	Analog 3.3V (Nominal) Supply
3	DIFFEN	Sample/Hold Single-Mode/Differential Mode Selection. When logic input is: Low: Single-mode sample/hold output High: Differential mode sample/hold output.
4	VIP2	20% Current Mirror Output. Connect to resistor to ground.
5	VIP1	80% Current Mirror Output. Connect to resistor to ground.
6	VIN	Negative Voltage Input. Connect to the same ground point as resistors connected to VIP1 and VIP2.
7	IOUT	10% Current Mirror Output. If unused, do not connect.
8	SENXOR	Sample Enable XOR. The start and stop of the sampling depend on the logic input of SENXOR and SEN. When SENXOR is low, the rising edge of the SEN pulse activates sampling, and the falling edge of the SEN pulse deactivates sampling. When SENXOR is high, the falling edge of the SEN pulse activates sampling, and the rising edge of the SEN pulse deactivates sampling. **Note:** If SENXOR is high, the discharge function should not be used. See Figure 3 for more detail.
9	SEN	Sample Enable Pulse. Logic input. See the description of SENXOR and Figure 3 for more detail.

Pin Description (continued)

PIN	NAME	FUNCTION
10	GND	Ground
11	VON	Negative Sample/Hold Voltage Output. Do not connect for single-ended mode.
12	VOP	Sample/Hold Voltage Output. Positive output in differential mode. Also used for single-ended output.
13	GAIN	Hold Amplifier Gain Indicator. Both as output and logic input. Indicates which current mirror's output is active. 3.5kΩ input/output impedance. Pin as input (mirror selection for sample/hold): Low: Sample/hold Conversion from Current Mirror 1 (VIP1); High: Sample/hold Conversion from Current Mirror 2 (VIP2). Pin as output (mirror indication for sample/hold): Low: Sample/hold Conversion from Current Mirror 1 (VIP1); High: Sample/hold Conversion from Current Mirror 2 (VIP2).
14	ISRC/ SHDN	Dual-Purpose Pin. ISRC: A resistor connected to this pin controls the amount of current flowing through a current source connected to MIROUT. (**Note:** During this mode of operation, the microcontroller pin (if connected) should be in the high impedance.) SHDN: If pulled high, sets MIROUT to high-impedance.
15	$\overline{\text{ILIMS}}$	Current-Limit Status. Active-low signal indicating that the current-limit threshold is exceeded.
16	APDV	APD Voltage Monitor. Provides output voltage used to calculate the voltage on the APD.
17	RLIM	Resistor Limit. Connect a resistor between RLIM and GND to set the current clamp limit.
18	DIS- CHARGE	Discharge Enable. When sampling is deactivated and the DISCHARGE pin logic input is low, the discharge function is disabled. When sampling is deactivated and the DISCHARGE pin logic input is high, the discharge function is enabled, and the DS3923 pulls current mirror outputs VIP1 and VIP2 low to ensure accurate sampling. During the sample time, the pin discaharge is internally disabled by the DS3923. See Figure 4 and Figure 5 for more detail. **Note:** The discharge function should not be used if SENXOR is a logic-high.
19	MIROUT	Current Mirror Output. Connect to APD.
20	HVG	High-Voltage NMOS FET Gate. Connect to ground if unused.
21	MIRCAP	Mirror Filter. Connect external capacitor to filter voltage at MIROUT.
22	MIRIN	Current Mirror Input. Connect to high voltage supply.
23	HVGND	High-Voltage NMOS FET Source
24	HVD	High-Voltage NMOS FET Drain. Connect to HVGND if unused.
—	EP	Exposed Pad. Connect to ground with a minimum of 9 vias for thermal conductivity improvement. It is acceptable to use solder mask between the IC and the ground pad. It is not necessary to electrically connect the exposed pad ground.

Detailed Description

The DS3923 contains circuits to monitor the APD bias current. The device includes three current mirrors, which allow for a wide dynamic monitoring range. The mirror response time is fast enough to comply with GPON Rx burst-mode monitoring requirements. The device has a built-in current-limiting feature to protect APDs. This current limit is adjustable using an external resistor. The APD current can also be shut down by ISRC/SHDN or thermal shutdown. The internal HV FET may be used as a fast APD shutdown. A dual range sample/hold circuit with a range selection multiplexeor is included to hold the analog voltage while an external ADC performs the conversion.

Current Mirrors

The DS3923 includes three current mirrors as shown in Figure 2. One is a 10:1 (10%) mirror connected at IOUT. The other two are a 1.25:1 (80%) and the 5:1 (20%) mirror connected to VIP1 and VIP2 as well as the internal sample/hold circuit. On pin VIP1 and VIP2, resistors to ground should be selected such that the maximum voltage is 0.625V (2.5V after the 4x gain of the built-in amplifier). For example, if the maximum monitored current through the APD is 1mA, the mirror is 1.25:1 ratio, and then the correct resistor is approximately 780Ω.

Current Mirror Filter

The DS3923 includes a filter to stabilize the MIROUT voltage. An external capacitor must be connected to pin MIRCAP. See specification t_{MIRCAP} in the *Electrical Characteristics* table for filter and capacitor settings.

Current Source for Mirror Bias

The current mirror response time is improved by providing a continuous current source. This source is adjustable by changing the resistor connected to the ISRC/SHDN pin. However, only one value is allowed to guarantee performance (see *Electrical Characteristics* table).

$$I_{ISRC} = (6 / R_{ISRC}) \pm 6\%$$

Typical R_{ISRC} value should be 30kΩ.

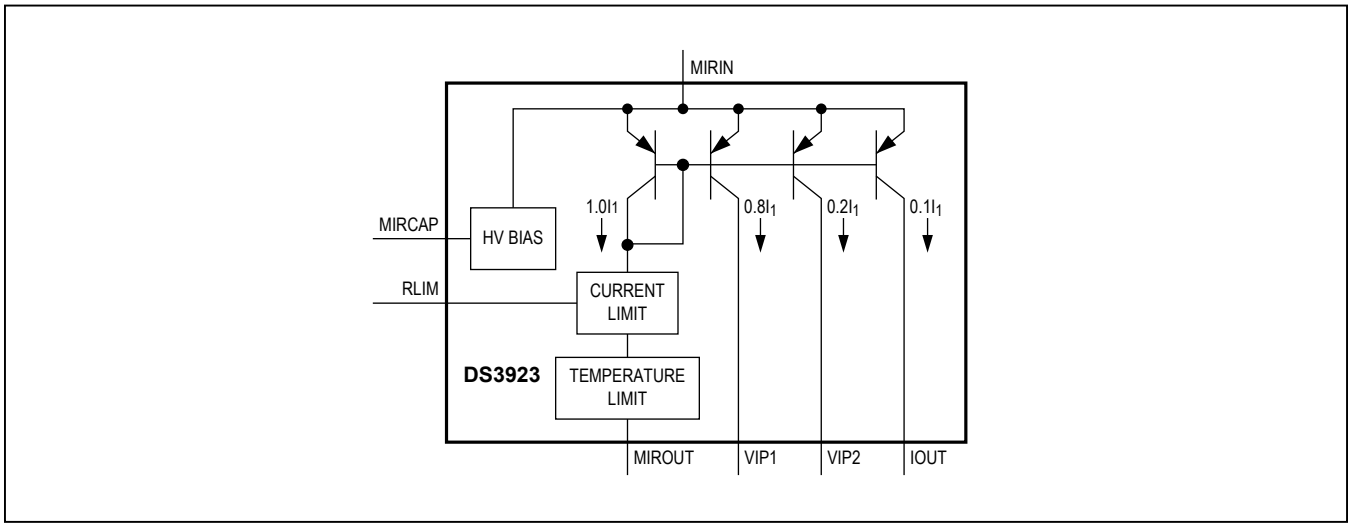


Figure 2. DS3923 Current Mirrors

Current Mirror Voltage Drop Monitor

The DS3923 includes a voltage monitor that indicates the voltage drop across the current mirror. This signal is output on APDV. This signal should be used to accurately maintain the correct APD bias voltage in conjunction with the feedback resistors for the APD bias boost converter.

$$APDV = (V_{MIRIN} - V_{MIROUT})/2$$

Current Clamp

The DS3923 has a current clamping circuit to protect the APD by limiting the amount of current from MIROUT. The current limit is defined by a resistor (R_{LIM}) connected between the RLIM pin and ground. A larger R_{LIM} results in a lower current clamp limit (see *Electrical Characteristics* table).

Shutdown

The MIROUT output can be set to a high-impedance state using the ISRC/SHDN pin, effectively disabling the APD. The ISRC/SHDN pin is active-high.

Sample/Hold

As shown in the block diagram, the DS3923 Sample/Hold consists of sampling capacitors (C_S), control logic and a differential output amplifier. The control logic selects the current mirror for the sample/hold. Additionally, it controls the sample time by taking a logic input from SENXOR pin as shown in Figure 4. The sample/hold has a discharge circuit to discharge parasitic capacitance on the mirror outputs VIP1, VIP2, V_{IN} and the sample capacitor before it starts sampling.

During the sample time (t_S) the sample/hold capacitor is connected to sample/hold input for sampling of the input signal either from VIP1 or VIP2 which is selected by the sample/hold control circuit. As shown below in Figure 3, the sampling start and stop depends upon the logic input of SENXOR and SEN. Sampling stops at the SEN falling edge (when SENXOR is low) or rising edge (when SENXOR is high), and the voltage stored at the sampling capacitors is then amplified by the hold amplifier.

The voltage at current mirrors VIP1, VIP2, and IOUT pins can be shown as:

$$VIP1 = 0.8 \times I1 \times R4$$

$$VIP2 = 0.2 \times I1 \times R5$$

$$I_{OUT} = 0.1 \times I1 \times R6$$

I1, R4, R5, and R6 are shown in the *Typical Application Circuit*.

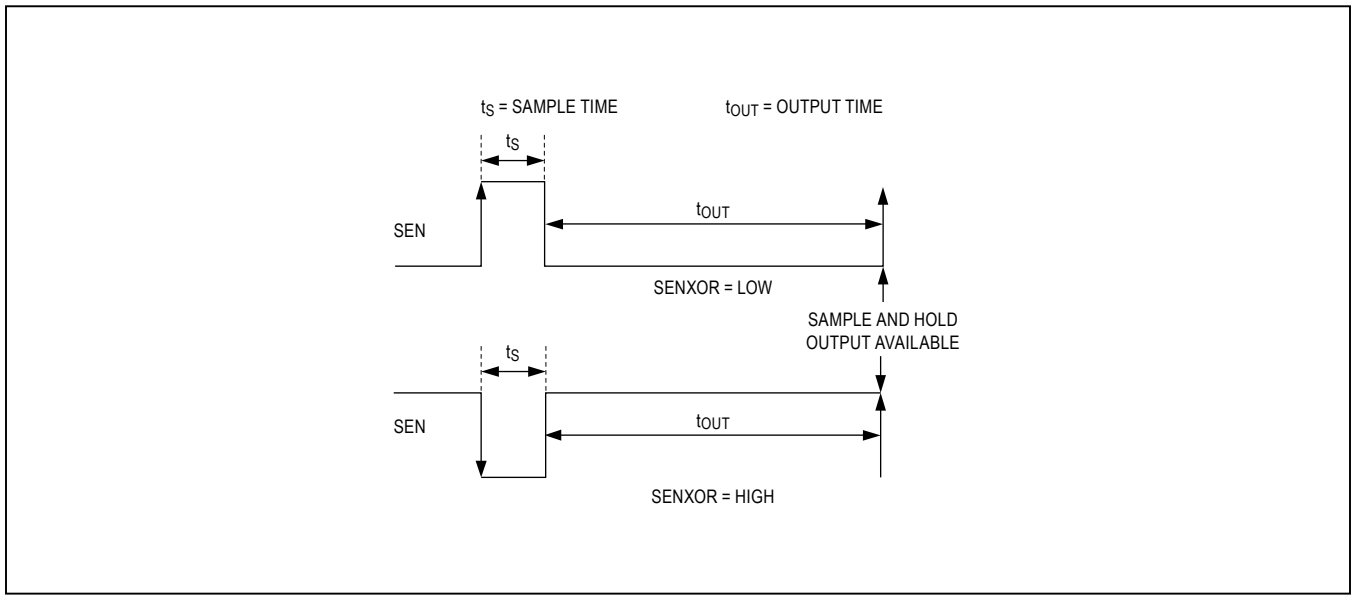


Figure 3. SEN Pulse and Sample/Hold Output Timing Diagram

Table 1. Sample/Hold Output Voltage vs. Input

INPUT SELECTED (AUTO OR FORCED)	SAMPLE/HOLD OUTPUT VOLTAGE
VIP1	$4 \times VIP1 = 4 \times 0.8 \times I1 \times R4$ $= 3.2 \times I1 \times R4$
VIP2	$4 \times VIP2 = 4 \times 0.2 \times I1 \times R5$ $= 0.8 \times I1 \times R5$

In addition to VIP1 or VIP2 auto selection, the DS3923 allows VIP1 or VIP2 forced selection using the GAIN pin. The sample/hold amplifier output is shown in Table 1.

Sampling Capacitors

Each sample/hold input voltage is sampled using an internal capacitor. As shown in the *Block Diagram*, when SENXOR is low, the capacitors are connected to the input during the high time of the SEN pulse. When SENXOR is high, the capacitors are connected to the input during the low time of the SEN pulse. These capacitors must be fully charged before SEN becomes inactive in order to ensure accurate sampling. An RC time constant is created by the resistance of the voltage source connected to the sample/hold's input and the DS3923's sampling capacitors. An external capacitor may be used on the sample/hold's inputs. This external capacitance will be in parallel with the pin's ESD capacitance (~7pF). These capacitors can be discharged when the DS3923 is not sampling the input by setting the DISCHARGE pin to high.

Discharge

When the DISCHARGE pin is set to logic-high, the DS3923 pulls down current mirror outputs VIP1 and VIP2 to low. The discharge strength is about 50Ω. During the sample time t_S, the pin discharge is internally disabled by the DS3923 as shown in Figure 4 and Figure 5. When the DISCHARGE pin is set to logic-low, the pin discharge function is disabled.

Note: The discharge function should not be used if SENXOR is a logic high.

Gain Selection

The sample/hold circuit has a native gain of 4 applied to the input presented. Depending on the level of VIP1, a selection is made to present either VIP1 or VIP2 to the sample/hold circuit when SEN pulse is applied. The sample circuit applied to this buffer is chosen by a reference voltage (400mV) and a comparator to avoid outputing a clipped value. Table 2 lists the conditions that make the choice. The choice made is indicated on the GAIN pin.

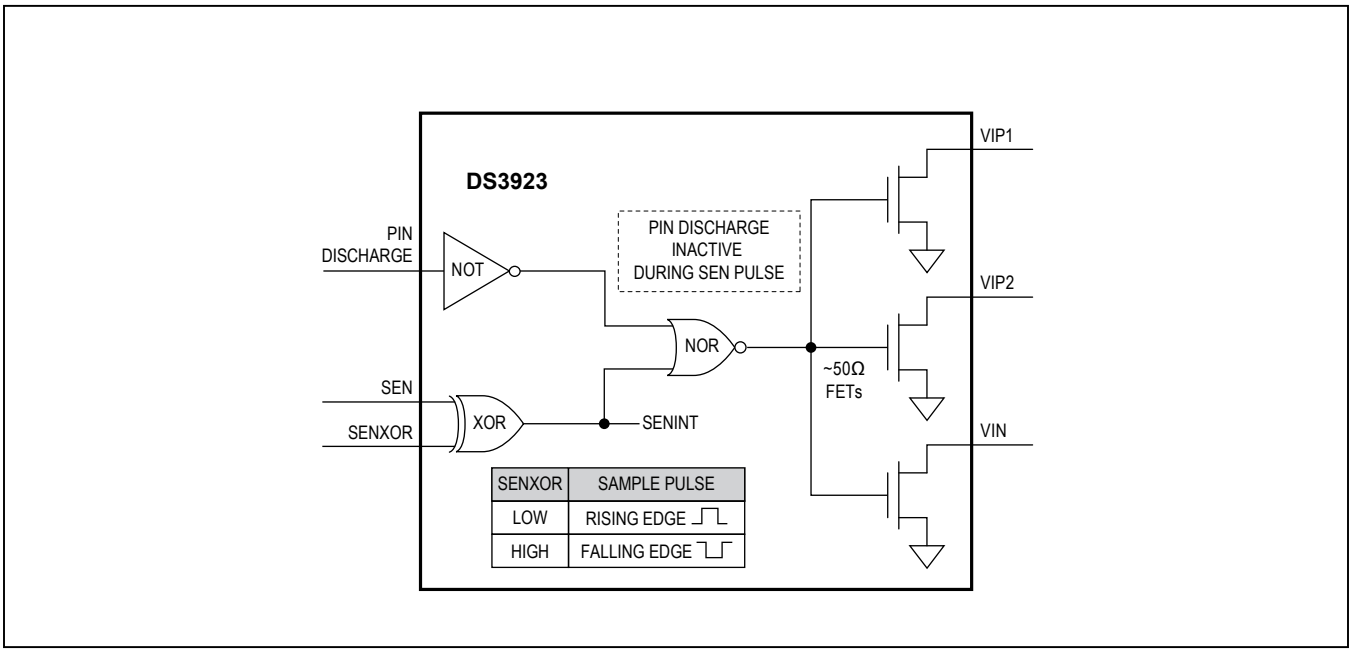


Figure 4. Discharge Logic Diagram

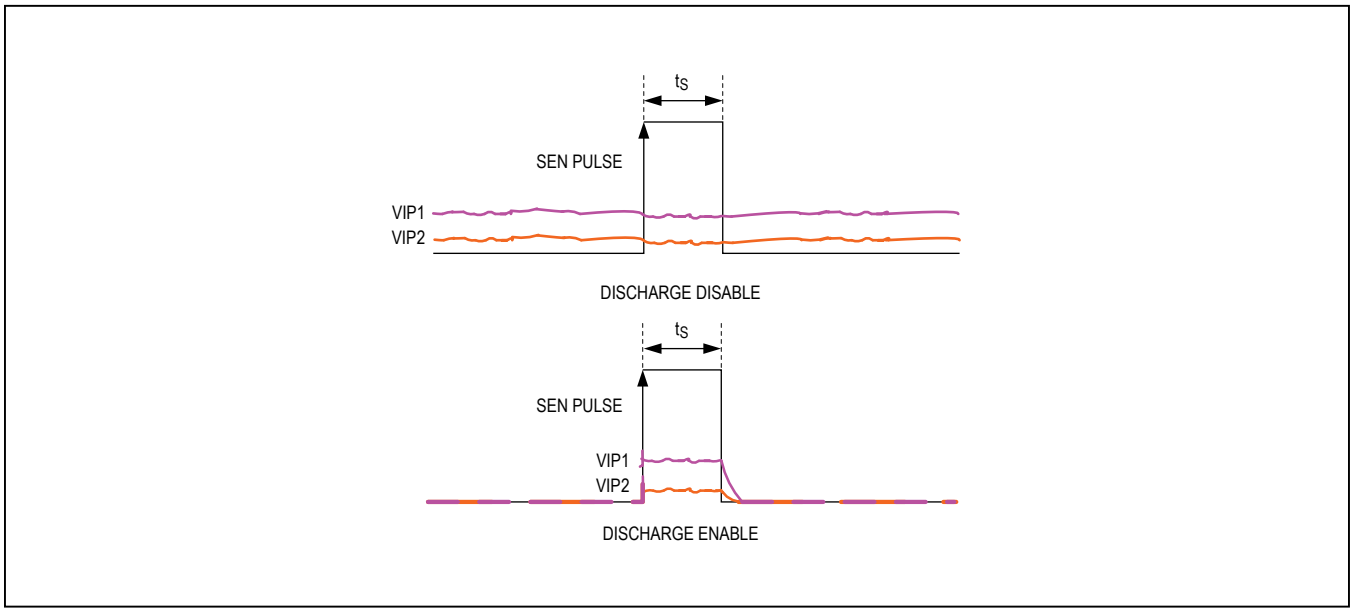


Figure 5. Discharge, Current Mirror, and SEN Pulse Timing Diagram

Table 2. Sample/Hold Input Selection

VIP1	INPUT SELECTED	OUTPUT VOLTAGE	GAIN OUTPUT
< 0.4V	VIP1	4 × VIP1	0
≥ 0.4V	VIP2	4 × VIP2	V_{CC}

Alternatively, forcing GAIN = 0 always chooses VIP1 and forcing GAIN = V_{CC} chooses VIP2. By default, GAIN pin is pulled high.

The logical circuit is shown in Figure 6.

Output Buffer

After sampling is complete, the sampling capacitor is switched to the output buffer. This buffer requires a small amount of time to settle, t_{OUT} (see the *Electrical Characteristics* table) as shown in Figure 3. When an ADC is used to measure the DS3923's output, a step will occur at the ADC's input caused by its sampling capacitor. The DS3923's t_{REC} is dependent on the size of this sampling capacitor and the voltage applied across it. To maximize accuracy, the ADC's sampling speed (ADC clock frequency) should be slowed down until the ADC's acquisition window is larger than the DS3923's recovery time.

Sampling Time and Output Error

As sampling time (t_S) decreases, V_{ERR} increases. V_{ERR} is largely dependent on the settling time of the sampling capacitor, and to a lesser degree to the buffer's gain error and offset voltage. Settling time can be reduced by reducing the resistor connected between the sample/hold amplifier's input and ground. However, a smaller resistor will decrease the amplitude of the sampled signal, and cause the relative offset errors to become more significant.

High-Voltage (HV) Switch FET

A high-voltage (HV) switching FET is included to optionally be used to quickly turn off the bias voltage to the APD. The strong HV FET can quickly discharge the capacitance on the MIRIN pin.

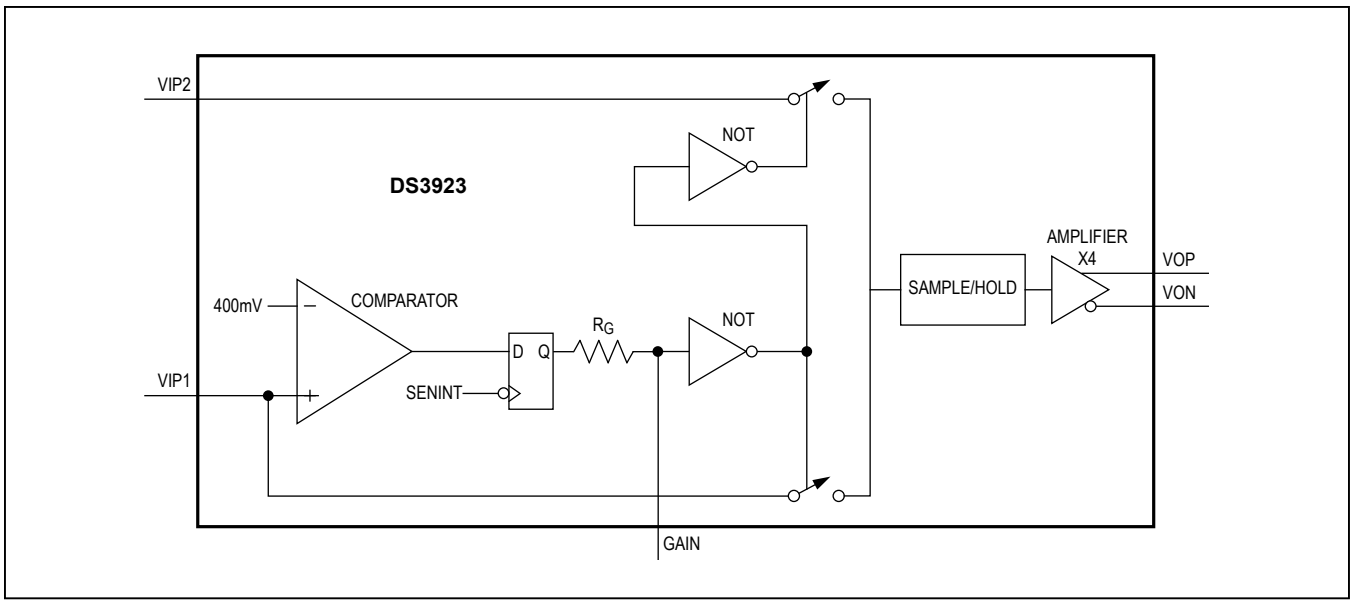


Figure 6. GAIN Selection Logic Diagram

Applications Information

Layout Considerations

Keeping all PCB traces as short as possible reduces radiated noise, stray capacitance, and trace resistance.

Ordering Information

PART	TEMP TANGE	PIN-PACKAGE
DS3923T+	-40°C to +95°C	24-TQFN-EP**
DS3923T+T*	-40°C to +95°C	24-TQFN-EP**

+Denotes a lead(Pb)-free/RoHS-compliant package.

**First T denotes package type. Second T denotes Tape and reel.*

***EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T243A3+1	21-0188	90-0122

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/13	Initial release	—
1	8/14	Notes added to *Pin Description* and *Discharge* section stating SENXOR should not be a logic-high if the discharge feature is being used.	8, 9, 12
2	3/15	Revised recommended usage of HV FET. Revised *General Description*, *Features*, *Applications*, *Pin Description*, *Detailed Description*, and *Typical Application Circuit*. Updated the *Benefits and Features* section.	1, 9, 10, 13, 14

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