# PI7C9X2G304EL

PCI EXPRESS GEN 2 PACKET SWITCH

**3-Port, 4-Lane, ExtremeLo PCIe2.0 Packet Switch**

*DATASHEET*

REVISION 2-2

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A Product Line of Diodes Incorporated

**1545 Barber Lane Milpitas, CA 95035**
**Telephone: 408-232-9100**
**FAX: 408-434-1040**
**Internet: http://www.diodes.com**

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# REVISION HISTORY

| Date | Revision Number | Description |
|---|---|---|
| 03/13/14 | 0.1 | Preliminary Datasheet |
| 07/18/14 | 1.0 | Updated Section 3 Pin Description<br>Updated Section 4 Pin Assignments |
| 11/17/14 | 1.1 | Updated Section 7.2 Transparent Mode Configuration Registers<br>Updated Section 8 Clock Scheme |
| 07/16/15 | 1.2 | Updated Section 3.1 PCI Express Interface Signals<br>Updated Section 3.2 Port Configuration Signals<br>Updated Section 5.1 Physical Layer Circuit<br>Updated Section 6.1 EEPROM Interface<br>Updated Section 7.2 Transparent Mode Configuration Registers<br>Updated Section 8 Clock Scheme<br>Updated Table 9-1 Instruction Register Codes<br>Updated Table 9-2 JTAG Device ID Register<br>Updated Table 9-3 JTAG Boundary Scan Register Definition<br>Updated Table 11-2 DC Electrical Characteristics |
| 09/11/15 | 1.3 | Updated Table 11-1 Absolute Maximum Ratings |
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# 1 FEATURES

- 4-lane PCI Express Gen 2 Switch with 3 PCI Express ports
- Supports "Cut-through"(Default) as well as "Store and Forward" mode for packet switching
- Peer-to-peer switching between any two downstream ports
- 150 ns typical latency for packet routed through Switch without blocking
- Integrated reference clock for downstream ports
- Strapped pins configurable with optional EEPROM or SMBus
- SMBus interface support
- Compliant with System Management (SM) Bus, Version 1.0
- Compliant with *PCI Express Base Specification Revision 2.1*
- Compliant with *PCI Express CEM Specification Revision 2.0*
- Compliant with *PCI-to-PCI Bridge Architecture Specification Revision 1.2*
- Compliant with *Advanced Configuration Power Interface (ACPI) Specification*
- Reliability, Availability and Serviceability
  - Supports Data Poisoning and End-to-End CRC
  - Advanced Error Reporting and Logging
  - IEEE 1149.1 JTAG interface support
- Advanced Power Saving
  - Empty downstream ports are set to idle state to minimize power consumption
- Link Power Management
  - Supports L0, L0s, L1, L2, L2/$L3_{Ready}$ and L3 link power states
  - Active state power management for L0s and L1 states
- Device State Power Management
  - Supports D0, $D3_{Hot}$ and $D3_{Cold}$ device power states
  - 3.3V Aux Power support in $D3_{Cold}$ power state
- Port Arbitration: Round Robin (RR), Weighted RR and Time-based Weighted RR
- Extended Virtual Channel capability
  - Two Virtual Channels (VC) and Eight Traffic Class (TC) support
  - Disabled VCs' buffer is assigned to enabled VCs for resource sharing
  - Independent TC/VC mapping for each port
  - Provides VC arbitration selections: Strict Priority, Round Robin (RR) and Programmable Weighted RR
- Supports Isochronous Traffic
  - Isochronous traffic class mapped to VC1 only
  - Strict time based credit policing
- Supports up to 512-byte maximum payload size
- Programmable driver current and de-emphasis level at each individual port
- Support Access Control Service (ACS) for peer-to-peer traffic
- Support Address Translation (AT) packet for SR-IOV application
- Support OBFF and LTR
- Low Power Dissipation: 650 mW typical in L0 normal mode
- Industrial Temperature Range -40° to 85°C
- 136-pin aQFN 10mm x 10mm package


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# 2 GENERAL DESCRIPTION

Similar to the role of PCI/PCIX Bridge in PCI/PCIX bus architecture, the function of PCI Express (PCIE) Switch is to expand the connectivity to allow more end devices to be reached by host controllers in PCIE serial interconnect architecture. The 4-lane PCIe Switch is in 3-port type configuration. It provides users the flexibility to expand or fan-out the PCI Express lanes based on their application needs.

In the PCI Express Architecture, the PCIE Switch forwards posted and non-posted requests, and completion packets in either downstream or upstream direction concurrently as if a virtual PCI Bridge is in operation on each port. By visualizing the port as a virtual Bridge, the Switch can be logically viewed as two-level cascaded multiple virtual PCI-to-PCI Bridges, where one upstream-port Bridge sits on all downstream-port Bridges. Similar to a PCI Bridge during enumeration, each port is given a unique bus number, device number, and function number by the initiating software. The bus number, device number, and function number are combined to form a destination ID for each specific port. In addition to that, the memory-map and IO address ranges are exclusively allocated to each port as well. After the software enumeration is finished, the packets are routed to the dedicated port based on the embedded address or destination ID. To ensure the packet integrity during forwarding, the Switch is not allowed to split the packets to multiple small packets or merge the received packets into a large transmit packet. Also, the IDs of the requesters and completers are kept unchanged along the path between ingress and egress port.

The Switch employs the architecture of Combined Input and Output Queue (CIOQ) in implementation. The main reason for choosing CIOQ is that the required memory bandwidth of input queue equals to the bandwidth of ingress port rather than increasing proportionally with port numbers as an output queue Switch does. The CIOQ at each ingress port contains separate dedicated queues to store packets. The packets are arbitrated to the egress port based on the PCIe transaction-ordering rule. For the packets without ordering information, they are permitted to pass over each other in case that the addressed egress port is available to accept them. As to the packets required to follow the ordering rule, the Head-Of-Line (HOL) issue becomes unavoidable for packets destined to different egress ports since the operation of producer-consumer model has to be retained; otherwise the system might occur hang-up problem. On the other hand, the Switch places replay buffer at each egress port to defer the packets before sending it out. This can assure the maximum throughput being achieved and therefore the Switch works efficiently. Another advantage of implementing CIOQ in PCIe Switch is that the credit announcement to the counterpart is simplified and streamlined because of the credit-based flow control protocol. The protocol requires that each ingress port maintains the credits independently without checking other ports' credit availability, which is otherwise required by pure output queue architecture.

The Switch supports two virtual channels (VC0, VC1) and eight traffic classes (TC0 ~ TC7) at each port. The ingress port independently assigns packets into the preferred virtual channel while the egress port outputs the packet based on the predefined port and VC arbitration algorithm. For instance, the isochronous packet is given a special traffic class number other than TC0 and mapped into VC1 accordingly. By employing the strict time based credit policy for port arbitration and assigning higher priority to VC1 than VC0, the Switch can therefore guarantee the time-sensitive packet is not blocked by regular traffic to assure the quality of service. In addition, some data-centric applications only carry TC0/VC0 traffic. As a result, there are no packets that would consume VC1 bandwidth. In order to improve the efficiency of buffer usage, the unused VC1 queues can be reassigned to VC0 and enable each of the ingress ports to handle more data traffic bursts. This virtual channel resource relocation feature enhances the performance of the PCIe Switch further.

The Switch provides the advanced feature of Access Control Service (ACS). This feature regulates which components are allowed to communicate with each other within the PCIe multiple-point fabric, and allows the system to have more control over packet routing in the Switch. As a result, peer-to-peer traffic can be facilitated more accurately and efficiently. When the system also implements Address Translation Service (ATS), the peer-to-peer requests with translated address can be routed directly by enabling the corresponding option in ACS to avoid possible performance bottleneck associated with re-direction, which introduces extra latency and may increase link and RC congestion.


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The built-in Integrated Reference Clock Buffer of the PCI Express Switch supports three reference clock outputs. The clock buffer is from a single 100MHz clock input, and distributes the clock source to three outputs, which can be used by the downstream PCI Express end devices. The clock buffer feature can be enabled and disabled by strapping pin setting.


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# 3 PIN DESCRIPTION

## 3.1 PCI EXPRESS INTERFACE SIGNALS

| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| REFCLKP<br>REFCLKN | A21<br>A19 | I | **Reference Clock Input Pair:** Connect to 100MHz differential clock when integrated reference clock buffer is disabled (CLKBUF_PD=1), or connect to one of the Integrated Reference Clock Output Pairs (REFCLKO_P and REFCLKO_N) of this Switch when integrated reference clock buffer is enabled (CLKBUF_PD=0).<br><br>The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered. It is recommended that a 0.1uF be used in the AC-coupling. |
| PERP [3:0] | B10, B26, B32, B4 | I | **PCI Express Data Serial Input Pairs:** Differential data receive signals in four ports.<br><br>Port 0 (Upstream Port) Lane 0 is PERP[0] and PERN[0]<br>Port 0 (Upstream Port) Lane 1 is PERP[3] and PERN[3]<br>Port 1 (Downstream Port) is PERP[1] and PERN[1]<br>Port 2 (Downstream Port) is PERP[2] and PERN[2] |
| PERN [3:0] | A9, A27, B30, B6, | I | |
| PETP [3:0] | A11, A25, A31, A5 | O | **PCI Express Data Serial Output Pairs:** Differential data transmit signals in four ports.<br><br>Port 0 (Upstream Port) Lane 0 is PERP[0] and PERN[0]<br>Port 0 (Upstream Port) Lane 1 is PERP[3] and PERN[3]<br>Port 1 (Downstream Port) is PERP[1] and PERN[1]<br>Port 2 (Downstream Port) is PERP[2] and PERN[2] |
| PETN [3:0] | A13, A23, A29, A7 | O | |
| PERST_L | N1 | I | **System Reset (Active LOW):** When PERST_L is asserted, the internal states of whole chip except sticky logics are initialized.<br><br>Please refer to Table 11-2 for PERST_L spec. |
| DWNRST_L[2:1] | K2, G1 | O | **Downstream Device Reset (Active LOW):** DWNRST_L provides a reset signal to the devices connected to the downstream ports of the switch. The signal is active when either PERST_L is asserted or the device is just plugged into the switch. DWNRST_L [x] corresponds to Portx, where x= 1,2,3. |
| REXT | B14 | I | **External Reference Resistor:** Connect an external resistor (1.43K Ohm +/- 1%) to REXT_GND to provide a reference to both the bias currents and impedance calibration circuitry. |
| REXT_GND | B16 | I | **External Reference Resistor Ground:** Connect to an external resistor to REXT. |
| REFCLKI_P,<br>REFCLKI_N | AG35<br>AF34 | I | **Integrated Reference Clock Input Pair:** Connect to external 100MHz differential clock for the integrated reference clock buffer. |
| REFCLKO_P[2:0] | AA35, U35, N35 | O | **Integrated Reference Clock Output Pairs:** 100MHz external differential HCSL clock outputs for the integrated reference clock buffer. |
| REFCLKO_N[2:0] | AC35, W35, R35 | O | |
| IREF | M34 | I | **Differential Reference Clock Output Current Resistor:** External resistor (475 Ohm +/- 1%) connection to set the differential reference clock output current. |
| CLKBUF_PD | AP28 | I | **Reference Clock Output Pairs Power Down:** When CLKBUF_PD is asserted high, the integrated reference clock buffer and Reference Clock Outputs are disabled. When it is asserted low, the integrated reference clock buffer and Reference Clock Outputs are enabled. This pin has internal pull-down. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used. |


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## 3.2 PORT CONFIGURATION SIGNALS

| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| VC1_EN | W1 | I | **Virtual Channel 1 Resource Sharing Enable:** The chip provides the capability to support virtual channel 1 (VC1), in addition to the standard virtual channel 0. When this pin is asserted high, Virtual Channel 1 is enabled, and virtual channel resource sharing is not available. When it is asserted low, the chip would allocate the additional VC1 resource to VC0, and VC1 capability is disabled. This pin has internal pull-down resistor. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used. |
| RXPOLINV_DIS | AD2 | I | **Rx Polarity Inversion Disable:** When RXPOLINV_DIS is asserted high, it indicates to disable Rx Polarity Inversion detection function. Otherwise, it indicates to enable Rx Polarity Inversion detection function. This pin has internal pull-down resistor. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used. |
| PL_512B | AP22 | I | **Max. Payload Size 512B:** When PL_512B is asserted high, it indicates the max. payload size capability is 512B. Otherwise, it indicates the max. Payload size is 256B. This pin has internal pull-down resistor. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used. |
| PRSNT[2:1] | AA1, Y2 | I | **Present:** When PRSNT is asserted low, it indicates that the device is present in the slot of downstream port. Otherwise, it indicates the absence of the device. PRSNT[x] is correspondent to Port x, where x=1,2. These pins have internal pull-down resistors. |
| SLOTCLK | AP6 | I | **Slot Clock Configuration:** It determines if the downstream component uses the same physical reference clock that the platform provides on the connector. When SLOTCLK is high, the platform reference clock is employed. By default, all downstream ports use the same physical reference clock provided by platform. This pin has internal pull-down resistor. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used. |
| SLOT_IMP[2:1] | AR15, AP14 | I | **Slot Implemented:** These signals are asserted to indicate that the downstream ports are connected to slots. SLOT_IMP[x] corresponds to Port x, where x= 1, 2. When SLOT_IMP[x] is asserted, the Port x is connected to slot. Otherwise, it is chip-to-chip connection directly. These pins have internal pull-down resistors. If no board trace is connected to these pins, the internal pull-down resistors of these pins are enough. However, if pins are connected to a board trace and not driven, it is recommended that external 330-ohm pull-down resistors be used. |
| PORTSTATUS[2:0] | AK34, AN35, AM34 | O | **Port Status:** These signals indicate the status of each port. Please connect to pin header for debug used.<br><br>PORTSTATUS[x] is correspondent to Port x, where x=0, 1, 2. |

## 3.3 MISCELLANEOUS SIGNALS

| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| EECLK | AL35 | O | **EEPROM Clock:** Clock signal to the EEPROM interface. |
| EEPD | AH34 | I/O | **EEPROM Data:** Bi-directional serial data interface to and from the EEPROM. The pin is set to '1' by default. |
| SMBCLK | AG1 | I | **SMBus Clock:** System management Bus Clock. This pin requires an external 5.1K-ohm pull-up resistor. |


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| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| SMBDATA | AF2 | I/O | **SMBus Data:** Bi-Directional System Management Bus Data. This pin requires an external 5.1K-ohm pull-up resistor. |
| SCAN_EN | AJ35 | I/O | **Full-Scan Enable Control:** For normal operation, SCAN_EN is an output with a value of "0". SCAN_EN becomes an input during manufacturing testing. |
| GPIO[7:0] | AR13, AP12, AR11, AR9, AP10, AR7, AR5, AP8 | I/O | **General Purpose Input and Output:** These eight general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register.<br>When SMBus is implemented, GPIO[7:5] act as the SMBus address pins, which set Bit 2 to 0 of the SMBus address.<br><br>**Debug Mode Selection:** In debug mode, GPIO[4:0] are used for Debug Mode Selection. |
| PWR_SAV | AH2 | I | **Power Saving Mode:** PWR_SAV is a strapping pin. When this pin is pulled high when system is reset, the Power Saving Mode is enabled. When this pin is pulled low when system is reset, the Power Saving Mode is disabled. When this pin is pulled low, it should be tied to ground through a 330-ohm pull-down resistor. When this pin is pulled high, a 5.1K-ohm pull-up resistor should be used. |
| TEST3<br>TEST5<br>TEST6 | V2<br>AE1<br>AP20 | I | **Test3/5/6:** These pins are for internal test purpose. Test3, Test5 and Test6 should be tied to ground through a 330-ohm pull-down resistor. |
| TEST4 | AC1 | I | **Test4:** The pin is for internal test purpose. It should be tied to ground through a 330-ohm pull-down resistor for normal operation.<br><br>**Port Status Output Enable: I**n debug mode, it is used to enable Port Status output. |
| TEST1 | L1 | I | **Test1:** The pin is for internal test purpose. It should be tied to 3.3V through a 5.1K-ohm pull-up resistor for normal operation.<br><br>**Debug Mode Enable**: In debug mode, it need be tired to low through a 330-ohm pull-down resistor. |
| TEST2 | U1 | I | **Test2:** The pin is for internal test purpose. Test2 should be tied to 3.3V through a 5.1K-ohm pull-up resistor. |
| NC | A1, A3, A15, A33, A35, B1, B2, B8, B12, B20, B24, B28, B34, B35, C1, C35, D2, D34, E1, E35, H2, J1, AB2, AD34, AE35, AJ1, AK2, AL1, AM2, AN1, AP1, AP2, AP4, AP16, AP24, AP26, AP32, AP34, AP35, AR1, AR3, AR17, AR21, AR23, AR25, AR27, AR29, AR33, AR35 | | **Not Connected:** These pins can be just left open. |


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## 3.4 JTAG BOUNDARY SCAN SIGNALS

| Name | Pin | Type | Description |
|---|---|---|---|
| TCK | J35 | I | **Test Clock:** Used to clock state information and data into and out of the chip during boundary scan. When JTAG boundary scan function is not implemented, this pin should be left open (NC). |
| TMS | K34 | I | **Test Mode Select:** Used to control the state of the Test Access Port controller. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 330-Ohm pull-down resistor. |
| TDO | L35 | O | **Test Data Output:** When SCAN_EN is high, it is used (in conjunction with TCK) to shift data out of the Test Access Port (TAP) in a serial bit stream. When JTAG boundary scan function is not implemented, this pin should be left open (NC). |
| TDI | G35 | I | **Test Data Input:** When SCAN_EN is high, it is used (in conjunction with TCK) to shift data and instructions into the TAP in a serial bit stream. When JTAG boundary scan function is not implemented, this pin should be left open (NC). |
| TRST_L | H34 | I | **Test Reset (Active LOW):** Active LOW signal to reset the TAP controller into an initialized state. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 330-Ohm pull-down resistor. |

## 3.5 POWER PINS

| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| VDDC | B, L, R | P | **VDDC Supply (1.0V):** Used as digital core power pins. |
| VDDR | F2, F34, M2 AP18, AP30, AR31, AR19 | P | **VDDR Supply (3.3V):** Used as digital I/O power pins. |
| CVDDR | P34, T34, Y34 | P | **VDDR Supply (3.3V):** Used as reference clock power pins. |
| VDDCAUX | P2, R1 | P | **VDDCAUX Supply (1.0V):** Used as auxiliary core power pins. |
| VAUX | T2 | P | **VAUX Supply (3.3V):** Used as auxiliary I/O power pins. |
| AVDD | T | P | **AVDD Supply (1.0V):** Used as PCI Express analog power pins. |
| AVDDH | A17 | P | **AVDDH Supply (3.3V):** Used as PCI Express analog high voltage power pins. |
| CGND | V34, AB34 | P | **Ground:** Used as reference clock ground pins. |
| AGND | B18, B22 | P | **Ground:** Used as analog ground pins. |
| VSS | GND | P | **VSS Ground:** Used as ground pins. |


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# 4 PIN ASSIGNMENTS

## *4.1 PIN LIST of 136-PIN aQFN*

| PIN | NAME | PIN | NAME | PIN | NAME | PIN | NAME |
|---|---|---|---|---|---|---|---|
| A1 | NC | B35 | NC | Y34 | CVDDR | AP18 | VDDR |
| A3 | NC | C1 | NC | AA1 | PRSNT[2] | AP20 | TEST6 |
| A5 | PETP[0] | C35 | NC | AA35 | REFCLKO_P[2] | AP22 | PL_512B |
| A7 | PETN[0] | D2 | NC | AB2 | NC | AP24 | NC |
| A9 | PERN[3] | D34 | NC | AB34 | CGND | AP26 | NC |
| A11 | PETP[3] | E1 | NC | AC1 | TEST4 | AP28 | CLKBUF_PD |
| A13 | PETN[3] | E35 | NC | AC35 | REFCLKO_N[2] | AP30 | VDDR |
| A15 | NC | F2 | VDDR | AD2 | RXPOLINV_DIS | AP32 | NC |
| A17 | AVDDH | F34 | VDDR | AD34 | NC | AP34 | NC |
| A19 | REFCLKN | G1 | DWNRST_L[1] | AE1 | TEST5 | AP35 | NC |
| A21 | REFCLKP | G35 | TDI | AE35 | NC | AR1 | NC |
| A23 | PETN[2] | H2 | NC | AF2 | SMBDATA | AR3 | NC |
| A25 | PETP[2] | H34 | TRST_L | AF34 | REFCLKI_N | AR5 | GPIO[1] |
| A27 | PERN[2] | J1 | NC | AG1 | SMBCLK | AR7 | GPIO[2] |
| A29 | PETN[1] | J35 | TCK | AG35 | REFCLKI_P | AR9 | GPIO[4] |
| A31 | PETP[1] | K2 | DWNRST_L[2] | AH2 | PWR_SAV | AR11 | GPIO[5] |
| A33 | NC | K34 | TMS | AH34 | EEPD | AR13 | GPIO[7] |
| A35 | NC | L1 | TEST1 | AJ1 | NC | AR15 | SLOT_IMP[2] |
| B1 | NC | L35 | TDO | AJ35 | SCAN_EN | AR17 | NC |
| B2 | NC | M2 | VDDR | AK2 | NC | AR19 | VDDR |
| B4 | PERP[0] | M34 | IREF | AK34 | PORTSTATUS[2] | AR21 | NC |
| B6 | PERN[0] | N1 | PERST_L | AL1 | NC | AR23 | NC |
| B8 | NC | N35 | REFCLKO_P[0] | AL35 | EECLK | AR25 | NC |
| B10 | PERP[3] | P2 | VDDCAUX | AM2 | NC | AR27 | NC |
| B12 | NC | P34 | CVDDR | AM34 | PORTSTATUS[0] | AR29 | NC |
| B14 | REXT | R1 | VDDCAUX | AN1 | NC | AR31 | VDDR |
| B16 | REXT_GND | R35 | REFCLKO_N[0] | AN35 | PORTSTATUS[1] | AR33 | NC |
| B18 | AGND | T2 | VAUX | AP1 | NC | AR35 | NC |
| B20 | NC | T34 | CVDDR | AP2 | NC | T | AVDD |
| B22 | AGND | U1 | TEST2 | AP4 | NC | B | VDDC |
| B24 | NC | U35 | REFCLKO_P[1] | AP6 | SLOTCLK | R | VDDC |
| B26 | PERP[2] | V2 | TEST3 | AP8 | GPIO[0] | L | VDDC |
| B28 | NC | V34 | CGND | AP10 | GPIO[3] | GND | VSS |
| B30 | PERN[1] | W1 | VC1_EN | AP12 | GPIO[6] | | |
| B32 | PERP[1] | W35 | REFCLKO_N[1] | AP14 | SLOT_IMP[1] | | |
| B34 | NC | Y2 | PRSNT[1] | AP16 | NC | | |


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# 5 FUNCTIONAL DESCRIPTION

Multiple virtual PCI-to-PCI Bridges (VPPB), connected by a virtual PCI bus, reside in the Switch. Each VPPB contains the complete PCIe architecture layers that consist of the physical, data link, and transaction layer. The packets entering the Switch via one of VPPBs are first converted from serial bit-stream into parallel bus signals in physical layer, stripped off the link-related header by data link layer, and then relayed up to the transaction layer to extract out the transaction header. According to the address or ID embedded in the transaction header, the entire transaction packets are forwarded to the destination VPPB for formatting as a serial-type PCIe packet through the transmit circuits in the data link layer and physical layer. The following sections describe these function elements for processing PCIe packets within the Switch.

## *5.1 PHYSICAL LAYER CIRCUIT*

The physical layer circuit design is based on the PHY Interface for PCI Express Architecture (PIPE). It contains Physical Media Attachment (PMA) and Physical Coding Sub-layer (PCS) blocks. PMA includes Serializer/ Deserializer (SERDES), PLL[1], Clock Recovery module, receiver detection circuits, beacon transmitter, electrical idle detector, and input/output buffers. PCS consists of framer, 8B/10B encoder/decoder, receiver elastic buffer, and PIPE PHY control/status circuitries. To provide the flexibility for port configuration, each lane has its own control and status signals for MAC to access individually. In addition, a pair of PRBS generator and checker is included for PHY built-in self test. The main functions of physical layer circuits include the conversion between serial-link and parallel bus, provision of clock source for the Switch, resolving clock difference in receiver end, and detection of physical layer errors.

In order to meet the needs of different application, the drive amplitude, de-emphasis and equalization of each transmitting channels can be adjusted using EEPROM individually. De-emphasis of -3.5 db is implemented by the transmitters when full swing signaling is used, while an offset can be individually applied to each channel.

### 5.1.1 RECEIVER DETECTION

The physical layer circuits implement receiver detection, which detects the presence of an attached 50 ohm to ground termination as per PCI Express Specification. The detect circuits determine if the voltage levels of the receiver have crossed the internal threshold after a configurable time determined by the Receiver Detection Threshold field in the PHY Parameter 2 Register (offset 7Ch, bit[6:4]) as listed in Table 5-1, which can be configured by EEPROM or SMBUS settings.

**Table 5-1 Receiver Detection Threshold Settings**

| Receiver Detection Threshold | Threshold |
|---|---|
| 000 | 1.0 us |
| 001 | 2.0 us |
| 010 | 4.0 us (Recommended) |
| 011 | 5.0 us |
| 100 | 10 us |
| 101 | 20 us |
| 110 | 40 us |
| 111 | 50 us |

[1] Multiple lanes could share the PLL.


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### 5.1.2 RECEIVER SIGNAL DETECTION

Receiver signal idling is detected with levels above a programmable threshold specified by Receiver Signal Detect field in the PHY Parameter 2 Register (Offset 7Ch, bit[21:20]) as listed in Table 5-2, which can be configured on a per-port basis via EEPROM or SMBUS settings.

**Table 5-2 Receiver Signal Detect Threshold**

| Receiver Signal Detect | Min (mV ppd) | Max (mV ppd) |
|---|---|---|
| 00 | 50 | 80 |
| 01 (Recommended) | 65 | 175 |
| 10 | 75 | 200 |
| 11 | 120 | 240 |

### 5.1.3 RECEIVER EQUALIZATION

The receiver implements programmable equalizer via the Receiver Equalization field in the PHY Parameter 2 Register (Offset 7Ch, bit[25:22]) as listed in Table 5-3, which can be configured on a per-port basis via EEPROM or SMBUS settings.

**Table 5-3 Receiver Equalization Settings**

| Receiver Equalization | Equalization |
|---|---|
| 0000 | Off |
| 0010 | Low |
| 0110 (Recommended) | Medium |
| 1110 | High |

### 5.1.4 TRANSMITTER SWING

The PCI Express transmitters support implementations of both full voltage swing and half (low) voltage swing. In full swing signaling mode, the transmitters implement de-emphasis, while in half swing mode, the transmitters do not. The Transmitter Swing field in the PHY Parameter 2 Register (offset 7Ch, Bit[30]) is used for the selection of full swing signaling or half swing signaling, which can be configured on a per-port basis via EEPROM or SMBUS settings.

**Table 5-4 Transmitter Swing Settings**

| Transmitter Swing | Mode | De-emphasis |
|---|---|---|
| 0 | Full Voltage Swing | Implemented |
| 1 | Half Voltage Swing | Not implemented |

### 5.1.5 DRIVE AMPLITUDE AND DE-EMPHASIS SETTINGS

Depending on the operation condition (voltage swing and de-emphasis condition), one of the Drive Amplitude Base Level fields in the Switch Operation Mode Register (offset 74h) and one of the Drive De-Emphasis Base Level fields in the PHY Parameter 1 Register (offset 7Ah) are active for configuration of the amplitude and de-emphasis.

The final drive amplitude and drive de-emphasis are the summation of the base level value and the offset value. The offset value for drive amplitude is 25 mV pd, and 6.25 mV pd for drive de-emphasis.


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The driver output waveform is the synthesis of amplitude and de-emphasis as shown in Figure 5-1. The driver amplitude without de-emphasis is specified as a peak differential voltage level (mVpd), and the driver de-emphasis modifies the driver amplitude.

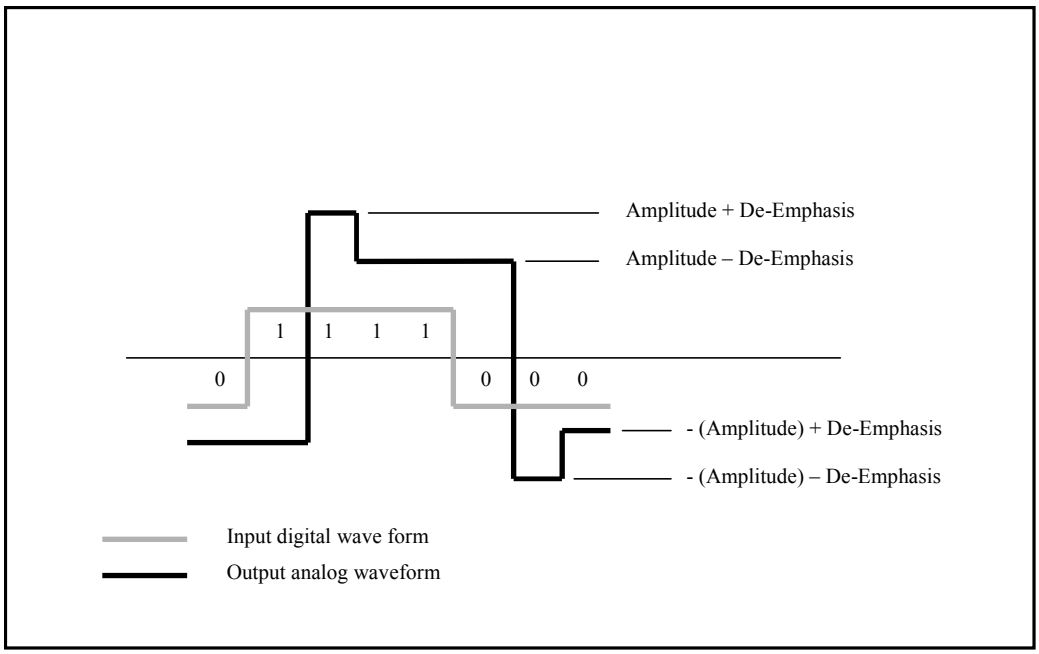


**Figure 5-1 Driver Output Waveform**

## 5.1.6 DRIVE AMPLITUDE

Only one of the Drive Amplitude Level field in the Switch Operation Mode Register (offset 74h, bit[20:16], bit[25:21] and bit[30:26]) listed in Table 5-5 is active depending on the de-emphasis and swing condition. The settings and the corresponding values of the amplitude level are listed in Table 5-6, which can be configured by EEPROM or SMBUS settings.

**Table 5-5 Drive Amplitude Base Level Registers**

| Active Register | De-Emphasis Condition | Swing Condition |
|---|---|---|
| C_DRV_LVL_3P5_NOM | -3.5 db | Full |
| C_DRV_LVL_6P0_NOM | -6.0 db | Full |
| C_DRV_LVL_HALF_NOM | N/A | Half |

**Table 5-6 Drive Amplitude Base Level Settings**

| Setting | Amplitude (mV pd) | Setting | Amplitude (mV pd) | Setting | Amplitude (mV pd) |
|---|---|---|---|---|---|
| 00000 | 0 | 00111 | 175 | 01110 | 350 |
| 00001 | 25 | 01000 | 200 | 01111 | 375 |
| 00010 | 50 | 01001 | 225 | 10000 | 400 |
| 00011 | 75 | 01010 | 250 | 10001 | 425 |
| 00100 | 100 | 01011 | 275 | 10010 | 450 |
| 00101 | 125 | 01100 | 300 | 10011 | 475 |
| 00110 | 150 | 01101 | 325 | Others | Reserved |

**Note**:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.


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2. The maximum nominal amplitude of the output driver is 475 mVpd. Combined values of driver amplitude and de-emphasis greater than 475 mVpd should be avoided.
3. At higher amplitudes, actual swings will be less than the theoretical value due to process variations and environment factors, such as voltage overhead compression, package losses, board losses, and other effects.

### 5.1.7 DRIVE DE-EMPHASIS

The Drive De-Emphasis Level field in the PHY Parameter 1 Register (Offset 78h, bit[20:16], bit[25:21] and bit[30:26]) listed in Table 5-7 controls the de-emphasis base level. The settings and the corresponding values of the de-emphasis level are listed in Table 5-8, which can be configured globally via EEPROM or SMBUS settings.

**Table 5-7 Drive De-Emphasis Base Level Register**

| Register | De-Emphasis Condition |
|---|---|
| C_EMP_POST_GEN1_3P5_NOM | -3.5 db |
| C_EMP_POST_GEN2_3P5_NOM | -3.5 db |
| C_EMP_POST_GEN2_6P0_NOM | -6.0 db |

**Table 5-8 Drive De-Emphasis Base Level Settings**

| Setting | De-Emphasis (mV pd) | Setting | De-Emphasis (mV pd) | Setting | De-Emphasis (mV pd) |
|---|---|---|---|---|---|
| 00000 | 0.0 | 01011 | 69.0 | 10110 | 137.5 |
| 00001 | 6.0 | 01100 | 75.0 | 10111 | 144.0 |
| 00010 | 12.5 | 01101 | 81.0 | 11000 | 150.0 |
| 00011 | 19.0 | 01110 | 87.0 | 11001 | 156.0 |
| 00100 | 25.0 | 01111 | 94.0 | 11010 | 162.5 |
| 00101 | 31.0 | 10000 | 100.0 | 11011 | 169.0 |
| 00110 | 37.5 | 10001 | 106.0 | 11100 | 175.0 |
| 00111 | 44.0 | 10010 | 112.5 | 11101 | 181.0 |
| 01000 | 50.0 | 10011 | 119.0 | 11110 | 187.5 |
| 01001 | 56.0 | 10100 | 125.0 | 11111 | 194.0 |
| 01010 | 62.5 | 10101 | 131.0 | - | - |

**Note**:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mVpd. Combined values of driver amplitude and de-emphasis greater than 475 mVpd should be avoided.
3. At higher amplitudes, actual swings will be less than the theoretical value due to process variations and environment factors, such as voltage overhead compression, package losses, board losses, and other effects.

### 5.1.8 TRANSMITTER ELECTRICAL IDLE LATENCY

After the last character of the PCI Express transmission, the output current is reduced, and a differential voltage of less than 20 mV with common mode of VTX-CM-DC is established within 20 UI. This delay time is programmable via Transmitter PHY Latency field in the PHY Parameter 2 Register (Offset 7Ch, bit[3:0]), which can be configured by EEPROM or SMBUS settings.

## *5.2 DATA LINK LAYER (DLL)*

The Data Link Layer (DLL) provides a reliable data transmission between two PCI Express points. An ACK/NACK protocol is employed to guarantee the integrity of the packets delivered. Each Transaction Layer Packet (TLP) is protected by a 32-bit LCRC for error detection. The DLL receiver performs LCRC calculation to determine if the incoming packet is corrupted in the serial link. If an LCRC error is found, the DLL transmitter would issue a NACK data link layer packet (DLLP) to the opposite end to request a re-transmission, otherwise an ACK DLLP would be sent out to acknowledge on reception of a good TLP.


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In the transmitter, a retry buffer is implemented to store the transmitted TLPs whose corresponding ACK/NACK DLLP have not been received yet. When an ACK is received, the TLPs with sequence number equals to and smaller than that carried in the ACK would be flushed out from the buffer. If a NACK is received or no ACK/NACK is returned from the link partner after the replay timer expires, then a replay mechanism built in DLL transmitter is triggered to re-transmit the corresponding packet that receives NACK or time-out and any other TLP transmitted after that packet.

Meanwhile, the DLL is also responsible for the initialization, updating, and monitoring of the flow-control credit. All of the flow control information is carried by DLLP to the other end of the link. Unlike TLP, DLLP is guarded by 16-bit CRC to detect if data corruption occurs.

In addition, the Media Access Control (MAC) block, which is consisted of LTSSM, multiple lanes de-skew, scrambler/de-scrambler, clock correction from inserting skip order-set, and PIPE-related control/status circuits, is implemented to interface physical layer with data link layer.

## 5.3 TRANSACTION LAYER RECEIVE BLOCK (TLP DECAPSULATION)

The receiving end of the transaction layer performs header information retrieval and TC/VC mapping (see section 5.5), and it validates the correctness of the transaction type and format. If the TLP is found to contain an illegal header or the indicated packet length mismatches with the actual packet length, then a Malformed TLP is reported as an error associated with the receiving port. To ensure end-to-end data integrity, a 32-bit ECRC is checked against the TLP at the receiver if the digest bit is set in header.

## 5.4 ROUTING

The transaction layer implements three types of routing protocols: ID-based, address-based, and implicit routing. For configuration reads, configuration writes, transaction completion, and user-defined messages, the packets are routed by their destination ID constituted of bus number, device number, and function number. Address routing is employed to forward I/O or memory transactions to the destination port, which is located within the address range indicated by the address field carried in the packet header. The packet header indicates the packet types including memory read, memory write, IO read, IO write, Message Signaling Interrupt (MSI) and user-defined message. Implicit routing is mainly used to forward system message transactions such as virtual interrupt line, power management, and so on. The message type embedded in the packet header determines the routing mechanism.

If the incoming packet cannot be forwarded to any other port due to a miss to hit the defined address range or targeted ID, this is considered as Unsupported Request (UR) packet, which is similar to a master abort event in PCI protocol.

## 5.5 TC/VC MAPPING

The 3-bit TC field defined in the header identifies the traffic class of the incoming packets. To enable the differential service, a TC/VC mapping table at destination port that is pre-programmed by system software or EEPROM pre-load is utilized to cast the TC labeled packets into the desired virtual channel. Note that TC0 traffic is mapped into VC0 channel by default. After the TC/VC mapping, the receive block dispatches the incoming request, completion, or data into the appropriate VC0 and VC1 queues.


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## 5.6 QUEUE

In PCI Express, it defines six different packet types to represent request, completion, and data. They are respectively Posted Request Header (PH), Posted Request Data payload (PD), Non-Posted Request Header (NPH), Non-Posted Data Payload (NPD), Completion Header (CPLH) and Completion Data payload (CPLD). Each packet with different type would be put into a separate queue in order to facilitate the following ordering processor. Since NPD usually contains one DW, it can be merged with the corresponding NPH into a common queue named NPHD. Except NPHD, each virtual channel (VC0 or VC1) has its own corresponding packet header and data queue. When only VC0 is needed in some applications, VC1 can be disabled and its resources assigned to VC0 by asserting VC1_EN (Virtual Channel 1 Enable) to low.

### 5.6.1 PH

PH queue provides TLP header spaces for posted memory writes and various message request headers. Each header space occupies sixteen bytes to accommodate 3 DW or 4 DW headers. There are two PH queues for VC0 and VC1 respectively.

### 5.6.2 PD

PD queue is used for storing posted request data. If the received TLP is of the posted request type and is determined to have payload coming with the header, the payload data would be put into PD queue. There are two PD queues for VC0 and VC1 respectively.

### 5.6.3 NPHD

NPHD queue provides TLP header spaces for non-posted request packets, which include memory read, IO read, IO write, configuration read, and configuration write. Each header space takes twenty bytes to accommodate a 3-DW header, s 4-DW header, s 3-WD header with 1-DW data, and a 4-DW header with 1-DW data. There is only one NPHD queue for VC0, since non-posted request cannot be mapped into VC1.

### 5.6.4 CPLH

CPLH queue provides TLP header space for completion packets. Each header space takes twelve bytes to accommodate a 3-DW header. Please note that there are no 4-DW completion headers. There are two CPLH queues for VC0 and VC1 respectively.

### 5.6.5 CPLD

CPLD queue is used for storing completion data. If the received TLP is of the completion type and is determined to have payload coming with the header, the payload data would be put into CPLD queue. There are two CPLD queues for VC0 and VC1 respectively.

## 5.7 TRANSACTION ORDERING

Within a VPPB, a set of ordering rules is defined to regulate the transactions on the PCI Express Switch including Memory, IO, Configuration and Messages, in order to avoid deadlocks and to support the Producer-Consumer


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model. The ordering rules defined in table 5-4 apply within a single Traffic Class (TC). There is no ordering requirement among transactions within different TC labels. Since the transactions with the same TC label are not allowed to map into different virtual channels, it implies no ordering relationship between the traffic in VC0 and VC1.

**Table 5-9 Summary of PCI Express Ordering Rules**

| Row Pass Column | Posted Request | Read Request | Non-posted Write Request | Read Completion | Non-posted Write Completion |
|---|---|---|---|---|---|
| Posted Request | Yes/No[1] | Yes[5] | Yes[5] | Yes[5] | Yes[5] |
| Read Request | No[2] | Yes | Yes | Yes | Yes |
| Non-posted Write Request | No[2] | Yes | Yes | Yes | Yes |
| Read Completion | Yes/No[3] | Yes | Yes | Yes | Yes |
| Non-Posted Write Completion | Yes[4] | Yes | Yes | Yes | Yes |

1. When the Relaxed Ordering Attribute bit is cleared, the Posted Request transactions including memory write and message request must complete on the egress bus of VPPB in the order in which they are received on the ingress bus of VPPB. If the Relaxed Ordering Attribute bit is set, the Posted Request is permitted to pass over other Posted Requests occurring before it.

2. A Read Request transmitting in the same direction as a previously queued Posted Request transaction must push the posted write data ahead of it. The Posted Request transaction must complete on the egress bus before the Read Request can be attempted on the egress bus. The Read transaction can go to the same location as the Posted data. Therefore, if the Read transaction were to pass the Posted transaction, it would return stale data.

3. When the Relaxed Ordering Attribute bit is cleared, a Read completion must ''pull'' ahead of previously queued posted data transmitting in the same direction. In this case, the read data transmits in the same direction as the posted data, and the requestor of the read transaction is on the same side of the VPPB as the completer of the posted transaction. The posted transaction must deliver to the completer before the read data is returned to the requestor. If the Relaxed Ordering Attribute bit is set, then a read completion is permitted to pass a previously queued Memory Write or Message Request.

4. Non-Posted Write Completions are permitted to pass a previous Memory Write or Message Request transaction. Such transactions are actually transmitting in the opposite directions and hence have no ordering relationship.

5. Posted Request transactions must be given opportunities to pass Non-posted Read and Write Requests as well as Completions. Otherwise, deadlocks may occur when some older bridges, which do not support delayed transactions are mixed with PCIe Switch in the same system. A fairness algorithm is used to arbitrate between the Posted Write queue and the Non-posted transaction queue

## 5.8 PORT ARBITRATION

Among multiple ingress ports, the port arbitration built in the egress port determines which incoming packets to be forwarded to the output port. The arbitration algorithm contains hardware fixed Round Robin, 128-phase Weighted Round-Robin and programmable 128-phase time-based WRR. The port arbitration is held within the same VC channel. It means that each port has two port arbitration circuitries for VC0 and VC1 respectively. At the upstream ports, in addition to the inter-port packets, the intra-port packet such as configurations completion would also join the arbitration loop to get the service from Virtual Channel 0.


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## 5.9 VC ARBITRATION

After port arbitration, VC arbitration is executed among different VC channels within the same source. Three arbitration algorithms are provided to choose the appropriate VC: Strict Priority, Round Robin or Weighted Round Robin.

## 5.10 FLOW CONTROL

PCI Express employs Credit-Based Flow Control mechanism to make buffer utilization more efficient. The transaction layer transmitter ensures that it does not transmit a TLP to an opposite receiver unless the receiver has enough buffer space to accept the TLP. The transaction layer receiver has the responsibility to advertise the free buffer space to an opposite transmitter to avoid packet stale. In this Switch, each port has its own separate queues for different traffic types and the credits are sent to data link layer on the fly. The data link layer compares the current available credits with the monitored ones and reports the updated credit to the counterpart. If no new credit is acquired, the credit reported is scheduled for every 30 us to prevent the link from entering retrain. On the other hand, the receiver at each egress port gets the usable credits from the opposite end in a link. The output port broadcasts them to all the other ingress ports to get packet transmission.

## 5.11 TRANSATION LAYER TRANSMIT BLOCK (TLP ENCAPSULATION)

The transmit portion of transaction layer performs the following functions. They construct the all types of forwarded TLP generated from VC arbiter, respond with the completion packets when the local resource (i.e. configuration register) is accessed, and regenerate the message that terminates at receiver to RC if acting as an upstream port.

## 5.12 ACCESS CONTROLS SERVICE

Traditionally, the packet routing between the peer-to-peer downstream ports is determined by either the address or ID field embedded in the packet header. ACS provides a mechanism for customer to selectively control access between PCI Express Endpoints attached to the downstream ports of packet switch. If ACS is enabled in the ingress port, the peer-to-peer packet forwarding will follow the rule sets of ACS rather than the destination ID or address. ACS is implemented as a set of capabilities and control registers in the associated hardware component. It brings the following benefits such as preventing the silent data corruption presented in Requests from being incorrectly routed to a peer Endpoint, validating every Request transaction between two downstream components and enabling direct routing of peer-to-peer Memory Requests whose addresses have been Translated when ATS system is being used.


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# 6 EEPROM INTERFACE AND SYSTEM MANAGEMENT BUS

The EEPROM interface consists of two pins: EECLK (EEPROM clock output) and EEPD (EEPROM bi-directional serial data). The Switch may control an ISSI IS24C04 or compatible parts using into 512x8 bits. The EEPROM is used to initialize a number of registers before enumeration. This is accomplished after PRST# is de-asserted, at which time the data from the EEPROM is loaded. The EEPROM interface is organized into a 16-bit base, and the Switch supplies a 7-bit EEPROM word address. The Switch does not control the EEPROM address input. It can only access the EEPROM with address input set to 0.

The System Management Bus interface consists of two pins: SMBCLK (System Management Bus Clock input) and SMBDATA (System Management Bus Data input/ output).

## *6.1 EEPROM INTERFACE*

### 6.1.1 AUTO MODE EERPOM ACCESS

The Switch may access the EEPROM in a WORD format by utilizing the auto mode through a hardware sequencer. The EEPROM start-control, address, and read/write commands can be accessed through the configuration register. Before each access, the software should check the Autoload Status bit before issuing the next start.

### 6.1.2 EEPROM MODE AT RESET

During a reset, the Switch will automatically load the information/data from the EEPROM if the automatic load condition is met. The first offset in the EEPROM contains a signature. If the signature is recognized, the autoload initiates right after the reset.

During the autoload, the Bridge will read sequential words from the EEPROM and write to the appropriate registers. Before the Bridge registers can be accessed through the host, the autoload condition should be verified by reading bit [3] offset DCh (EEPROM Autoload Status). The host access is allowed only after the status of this bit is set to '0' which indicates that the autoload initialization sequence is complete.

### 6.1.3 EEPROM SPACE ADDRESS MAP

| 15 – 8 | 7 – 0 | BYTE OFFSET |
|---|---|---|
| EEPROM Signature (1516h) | | 00h |
| Vendor ID | | 02h |
| Device ID | | 04h |
| Extended VC Count / Link Capability / Switch Mode Operation / Interrupt pin for Port 1 ~ 2 | | 06h |
| Subsystem Vender ID | | 08h |
| Subsystem ID | | 0Ah |
| Max_Payload_Size Support / ASPM Support / Role_Base Error Reporting | | 0Ch |
| Global PHY TX Margin Parameter for Port 0~2 | | 0Eh |
| Global PHY Parameter 0 for Port 0~2 | | 10h |
| Global XPIP_CSR6[0] / Global PHY Parameter 1 for Port 0~2 | | 12h |
| Global XPIP_CSR6[4:1] / Global PHY Parameter 2/3 for Port 0~2 | | 14h |
| Global XPIP_CSR4[15:0] for Port 0~2 | | 16h |
| Global XPIP_CSR4[31:16] for Port 0~2 | | 18h |
| Global XPIP_CSR5[15:0] for Port 0~2 | | 1Ah |
| Buffer_ctrl[4:0] / Globe XPIP_CSR6[7:5] for Port 0~2 | Global XPIP_CSR5[23:16] for Port 0~2 | 1Ch |
| MAC_CTR / Global PHY Parameter 3 for Port 0~2 | | 1Eh |


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| 15 – 8 | 7 – 0 | BYTE OFFSET |
|---|---|---|
| NFTS / Scramble / XPIP_CSR2 / Deskew mode select for Port 0 | | 20h |
| NFTS / Scramble / XPIP_CSR2 / Deskew mode select for Port 1 | | 22h |
| NFTS / Scramble / XPIP_XSR2 / Deskew mode select for Port 2 | | 24h |
| Reserved | | 26h |
| Reserved | | 28h |
| Reserved | | 2Ah |
| Reserved | | 2Ch |
| Reserved | | 2Eh |
| PHY Parameter2_1 for Port 0 | | 30h |
| PHY Parameter2_1 for Port 1 | | 32h |
| PHY Parameter2_1 for Port 2 | | 34h |
| Reserved | | 36h |
| Reserved | | 38h |
| Reserved | | 3Ah |
| Reserved | | 3Ch |
| Reserved | | 3Eh |
| Do_change_rate_cnt/ XPIP_CSR_2 for Port 0 | PHY Parameter 3/ PHY Parameter2_2 for Port 0 | 40h |
| Sel_deemp/ Do_change_rate_cnt/ XPIP_CSR_2 for Port 1 | PHY Parameter 3/ PHY Parameter2_2 for Port 1 | 42h |
| Sel_deemp/ Do_change_rate_cnt/ XPIP_CSR_2 for Port 2 | PHY Parameter 3/ PHY Parameter2_2 for Port 2 | 44h |
| Reserved | | 46h |
| Reserved | | 48h |
| Reserved | | 4Ah |
| Reserved | | 4Ch |
| Reserved | | 4Eh |
| PM Data for Port 0 | PM Capability for Port 0 | 50h |
| PM Data for Port 1 | PM Capability for Port 1 | 52h |
| PM Data for Port 2 | PM Capability for Port 2 | 54h |
| Reserved | | 56h |
| Reserved | | 58h |
| Reserved | | 5Ah |
| Reserved | | 5Ch |
| Reserved | | 5Eh |
| TC/VC Map for Port 0 (VC0) | Slot Clock / LPVC Count / Port Num for Port 0 | 60h |
| TC/VC Map for Port 1 (VC0) | Slot Implemented / Slot Clock / LPVC Count / Port Num for Port 1 | 62h |
| TC/VC Map for Port 2 (VC0) | Slot Implemented / Slot Clock / LPVC Count / Port Num for Port 2 | 64h |
| Reserved | | 66h |
| Reserved | | 68h |
| Reserved | | 6Ah |
| Reserved | | 6Ch |
| Reserved | | 6Eh |
| Power Budgeting Capability Register for Port 0 | | 70h |
| Power Budgeting Capability Register for Port 1 | | 72h |
| Power Budgeting Capability Register for Port 2 | | 74h |
| Reserved | | 76h |
| Reserved | | 78h |
| Reserved | | 7Ah |
| Reserved | | 7Ch |
| Reserved | | 7Eh |
| XPIP_CSR5[30:24] for Port 0 | PM Control Para/Rx Polarity for Port 0 | 80h |
| XPIP_CSR5[30:24] for Port 1 | PM Control Para/Rx Polarity for Port 1 | 82h |
| XPIP_CSR5[30:24] for Port 2 | PM Control Para/Rx Polarity for Port 2 | 84h |
| Reserved | | 86h |
| Reserved | | 88h |
| Reserved | | 8Ah |


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| 15 – 8 | 7 – 0 | BYTE OFFSET |
|---|---|---|
| Reserved | | 8Ch |
| Reserved | | 8Eh |
| Reserved | | 90h |
| Slot Capability 0 for Port 1 | | 92h |
| Slot Capability 0 for Port 2 | | 94h |
| Reserved | | 96h |
| Reserved | | 98h |
| Reserved | | 9Ah |
| Reserved | | 9Ch |
| Reserved | | 9Eh |
| Reserved | | A0h |
| Slot Capability 1 for Port 1 | | A2h |
| Slot Capability 1 for Port 2 | | A4h |
| Reserved | | A6h |
| Reserved | | A8h |
| Reserved | | AAh |
| Reserved | | ACh |
| Reserved | | AEh |
| XPIP_CSR3[15:0] for Port 0 | | B0h |
| XPIP_CSR3[15:0] for Port 1 | | B2h |
| XPIP_CSR3[15:0] for Port 2 | | B4h |
| Reserved | | B6h |
| Reserved | | B8h |
| Reserved | | BAh |
| Reserved | | BCh |
| Reserved | | BEh |
| XPIP_CSR3[16:31] for Port 0 | | C0h |
| XPIP_CSR3[16:31] for Port 1 | | C2h |
| XPIP_CSR3[16:31] for Port 2 | | C4h |
| Reserved | | C6h |
| Reserved | | C8h |
| Reserved | | CAh |
| Reserved | | CCh |
| Reserved | | CEh |
| REV_TS_CTR/Replay Time-out Counter for Port 0 | | D0h |
| REV_TS_CTR /Replay Time-out Counter for Port 1 | | D2h |
| REV_TS_CTR /Replay Time-out Counter for Port 2 | | D4h |
| Reserved | | D6h |
| Reserved | | D8h |
| Reserved | | DAh |
| Reserved | | DCh |
| Reserved | | DEh |
| Acknowledge Latency Timer for Port 0 | | E0h |
| Acknowledge Latency Timer for Port 1 | | E2h |
| Acknowledge Latency Timer for Port 2 | | E4h |
| Reserved | | E6h |
| Reserved | | E8h |
| Reserved | | EAh |
| Reserved | | ECh |
| Reserved | | EEh |
| TC/VC Map for Port 0 (VC1) | Maximum Time Slot for Port 0 | F0h |
| TC/VC Map for Port 1 (VC1) | Maximum Time Slot for Port 0 | F2h |
| TC/VC Map for Port 2 (VC1) | Maximum Time Slot for Port 0 | F4h |
| Reserved | | F6h |
| Reserved | | F8h |
| Reserved | | FAh |
| Reserved | | FCh |
| Reserved | | FEh |


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## 6.1.4 MAPPING EEPROM CONTENTS TO CONFIGURATION REGISTERS

| ADDRESS | PCI CFG OFFSET | DESCRIPTION |
|---|---|---|
| 00h | | **EEPROM signature** – 1516h |
| 02h | **00h ~ 01h** | **Vendor ID** |
| 04h | **02h ~ 03h** | **Device ID** |
| 06h | **144h (Port 0~2)**<br>144h: Bit [0] | **Extended VC Count for Port 0~2**<br>▪ Bit [0]: It represents the supported VC count other than the default VC |
| | **CCh (Port 0~2)**<br>CCh: Bit [14:12]<br>CCh: Bit [17:15] | **Link Capability for Port 0~2**<br>▪ Bit [3:1]: It represents L0s Exit Latency for all ports<br>▪ Bit [6:4]: It represents L1 Exit Latency for all ports |
| | **74h (Port 0~2)**<br>74h: Bit [5]<br>74h: Bit [6]<br>74h: Bit [0]<br>74h: Bit [2:1]<br>74h: Bit [3]<br>74h: Bit [4] | **Switch Mode Operation for Port 0**<br>▪ Bit [8]: no ordering on packets for different egress port mode<br>▪ Bit [9]: no ordering on different tag of completion mode<br>▪ Bit [10]: Store and Forward<br>▪ Bit [12:11]: Cut-through Threshold<br>▪ Bit [13] : Port arbitrator Mode<br>▪ Bit [14]: Credit Update Mode |
| | **3Ch (Port 1~2)**<br>3Ch: Bit [8] | **Interrupt pin for Port 1~2**<br>▪ Bit [15]: Set when INTA is requested for interrupt resource |
| 08h | **B4h ~ B5h** | **Subsystem Vender ID** |
| 0Ah | **B6h ~ B7h** | **Subsystem ID** |
| 0Ch | **C4h (Port 0~2)**<br>C4h: Bit [1:0] | **Max_Payload_Size Support for Port 0~2**<br>▪ Bit [1:0]: Indicated the maximum payload size that the device can support for the TLP |
| | **CCh (Port 0~2)**<br>CCh: Bit [11:10] | **ASPM Support for Port 0~2**<br>▪ Bit [3:2] : Indicate the level of ASPM supported on the PCIe link |
| | **C4h (Port 0~2)**<br>C4h: Bit [15] | **Role_Base Error Reporting for Port 0~2**<br>▪ Bit [4] : Indicate implement the role-base error reporting |
| | **70h (Port 0~2)**<br>70h: Bit [14] | **MSI Capability Disable for Port 0~2**<br>▪ Bit [5] : Disable MSI capability |
| | **74h (Port 0~2)**<br>74h: Bit [15] | **Compliance Pattern Parity Control Disable for Port 0~2**<br>▪ Bit [6] : Disable compliance pattern parity |
| | **70h (Port 0~2)**<br>70h: Bit [13] | **Power Management Capability Disable for Port 0~2**<br>▪ Bit [7] : Disable Power Management Capability |
| | **8Ch (Port 0~2)**<br>8Ch: Bit [5] | **ORDER RULE5 Enable for port 0~2**<br>▪ Bit [8]: Capability for Post packet Pass Non-Post packet |
| | **CCh (Port 1~2)**<br>CCh: Bit [21] | **Link Bandwidth Notification Capability for port 1~2**<br>▪ Bit [9]: Link Bandwidth Notification Capability |
| | **8Ch (Port 0~2)**<br>8Ch: Bit [6] | **Ordering Frozen for Port 0~2**<br>▪ Bit [10]: Freeze the ordering feature |
| | **8Ch (Port 0~2)**<br>8Ch: Bit [0] | **TX SOF Latency Mode for Port 0~2**<br>▪ Bit [11]: Set to zero to shorten latency |
| | **CCh (Port 0~2)**<br>CCh: Bit [19] | **Surprise Down Capability Enable for Port 0~2**<br>▪ Bit [12]: Enable Surprise Down Capability |
| | **8Ch (Port 0~2)**<br>8Ch: Bit [1]<br>E4h (Port 0~2)<br>E4h: Bit [12] | **Power Management's Data Select Register R/W Capability for Port 0~2**<br>▪ Bit [13]: Enable Data Select Register R/W<br>**LTR Capability Enable for Port 0~2**<br>▪ Bit [14]: LTR capability enable |
| | **8Ch (Port 0~2)**<br>8Ch: Bit [3] | **4KB Boundary Check Enable for Port 0~2**<br>▪ Bit [15]: Enable 4KB Boundary Check |


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| ADDRESS | PCI CFG OFFSET | DESCRIPTION |
|---|---|---|
| 0Eh | **94h (Port 0~2)**<br>94h: Bit [4:0]<br>94h: Bit [9:5]<br>94h: Bit [14:10]<br><br>**E4h (Port 0~2)**<br>E4h: Bit [18] | **PHY TX Margin Parameter for Port 0~2**<br>▪ Bit [4:0]: C_DRV_LVL_3P5_MGN2<br>▪ Bit [9:5]: C_DRV_LVL_6P0_MGN2<br>▪ Bit [14:10]: C_DRV_LVL_HALF_MGN2<br><br>**OBFF Capability Enable for Port 0~2**<br>▪ Bit [15] : enable OBFF capability |
| 10h | **74h (Port 0~2)**<br>74h: Bit [20:16]<br>74h: Bit [25:21]<br>74h: Bit [30:26]<br><br>**8Ch (Port 0~2)**<br>8Ch: Bit [31] | **PHY Parameter 0 for Port 0~2**<br>▪ Bit [4:0]: C_DRV_LVL_3P5_NOM<br>▪ Bit [9:5]: C_DRV_LVL_6P0_NOM<br>▪ Bit [14:10]: C_DRV_LVL_HALF_NOM<br><br>**TL_CSR[31] for Port 0~2**<br>▪ Bit [15] : P35_GEN2_MODE |
| 12h | **78h (Port 0~2)**<br>78h: Bit [20:16]<br>78h: Bit [25:21]<br>78h: Bit [30:26]<br><br>**8Ch (Port 0~2)**<br>8Ch: Bit [16] | **PHY Parameter 1 for Port 0~2**<br>▪ Bit [4:0]: C_EMP_POST_GEN1_3P5_NOM<br>▪ Bit [9:5]: C_EMP_POST_GEN2_3P5_NOM<br>▪ Bit [14:10]: C_EMP_POST_GEN2_6P0_NOM<br><br>**XPIP_CSR6[0] for Port 0~2**<br>▪ Bit [15]: XPIP_CSR6[0] |
| 14h | **7Ch (Port 0~2)**<br>7Ch: Bit [3:0]<br>7Ch: Bit [6:4]<br><br>**90h (Port 0~2)**<br>90h: Bit [19:15]<br><br>**8Ch (Port 0~2)**<br>8Ch: Bit [20:17] | **PHY Parameter 2 for Port 0~2**<br>▪ Bit [3:0]: C_TX_PHY_LATENCY<br>▪ Bit [6:4]: C_REC_DETECT_USEC<br><br>**PHY Parameter 3 for Port 0~2**<br>▪ Bit [11:7]: C_EMP_POST_HALF_DELTA<br><br>**XPIP_CSR6[4:1] for Port 0~2**<br>▪ Bit [15:12]: XPIP_CSR6[4:1] |
| 16h | **84h (Port 0~2)**<br>84h: Bit [15:0] | **XPIP_CSR4[15:0] for Port 0~2**<br>▪ Bit [15:0]: XPIP_CSR4[15:0] |
| 18h | **84h (Port 0~2)**<br>84h: Bit [31:16] | **XPIP_CSR4[31:16] for Port 0~2**<br>▪ Bit [15:0]: XPIP_CSR4[31:16] |
| 1A | **88h (Port 0~2)**<br>88h: Bit [15:0] | **XPIP_CSR5[15:0] for Port 0~2**<br>Bit [15:0]: XPIP_CSR5[15:0] |
| 1C | **88h (Port 0~2)**<br>88h: Bit [23:16]<br><br>**8Ch (Port 0~2)**<br>8Ch: Bit [23:21]<br><br>**98h (Port 0~2)**<br>98h: Bit [20:16] | **XPIP_CSR5[28:16] for Port 0~2**<br>▪ Bit [7:0]: XPIP_CSR5[23:16]<br><br>**XPIP_CSR6[7:5] for Port 0~2**<br>▪ Bit [10:8]: XPIP_CSR6[7:5]<br><br>**BUFFER_CTRL[4:0] for Port 0~2**<br>▪ Bit [15:11]: Reference clock Buffer control |
| 1E | **90h (Port 0~2)**<br>90h: Bit [21:20]<br>90h: Bit [23:22]<br>90h: Bit [25:24]<br>90h: Bit [27:26]<br>90h: Bit [29:28]<br>90h: Bit [31:30]<br><br>**8Ch (Port 0~2)**<br>8Ch: Bit [29:26] | **PHY parameter 3 for Port 0~2**<br>▪ Bit [1:0]: C_DRV_LVL_3P5_DELTA<br>▪ Bit [3:2]: C_DRV_LVL_6P0_DELTA<br>▪ Bit [5:4]: C_DRV_LVL_HALF_DELTA<br>▪ Bit [7:6]: C_EMP_POST_GEN1_3P5_DELTA<br>▪ Bit [9:8]: C_EMP_POST_GEN2_3P5_DELTA<br>▪ Bit [11:10]: C_EMP_POST_GEN2_6P0_DELTA<br><br>**MAC control parameter for Port 0~2**<br>▪ Bit [15:12]: MAC_CTR |
| 20h | **78h (Port 0)**<br>78h: Bit [7 :0]<br><br>**68h (Port 0)**<br>68h: Bit [14:13]<br><br>**78h (Port 0)**<br>78h: Bit [9:8]<br>78h: Bit [10]<br><br>**78h (Port 0)**<br>78h: Bit [13:12] | **FTS Number for Port 0**<br>▪ Bit [7:0]: FTS number at receiver side<br><br>**Deskew Mode Select for Port 0**<br>▪ Bit [9:8]: deskew mode select<br><br>**Scrambler Control for Port 0**<br>▪ Bit [11:10]: scrambler control<br>▪ Bit [12]: L0s<br><br>**Change_Speed_Sel for Port 0**<br>▪ Bit [14:13]: Change Speed select |


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| ADDRESS | PCI CFG OFFSET | DESCRIPTION |
|---|---|---|
| | **78h (Port 0)**<br>78h: Bit [14] | **Change_Speed_En for Port 0**<br>▪ Bit [15]: Change Speed enable |
| 22h | **78h (Port 1)**<br>78h: Bit [7 :0] | **FTS Number for Port 1**<br>▪ Bit [7:0]: FTS number at receiver side |
| | **68h (Port 1)**<br>68h: Bit [14:13] | **Deskew Mode Select for Port 01** Bit [9:8]: deskew mode select |
| | **78h (Port 1)**<br>78h: Bit [9:8]<br>78h: Bit [10] | **Scrambler Control for Port 1**<br>▪ Bit [11:10]: scrambler control<br>▪ Bit [12]: L0s |
| | **78h (Port 1)**<br>78h: Bit [13:12] | **Change_Speed_Sel for Port 1**<br>▪ Bit[ 14:13]: Change Speed select |
| | **78h (Port 1)**<br>78h: Bit [14] | **Change_Speed_En for Port 1**<br>▪ Bit [15]: Change Speed enable |
| 24h | **78h (Port 2)**<br>78h: Bit [7 :0] | **FTS Number for Port 2**<br>▪ Bit [7:0]: FTS number at receiver side |
| | **68h (Port 2)**<br>68h: Bit [14:13] | **Deskew Mode Select for Port 2**<br>▪ Bit [9:8]: deskew mode select |
| | **78h (Port 2)**<br>78h: Bit [9:8]<br>78h: Bit [10] | **Scrambler Control for Port 2**<br>▪ Bit [11:10]: scrambler control<br>▪ Bit [12]: L0s |
| | **78h (Port 2)**<br>78h: Bit [13:12] | **Change_Speed_Sel for Port 2**<br>▪ Bit [14:13]: Change Speed select |
| | **78h (Port 2)**<br>78h: Bit [14] | **Change_Speed_En for Port 2**<br>▪ Bit [15]: Change Speed enable |
| 30h | **7Ch (Port 0)**<br>7Ch: Bit [30 :16] | **PHY Parameter2_1 for Port 0**<br>▪ Bit [14:0]: PHY parameter 2 |
| 32h | **7Ch (Port 1)**<br>7Ch: Bit [30 :16] | **PHY Parameter2_1 for Port 1**<br>▪ Bit [14:0]: PHY parameter 2 |
| 34h | **7Ch (Port 2)**<br>7Ch: Bit [30 :16] | **PHY Parameter2_1 for Port 2**<br>▪ Bit [14:0]: PHY parameter 2 |
| 40h | **7Ch (Port 0)**<br>7Ch: Bit [12 :8] | **PHY Parameter 2_1 for Port 0**<br>▪ Bit [4:0]: PHY parameter 2 |
| | **90h (Port 0)**<br>90h: Bit [6 :0] | **PHY Parameter 3 for Port 0**<br>▪ Bit [11:5]: PHY parameter 3 |
| | **F0h (Port 0)**<br>F0h: Bit [6] | **Selectable De-emphasis for Port 0**<br>▪ Bit [12]: Selectable De-emphasis |
| | **78h (Port 0)**<br>78h: Bit [11] | **Compliance to Detect for Port 0**<br>▪ Bit [13]: compliance to detect |
| | **8Ch (Port 0)**<br>8Ch: Bit [9:8] | **DO_CHG_DATA_CNT_SEL for Port 0**<br>▪ Bit [15:14]: DO_CHG_DATA_CNT_SEL |
| 42h | **7Ch (Port 1)**<br>7Ch: Bit [12 :8]<br>90h (Port 1)<br>90h: Bit [6 :0] | **PHY Parameter 2_1 for Port 1**<br>▪ Bit [4:0]: PHY parameter 2<br>**PHY Parameter 3 for Port 1**<br>▪ Bit [11:5]: PHY parameter 3 |
| | **F0h (Port 0)**<br>F0h: Bit [6] | **Selectable De-emphasis for Port 1**<br>▪ Bit [12]: Selectable De-emphasis |
| | **78h (Port 1)**<br>78h: Bit [11] | **Compliance to Detect for Port 1**<br>▪ Bit [13]: compliance to detect |
| | **8Ch (Port 1)**<br>8Ch: Bit [9:8] | **DO_CHG_DATA_CNT_SEL for Port 1**<br>▪ Bit [15:14]: DO_CHG_DATA_CNT_SEL |
| 44h | **7Ch (Port 2)**<br>7Ch: Bit [12 :8] | **PHY Parameter 2_1 for Port 2**<br>▪ Bit [4:0]: PHY parameter 2 |


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| ADDRESS | PCI CFG OFFSET | DESCRIPTION |
|---|---|---|
| | **90h (Port 2)**<br>90h: Bit [6 :0] | **PHY Parameter 3 for Port 2**<br>▪ Bit [11:5]: PHY parameter 3 |
| | **F0h (Port 2)**<br>F0h: Bit [6] | **Selectable De-emphasis for Port 2**<br>▪ Bit [12]: Selectable De-emphasis |
| | **78h (Port 2)**<br>78h: Bit [11] | **Compliance to Detect for Port 2**<br>▪ Bit [13]: compliance to detect |
| | **8Ch (Port 2)**<br>8Ch: Bit [9:8] | **DO_CHG_DATA_CNT_SEL for Port 2**<br>▪ Bit [15:14]: DO_CHG_DATA_CNT_SEL |
| 50h | **44h (Port 0)**<br>44h: Bit [3] | **No_Soft_Reset for Port 0**<br>▪ Bit [0]: No_Soft_Reset. |
| | **40h (Port 0)**<br>40h: Bit [24:22]<br>40h: Bit [25]<br>40h: Bit [26]<br>40h: Bit [29:28] | **Power Management Capability for Port 0**<br>▪ Bit [3:1]: AUX Current.<br>▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state<br>▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state<br>▪ Bit [7:6]: PME Support for D2 and D1 states |
| 51h | **44h (Port 0)**<br>44h: Bit [31:24] | **Power Management Data for Port 0**<br>▪ Bit [15:8]: read only as Data register |
| 52h | **44h (Port 1)**<br>44h: Bit [3] | **No_Soft_Reset for Port 1**<br>▪ Bit [0]: No_Soft_Reset. |
| | **40h (Port 1)**<br>40h: Bit [24:22]<br>40h: Bit [25]<br>40h: Bit [26]<br>40h: Bit [29:28] | **Power Management Capability for Port 1**<br>▪ Bit [3:1]: AUX Current.<br>▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state<br>▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state<br>▪ Bit [7:6]: PME Support for D2 and D1 states |
| 53h | **44h (Port 1)**<br>44h: Bit [31:24] | **Power Management Data for Port 1**<br>▪ Bit [15:8]: read only as Data register |
| 54h | **44h (Port 2)**<br>44h: Bit [3] | **No_Soft_Reset for Port 2**<br>▪ Bit [0]: No_Soft_Reset |
| | **40h (Port 2)**<br>40h: Bit [24:22]<br>40h: Bit [25]<br>40h: Bit [26]<br>40h: Bit [29:28] | **Power Management Capability for Port 2**<br>▪ Bit [3:1]: AUX Current<br>▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state<br>▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state<br>▪ Bit [7:6]: PME Support for D2 and D1 states |
| 55h | **44h (Port 2)**<br>44h: Bit [31:24] | **Power Management Data for Port 2**<br>▪ Bit [15:8]: read only as Data register |
| 60h | **D0h (Port 0)**<br>D0h: Bit [28] | **Slot Clock Configuration for Port 0**<br>▪ Bit [1]: When set, the component uses the clock provided on the connector |
| | **40h (Port 0)**<br>40h: Bit[21] | **Device specific Initialization for Port 0**<br>▪ Bit [2]: When set, the DSI is required |
| | 144h (Port 0)<br>144h: Bit [4] | **LPVC Count for Port 0**<br>▪ Bit [3]: When set, the VC1 is allocated to LPVC of Egress Port 0 |
| | **CCh (Port 0)**<br>CCh: Bit [26:24] | **Port Number for Port 0**<br>▪ Bit [6:4]: It represents the logic port numbering for physical port 0 |
| | **154h (Port 0)**<br>154h: Bit [7:1] | **VC0 TC/VC Map for Port 0**<br>▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0 |


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| ADDRESS | PCI CFG OFFSET | DESCRIPTION |
|---|---|---|
| 62h | **C0h (Port 1)**<br>C0h: Bit [24] | **PCIe Capability Slot Implemented for Port 1**<br>▪ Bit [0]: When set, the slot is implemented for Port 1 |
| | **D0h (Port 1)**<br>D0h: Bit [28] | **Slot Clock Configuration for Port 1**<br>▪ Bit [1]: When set, the component uses the clock provided on the Connector |
| | **40h (Port 1)**<br>40h: Bit [21] | **Device specific Initialization for Port 1**<br>▪ Bit [2]: When set, the DSI is required |
| | **144h (Port 1)**<br>144h: Bit [4] | **LPVC Count for Port 1**<br>▪ Bit [3]: When set, the VC1 is allocated to LPVC of Egress Port 1 |
| | **CCh (Port 1)**<br>CCh: Bit [26:24] | **Port Number for Port 1**<br>▪ Bit [6:4]: It represents the logic port numbering for physical port 1 |
| | **154h (Port 1)**<br>154h: Bit [7:1] | **VC0 TC/VC Map for Port 1**<br>▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0 |
| 64h | **C0h (Port 2)**<br>C0h: Bit [24] | **PCIe Capability Slot Implemented for Port 2**<br>▪ Bit [0]: When set, the slot is implemented for Port 2 |
| | **D0h (Port 2)**<br>D0h: Bit [28] | **Slot Clock Configuration for Port 2**<br>▪ Bit [1]: When set, the component uses the clock provided on the Connector |
| | **40h (Port 2)**<br>40h: Bit [21] | **Device specific Initialization for Port 2**<br>▪ Bit [2]: When set, the DSI is required |
| | **144h (Port 2)**<br>144h: Bit [4] | **LPVC Count for Port 2**<br>▪ Bit [3]: When set, the VC1 is allocated to LPVC of Egress Port 2 |
| | **CCh (Port 2)**<br>CCh: Bit [26:24] | **Port Number for Port 2**<br>▪ Bit [6:4]: It represents the logic port numbering for physical port 2 |
| | **154h (Port 2)**<br>154h: Bit [7:1] | **VC0 TC/VC Map for Port 2**<br>▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0 |
| 70h | **214h (Port 0)**<br>214h: Bit [7:0]<br>214h: Bit [9:8]<br>214h: Bit [14:13]<br>218h: Bit [0] | **Power Budget Register for Port 0**<br>▪ Bit [7:0]: Base Power<br>▪ Bit [9:8]: Data Scale<br>▪ Bit [11:10]: PM State<br>▪ Bit [15]: System Allocated |
| 72h | **214h (Port 1)**<br>214h: Bit [7:0]<br>214h: Bit [9:8]<br>214h: Bit [14:13]<br>218h: Bit [0] | **Power Budget Register for Port 1**<br>▪ Bit [7:0]: Base Power<br>▪ Bit [9:8]: Data Scale<br>▪ Bit [11:10]: PM State<br>▪ Bit [15]: System Allocated |
| 74h | **214h (Port 2)**<br>214h: Bit [7:0]<br>214h: Bit [9:8]<br>214h: Bit [14:13]<br>218h: Bit [0] | **Power Budget Register for Port 2**<br>▪ Bit [7:0]: Base Power<br>▪ Bit [9:8]: Data Scale<br>▪ Bit [11:10]: PM State<br>▪ Bit [15]: System Allocated |
| 80h | **74h (Port 0)**<br>74h: Bit [13:8]<br><br><br>74h: Bit [14] | **PM Control Parameter for Port 0**<br>▪ Bit [1:0] : D3 enters L1<br>▪ Bit [3:2] : L1 delay count select<br>Bit [5:4] : L0s enable<br>▪ Bit [6] : Disable Rx polarity capability |
| | **70h (Port 0)**<br>70h: Bit [31] | **VGA Decode Enable for Port 0**<br>▪ Bit [7]: Enable VGA decode |
| | **88h (Port 0)**<br>88h: Bit [31:24] | **XPIP_CSR5[31:24] for Port 0**<br>Bit[15:8]: XPIP_CSR5[31:24] |


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| ADDRESS | PCI CFG OFFSET | DESCRIPTION |
|---|---|---|
| 82h | **74h (Port 1)**<br>74h: Bit [13:8]<br><br><br>74h: Bit [14]<br><br>**70h (Port 1)**<br>70h: Bit [31]<br><br>**88h (Port 1)**<br>88h: Bit [31:24] | **PM Control Parameter for Port 1**<br>▪ Bit [1:0] : D3 enters L1<br>▪ Bit [3:2] : L1 delay count select<br>Bit [5:4] : L0s enable<br>▪ Bit [6] : Disable Rx polarity capability<br><br>**VGA Decode Enable for Port 1**<br>▪ Bit [7]: Enable VGA decode<br><br>**XPIP_CSR5[31:24] for Port 1**<br>▪ Bit[15:8]: XPIP_CSR5[31:24] |
| 84h | **74h (Port 2)**<br>74h: Bit [13:8]<br><br><br>74h: Bit [14]<br><br>**70h (Port 2)**<br>70h: Bit [31]<br><br>**88h (Port 2)**<br>88h: Bit [31:24] | **PM Control Parameter for Port 2**<br>▪ Bit [1:0] : D3 enters L1<br>▪ Bit [3:2] : L1 delay count select<br>Bit [5:4] : L0s enable<br>▪ Bit [6] : Disable Rx polarity capability<br><br>**VGA Decode Enable for Port 2**<br>▪ Bit [7]: Enable VGA decode<br><br>**XPIP_CSR5[31:24] for Port 2**<br>▪ Bit[15:8]: XPIP_CSR5[31:24] |
| 92h | **D4h (Port 1)**<br>D4h: Bit [15:0] | **Slot Capability 0 of Port 1**<br>▪ Bit [15:0]: Mapping to the low word of slot capability register |
| 94h | **D4h (Port 2)**<br>D4h: Bit [15:0] | **Slot Capability 0 of Port 2**<br>▪ Bit [15:0]: Mapping to the low word of slot capability register |
| A2h | **D4h (Port 1)**<br>D4h: Bit [31:16] | **Slot Capability 1 of Port 1**<br>▪ Bit [15:0]: Mapping to the high word of slot capability register |
| A4h | **D4h (Port 2)**<br>D4h: Bit [31:16] | **Slot Capability 1 of Port 2**<br>▪ Bit [15:0]: Mapping to the high word of slot capability register |
| B0h | **80h (Port 0)**<br>80h: Bit [15:0] | **XPIP_CSR3_0 for Port 0**<br>▪ Bit [15:0]: XPIP_CSR3[15:0] |
| B2h | **80h (Port 1)**<br>80h: Bit [15:0] | **XPIP_CSR3_0 for Port 1**<br>▪ Bit [15:0]: XPIP_CSR3[15:0] |
| B4h | **80h (Port 2)**<br>80h: Bit [15:0] | **XPIP_CSR3_0 for Port 2**<br>▪ Bit [15:0]: XPIP_CSR3[15:0] |
| C0h | **80h (Port 0)**<br>80h: Bit [31:16] | **XPIP_CSR3_1 for Port 0**<br>▪ Bit [15:0]: XPIP_CSR3[31:16] |
| C2h | **80h (Port 1)**<br>80h: Bit [31:16] | **XPIP_CSR3_1 for Port 1**<br>▪ Bit [15:0]: XPIP_CSR3[31:16] |
| C4h | **80h (Port 2)**<br>80h: Bit [31:16] | **XPIP_CSR3_1 for Port 2**<br>▪ Bit [15:0]: XPIP_CSR3[31:16] |
| D0h | **70h (Port 0)**<br>70h: Bit [12:0]<br><br>**8Ch (Port 0)**<br>8Ch: Bit [25:24] | **Replay Time-out Counter for Port 0**<br>▪ Bit [12:0]: Relay Time-out Counter<br><br>**REV_TS_CTR for Port 0**<br>▪ Bit [14:13] REV_TS_CTR |
| D2h | **70h (Port 1)**<br>70h: Bit [12:0]<br><br>**8Ch (Port 1)**<br>8Ch: Bit [25:24] | **Replay Time-out Counter for Port 1**<br>▪ Bit [12:0]: Relay Time-out Counter<br><br>**REV_TS_CTR for Port 1**<br>▪ Bit [14:13] REV_TS_CTR |
| D4h | **70h (Port 2)**<br>70h: Bit [12:0]<br><br>**8Ch (Port 2)**<br>8Ch: Bit [25:24] | **Replay Time-out Counter for Port 2**<br>▪ Bit [12:0]: Relay Time-out Counter<br><br>**REV_TS_CTR for Port 2**<br>▪ Bit [14:13] REV_TS_CTR |
| E0h | **70h (Port 0)**<br>70h: Bit [30:16] | **Acknowledge Latency Timer for Port 0**<br>▪ Bit [30:16]: Acknowledge Latency Timer |
| E2h | **70h (Port 1)**<br>70h: Bit [30:16] | **Acknowledge Latency Timer for Port 1**<br>▪ Bit [30:16]: Acknowledge Latency Timer |
| E4h | **70h (Port 2)**<br>70h: Bit [30:16] | **Acknowledge Latency Timer for Port 2**<br>▪ Bit [30:16]: Acknowledge Latency Timer |


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| ADDRESS | PCI CFG OFFSET | DESCRIPTION |
|---|---|---|
| F0h | **15Ch (Port 0)**<br>15Ch: Bit [22:16]<br><br>**160h (Port 0)**<br>160h: Bit [7:0] | **VC1 MAX Time Slot and TC/VC Map for Port 0**<br>▪ Bit [6:0]: The maximum time slot supported by VC1<br><br>**TC/VC Map for Port 0**<br>▪ Bit [15:8]: When set, it indicates the corresponding TC is mapped into VC1 |
| F2h | **15Ch (Port 1)**<br>15Ch: Bit [22:16]<br><br>**160h (Port 1)**<br>160h: Bit [7:0] | **VC1 MAX Time Slot and TC/VC Map for Port 1**<br>▪ Bit [6:0]: The maximum time slot supported by VC1<br><br>**TC/VC Map for Port 1**<br>▪ Bit [15:8]: When set, it indicates the corresponding TC is mapped into VC1 |
| F4h | **15Ch (Port 2)**<br>15Ch: Bit [22:16]<br><br>**160h (Port 2)**<br>160h: Bit [7:0] | **VC1 MAX Time Slot and TC/VC Map for Port 2**<br>▪ Bit [6:0]: The maximum time slot supported by VC1<br><br>**TC/VC Map for Port 2**<br>▪ Bit [15:8]: When set, it indicates the corresponding TC is mapped into VC1 |


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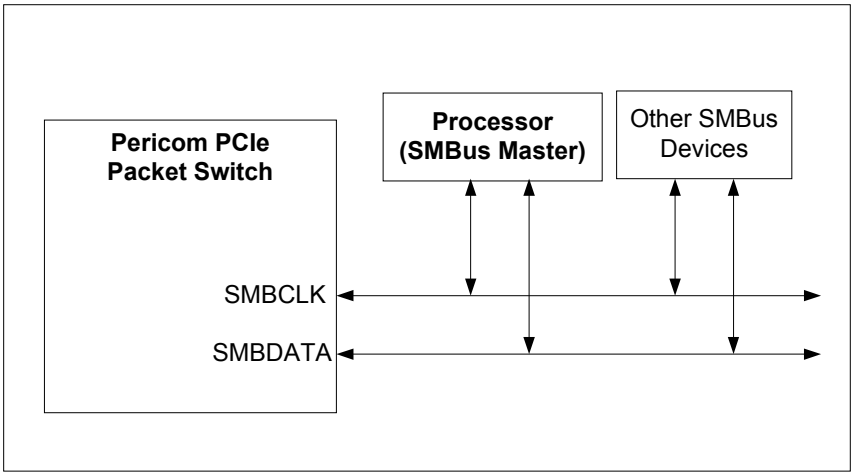
## 6.2 SMBus INTERFACE

The PI7C9X2G304EL provides the System Management Bus (SMBus), a two-wire interface through which a simple device can communicate with the rest of the system. The SMBus interface on the PI7C9X2G304EL is a bi-directional slave interface. It can receive data from the SMBus master or send data to the master. The interface allows full access to the configuration registers. A SMBus master, such as the processor or other SMBus devices, can read or write to every RW configuration register (read/write register). In addition, the RO and HwInt registers (read-only and hardware initialized registers) that can be auto-loaded by the EEPROM interface can also be read and written by the SMBus interface. This feature allows increases in the system expandability and flexibility in system implementation.

**Figure 6-1 SMBus Architecture Implementation on PI7C9X2G304EL**




The SMBus interface on the PI7C9X2G304EL consists of one SMBus clock pin (SMBCLK), a SMBus data pin (SMBDATA), and 3 SMBus address pins (GPIO[5:7]). The SMBus clock pin provides or receives the clock signal. The SMBus data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The SMBus address pins determine the address to which the PI7C9X2G304EL responds to. The SMBus address pins generate addresses according to the following table:

**Table 6-1 SMBus Address Pin Configuration**

| BIT | SMBus Address |
|---|---|
| 0 | GPIO[5] |
| 1 | GPIO[6] |
| 2 | GPIO[7] |
| 3 | 1 |
| 4 | 0 |
| 5 | 1 |
| 6 | 1 |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# 7 REGISTER DESCRIPTION

## 7.1 REGISTER TYPES

| REGISTER TYPE | DEFINITION |
|---|---|
| HwInt | Hardware Initialization |
| RO | Read Only |
| RW | Read / Write |
| RWC | Read / Write 1 to Clear |
| RWCS | Sticky – Read Only / Write 1 to Clear |
| RWS | Sticky – Read / Write |
| ROS | Sticky – Read Only |

## 7.2 TRANSPARENT MODE CONFIGURATION REGISTERS

When the port of the Switch is set to operate at the transparent mode, it is represented by a logical PCI-to-PCI Bridge that implements type 1 configuration space header. The following table details the allocation of the register fields of the PCI 2.3 compatible type 1 configuration space header.

| 31 –24 | 23 – 16 | 15 – 8 | 7 –0 | BYTE OFFSET |
|---|---|---|---|---|
| Device ID | | Vendor ID | | 00h |
| Primary Status | | Command | | 04h |
| Class Code | | | Revision ID | 08h |
| Reserved | Header Type | Primary Latency Timer | Cache Line Size | 0Ch |
| Reserved | | | | 10h – 17h |
| Secondary Latency Timer | Subordinate Bus Number | Secondary Bus Number | Primary Bus Number | 18h |
| Secondary Status | | I/O Limit Address | I/O Base Address | 1Ch |
| Memory Limit Address | | Memory Base Address | | 20h |
| Prefetchable Memory Limit Address | | Prefetchable Memory Base Address | | 24h |
| Prefetchable Memory Base Address Upper 32-bit | | | | 28h |
| Prefetchable Memory Limit Address Upper 32-bit | | | | 2Ch |
| I/O Limit Address Upper 16-bit | | I/O Base Address Upper 16-bit | | 30h |
| Reserved | | | Capability Pointer to 80h(40h) | 34h |
| Reserved | | | | 38h |
| Bridge Control | | Interrupt Pin | Interrupt Line | 3Ch |
| Power Management Capabilities | | Next Item Pointer=4C (5C) | Capability ID=01 | 40h |
| PM Data | PPB Support Extensions | Power Management Data | | 44h |
| Message Control | | Next Item Pointer=: 64 | Capability ID=05 | 4Ch |
| Message Address | | | | 50h |
| Message Upper Address | | | | 54h |
| Reserved | | Message Data | | 58h |
| VPD Register | | Next Item Pointer=64 | Capability ID=03 | 5Ch |
| VPD Data Register | | | | 60h |
| Length in Bytes (34h) | | Next Item Pointer=B0 | Capability ID=09 | 64h |
| XPIP_CSR0 | | | | 68h |
| XPIP_CSR1 | | | | 6Ch |
| ACK Latency Timer | | Replay Time-out Counter | | 70h |
| PHY Parameter 0 | | Switch Modes | | 74h |
| PHY Parameter 1 | | XPIP_CSR2 | | 78h |
| PHY Parameter 2 | | | | 7Ch |
| XPIP_CSR3 | | | | 80h |
| XPIP_CSR4 | | | | 84h |
| XPIP_CSR5 | | | | 88h |
| XPIP_CSR7 | XPIP_CSR6 | TL_CSR | | 8Ch |


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| 31 –24 | 23 – 16 | 15 – 8 | 7 –0 | BYTE OFFSET |
|---|---|---|---|---|
| PHY parameter 3 | | | | 90h |
| Reserved | PHYL1 RXEQ | PHY TX Margin parameter | | 94h |
| Reserved | Buffer Ctrl | OP Mode | | 98h |
| Reserved | | | | (9Ch – ACh) |
| Reserved | | Next Item Pointer=C0 | SSID/SSVID Capability ID=0D | B0h |
| SSID | | SSVID | | B4h |
| GPIO Data and Control | | | | B8h |
| EEPROM Data | | EEPROM Address | EEPROM Control | BCh |
| PCI Express Capabilities Register | | Next Item Pointer=00 | Capability ID=10 | C0h |
| Device Capabilities | | | | C4h |
| Device Status | | Device Control | | C8h |
| Link Capabilities | | | | CCh |
| Link Status | | Link Control | | D0h |
| Slot Capabilities | | | | D4h |
| Slot Status | | Slot Control | | D8h |
| Reserved | | | | DCh |
| Reserved | | | | E0h |
| Device Capabilities 2 | | | | E4h |
| Device Status / Control 2 | | | | E8h |
| Link Capabilities 2 | | | | ECh |
| Link Status /Control 2 | | | | F0h |
| Slot Capabilities 2 | | | | F4h |
| Slot Status /Control 2 | | | | F8h |
| Reserved | | | | FCh |

Other than the PCI 2.3 compatible configuration space header, the Switch also implements PCI express extended configuration space header, which includes advanced error reporting, virtual channel, and power budgeting capability registers. The following table details the allocation of the register fields of PCI express extended capability space header. The first extended capability always begins at offset 100h with a PCI Express Enhanced Capability header and the rest of capabilities are located at an offset greater than 0FFh relative to the beginning of PCI compatible configuration space.

| 31 –24 | 23 – 16 | 15 - 8 | 7 –0 | BYTE OFFSET |
|---|---|---|---|---|
| Next Capability Offset=140h | Cap. Version | PCI Express Extended Capability ID=0001h | | 100h |
| Uncorrectable Error Status Register | | | | 104h |
| Uncorrectable Error Mask Register | | | | 108h |
| Uncorrectable Error Severity Register | | | | 10Ch |
| Correctable Error Status Register | | | | 110h |
| Correctable Error Mask Register | | | | 114h |
| Advanced Error Capabilities and Control Register | | | | 118h |
| Header Log Register | | | | 11Ch – 128h |
| Reserved | | | | 12Ch – 13Fh |
| Next Capability Offset=20Ch | Cap. Version | PCI Express Extended Capability ID=0002h | | 140h |
| Port VC Capability Register 1 | | | | 144h |
| VC Arbitration Table Offset=3 | Port VC Capability Register 2 | | | 148h |
| Port VC Status Register | | Port VC Control Register | | 14Ch |
| Port Arbitration Table Offset=4 | VC Resource Capability Register (0) | | | 150h |
| VC Resource Control Register (0) | | | | 154h |
| VC Resource Status Register (0) | | Reserved | | 158h |
| Port Arbitration Table Offset=6 | VC Resource Capability Register (1) | | | 15Ch |
| VC Resource Control Register (1) | | | | 160h |
| VC Resource Status Register (1) | | Reserved | | 164h |
| Reserved | | | | 16Ch – 168h |
| VC Arbitration Table with 32 Phases | | | | 170h – 17Ch |
| Port Arbitration Table with 128 Phases for VC0 | | | | 180h – 1BCh |
| Port Arbitration Table with 128 Phases for VC1 | | | | 1C0h – 1FCh |
| Reserved | | | | 200h – 20Bh |


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| 31 –24 | 23 – 16 | 15 - 8 | 7 –0 | BYTE OFFSET |
|---|---|---|---|---|
| Next Capability Offset=220/230h | Cap. Version | PCI Express Extended Capability ID=0004h | | 20Ch |
| Reserved | | | Data Select Register | 210h |
| Data Register | | | | 214h |
| Reserved | | | Power Budget Capability Register | 218h |
| Reserved | | | | 21Ch |
| Next Capability Offset=000h | Cap version | PCI Express Extended Capability ID=000Dh | | 220h |
| ACS Control | | ACS Capability | | 224h |
| Reserved | | | Egress Control Vector | 228h |
| Reserved | | | | 22Ch |
| Next Capability Offset=000h | Cap version | PCI Express Extended Capability ID=0018h | | 230h |

| Reserved | Max No-Snoop Latency Scale | Max No-Snoop Latency Value | Reserved | Max Snoop Latency Scale | Max Snoop Latency Value | 234h |
|---|---|---|---|---|---|---|

## 7.2.1 VENDOR ID REGISTER – OFFSET 00h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | Vendor ID | RO | Identifies Pericom as the vendor of this device. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 12D8h. |

## 7.2.2 DEVICE ID REGISTER – OFFSET 00h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:16 | Device ID | RO | Identifies this device as the PI7C9X2G303EL. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Resets to 2304h. |

## 7.2.3 COMMAND REGISTER – OFFSET 04h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | I/O Space Enable | RW | 0b: Ignores I/O transactions on the primary interface<br>1b: Enables responses to I/O transactions on the primary interface<br><br>Resets to 0b. |
| 1 | Memory Space Enable | RW | 0b: Ignores memory transactions on the primary interface<br>1b: Enables responses to memory transactions on the primary interface<br><br>Reset to 0b. |
| 2 | Bus Master Enable | RW | 0b: Does not initiate memory or I/O transactions on the upstream port and handles as an Unsupported Request (UR) to memory and I/O transactions on the downstream port. For Non-Posted Requests, a completion with UR completion status must be returned<br>1b: Enables the Switch Port to forward memory and I/O Read/Write transactions in the upstream direction<br><br>Reset to 0b. |
| 3 | Special Cycle Enable | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 4 | Memory Write And Invalidate Enable | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 5 | VGA Palette Snoop Enable | RO | Does not apply to PCI Express. Must be hardwired to 0b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 6 | Parity Error Response Enable | RW | 0b: Switch may ignore any parity errors that it detects and continue normal operation<br>1b: Switch must take its normal action when a parity error is detected<br><br>Reset to 0b. |
| 7 | Wait Cycle Control | RO | Does not apply to PCI Express. Must be hardwired to 0. |
| 8 | SERR# enable | RW | 0b: Disables the reporting of Non-fatal and Fatal errors detected by the Switch to the Root Complex<br>b1: Enables the Non-fatal and Fatal error reporting to Root Complex<br><br>Reset to 0b. |
| 9 | Fast Back-to-Back Enable | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 10 | Interrupt Disable | RW | Controls the ability of a PCI Express device to generate INTx Interrupt Messages. In the Switch, this bit does not affect the forwarding of INTx messages from the downstream ports.<br><br>Reset to 0b. |
| 15:11 | Reserved | RsvdP | Not Support. |

## 7.2.4 PRIMARY STATUS REGISTER – OFFSET 04h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 18:16 | Reserved | RsvdP | Not Support. |
| 19 | Interrupt Status | RO | Indicates that an INTx Interrupt Message is pending internally to the device. In the Switch, the forwarding of INTx messages from the downstream device of the Switch port is not reflected in this bit. Must be hardwired to 0b. |
| 20 | Capabilities List | RO | Set to 1 to enable support for the capability list (offset 34h is the pointer to the data structure).<br><br>Reset to 1b. |
| 21 | 66MHz Capable | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 22 | Reserved | RsvdP | Not Support. |
| 23 | Fast Back-to-Back Capable | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 24 | Master Data Parity Error | RWC | Set to 1 (by a requester) whenever a Parity error is detected or forwarded on the primary side of the port in a Switch.<br><br>If the Parity Error Response Enable bit is cleared, this bit is never set.<br><br>Reset to 0b. |
| 26:25 | DEVSEL# timing | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 27 | Signaled Target Abort | RO | Set to 1 (by a completer) whenever completing a request on the primary side using the Completer Abort Completion Status.<br><br>Reset to 0b. |
| 28 | Received Target Abort | RO | Set to 1 (by a requestor) whenever receiving a Completion with Completer Abort Completion Status on the primary side.<br><br>Reset to 0b. |
| 29 | Received Master Abort | RO | Set to 1 (by a requestor) whenever receiving a Completion with Unsupported Request Completion Status on primary side.<br><br>Reset to 0b. |
| 30 | Signaled System Error | RWC | Set to 1 when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1.<br><br>Reset to 0b. |
| 31 | Detected Parity Error | RWC | Set to 1 whenever the primary side of the port in a Switch receives a Poisoned TLP.<br><br>Reset to 0b. |


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### 7.2.5 REVISION ID REGISTER – OFFSET 08h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Revision | RO | Indicates revision number of device. Hardwired to 05h. |

### 7.2.6 CLASS CODE REGISTER – OFFSET 08h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:8 | Programming Interface | RO | Read as 00h to indicate no programming interfaces have been defined for PCI-to-PCI Bridges. |
| 23:16 | Sub-Class Code | RO | Read as 04h to indicate device is a PCI-to-PCI Bridge. |
| 31:24 | Base Class Code | RO | Read as 06h to indicate device is a Bridge device. |

### 7.2.7 CACHE LINE REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Cache Line Size | RW | The cache line size register is set by the system firmware and the operating system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility, but it has no impact on any PCI Express device functionality.<br><br>Reset to 00h. |

### 7.2.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:8 | Primary Latency timer | RO | Does not apply to PCI Express. Must be hardwired to 00h. |

### 7.2.9 HEADER TYPE REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 23:16 | Header Type | RO | Read as 01h to indicate that the register layout conforms to the standard PCI-to-PCI Bridge layout. |

### 7.2.10 PRIMARY BUS NUMBER REGISTER – OFFSET 18h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Primary Bus Number | RW | Indicates the number of the PCI bus to which the primary interface is connected. The value is set in software during configuration.<br><br>Reset to 00h. |

### 7.2.11 SECONDARY BUS NUMBER REGISTER – OFFSET 18h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:8 | Secondary Bus Number | RW | Indicates the number of the PCI bus to which the secondary interface is connected. The value is set in software during configuration.<br><br>Reset to 00h. |


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### 7.2.12 SUBORDINATE BUS NUMBER REGISTER – OFFSET 18h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 23:16 | Subordinate Bus Number | RW | Indicates the number of the PCI bus with the highest number that is subordinate to the Bridge. The value is set in software during configuration.<br><br>Reset to 00h. |

### 7.2.13 SECONDARY LATENCY TIMER REGISTER – OFFSET 18h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:24 | Secondary Latency Timer | RO | Does not apply to PCI Express. Must be hardwired to 00h. |

### 7.2.14 I/O BASE ADDRESS REGISTER – OFFSET 1Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 3:0 | 32-bit Indicator | RO | Read as 01h to indicate 32-bit I/O addressing. |
| 7:4 | I/O Base Address [15:12] | RW | Defines the bottom address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be 0. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O base address upper 16 bits address register.<br><br>Reset to 0h. |

### 7.2.15 I/O LIMIT ADDRESS REGISTER – OFFSET 1Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 11:8 | 32-bit Indicator | RO | Read as 01h to indicate 32-bit I/O addressing. |
| 15:12 | I/O Limit Address [15:12] | RW | Defines the top address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be FFFh. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O limit address upper 16 bits address register.<br><br>Reset to 0h. |

### 7.2.16 SECONDARY STATUS REGISTER – OFFSET 1Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 20:16 | Reserved | RsvdP | Not Support. |
| 21 | 66MHz Capable | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 22 | Reserved | RsvdP | Not Support. |
| 23 | Fast Back-to-Back Capable | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 24 | Master Data Parity Error | RWC | Set to 1 (by a requester) whenever a Parity error is detected or forwarded on the secondary side of the port in a Switch.<br><br>If the Parity Error Response Enable bit is cleared, this bit is never set.<br><br>Reset to 0b. |
| 26:25 | DEVSEL_L timing | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 27 | Signaled Target | RO | Set to 1 (by a completer) whenever completing a request in the secondary |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| | Abort | | side using Completer Abort Completion Status.<br><br>Reset to 0b. |
| 28 | Received Target Abort | RO | Set to 1 (by a requestor) whenever receiving a Completion with Completer Abort Completion Status in the secondary side.<br><br>Reset to 0b. |
| 29 | Received Master Abort | RO | Set to 1 (by a requestor) whenever receiving a Completion with Unsupported Request Completion Status in secondary side.<br><br>Reset to 0b. |
| 30 | Received System Error | RWC | Set to 1 when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Bridge Control register is 1.<br><br>Reset to 0b. |
| 31 | Detected Parity Error | RWC | Set to 1 whenever the secondary side of the port in a Switch receives a Poisoned TLP.<br><br>Reset to 0b. |

## 7.2.17 MEMORY BASE ADDRESS REGISTER – OFFSET 20h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 3:0 | Reserved | RsvdP | Not Support. |
| 15:4 | Memory Base Address [15:4] | RW | Defines the bottom address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are able to be written to. The lower 20 bits corresponding to address bits [19:0] are assumed to be 0.<br><br>Reset to 000h. |

## 7.2.18 MEMORY LIMIT ADDRESS REGISTER – OFFSET 20h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 19:16 | Reserved | RsvdP | Not Support. |
| 31:20 | Memory Limit Address [31:20] | RW | Defines the top address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits corresponding to address bits [19:0] are assumed to be FFFFFh.<br><br>Reset to 000h. |

## 7.2.19 PREFETCHABLE MEMORY BASE ADDRESS REGISTER – OFFSET 24h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 3:0 | 64-bit addressing | RO | Read as 0001b to indicate 64-bit addressing. |
| 15:4 | Prefetchable Memory Base Address [31:20] | RW | Defines the bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be 0. The memory base register upper 32 bits contain the upper half of the base address.<br><br>Reset to 000h. |


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### 7.2.20 PREFETCHABLE MEMORY LIMIT ADDRESS REGISTER – OFFSET 24h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 19:16 | 64-bit addressing | RO | Read as 0001b to indicate 64-bit addressing. |
| 31:20 | Prefetchable Memory Limit Address [31:20] | RW | Defines the top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be FFFFFh. The memory limit upper 32 bits register contains the upper half of the limit address.<br><br>Reset to 000h. |

### 7.2.21 PREFETCHABLE MEMORY BASE ADDRESS UPPER 32-BITS REGISTER – OFFSET 28h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:0 | Prefetchable Memory Base Address, Upper 32-bits [63:32] | RW | Defines the upper 32-bits of a 64-bit bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other.<br><br>Reset to 0000_0000h. |

### 7.2.22 PREFETCHABLE MEMORY LIMIT ADDRESS UPPER 32-BITS REGISTER – OFFSET 2Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:0 | Prefetchable Memory Limit Address, Upper 32-bits [63:32] | RW | Defines the upper 32-bits of a 64-bit top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other.<br><br>Reset to 0000_0000h. |

### 7.2.23 I/O BASE ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | I/O Base Address, Upper 16-bits [31:16] | RW | Defines the upper 16-bits of a 32-bit bottom address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other.<br><br>Reset to 0000h. |

### 7.2.24 I/O LIMIT ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:16 | I/O Limit Address, Upper 16-bits [31:16] | RW | Defines the upper 16-bits of a 32-bit top address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other.<br><br>Reset to 0000h. |


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### 7.2.25 CAPABILITY POINTER REGISTER – OFFSET 34h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Capability Pointer | RO | Pointer points to the PCI power management registers.<br><br>Reset to 40h. |

### 7.2.26 INTERRUPT LINE REGISTER – OFFSET 3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Interrupt Line | RW | Reset to 00h. |

### 7.2.27 INTERRUPT PIN REGISTER – OFFSET 3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:8 | Interrupt Pin | RO | The Switch implements INTA virtual wire interrupt signals to represent hot-plug events at downstream ports. The default value on the downstream ports may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 00h. |

### 7.2.28 BRIDGE CONTROL REGISTER – OFFSET 3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 16 | Parity Error Response | RW | 0b: Ignore Poisoned TLPs on the secondary interface<br>1b: Enable the Poisoned TLPs reporting and detection on the secondary interface<br><br>Reset to 0b. |
| 17 | S_SERR# enable | RW | 0b: Disables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface<br>1b: Enables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface<br><br>Reset to 0b. |
| 18 | ISA Enable | RW | 0b: Forwards downstream all I/O addresses in the address range defined by the I/O Base, I/O Base, and Limit registers<br>1b: Forwards upstream all I/O addresses in the address range defined by the I/O Base and Limit registers that are in the first 64KB of PCI I/O address space (top 768 bytes of each 1KB block)<br><br>Reset to 0b. |
| 19 | VGA Enable | RW | 0b: Ignores access to the VGA memory or IO address range<br>1b: Forwards transactions targeted at the VGA memory or IO address range<br><br>VGA memory range starts from 000A 0000h to 000B FFFFh<br>VGA IO addresses are in the first 64KB of IO address space.<br>AD [9:0] is in the ranges 3B0 to 3BBh and 3C0h to 3DFh.<br><br>Reset to 0b. |
| 20 | VGA 16-bit decode | RW | 0b: Executes 10-bit address decoding on VGA I/O accesses<br>1b: Executes 16-bit address decoding on VGA I/O accesses<br><br>Reset to 0b. |
| 21 | Master Abort Mode | RO | Does not apply to PCI Express. Must be hardwired to 0b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 22 | Secondary Bus Reset | RW | 0b: Does not trigger a hot reset on the corresponding PCI Express Port<br>1b: Triggers a hot reset on the corresponding PCI Express Port<br>At the downstream port, it asserts PORT_RST# to the attached downstream device.<br>At the upstream port, it asserts the PORT_RST # at all the downstream ports.<br><br>Reset to 0b. |
| 23 | Fast Back-to-Back Enable | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 24 | Primary Master Timeout | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 25 | Secondary Master Timeout | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 26 | Master Timeout Status | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 27 | Discard Timer SERR# enable | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 31:28 | Reserved | RsvdP | Not Support. |

## 7.2.29 POWER MANAGEMENT CAPABILITY REGISTER – OFFSET 40h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Enhanced Capabilities ID | RO | Read as 01h to indicate that these are power management enhanced capability registers. |
| 15:8 | Next Item Pointer | RO | The pointer points to the Vital Protocol Data (VPD) capability register/the Message capability register.<br><br>Reset to 5Ch (Upstream port).<br>Reset to 4Ch (Downstream ports). |
| 18:16 | Power Management Revision | RO | Read as 011b to indicate the device is compliant to Revision 1.2 of *PCI Power Management Interface Specifications*. |
| 19 | PME# Clock | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 20 | Reserved | RsvdP | Not Support. |
| 21 | Device Specific Initialization | RO | Read as 0b to indicate Switch does not have device specific initialization requirements. The default value may be changed by SMBus or auto-loading from EEPROM. |
| 24:22 | AUX Current | RO | Reset as 111b to indicate the Switch needs 375 mA in D3 state. The default value may be changed by SMBus or auto-loading from EEPROM. |
| 25 | D1 Power State Support | RO | Read as 1b to indicate Switch supports the D1 power management state. The default value may be changed by SMBus or auto-loading from EEPROM. |
| 26 | D2 Power State Support | RO | Read as 1b to indicate Switch supports the D2 power management state. The default value may be changed by SMBus or auto-loading from EEPROM. |
| 31:27 | PME# Support | RO | Read as 11111b to indicate Switch supports the forwarding of PME# message in all power states. The default value may be changed by SMBus or auto-loading from EEPROM. |

## 7.2.30 POWER MANAGEMENT DATA REGISTER – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 1:0 | Power State | RW | Indicates the current power state of the Switch. Writing a value of D0 when the previous state was D3 cause a hot reset without asserting DWNRST_L.<br><br>00b: D0 state<br>01b: D1 state<br>10b: D2 state<br>11b: D3 hot state<br><br>Reset to 00b. |
| 2 | Reserved | RsvdP | Not Support. |
| 3 | No_Soft_Reset | RO | When set, this bit indicates that device transitioning from D3hot to D0 does |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| | | | not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. This bit can be rewritten with EEPROM programming. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 1b. |
| 7:4 | Reserved | RsvdP | Not Support. |
| 8 | PME# Enable | RWS | When asserted, the Switch will generate the PME# message.<br><br>Reset to 0b. |
| 12:9 | Data Select | RW | Select data registers.<br><br>Reset to 0h. |
| 14:13 | Data Scale | RO | Reset to 00b. |
| 15 | PME status | ROS | Read as 0b as the PME# message is not implemented.<br><br>Reset to 0b. |

## 7.2.31 PPB SUPPORT EXTENSIONS – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 21:16 | Reserved | RsvdP | Not Support. |
| 22 | B2_B3 Support for $D3_{HOT}$ | RO | Does not apply to PCI Express. Must be hardwired to 0b. |
| 23 | Bus Power / Clock Control Enable | RO | Does not apply to PCI Express. Must be hardwired to 0b. |

## 7.2.32 DATA REGISTER – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:24 | Data Register | RO | Data Register. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 00h. |

## 7.2.33 MSI CAPABILITY REGISTER – OFFSET 4Ch (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Enhanced Capabilities ID | RO | Read as 05h to indicate that this is message signal interrupt capability register. |
| 15:8 | Next Item Pointer | RO | Pointer points to the Vendor specific capability register.<br><br>Reset to 64h. |

## 7.2.34 MESSAGE CONTROL REGISTER – OFFSET 4Ch (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 16 | MSI Enable | RW | 0b: The function is prohibited from using MSI to request service<br>1b: The function is permitted to use MSI to request service and is prohibited from using its INTx# pin<br><br>Reset to 0b. |
| 19:17 | Multiple Message Capable | RO | Read as 000b. |
| 22:20 | Multiple Message Enable | RW | Reset to 000b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 23 | 64-bit address capable | RO | 0b: The function is not capable of generating a 64-bit message address<br>1b: The function is capable of generating a 64-bit message address<br><br>Reset to 1b. |
| 31:24 | Reserved | RsvdP | Not Support. |

## 7.2.35 MESSAGE ADDRESS REGISTER – OFFSET 50h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 1:0 | Reserved | RsvdP | Not Support. |
| 31:2 | Message Address | RW | If the message enable bit is set, the contents of this register specify the DWORD aligned address for MSI memory write transaction.<br><br>Reset to 0000_0000h. |

## 7.2.36 MESSAGE UPPER ADDRESS REGISTER – OFFSET 54h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:0 | Message Upper Address | RW | This register is only effective if the device supports a 64-bit message address is set.<br><br>Reset to 0000_0000h. |

## 7.2.37 MESSAGE DATA REGISTER – OFFSET 58h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | Message Data | RW | Reset to 0000h. |
| 31:16 | Reserved | RsvdP | Not Support. |

## 7.2.38 VPD CAPABILITY REGISTER – OFFSET 5Ch (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Enhanced Capabilities ID | RO | Read as 03h to indicate that these are VPD enhanced capability registers. |
| 15:8 | Next Item Pointer | RO | Pointer points to the Vendor specific capability register.<br><br>Reset to 64h. |

## 7.2.39 VPD REGISTER – OFFSET 5Ch (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 17:16 | Reserved | RsvdP | Not Support. |
| 23:18 | VPD Address | RW | Contains DWORD address that is used to generate read or write cycle to the VPD table stored in EEPROM.<br><br>Reset to 00_0000b. |
| 30:24 | Reserved | RsvdP | Not Support. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31 | VPD operation | RW | 0b: Performs VPD read command to VPD table at the location as specified in VPD address. This bit is kept '0' and then set to '1' automatically after EEPROM cycle is finished<br>1b: Performs VPD write command to VPD table at the location as specified in VPD address. This bit is kept '1' and then set to '0' automatically after EEPROM cycle is finished.<br><br>Reset to 0b. |

## 7.2.40 VPD DATA REGISTER – OFFSET 60h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:0 | VPD Data | RW | When read, it returns the last data read from VPD table at the location as specified in VPD Address.<br><br>When written, it places the current data into VPD table at the location as specified in VPD Address.<br><br>Reset to 0000_0000h. |

## 7.2.41 VENDOR SPECIFIC CAPABILITY REGISTER – OFFSET 64h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Enhanced Capabilities ID | RO | Read as 09h to indicate that these are vendor specific capability registers. |
| 15:8 | Next Item Pointer | RO | Pointer points to the SSID/SSVID capability register.<br><br>Reset to B0h. |
| 31:16 | Length Information | RO | The length field provides the information for number of bytes in the capability structure (including the ID and Next pointer bytes).<br><br>Reset to 0034h. |

## 7.2.42 XPIP CSR0 – OFFSET 68h (Test Purpose Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:0 | XPIP_CSR0 | RW | Reset to 0400_1060h. |

## 7.2.43 XPIP CSR1 – OFFSET 6Ch (Test Purpose Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:0 | XPIP_CSR1 | RW | Reset to 0400_0800h. |

## 7.2.44 REPLAY TIME-OUT COUNTER – OFFSET 70h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 11:0 | User Replay Timer | RW | A 12-bit register contains a user-defined value. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 000h. |
| 12 | Enable User Replay Timer | RW | When asserted, the user-defined replay time-out value is be employed. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 13 | Power Management Capability Disable | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 14 | MSI Capability Disable | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 15 | Reserved | RsvdP | Not Support. |

## 7.2.45 ACKNOWLEDGE LATENCY TIMER – OFFSET 70h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 29:16 | User ACK Latency Timer | RW | A 14-bit register contains a user-defined value. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0000h. |
| 30 | Enable User ACK Latency | RW | When asserted, the user-defined ACK latency value is be employed. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 31 | VGA decode enable | RO | Enable the VGA range decode.<br><br>Reset to 1b. |

## 7.2.46 SWITCH OPERATION MODE – OFFSET 74h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | Store-Forward | RW | When set, a store-forward mode is used. Otherwise, the chip is working under cut-through mode. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 2:1 | Cut-through Threshold | RW | Cut-through Threshold. When forwarding a packet from low-speed port to high-speed mode, the chip provides the capability to adjust the forwarding threshold. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>00b: the threshold is set at the middle of forwarding packet<br>01b: the threshold is set ahead 1-cycle of middle point<br>10b: the threshold is set ahead 2-cycle of middle point<br>11b: the threshold is set ahead 3-cycle of middle point<br><br>Reset to 01b. |
| 3 | Port Arbitration Mode | RW | When set, the round-robin arbitration will stay in the arbitrated port even if the credit is not enough but request is pending.<br>When clear, the round-robin arbitration will always go to the requesting port, which the outgoing credit is enough for the packet queued in the port.<br>The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 4 | Credit Update Mode | RW | When set, the frequency of releasing new credit to the link partner will be all types per update.<br>When clear, the frequency of releasing new credit to the link partner will be type oriented per update.<br><br>The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 5 | Ordering on Different Egress Port Mode | RW | When set, there has ordering rule on packets for different egress port. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 6 | Ordering on Different Tag of Completion Mode | RW | When set, there has ordering rule between completion packet with different tag. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 7 | Reserved | RsvdP | Not Support. |
| 13:8 | Power management Control parameter | RW | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 00_0001b. |
| 14 | RX Polarity Inversion Disable | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 15 | Compliance pattern Parity Control Disable | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 20:16 | C_DRV_LVL_3P5_NOM | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 1_0011b. |
| 25:21 | C_DRV_LVL_6P0_NOM | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 1_0011b. |
| 30:26 | C_DRV_LVL_HALF_NOM | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0_0010b. |
| 31 | Reserved | RsvdP | Not Support. |

## 7.2.47 SWITCH OPERATION MODE – OFFSET 74h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Reserved | RsvdP | Not Support. |
| 13:8 | Power Management Control Parameter | RW | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 00_0001b. |
| 14 | RX Polarity Inversion Disable | HwInt RO | The default value may be changed by the status of strapped pin, SMBus or auto-loading from EEPROM.<br><br>Reset to the status of RXPOLINV_DIS strapped pin. |
| 15 | Compliance Pattern Parity Control Disable | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 20:16 | C_DRV_LVL_3P5_NOM | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 1_0011b. |
| 25:21 | C_DRV_LVL_6P0_NOM | RO | .The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 1_0011b. |
| 30:26 | C_DRV_LVL_6P0_NOM | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0_0010b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31 | Reserved | RsvdP | Not Support. |

## 7.2.48 XPIP_CSR2 – OFFSET 78h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | XPIP_CSR2 | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0080h. |

## 7.2.49 PHY PARAMETER 1 – OFFSET 78h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 20:16 | C_EMP_POST_ GEN1_3P5_NOM | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 1_0101b. |
| 25:21 | C_EMP_POST_ GEN2_3P5_NOM | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 1_0101b. |
| 30:26 | C_EMP_POST_ GEN2_6P0_NOM | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 1_1101b. |
| 31 | Reserved | RsvdP | Not Support. |

## 7.2.50 PHY PARAMETER 2 – OFFSET 7Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 3:0 | C_TX_PHY_ LATENCY | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0111b. |
| 6:4 | C_REC_DETECT_ USEC | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 010b. |
| 7 | Reserved | RsvdP | Not Support. |
| 8 | P_CDR_FREQLOOP _EN | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 1b. |
| 10:9 | P_CDR_ THRESHOLD | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 10b. |
| 12:11 | P_CDR_FREQLOOP _GAIN | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 11b. |
| 15:13 | Reserved | RsvdP | Not Support. |
| 16 | P_DRV_LVL_MGN_ DELATA_EN | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 17 | P_DRV_LVL_NOM_DELATA_EN | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 18 | P_EMP_POST_MGN_DELATA_EN | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 19 | P_EMP_POST_NOM_DELATA_EN | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 21:20 | P_RX_SIGDET_LVL | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 01b. |
| 25:22 | P_RX_EQ_1 | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0110b. |
| 29:26 | P_RX_EQ_2 | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 1000b. |
| 30 | P_TXSWING | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 31 | Reserved | RsvdP | Not Support. |

### 7.2.51 XPIP_CSR3 – OFFSET 80h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:0 | XPIP_CSR3 | RW | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 000F_0000h. |

### 7.2.52 XPIP_CSR4 – OFFSET 84h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:0 | XPIP_CSR4 | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0000_0000h. |

### 7.2.53 XPIP_CSR5 – OFFSET 88h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 29:0 | XPIP_CSR5 | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 7308_3333h (Upstream port).<br>Reset to 3308_3333h (Downstream ports). |
| 30 | DO_CHG_DATA_RATE_CTRL | RO | The default value may be changed by SMBus, I2C or auto-loading from EEPROM.<br><br>Reset to 1b (Upstream port).<br>Reset to 0b (Downstream ports). |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31 | Gen1_Cap_Only | RO | The default value may be changed by SMBus, I2C or auto-loading from EEPROM.<br><br>Reset to 0b. |

## 7.2.54 TL_CSR – OFFSET 8Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | TX_SOF_FORM | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 1 | PM Data Select Register R/W Capability | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 2 | FC_UPDATE_MODE | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 3 | 4K Boundary Check Enable | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 4 | FIFOERR_FIX_SEL | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 1b. |
| 5 | MW Overpass Disable | RW | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 6 | Ordering Frozen Disable | RW | Disable the RO ordering rule.<br>The default value may be changed by SMBus or auto-loading from EEPROM<br><br>Reset to 0b. |
| 7 | GNT_FAIL2IDLE | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 9:8 | DO_CHG_DATA_CNT_SEL | RO | The trying number for doing change data rate. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 00b. |
| 10 | Port Disable | RO | Disable this port. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 11 | Reset Select | RO | Reset select (upstream port only). The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 12 | ARB_VCFLG_SEL | RO | Reset to 0b. |
| 15:13 | Reserved | RsvdP | Not Support. |
| 23:16 | XPIP_CSR6 | RO | XPIP_CSR6 Value. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 79h. |
| 25:24 | REV_TS_CTR | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 00b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 29:26 | MAC Control Parameter | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0h. |
| 30 | Reserved | RsvdP | Not Support. |
| 31 | P35_GEN2_MODE | RO | The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |

## 7.2.55 PHY PARAMETER 3 – OFFSET 90h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 6:0 | PHY Parameter3 (per lane) | RO | PHY's Lane mode.<br><br>Reset to 00h. |
| 14:7 | Reserved | RsvdP | Not Support. |
| 31:15 | PHY Parameter3 (global) | RO | PHY's delta value setting.<br><br>Reset to 0_0001h. |

## 7.2.56 PHY PARAMETER 4 - OFFSET 94h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | PHY TX Margin | RO | Reset to 116Bh. |
| 23:16 | Multilane RXEQ | RO | Upstream Port only. Reset to 86h.<br>Reserved for Downstream Port. Reset to 00h. |
| 31:24 | Reserved | RsvdP | Not Support. |

## 7.2.57 OPERATION MODE –OFFSET 98h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | Operation mode | RO | { 7'd0, SCAN_MODE, PKG_SEL[2:0], PHY_MODE, DEBUG_MODE, FAST_MODE, IDDQB, SROM_BYPASS} |
| 20:16 | Clock buffer control | HwInt RO | For Reference clock buffer control. The default value may be changed by the status of strapped pin, SMBus or auto-loading from EEPROM.<br><br>Bit[20]: Reset to the status of CLKBUF_PD strapped pin.<br>Bit[19:16]: Reset to Fh.<br><br>Bit[20]: enable or disable reference clock outputs<br>0b: enable reference clock outputs<br>1b: disable reference clock outputs<br>Bit[19]: reserved<br>Bit[18:16]: enable or disable REFCLKO_P/N[2:0]<br>0b: disable<br>1b: enable |
| 31:21 | Reserved | RsvdP | Not Support. |

## 7.2.58 SSID/SSVID CAPABILITY REGISTER – OFFSET B0h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | SSID/SSVID Capabilities ID | RO | Read as 0Dh to indicate that these are SSID/SSVID capability registers. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:8 | Next Item Pointer | RO | Pointer points to the PCI Express capability register.<br><br>Reset to C0h. |

## 7.2.59 SUBSYSTEM VENDOR ID REGISTER – OFFSET B4h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | SSVID | RO | It indicates the sub-system vendor id. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0000h. |

## 7.2.60 SUBSYSTEM ID REGISTER – OFFSET B4h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:16 | SSID | RO | It indicates the sub-system device id. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0000h. |

## 7.2.61 GPIO CONTROL REGISTER – OFFSET B8h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | GPIO [0] Input | RO | State of GPIO [0] pin |
| 1 | GPIO [0] Output Enable | RW | 0b: GPIO [0] is an input pin<br>1b: GPIO [0] is an output pin<br><br>Reset to 0b. |
| 2 | GPIO [0] Output Register | RW | Value of this bit will be output to GPIO [0] pin if GPIO [0] is configured as an output pin.<br><br>Reset to 0b. |
| 3 | Reserved | RsvdP | Not Support. |
| 4 | GPIO [1] Input | RO | State of GPIO [1] pin. |
| 5 | GPIO [1] Output Enable | RW | 0b: GPIO [1] is an input pin<br>1b: GPIO [1] is an output pin<br><br>Reset to 0b. |
| 6 | GPIO [1] Output Register | RW | Value of this bit will be output to GPIO [1] pin if GPIO [1] is configured as an output pin.<br><br>Reset to 0b. |
| 7 | Reserved | RsvdP | Not Support. |
| 8 | GPIO [2] Input | RO | State of GPIO [2] pin |
| 9 | GPIO [2] Output Enable | RW | 0b: GPIO [2] is an input pin<br>1b: GPIO [2] is an output pin<br><br>Reset to 0b. |
| 10 | GPIO [2] Output Register | RW | Value of this bit will be output to GPIO [2] pin if GPIO [2] is configured as an output pin.<br><br>Reset to 0b. |
| 11 | Reserved | RsvdP | Not Support. |
| 12 | GPIO [3] Input | RO | State of GPIO [3] pin. |
| 13 | GPIO [3] Output Enable | RW | 0b: GPIO [3] is an input pin<br>1b: GPIO [3] is an output pin<br><br>Reset to 0b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 14 | GPIO [3] Output Register | RW | Value of this bit will be output to GPIO [3] pin if GPIO [3] is configured as an output pin.<br><br>Reset to 0b. |
| 15 | Reserved | RsvdP | Not Support. |
| 16 | GPIO [4] Input | RO | State of GPIO [4] pin. |
| 17 | GPIO [4] Output Enable | RW | 0b: GPIO [4] is an input pin<br>1b: GPIO [4] is an output pin<br><br>Reset to 0b. |
| 18 | GPIO [4] Output Register | RW | Value of this bit will be output to GPIO [4] pin if GPIO [4] is configured as an output pin.<br><br>Reset to 0b. |
| 19 | Reserved | RsvdP | Not Support. |
| 20 | GPIO [5] Input | RO | State of GPIO [5] pin. |
| 21 | GPIO [5] Output Enable | RW | 0b: GPIO [5] is an input pin<br>1b: GPIO [5] is an output pin<br><br>Reset to 0b. |
| 22 | GPIO [5] Output Register | RW | Value of this bit will be output to GPIO [5] pin if GPIO [5] is configured as an output pin.<br><br>Reset to 0b. |
| 23 | Reserved | RsvdP | Not Support. |
| 24 | GPIO [6] Input | RO | State of GPIO [6] pin. |
| 25 | GPIO [6] Output Enable | RW | 0b: GPIO [6] is an input pin<br>1b: GPIO [6] is an output pin<br><br>Reset to 0b. |
| 26 | GPIO [6] Output Register | RW | Value of this bit will be output to GPIO [6] pin if GPIO [6] is configured as an output pin.<br><br>Reset to 0b. |
| 27 | Reserved | RsvdP | Not Support. |
| 28 | GPIO [7] Input | RO | State of GPIO [7] pin. |
| 29 | GPIO [7] Output Enable | RW | 0b: GPIO [7] is an input pin<br>1b: GPIO [7] is an output pin<br><br>Reset to 0b. |
| 30 | GPIO [7] Output Register | RW | Value of this bit will be output to GPIO [7] pin if GPIO [7] is configured as an output pin.<br><br>Reset to 0b. |
| 31 | Reserved | RsvdP | Not Support. |

## 7.2.62 EEPROM CONTROL REGISTER – OFFSET BCh (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | EEPROM Start | RW | Starts the EEPROM read or write cycle.<br><br>Reset to 0b. |
| 1 | EEPROM Command | RW | Sends the command to the EEPROM.<br><br>0b: EEPROM read<br>1b: EEPROM write<br><br>Reset to 0b. |
| 2 | EEPROM Error Status | RO | 1b: EEPROM acknowledge was not received during the EEPROM cycle.<br><br>Reset to 0b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 3 | EEPROM Autoload Success | RO | 0b: EEPROM autoload was unsuccessful or is disabled<br>1b: EEPROM autolad occurred successfully after RESET. Configuration registers were loaded with values in the EEPROM<br><br>It will be cleared when read at this bit. |
| 4 | EEPROM Autoload Status | RO | 0b: EEPROM autoload was unsuccessful or is disabled<br>1b: EEPROM autoload occurred successfully after PREST. Configuration registers were loaded with values stored in the EEPROM<br><br>Reset to 0b. |
| 5 | EEPROM Autoload Disable | RW | 0b: EEPROM autoload enabled<br>1b: EEPROM autoload disabled<br><br>Reset to 1b. |
| 7:6 | EEPROM Clock Rate | RW | Determines the frequency of the EEPROM clock, which is derived from the primary clock.<br><br>00b: Reserved<br>01b: PEXCLK / 1024 (PEXCLK is 125MHz)<br>10b: Reserved<br>11b: Test Mode<br><br>Reset to 01b. |

## 7.2.63 EEPROM ADDRESS REGISTER – OFFSET BCh (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 8 | Reserved | RsvdP | Not Support. |
| 15:9 | EEPROM Address | RW | Contains the EEPROM address.<br><br>Reset to 0000h. |

## 7.2.64 EEPROM DATA REGISTER – OFFSET BCh (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:16 | EEPROM Data | RW | Contains the data to be written to the EEPROM. After completion of a read cycle, this register will contain the data from the EEPROM.<br><br>Reset to 0000h. |

## 7.2.65 PCI EXPRESS CAPABILITY REGISTER – OFFSET C0h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Enhanced Capabilities ID | RO | Read as 10h to indicate that these are PCI express enhanced capability registers. |
| 15:8 | Next Item Pointer | RO | Read as 00h. No other ECP registers. |
| 19:16 | Capability Version | RO | Read as 0010b to indicate the device is compliant to Revision .2.0a of *PCI Express Base Specifications.* |
| 23:20 | Device/Port Type | RO | Indicates the type of PCI Express logical device.<br><br>Reset to 0101b (Upstream port).<br>Reset to 0110b (Downstream ports). |
| 24 | Slot Implemented | HwInt RO | When set, indicates that the PCIe Link associated with this Port is connected to a slot. This field is valid for downstream port of the Switch. The default value may be changed by the status of strapped pin, SMBus or auto-loading from EEPROM.<br><br>Reset to the status of SLOT_IMP strapped pin. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 29:25 | Interrupt Message Number | RO | Read as 0b. No MSI messages are generated in the transparent mode. |
| 31:30 | Reserved | RsvdP | Not Support. |

## 7.2.66 DEVICE CAPABILITIES REGISTER – OFFSET C4h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 2:0 | Max_Payload_Size Supported | HwInt RO | Indicates the maximum payload size that the device can support for TLPs. The default value may be changed by the status of strapped pin, SMBus or auto-loading from EEPROM.<br><br>Reset to 001b when PL_512B strapped pin is set to 0.<br>Reset to 010b when PL_512B strapped pin is set to 1. |
| 4:3 | Phantom Functions Supported | RO | Indicates the support for use of unclaimed function numbers as Phantom functions. Read as 00b, since the Switch does not act as a requester.<br><br>Reset to 00b. |
| 5 | Extended Tag Field Supported | RO | Indicates the maximum supported size of Tag field as a Requester. Read as 0, since the Switch does not act as a requester.<br><br>Reset to 0b. |
| 8:6 | Endpoint L0s Acceptable Latency | RO | Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. For Switch, the ASPM software would not check this value.<br><br>Reset to 000b. |
| 11:9 | Endpoint L1 Acceptable Latency | RO | Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. For Switch, the ASPM software would not check this value.<br><br>Reset to 000b. |
| 14:12 | Reserved | RsvdP | Not Support. |
| 15 | Role_Based Error Reporting | RO | When set, indicates that the device implements the functionality originally defined in the Error Reporting ECN. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 1b. |
| 17:16 | Reserved | RsvdP | Not Support. |
| 25:18 | Captured Slot Power Limit Value | RO | It applies to Upstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot.<br><br>This value is set by the Set_Slot_Power_Limit message or hardwired to 00h.<br><br>Reset to 00h. |
| 27:26 | Captured Slot Power Limit Scale | RO | It applies to Upstream Port only. Specifies the scale used for the Slot Power Limit Value.<br><br>This value is set by the Set_Slot_Power_Limit message or hardwired to 00b.<br><br>Reset to 00b. |
| 31:28 | Reserved | RsvdP | Not Support. |

## 7.2.67 DEVICE CONTROL REGISTER – OFFSET C8h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | Correctable Error Reporting Enable | RW | 0b: Disable Correctable Error Reporting<br>1b: Enable Correctable Error Reporting<br><br>Reset to 0b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | Non-Fatal Error Reporting Enable | RW | 0b: Disable Non-Fatal Error Reporting<br>1b: Enable Non-Fatal Error Reporting<br><br>Reset to 0b. |
| 2 | Fatal Error Reporting Enable | RW | 0b: Disable Fatal Error Reporting<br>1b: Enable Fatal Error Reporting<br><br>Reset to 0b. |
| 3 | Unsupported Request Reporting Enable | RW | 0b: Disable Unsupported Request Reporting<br>1b: Enable Unsupported Request Reporting<br><br>Reset to 0b. |
| 4 | Enable Relaxed Ordering | RO | When set, it permits the device to set the Relaxed Ordering bit in the attribute field of transaction. Since the Switch can not either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read.<br><br>Reset to 0b. |
| 7:5 | Max_Payload_Size | RW | This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value.<br><br>Reset to 000b. |
| 8 | Extended Tag Field Enable | RW | Does not apply to PCI Express Switch. Returns '0' when read.<br><br>Reset to 0b. |
| 9 | Phantom Function Enable | RW | Does not apply to PCI Express Switch. Returns '0' when read.<br><br>Reset to 0b. |
| 10 | Auxiliary (AUX) Power PM Enable | RWS | When set, indicates that a device is enabled to draw AUX power independent of PME AUX power.<br><br>Reset to 0b. |
| 11 | Enable No Snoop | RO | When set, it permits to set the No Snoop bit in the attribute field of transaction. Since the Switch can not either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read.<br><br>Reset to 0b. |
| 14:12 | Max_Read_ Request_Size | RO | This field sets the maximum Read Request size for the device as a Requester. Since the Switch does not generate read request by itself, these bits are hardwired to 000b.<br><br>Reset to 000b. |
| 15 | Reserved | RsvdP | Not Support. |

## 7.2.68 DEVICE STATUS REGISTER – OFFSET C8h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 16 | Correctable Error Detected | RW1C | Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.<br><br>Reset to 0b. |
| 17 | Non-Fatal Error Detected | RW1C | Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.<br><br>Reset to 0b. |
| 18 | Fatal Error Detected | RW1C | Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.<br><br>Reset to 0b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 19 | Unsupported Request Detected | RW1C | Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.<br><br>Reset to 0b. |
| 20 | AUX Power Detected | RO | Asserted when the AUX power is detected by the Switch<br><br>Reset to 1b. |
| 21 | Transactions Pending | RO | Each port of Switch does not issue Non-posted Requests on its own behalf, so this bit is hardwired to 0b.<br><br>Reset to 0b. |
| 31:22 | Reserved | RsvdP | Not Support. |

## 7.2.69 LINK CAPABILITIES REGISTER – OFFSET CCh

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 3:0 | Maximum Link Speed | RO | Indicates the maximum speed of the Express link. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0010b (5 Gb/s). |
| 9:4 | Maximum Link Width | RO | Indicates the maximum width of the given PCIe Link.<br><br>Reset to 00_0010b (x2) (Upstream port).<br>Reset to 00_0001b (x1) (Downstream ports). |
| 11:10 | Active State Power Management (ASPM) Support | RO | Indicates the level of ASPM supported on the given PCIe Link. Each port of Switch supports L0s and L1 entry. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 00b. |
| 14:12 | L0s Exit Latency | RO | Indicates the L0s exit latency for the given PCIe Link.<br>The length of time this port requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 011b. |
| 17:15 | L1 Exit Latency | RO | Indicates the L1 exit latency for the given PCIe Link.<br>The length of time this port requires to complete transition from L1 to L0 is in the range of 16us to less than 32us. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 000b. |
| 19:18 | Reserved | RsvdP | Not Support. |
| 20 | Data Link Layer Active Reporting Capable | RO | For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port, this bit must be set to 1b.<br><br>For Upstream Port, this bit must be hardwired to 0b.<br><br>Reset to 0b. |
| 21 | Link bw notify cap | RO | Reset to 0b (Upstream port).<br>Reset to 1b (Downstream ports). |
| 23:21 | Reserved | RsvdP | Not Support. |
| 31:24 | Port Number | RO | Indicates the PCIe Port Number for the given PCIe Link. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 00h for Port 0.<br>Reset to 01h for Port 1.<br>Reset to 02h for Port 2. |


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## 7.2.70 LINK CONTROL REGISTER – OFFSET D0h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 1:0 | Active State Power Management (ASPM) Control | RW | 00b: ASPM is Disabled<br>01b: L0s Entry Enabled<br>10b: L1 Entry Enabled<br>11b: L0s and L1 Entry Enabled<br><br>Note that the receiver must be capable of entering L0s even when the field is disabled.<br><br>Reset to 00b. |
| 2 | Reserved | RsvdP | Not Support. |
| 3 | Read Completion Boundary (RCB) | RO | Does not apply to PCI Express Switch. Returns '0' when read.<br><br>Reset to 0b. |
| 4 | Link Disable | RW | At upstream port, it is not allowed to disable the link, so this bit is hardwired to '0'. For downstream ports, it disables the link when this bit is set.<br><br>Reset to 0b. |
| 5 | Retrain Link | RW | At upstream port, it is not allowed to retrain the link, so this bit is hardwired to 0b. For downstream ports, it initiates Link Retraining when this bit is set.<br><br>This bit always returns 0b when read. |
| 6 | Common Clock Configuration | RW | 0b: The components at both ends of a link are operating with asynchronous reference clock<br>1b: The components at both ends of a link are operating with a distributed common reference clock<br><br>Reset to 0b. |
| 7 | Extended Synch | RW | When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state.<br><br>Reset to 0b. |
| 8 | Reserved | RsvdP | Not Support. |
| 9 | HW Autonomous width Disable | RW | Reset to 0b. |
| 10 | Link Bandwidth Management Interrupt Enable | RO/RW | For upstream Port is RO.<br>For downstream Port is RW.<br><br>Reset to 0b. |
| 11 | Link Autonomous Bandwidth Interrupt Enable | RO/RW | For upstream Port is RO.<br>For downstream Port is RW.<br><br>Reset to 0b. |
| 15:12 | Reserved | RsvdP | Not Support. |

## 7.2.71 LINK STATUS REGISTER – OFFSET D0h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 19:16 | Link Speed | RO | Indicate the negotiated speed of the Express link.<br><br>0001b: 2.5 Gb/s.<br>0010b: 5 Gb/s.<br><br>Reset to 0010b. |
| 25:20 | Negotiated Link Width | RO | Indicates the negotiated width of the given PCIe link.<br><br>Reset to 00_0010b (x2) (Upstream port).<br>Reset to 00_0001b (x1) (Downstream ports). |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 26 | Training Error | RO | When set, indicates a Link training error occurred.<br>This bit is cleared by hardware upon successful training of the link to the L0 link state.<br><br>Reset to 0b. |
| 27 | Link Training | RO | When set, indicates the link training is in progress. Hardware clears this bit once link training is complete.<br><br>Reset to 0b. |
| 28 | Slot Clock Configuration | HwInt RO | 0b: the Switch uses an independent clock irrespective of the presence of a reference on the connector<br>1b: the Switch uses the same reference clock that the platform provides on the connector<br><br>The default value may be changed by the status of strapped pin, SMBus or auto-loading from EEPROM.<br><br>Reset to the status of SLOTCLK strapped pin. |
| 29 | Data Link Layer Link Active | RO | Indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise.<br><br>Reset to 0b. |
| 31:30 | Reserved | RsvdP | Not Support. |

## 7.2.72 SLOT CAPABILITIES REGISTER – OFFSET D4h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | Attention Button Present | RO | When set, it indicates that an Attention Button is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 1 | Power Controller Present | RO | When set, it indicates that a Power Controller is implemented for this slot. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 2 | Reserved | RsvdP | Not Support. |
| 3 | Attention Indicator Present | RO | When set, it indicates that an Attention Indicator is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 4 | Power Indicator Present | RO | When set, it indicates that a Power Indicator is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 5 | Hot-Plug Surprise | RO | When set, it indicates that a device present in this slot might be removed from the system without any prior notification. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 6 | Hot-Plug Capable | RO | When set, it indicates that this slot is capable of supporting Hot-Plug operation. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0b. |
| 14:7 | Slot Power Limit Value | RW | It applies to Downstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 00h. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 16:15 | Slot Power Limit Scale | RW | It applies to Downstream Port only. Specifies the scale used for the Slot Power Limit Value. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 00b. |
| 18:17 | Reserved | RsvdP | Not Support. |
| 31:19 | Physical Slot Number | RO | It indicates the physical slot number attached to this Port. The default value may be changed by SMBus or auto-loading from EEPROM.<br><br>Reset to 0000h. |

## 7.2.73 SLOT CONTROL REGISTER – OFFSET D8h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | Attention Button Pressed Enable | RW | When set, it enables the generation of Hot-Plug interrupt or wakeup event on an attention button pressed event.<br><br>Reset to 0b. |
| 1 | Power Fault Detected Enable | RW | When set, it enables the generation of Hot-Plug interrupt or wakeup event on a power fault event.<br><br>Reset to 0b. |
| 2 | Reserved | RsvdP | Not Support. |
| 3 | Presence Detect Changed Enable | RW | When set, it enables the generation of Hot-Plug interrupt or wakeup event on a presence detect changed event.<br><br>Reset to 0b. |
| 4 | Command Completed Interrupt Enable | RW | When set, it enables the generation of Hot-Plug interrupt when the Hot-Plug Controller completes a command.<br><br>Reset to 0b. |
| 5 | Hot-Plug Interrupt Enable | RW | When set, it enables generation of Hot-Plug interrupt on enabled Hot-Plug events.<br><br>Reset to 0b. |
| 7:6 | Attention Indicator Control | RW | Controls the display of Attention Indicator.<br><br>00b: Reserved<br>01b: On<br>10b: Blink<br>11b: Off<br><br>Writes to this register also cause the Port to send the ATTENTION_INDICATOR_* Messages.<br><br>Reset to 11b. |
| 9:8 | Power Indicator Control | RW | Controls the display of Power Indicator.<br><br>00b: Reserved<br>01b: On<br>10b: Blink<br>11b: Off<br><br>Writes to this register also cause the Port to send the POWER_INDICATOR_* Messages.<br><br>Reset to 11b. |
| 10 | Power Controller Control | RW | 0b: reset the power state of the slot (Power On)<br>1b: set the power state of the slot (Power Off)<br><br>Reset to 0b. |
| 11 | Reserved | RsvdP | Not Support. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 12 | Data Link Layer State Changed Enable | RW | If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed.<br><br>Reset to 0b. |
| 15:13 | Reserved | RsvdP | Not Support. |

## 7.2.74 SLOT STATUS REGISTER OFFSET D8h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 16 | Attention Button Pressed | RW1C | When set, it indicates the Attention Button is pressed.<br><br>Reset to 0b. |
| 17 | Power Fault Detected | RW1C | When set, it indicates a Power Fault is detected.<br><br>Reset to 0b. |
| 18 | MRL Sensor Changed | RO | When set, it indicates a MRL Sensor Changed is detected.<br><br>Reset to 0b. |
| 19 | Presence Detect Changed | RW1C | When set, it indicates a Presence Detect Changed is detected.<br><br>Reset to 0b. |
| 20 | Command Completed | RW1C | When set, it indicates the Hot-Plug Controller completes an issued command.<br><br>Reset to 0b. |
| 21 | MRL Sensor State | RO | Reflects the status of MRL Sensor.<br><br>0b: MRL Closed<br>1b: MRL Opened<br><br>Reset to 0b. |
| 22 | Presence Detect State | HwInt RO | Indicates the presence of a card in the slot.<br><br>0b: Slot Empty<br>1b: Card Present in slot<br><br>This register is implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities register is 0b), this bit returns 1b.<br><br>Reset to 1b when PRSNT strapped pin is set to 0.<br>Reset to 0b when PRSNT strapped pin is set to 1. |
| 23 | Reserved | RsvdP | Not Support. |
| 24 | Data Link Layer State Changed | RW1C | This bit is set when the value reported in the Data Link Layer Link Active field of the Link Status register is changed.<br><br>Reset to 0b. |
| 31:25 | Reserved | RsvdP | Not Support. |

## 7.2.75 DEVICE CAPABILITIES REGISTER 2 – OFFSET E4h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 10:0 | Device Capabilities 2 | RO | Reset to 000h. |
| 11 | LTR Mechanism Supported | RO | A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism.<br><br>Reset to 1b. |
| 17:12 | Device Capabilities 2 | RO | Reset to 00h. |
| 19:18 | OBFF Supported | RO | This field indicates if OBFF is supported.<br><br>Reset to 01b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:20 | Device Capabilities 2 | RO | Reset to 000h. |

## 7.2.76 DEVICE CONTROL REGISTER 2 – OFFSET E8h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 9:0 | Device Control 2 | RO | Reset to 000h. |
| 10 | LTR Mechanism Enable | RW | Enable LTR Mechanism.<br><br>Reset to 0b. |
| 12:11 | Device Control 2 | RO | Reset to 00b. |
| 14:13 | OBFF enable | RW | Enable OBFF Mechanism and select the signaling method.<br><br>Reset to 00b. |
| 15 | Device Control 2 | RO | Reset to 0b. |

## 7.2.77 DEVIDE STATUS REGISTER 2 – OFFSET E8h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:16 | Device status 2 | RO | Reset to 0000h. |

## 7.2.78 LINK CAPABILITIES REGISTER 2 – OFFSET ECh

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:0 | Link Capabilities 2 | RO | Reset to 0000_0000h. |

## 7.2.79 LINK CONTROL REGISTER 2 – OFFSET F0h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 3:0 | Target Link Speed | RWS | Reset to 0010b. |
| 4 | Enter Compliance | RWS | Reset to 0b. |
| 5 | HW_AutoSpeed_Dis | RW | Reset to 0b. |
| 6 | Select_Deemp | RO | Reset to 0b (Upstream port).<br>Reset to 1b (Downstream ports). |
| 9:7 | Tran_Margin | RWS | Reset to 000b. |
| 10 | Enter Modify Compliance | RWS | Reset to 0b. |
| 11 | Compliance SOS | RWS | Reset to 0b. |
| 12 | Compliance_Deemp | RWS | Reset to 0b. |
| 15:13 | Reserved | RsvdP | Not Support. |

## 7.2.80 LINK STATUS REGISTER 2 – OFFSET F0h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 16 | Current De-emphasis Level | RO | Reset to 0b (Upstream port).<br>Reset to 1b (Downstream ports). |
| 31:17 | Link Status 2 | RO | Reset to 0000h. |


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### 7.2.81 SLOT CAPABILITIES REGISTER 2 – OFFSET F4h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:0 | Slot Capabilities 2 | RO | Reset to 0000_0000h. |

### 7.2.82 SLOT CONTORL REGISTER 2 – OFFSET F8h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | Slot Control2 | RO | Reset to 0000h. |

### 7.2.83 SLOT STATUS REGISTER 2 – OFFSET F8h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:16 | Slot Status 2 | RO | Reset to 0000h. |

### 7.2.84 PCI EXPRESS ADVANCED ERROR REPORTING CAPABILITY REGISTER – OFFSET 100h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | Extended Capabilities ID | RO | Read as 0001h to indicate that these are PCI express extended capability registers for advance error reporting. |
| 19:16 | Capability Version | RO | Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number. |
| 31:20 | Next Capability Offset | RO | Pointer points to the PCI Express Extended VC capability register.<br><br>Reset to 140h. |

### 7.2.85 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 104h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | Training Error Status | RW1CS | When set, indicates that the Training Error event has occurred.<br><br>Reset to 0b. |
| 3:1 | Reserved | RsvdP | Not Support. |
| 4 | Data Link Protocol Error Status | RW1CS | When set, indicates that the Data Link Protocol Error event has occurred.<br><br>Reset to 0b. |
| 11:5 | Reserved | RsvdP | Not Support. |
| 12 | Poisoned TLP Status | RW1CS | When set, indicates that a Poisoned TLP has been received or generated.<br><br>Reset to 0b. |
| 13 | Flow Control Protocol Error Status | RW1CS | When set, indicates that the Flow Control Protocol Error event has occurred.<br><br>Reset to 0b. |
| 14 | Completion Timeout Status | RW1CS | When set, indicates that the Completion Timeout event has occurred.<br><br>Reset to 0b. |
| 15 | Completer Abort Status | RW1CS | When set, indicates that the Completer Abort event has occurred.<br><br>Reset to 0b. |
| 16 | Unexpected Completion Status | RW1CS | When set, indicates that the Unexpected Completion event has occurred.<br><br>Reset to 0b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 17 | Receiver Overflow Status | RW1CS | When set, indicates that the Receiver Overflow event has occurred.<br><br>Reset to 0b. |
| 18 | Malformed TLP Status | RW1CS | When set, indicates that a Malformed TLP has been received.<br><br>Reset to 0b. |
| 19 | ECRC Error Status | RW1CS | When set, indicates that an ECRC Error has been detected.<br><br>Reset to 0b. |
| 20 | Unsupported Request Error Status | RW1CS | When set, indicates that an Unsupported Request event has occurred.<br><br>Reset to 0b. |
| 21 | ACS Violation Status | RW1CS | When set, indicates that an ACS Violation event has occurred<br><br>Reset to 0b. |
| 31:21 | Reserved | RsvdP | Not Support. |

## 7.2.86 UNCORRECTABLE ERROR MASK REGISTER – OFFSET 108h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | Training Error Mask | RWS | When set, the Training Error event is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 3:1 | Reserved | RsvdP | Not Support. |
| 4 | Data Link Protocol Error Mask | RWS | When set, the Data Link Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 11:5 | Reserved | RsvdP | Not Support. |
| 12 | Poisoned TLP Mask | RWS | When set, an event of Poisoned TLP has been received or generated is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 13 | Flow Control Protocol Error Mask | RWS | When set, the Flow Control Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 14 | Completion Timeout Mask | RWS | When set, the Completion Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 15 | Completer Abort Mask | RWS | When set, the Completer Abort event is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 16 | Unexpected Completion Mask | RWS | When set, the Unexpected Completion event is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 17 | Receiver Overflow Mask | RWS | When set, the Receiver Overflow event is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 18 | Malformed TLP Mask | RWS | When set, an event of Malformed TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 19 | ECRC Error Mask | RWS | When set, an event of ECRC Error has been detected is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 20 | Unsupported Request Error Mask | RWS | When set, the Unsupported Request event is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 21 | ACS violation mask | RWS | Reset to 0b |
| 31:22 | Reserved | RsvdP | Not Support. |

## 7.2.87 UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 10Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | Training Error Severity | RWS | 0b: Non-Fatal<br>1b: Fatal<br><br>Reset to 1b. |
| 3:1 | Reserved | RsvdP | Not Support. |
| 4 | Data Link Protocol Error Severity | RWS | 0b: Non-Fatal<br>1b: Fatal<br><br>Reset to 1b. |
| 11:5 | Reserved | RsvdP | Not Support. |
| 12 | Poisoned TLP Severity | RWS | 0b: Non-Fatal<br>1b: Fatal<br><br>Reset to 0b. |
| 13 | Flow Control Protocol Error Severity | RWS | 0b: Non-Fatal<br>1b: Fatal<br><br>Reset to 1b. |
| 14 | Completion Timeout Error Severity | RWS | 0b: Non-Fatal<br>1b: Fatal<br><br>Reset to 0b. |
| 15 | Completer Abort Severity | RWS | 0b: Non-Fatal<br>1b: Fatal<br><br>Reset to 0b. |
| 16 | Unexpected Completion Severity | RWS | 0b: Non-Fatal<br>1b: Fatal<br><br>Reset to 0b. |
| 17 | Receiver Overflow Severity | RWS | 0b: Non-Fatal<br>1b: Fatal<br><br>Reset to 1b. |
| 18 | Malformed TLP Severity | RWS | 0b: Non-Fatal<br>1b: Fatal<br><br>Reset to 1b. |
| 19 | ECRC Error Severity | RWS | 0b: Non-Fatal<br>1b: Fatal<br><br>Reset to 0b. |
| 20 | Unsupported Request Error Severity | RWS | 0b: Non-Fatal<br>1b: Fatal<br><br>Reset to 0b. |
| 21 | ACS violation severity | RWS | 0b: Non-Fatal<br>1b: Fatal<br><br>Reset to 0b. |
| 31:21 | Reserved | RsvdP | Not Support. |


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## 7.2.88 CORRECTABLE ERROR STATUS REGISTER – OFFSET 110 h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | Receiver Error Status | RW1CS | When set, the Receiver Error event is detected.<br><br>Reset to 0b. |
| 5:1 | Reserved | RsvdP | Not Support. |
| 6 | Bad TLP Status | RW1CS | When set, the event of Bad TLP has been received is detected.<br><br>Reset to 0b. |
| 7 | Bad DLLP Status | RW1CS | When set, the event of Bad DLLP has been received is detected.<br><br>Reset to 0b. |
| 8 | REPLAY_NUM Rollover status | RW1CS | When set, the REPLAY_NUM Rollover event is detected.<br><br>Reset to 0b. |
| 11:9 | Reserved | RsvdP | Not Support. |
| 12 | Replay Timer Timeout status | RW1CS | When set, the Replay Timer Timeout event is detected.<br><br>Reset to 0b. |
| 13 | Advisory Non-Fatal Error status | RW1CS | When set, the Advisory Non-Fatal Error event is detected.<br><br>Reset to 0b. |
| 31:14 | Reserved | RsvdP | Not Support. |

## 7.2.89 CORRECTABLE ERROR MASK REGISTER – OFFSET 114 h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | Receiver Error Mask | RWS | When set, the Receiver Error event is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 5:1 | Reserved | RsvdP | Not Support. |
| 6 | Bad TLP Mask | RWS | When set, the event of Bad TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 7 | Bad DLLP Mask | RWS | When set, the event of Bad DLLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 8 | REPLAY_NUM Rollover Mask | RWS | When set, the REPLAY_NUM Rollover event is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 11:9 | Reserved | RsvdP | Not Support. |
| 12 | Replay Timer Timeout Mask | RWS | When set, the Replay Timer Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either.<br><br>Reset to 0b. |
| 13 | Advisory Non-Fatal Error Mask | RWS | When set, the Advisory Non-Fatal Error event is not logged in the Header Long register and not issued as an Error Message to RC either.<br><br>Reset to 1b. |
| 31:14 | Reserved | RsvdP | Not Support. |


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### 7.2.90 ADVANCE ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET 118h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 4:0 | First Error Pointer | ROS | It indicates the bit position of the first error reported in the Uncorrectable Error Status register.<br><br>Reset to 0_0000b. |
| 5 | ECRC Generation Capable | RO | When set, it indicates the Switch has the capability to generate ECRC.<br><br>Reset to 1b. |
| 6 | ECRC Generation Enable | RWS | When set, it enables the generation of ECRC when needed.<br><br>Reset to 0b. |
| 7 | ECRC Check Capable | RO | When set, it indicates the Switch has the capability to check ECRC.<br><br>Reset to 1b. |
| 8 | ECRC Check Enable | RWS | When set, the function of checking ECRC is enabled.<br><br>Reset to 0b. |
| 31:9 | Reserved | RsvdP | Not Support. |

### 7.2.91 HEADER LOG REGISTER – OFFSET From 11Ch to 128h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:0 | 1st DWORD | ROS | Hold the 1st DWORD of TLP Header. The Head byte is in big endian. |
| 63:32 | 2nd DWORD | ROS | Hold the 2nd DWORD of TLP Header. The Head byte is in big endian. |
| 95:64 | 3rd DWORD | ROS | Hold the 3rd DWORD of TLP Header. The Head byte is in big endian. |
| 127:96 | 4th DWORD | ROS | Hold the 4th DWORD of TLP Header. The Head byte is in big endian. |

### 7.2.92 PCI EXPRESS VIRTUAL CHANNEL CAPABILITY REGISTER – OFFSET 140h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | Extended Capabilities ID | RO | Read as 0002h to indicate that these are PCI express extended capability registers for virtual channel. |
| 19:16 | Capability Version | RO | Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number. |
| 31:20 | Next Capability Offset | RO | Pointer points to the PCI Express Power Budgeting Capability register.<br><br>Reset to 20Ch. |

### 7.2.93 PORT VC CAPABILITY REGISTER 1 – OFFSET 144h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 2:0 | Extended VC Count | HwInt RO | It indicates the number of extended Virtual Channels in addition to the default VC supported by the Switch. The default value may be changed by the status of strapped pin, or auto-loading from EEPROM.<br><br>Bit[2:1]: Reset to 00b.<br>Bit[0]: Reset to the status of VC1_EN strapped pin. |
| 3 | Reserved | RsvdP | Not Support. |
| 6:4 | Low Priority Extended VC Count | RO | It indicates the number of extended Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group. The default value may be changed by auto-loading from EEPROM.<br><br>Reset to 000b. |
| 7 | Reserved | RsvdP | Not Support. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 9:8 | Reference Clock | RO | It indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. Defined encoding is 00b for 100 ns reference clock.<br><br>Reset to 00b. |
| 11:10 | Port Arbitration Table Entry Size | RO | Read as 10b to indicate the size of Port Arbitration table entry in the device is 4 bits.<br><br>Reset to 10b. |
| 31:12 | Reserved | RsvdP | Not Support. |

## 7.2.94 PORT VC CAPABILITY REGISTER 2 – OFFSET 148h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | VC Arbitration Capability | RO | It indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid when LPVC is greater than 0. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin and Weight Round Robin arbitration with 32 phases in LPVC.<br><br>Reset to 03h if offset 144h.bit[0]=1.<br>Reset to 00h if offset 144h.bit[0]=0. |
| 23:8 | Reserved | RsvdP | Not Support. |
| 31:24 | VC Arbitration Table Offset | RO | It indicates the location of the VC Arbitration Table as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes).<br><br>Reset to 03h if offset 144h.bit[0]=1.<br>Reset to 00h if offset 144h.bit[0]=0. |

## 7.2.95 PORT VC CONTROL REGISTER – OFFSET 14Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | Load VC Arbitration Table | RW | When set, the programmed VC Arbitration Table is applied to the hardware. This bit always returns 0b when read.<br><br>Reset to 0b. |
| 3:1 | VC Arbitration Select | RW | This field is used to configure the VC Arbitration by selecting one of the supported VC Arbitration schemes. The valid values for the schemes supported by Switch are 0b and 1b. Other value than these written into this register will be treated as default.<br><br>Reset to 000b. |
| 15:4 | Reserved | RsvdP | Not Support. |

## 7.2.96 PORT VC STATUS REGISTER – OFFSET 14Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 16 | VC Arbitration Table Status | RO | When set, it indicates that any entry of the VC Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the VC Arbitration Table after the bit of "Load VC Arbitration Table" is set.<br><br>Reset to 0b. |
| 31:17 | Reserved | RsvdP | Not Support. |


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## 7.2.97 VC RESOURCE CAPABILITY REGISTER (0) – OFFSET 150h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Port Arbitration Capability | RO | It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1.<br><br>Reset to 19h. |
| 13:8 | Reserved | RsvdP | Not Support. |
| 14 | Advanced Packet Switching | RO | When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS).<br><br>Reset to 0b. |
| 15 | Reject Snoop Transactions | RO | This bit is not applied to PCIe Switch.<br><br>Reset to 0b. |
| 22:16 | Maximum Time Slots | RO | It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. The default value may be changed by auto-loading from EEPROM.<br><br>Reset to 7Fh. |
| 23 | Reserved | RsvdP | Not Support. |
| 31:24 | Port Arbitration Table Offset | RO | It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes).<br><br>Reset to 04h for Port Arbitration Table (0). |

## 7.2.98 VC RESOURCE CONTROL REGISTER (0) – OFFSET 154h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | TC/VC Map | RW | This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. The default value may be changed by auto-loading from EEPROM.<br><br>Reset to FFh. |
| 15:8 | Reserved | RsvdP | Not Support. |
| 16 | Load Port Arbitration Table | RW | When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read.<br><br>Reset to 0b. |
| 19:17 | Port Arbitration Select | RW | This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b and 011b at VC0, other value than these written into this register will be treated as default.<br><br>Reset to 000b. |
| 23:20 | Reserved | RsvdP | Not Support. |
| 26:24 | VC ID | RO | This field assigns a VC ID to the VC resource.<br><br>Reset to 000b. |
| 30:27 | Reserved | RsvdP | Not Support. |
| 31 | VC Enable | RW | 0b: disables this Virtual Channel<br>1b: enables this Virtual Channel<br><br>Reset to 1b. |


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### 7.2.99 VC RESOURCE STATUS REGISTER (0) – OFFSET 158h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | Reserved | RsvdP | Not Support. |
| 16 | Port Arbitration Table Status | RO | When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of "Load Port Arbitration Table" is set.<br><br>Reset to 0b. |
| 17 | VC Negotiation Pending | RO | When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete.<br><br>Reset to 0b. |
| 31:18 | Reserved | RsvdP | Not Support. |

### 7.2.100 VC RESOURCE CAPABILITY REGISTER (1) – OFFSET 15Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Port Arbitration Capability | RO | It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1.<br><br>Reset to 19h if offset 144h.bit[0]=1.<br>Reset to 00h if offset 144h.bit[0]=0. |
| 13:8 | Reserved | RsvdP | Not Support. |
| 14 | Advanced Packet Switching | RO | When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS).<br><br>Reset to 0b. |
| 15 | Reject Snoop Transactions | RO | This bit is not applied to PCIe Switch.<br><br>Reset to 0b. |
| 22:16 | Maximum Time Slots | RO | It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. The default value may be changed by auto-loading from EEPROM.<br><br>Reset to 7Fh if offset 144h.bit[0]=1.<br>Reset to 00h if offset 144h.bit[0]=0. |
| 23 | Reserved | RsvdP | Not Support. |
| 31:24 | Port Arbitration Table Offset | RO | It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes).<br><br>Reset to 08h for Port Arbitration Table (1) if offset 144h.bit[0]=1.<br>Reset to 00h if offset 144h.bit[0]=0. |

### 7.2.101 VC RESOURCE CONTROL REGISTER (1) – OFFSET 160h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | TC/VC Map | RW (Exception for bit0) | This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. Bit 0 of this filed is read-only and must be set to "0" for the VC1. The default value may be changed by auto-loading from EEPROM.<br><br>Reset to 00h. |
| 15:8 | Reserved | RsvdP | Not Support. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 16 | Load Port Arbitration Table | RW | When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read.<br><br>Reset to 0b. |
| 19:17 | Port Arbitration Select | RW | This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b, 011b and 100b at VC1, other value than these written into this register will be treated as default.<br><br>Reset to 000b. |
| 23:20 | Reserved | RsvdP | Not Support. |
| 26:24 | VC ID | RW | This field assigns a VC ID to the VC resource.<br><br>Reset to 001b if offset 144h.bit[0]=1.<br>Reset to 000b if offset 144h.bit[0]=0. |
| 30:27 | Reserved | RsvdP | Not Support. |
| 31 | VC Enable | RW | 0b: disables this Virtual Channel<br>1b: enables this Virtual Channel<br><br>Reset to 0b. |

## 7.2.102 VC RESOURCE STATUS REGISTER (1) – OFFSET 164h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | Reserved | RsvdP | Not Support. |
| 16 | Port Arbitration Table Status | RO | When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of "Load Port Arbitration Table" is set.<br><br>Reset to 0b. |
| 17 | VC Negotiation Pending | RO | When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete.<br><br>Reset to 0b. |
| 31:18 | Reserved | RsvdP | Not Support. |

## 7.2.103 VC ARBITRATION TABLE REGISTER – OFFSET 170h

The VC arbitration table is a read-write register array that contains a table for VC arbitration. Each table entry allocates four bits, of which three bits are used to represent VC ID and one bit is reserved. A total of 32 entries are used to construct the VC arbitration table. The layout for this register array is shown below.

**Table 7-1 Register Array Layout for VC Arbitration**

| 31 - 28 | 27 - 24 | 23 - 20 | 19 - 16 | 15 - 12 | 11 - 8 | 7 - 4 | 3 - 0 | Byte Location |
|---|---|---|---|---|---|---|---|---|
| Phase [7] | Phase [6] | Phase [5] | Phase [4] | Phase [3] | Phase [2] | Phase [1] | Phase [0] | 00h |
| Phase [15] | Phase [14] | Phase [13] | Phase [12] | Phase [11] | Phase [10] | Phase [9] | Phase [8] | 04h |
| Phase [23] | Phase [22] | Phase [21] | Phase [20] | Phase [19] | Phase [18] | Phase [17] | Phase [16] | 08h |
| Phase [31] | Phase [30] | Phase [29] | Phase [28] | Phase [27] | Phase [26] | Phase [25] | Phase [24] | 0Ch |


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### 7.2.104 PORT ARBITRATION TABLE REGISTER (0) and (1) – OFFSET 180h and 1C0h

The Port arbitration table is a read-write register array that contains a table for Port arbitration. Each table entry allocates two bits to represent Port Number. The table entry size is dependent on the number of enabled ports (refer to bit 10 and 11 of Port VC capability register 1). The arbitration table contains 128 entries if three or four ports are to be enabled. The following table shows the register array layout for the size of entry equal to two.

**Table 7-2 Table Entry Size in 4 Bits**

| 63 - 56 | 55 - 48 | 47 - 40 | 39 - 32 | 31 - 24 | 23 - 16 | 15 - 8 | 7 - 0 | Byte Location |
|---|---|---|---|---|---|---|---|---|
| Phase [15:14] | Phase [13:12] | Phase [11:10] | Phase [9:8] | Phase [7:6] | Phase [5:4] | Phase [3:2] | Phase [1:0] | 00h |
| Phase [31:30] | Phase [29:28] | Phase [27:26] | Phase [25:24] | Phase [23:22] | Phase [21:20] | Phase [19:18] | Phase [17:16] | 08h |
| Phase [47:46] | Phase [45:44] | Phase [43:42] | Phase [41:40] | Phase [39:38] | Phase [37:36] | Phase [35:34] | Phase [33:32] | 10h |
| Phase [63:62] | Phase [61:60] | Phase [59:58] | Phase [57:56] | Phase [55:54] | Phase [53:52] | Phase [51:50] | Phase [49:48] | 18h |
| Phase [79:78] | Phase [77:76] | Phase [75:74] | Phase [73:72] | Phase [71:70] | Phase [69:68] | Phase [67:66] | Phase [65:64] | 20h |
| Phase [95:94] | Phase [93:92] | Phase [91:90] | Phase [89:88] | Phase [87:86] | Phase [85:84] | Phase [83:82] | Phase [81:80] | 28h |
| Phase [111:110] | Phase [109:108] | Phase [107:106] | Phase [105:104] | Phase [103:102] | Phase [101:100] | Phase [99:98] | Phase [97:96] | 30h |
| Phase [127:126] | Phase [125:124] | Phase [123:122] | Phase [121:120] | Phase [119:118] | Phase [117:116] | Phase [115:114] | Phase [113:112] | 38h |

### 7.2.105 PCI EXPRESS POWER BUDGETING CAPABILITY REGISTER – OFFSET 20Ch

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | Extended Capabilities ID | RO | Read as 0004h to indicate that these are PCI express extended capability registers for power budgeting. |
| 19:16 | Capability Version | RO | Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number. |
| 31:20 | Next Capability Offset | RO | Pointer points to the PCI Express Extended ACS capability register/LTR capability register.<br><br>Reset to 230h (Upstream port).<br>Reset to 220h (Downstream ports). |

### 7.2.106 DATA SELECT REGISTER – OFFSET 210h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Data Selection | RW | It indexes the power budgeting data reported through the data register.<br><br>When 00h, it selects D0 Max power budget<br>When 01h, it selects D0 Sustained power budget<br>Other values would return zero power budgets, which means not supported<br><br>Reset to 00h. |
| 31:8 | Reserved | RsvdP | Not Support. |


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### 7.2.107 POWER BUDGETING DATA REGISTER – OFFSET 214h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Base Power | RO | It specifies the base power value in watts. This value represents the required power budget in the given operation condition. The default value may be changed by auto-loading from EEPROM.<br><br>Reset to 04h. |
| 9:8 | Data Scale | RO | It specifies the scale to apply to the base power value.<br><br>Reset to 00b. |
| 12:10 | PM Sub State | RO | It specifies the power management sub state of the given operation condition. It is initialized to the default sub state.<br><br>Reset to 000b. |
| 14:13 | PM State | RO | It specifies the power management state of the given operation condition. It defaults to the D0 power state.<br><br>Reset to 00b. |
| 17:15 | Type | RO | It specifies the type of the given operation condition. It defaults to the Maximum power state.<br><br>Reset to 111b. |
| 20:18 | Power Rail | RO | It specifies the power rail of the given operation condition.<br><br>Reset to 010b. |
| 31:21 | Reserved | RsvdP | Not Support. |

### 7.2.108 POWER BUDGET CAPABILITY REGISTER – OFFSET 218h

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | System Allocated | RO | When set, it indicates that the power budget for the device is included within the system power budget. The default value may be changed by auto-loading from EEPROM.<br><br>Reset to 0b. |
| 31:1 | Reserved | RsvdP | Not Support. |

### 7.2.109 ACS EXTENDED CAPABILITY HEADER – OFFSET 220h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | PCI Express Extended Capability ID | RO | Read as 000Dh to indicate PCI Express Extended Capability ID for ACS Extended Capability. |
| 19:16 | Capability Version | RO | Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number. |
| 31:20 | Next Capability ID | RO | Read as 000h. No other ECP registers. |

### 7.2.110 ACS CAPABILITY REGISTER – OFFSET 224h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 0 | ACS Source Validation | RO | Indicated the implements of ACS Source Validation.<br><br>Reset to 1b. |
| 1 | ACS Translation Blocking | RO | Indicated the implements of ACS Translation Blocking.<br><br>Reset to 1b. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 2 | ACS P2P Request Redirect | RO | Indicated the implements of ACS P2P Request Redirect.<br><br>Reset to 1b. |
| 3 | ACS P2P Completion Redirect | RO | Indicated the implements of ACS P2P Completion Redirect.<br><br>Reset to 1b. |
| 4 | ACS Upstream Forwarding | RO | Indicated the implements of ACS Upstream Forwarding.<br><br>Reset to 1b. |
| 5 | ACS P2P Egress control | RO | Indicated the implements of ACS P2P Egress control.<br><br>Reset to 1 b. |
| 6 | ACS Direct Translated P2P | RO | Indicated the implements of ACS Direct Translated P2P.<br><br>Reset to 1b. |
| 7 | Reserved | RsvdP | Not Support. |
| 15:8 | Egress Control Vector Size | RO | Encodings 01h –FFh directly indicate the number of applicable bits in the Egress Control Vector.<br><br>Reset to 08h. |
| 16 | ACS Source Validation Enable | RW | Enable the source validation.<br><br>Reset to 0b. |
| 17 | ACS Translation Blocking Enable | RW | Enable ACS Translation Blocking.<br><br>Reset to 0b. |
| 18 | ACS P2P Request Redirect | RW | Enable ACS P2P Request Redirect.<br><br>Reset to 0b. |
| 19 | ACS P2P Completion Redirect Enable | RW | Enable ACS P2P Completion Redirect<br><br>Reset to 0b. |
| 20 | ACS Upstream Forwarding Enable | RW | Enable ACS Upstream Forwarding.<br><br>Reset to 0b. |
| 21 | ACS P2P Egress control Enable | RW | Enable ACS P2P Egress control.<br><br>Reset to 0b. |
| 22 | ACS Direct Translated P2P Enable | RW | Enable ACS Direct Translated P2P.<br><br>Reset to 0b. |
| 31:23 | Reserved | RsvdP | Not Support. |

## 7.2.111 EGRESS CONTROL VECTOR – OFFSET 228h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 7:0 | Egress Control Vector | RW | When a given bit is set, peer-to-peer requests targeting the associated Port are blocked or redirected.<br><br>Reset to 00h. |
| 31:8 | Reserved | RsvdP | Not Support. |

## 7.2.112 LTR EXTENDED CAPABILITY HEADER – OFFSET 230h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 15:0 | PCI Express Extended Capability ID | RO | Read as 0018h to indicate PCI Express Extended Capability ID for LTR Extended Capability. |
| 19:16 | Capability Version | RO | Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number. |


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| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 31:20 | Next Capability ID | RO | Read as 000h. No other ECP registers. |

## 7.2.113 MAX SNOOP LATENCY REGISTER – OFFSET 234h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 9:0 | Max Snoop Latency Value | RW | .Specifies the maximum snoop latency that a device is permitted to request<br><br>Reset to 000h. |
| 12:10 | Max Snoop Latency Scale | RW | This register provides a scale for the value contained within the Maximum Snoop Latency Value field<br><br>Reset to 000b |
| 15:13 | Reserved | RsvdP | Not Support. |

## 7.2.114 MAX NO-SNOOP LATENCY REGISTER – OFFSET 234h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|
| 25:16 | Max No-Snoop Latency Value | RW | .Specifies the maximum no-snoop latency that a device is permitted to request<br><br>Reset to 000h. |
| 28:26 | Max No-Snoop Latency Scale | RW | This register provides a scale for the value contained within the Maximum No-Snoop Latency Value field<br><br>Reset to 000b |
| 31:29 | Reserved | RsvdP | Not Support. |


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# 8 CLOCK SCHEME

The built-in Integrated Reference Clock Buffer of the PI7C9X2G304EL supports three reference clock outputs. The clock buffer feature can be enabled and disabled by strapping the CLKBUF_PD pin.

When CLKBUF_PD pin is asserted low, the clock buffer is enabled. The clock buffer distributes a single 100MHz reference clock input to three Reference Clock Output Pairs, REFCLKO_P[2:0] and REFCLKO_N[2:0]. The clock buffer requires 100MHz differential clock inputs through REFCLKI_P and REFCLKI_N Pins as show in the following table.

When CLKBUF_PD pin is asserted high, the clock buffer is in power down mode and disabled. The 100MHz Reference Clock Output Pairs are disabled, and The PI7C9X2G304EL requires 100MHz differential clock inputs through REFCLKP and REFCLKN Pins as shown in the following table.

**Table 8-1 AC Switching Characteristics**

| Symbol | Parameters | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{IN}$ | Reference Clock Frequency | | 100 | | MHz |
| $T_{rise}$/ $T_{fall}$ [1] | Rise and Fall Time in 20-80% | 175 | | 700 | ps |
| $DT_{rise}$/ $DT_{fall}$ [1] | Rise and Fall Time Variation | | | 125 | ps |
| $T_{pd}$ | Propagation Delay | 2.5 | | 6.5 | ns |
| $V_{swing}$ [1] | Voltage including overshoot | 550 | | 1150 | mV |
| $T_{DC}$ [2] | Duty Cycle | 45 | | 55 | % |

**Note:**
1. Measurement taken from Single Ended waveform.
2. Measurement taken from Differential waveform.
3. In general rule, use ac-coupling when differential input >500mV; use dc-coupling when differential input <400mV, such as LVDS drive with 100 ohm across at the inputs.


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# 9 IEEE 1149.1 COMPATIBLE JTAG CONTROLLER

An IEEE 1149.1 compatible Test Access Port (TAP) controller and associated TAP pins are provided to support boundary scan in PI7C9X2G304EL for board-level continuity test and diagnostics. The TAP pins assigned are TCK, TDI, TDO, TMS and TRST_L. All digital input, output, input/output pins are tested except TAP pins.

## 9.1 INSTRUCTION REGISTER

The IEEE 1149.1 Test Logic consists of a TAP controller, an instruction register, and a group of test data registers including Bypass and Boundary Scan registers. The TAP controller is a synchronous 16-state machine driven by the Test Clock (TCK) and the Test Mode Select (TMS) pins. An independent power on reset circuit is provided to ensure the machine is in TEST_LOGIC_RESET state at power-up.
PI7C9X2G304EL implements a 5-bit Instruction register to control the operation of the JTAG logic. The defined instruction codes are shown in the following table. Those bit combinations that are not listed are equivalent to the BYPASS (11111) instruction.

**Table 9-1 Instruction Register Codes**

| Instruction | Operation Code (binary) | Register Selected | Operation |
|---|---|---|---|
| EXTEST | 00000 | Boundary Scan | Drives / receives off-chip test data |
| SAMPLE | 00001 | Boundary Scan | Samples inputs / pre-loads outputs |
| HIGHZ | 00101 | Bypass | Tri-states output and I/O pins except TDO pin |
| CLAMP | 00100 | Bypass | Drives pins from boundary-scan register and selects Bypass register for shifts |
| IDCODE | 01100 | Device ID | Accesses the Device ID register, to read manufacturer ID, part number, and version number |
| BYPASS | 11111 | Bypass | Selected Bypass Register |
| INT_SCAN | 00010 | Internal Scan | Scan test |
| PHY_TEST_SIG | 01001 | Private | Private |
| MEM_BIST | 01010 | Memory BIST | Memory BIST test |

## 9.2 BYPASS REGISTER

The required bypass register (one-bit shift register) provides the shortest path between TDI and TDO when a bypass instruction is in effect. This allows rapid movement of test data to and from other components on the board. This path can be selected when no test operation is being performed on the PI7C9X2G304EL.

## 9.3 DEVICE ID REGISTER

This register identifies Pericom as the manufacturer of the device and details the part number and revision number for the device.

**Table 9-2 JTAG Device ID Register**

| Bit | Type | Value | Description |
|---|---|---|---|
| 31-28 | RO | 0001 | Version number |
| 27-12 | RO | 0000010100001000 | Last 4 digits (hex) of the die part number |
| 11-1 | RO | 01000111111 | Pericom identifier assigned by JEDEC |
| 0 | RO | 1 | Fixed bit equal to 1'b1 |


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## 9.4 BOUNDARY SCAN REGISTER

The boundary scan register has a set of serial shift-register cells. A chain of boundary scan cells is formed by connected the internal signal of the PI7C9X2G304EL package pins. The VDD, VSS, and JTAG pins are not in the boundary scan chain. The input to the shift register is TDI and the output from the shift register is TDO. There are 4 different types of boundary scan cells, based on the function of each signal pin.

The boundary scan register cells are dedicated logic and do not have any system function. Data may be loaded into the boundary scan register master cells from the device input pins and output pin-drivers in parallel by the mandatory SAMPLE and EXTEST instructions. Parallel loading takes place on the rising edge of TCK.

## 9.5 JTAG BOUNDARY SCAN REGISTER ORDER

**Table 9-3 JTAG Boundary Scan Register Definition**

| Boundary Scan Register Number | Pin Name | Ball Location | Type | Tri-state Control Cell |
|---|---|---|---|---|
| 0 | DWNRST_L[1] | G1 | Output2 | |
| 1 | DWNRST_L[2] | K2 | Output2 | |
| 2 | | | Internal | |
| 3 | TEST1 | L1 | Input | |
| 4 | PERST_L | N1 | Input | |
| 5 | TEST2 | U1 | Input | |
| 6 | TEST3 | V2 | Birdir | 12 |
| 7 | VC1_EN | W1 | Birdir | 12 |
| 8 | PRSNT[1] | Y2 | Birdir | 12 |
| 9 | PRSNT[2] | AA1 | Birdir | 12 |
| 10 | | | Internal | |
| 11 | TEST4 | AC1 | Birdir | 12 |
| 12 | | | Control | |
| 13 | RXPOLINV_DIS | AD2 | Birdir | 12 |
| 14 | TEST5 | AE1 | Birdir | 12 |
| 15 | SMBCLK | AG1 | Birdir | 12 |
| 16 | SMBDATA | AF2 | Birdir | 12 |
| 17 | PWR_SAV | AH2 | Birdir | 12 |
| 18 | SLOTCLK | AP6 | Birdir | 12 |
| 19 | GPIO[0] | AP8 | Birdir | 20 |
| 20 | | | Control | |
| 21 | GPIO[1] | AR5 | Birdir | 22 |
| 22 | | | Control | |
| 23 | GPIO[2] | AR7 | Birdir | 24 |
| 24 | | | Control | |
| 25 | GPIO[3] | AP10 | Birdir | 26 |
| 26 | | | Control | |
| 27 | GPIO[4] | AR9 | Birdir | 28 |
| 28 | | | Control | |
| 29 | GPIO[5] | AR11 | Birdir | 30 |
| 30 | | | Control | |
| 31 | GPIO[6] | AP12 | Birdir | 32 |
| 32 | | | Control | |
| 33 | GPIO[7] | AR13 | Birdir | 34 |
| 34 | | | Control | |
| 35 | SLOT_IMP[1] | AP14 | Birdir | 45 |
| 36 | SLOT_IMP[2] | AR15 | Birdir | 45 |
| 37 | | | Internal | |
| 38 | | | Internal | |
| 39 | TEST6 | AP20 | Birdir | 45 |
| 40 | | | Internal | |
| 41 | PL_512B | AP22 | Birdir | 45 |
| 42 | | | Internal | |


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| Boundary Scan Register Number | Pin Name | Ball Location | Type | Tri-state Control Cell |
|---|---|---|---|---|
| 43 | | | Internal | |
| 44 | | | Internal | |
| 45 | | | Control | |
| 46 | | | Internal | |
| 47 | CLKBUF_PD | AP28 | Birdir | 45 |
| 48 | | | Internal | |
| 49 | | | Internal | |
| 50 | | | Internal | |
| 51 | EECLK | AL35 | Output2 | |
| 52 | EEPD | AH34 | Birdir | 53 |
| 53 | | | Control | |


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# 10 POWER MANAGEMENT

The PI7C9X2G304EL supports D0, D1, D2, D3-hot, and D3-cold Power States. The PCI Express Physical Link Layer of the PI7C9X2G304EL device supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L3 Power States.

During the transition from D3-hot to D3-cold state, the main power supplies of VDDC and VDDR are turned off to save power while keeping the VDDCAUX and VAUX with the auxiliary power supplies to maintain all necessary information to be restored to the full power D0 state. PI7C9X2G304EL has been designed to have sticky registers that are powered by auxiliary power supplies. PI7C9X2G304EL forwards power management messages to the upstream Switches or root complex.

PI7C9X2G304EL also supports ASPM (Active State Power Management) to facilitate the link power saving.


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# 11 POWER SEQUENCE

As long as PERST# is active, all PCI Express functions are held in reset. The main supplies ramp up to their specified levels (3.3V). Sometime during this stabilization time, the REFCLK starts and stabilizes. After there has been time (100 ms) for the power and clock to become stable, PERST# is deasserted high and the PCI Express functions can start up.

It is recommended to power up the I/O voltage (3.3V) first and then the core voltage (1.0V) or power up I/O voltage and core voltage simultaneously for both Aux and Main power rails.

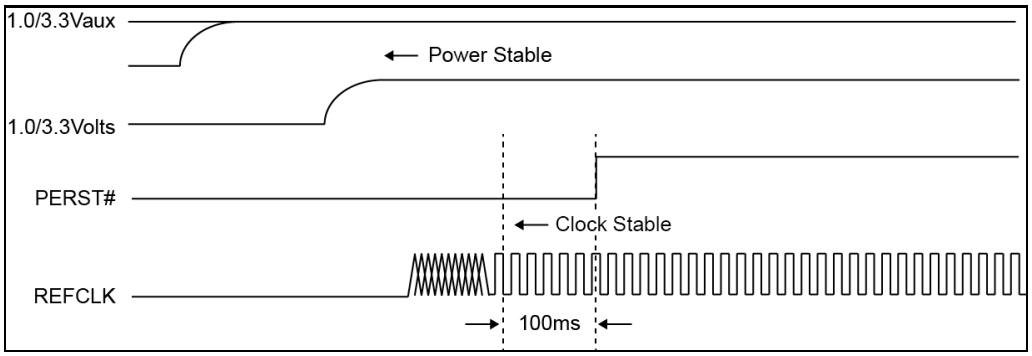


**Figure 11-1 Initial Power-Up Sequence**

Power-down sequence is the reverse of power-up sequence.


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# 12 ELECTRICAL AND TIMING SPECIFICATIONS

## 12.1 ABSOLUTE MAXIMUM RATINGS

**Table 12-1 Absolute Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

| Item | Absolute Max. Rating |
|---|---|
| Storage Temperature ($T_{store}$) | -65°C to 150°C |
| Junction Temperature ($T_j$) | 125 °C |
| Digital core and analog supply voltage to ground potential (VDDC, AVDD and VDDCAUX) | -0.3v to 1.5v |
| Digital I/O and analog high supply voltage to ground potential (VDDR, CVDDR, AVDDH and VAUX) | -0.3v to 4.0v |
| DC input voltage for Digital I/O signals | -0.3v to 4.0v |

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## 12.2 DC SPECIFICATIONS

**Table 12-2 DC Electrical Characteristics**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VDDC[1] | Digital Core Power | 0.95 | 1.0 | 1.1 | V |
| VDDR | Digital I/O Power | 3.0 | 3.3 | 3.6 | |
| CVDDR | Reference Clock Power | 3.0 | 3.3 | 3.6 | |
| VDDCAUX | Auxiliary Core Power | 0.95 | 1.0 | 1.1 | |
| VAUX | Auxiliary I/O Power | 3.0 | 3.3 | 3.6 | |
| AVDD | PCI Express Analog Power | 0.95 | 1.0 | 1.1 | |
| AVDDH | PCI Express Analog High Voltage Power | 3.0 | 3.3 | 3.6 | |
| $V_{IH}$ | Input High Voltage | 2.0 | | 5.5 | |
| $V_{IL}$ | Input Low Voltage | -0.3 | | 0.8 | |
| $V_{OH}$ | Output High Voltage | 2.4 | | | |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | |
| $R_{PU}$ | Pull-up Resistor | 63K | 92K | 142K | Ω |
| $R_{PD}$ | Pull-down Resistor | 57K | 91K | 159K | |
| RST#$_{Slew}$[2] | PERST_L Slew Rate | 50 | | | mV/ns |

**Note:**
1. In order to support auxiliary power management fully, it is recommended to have VDDC and VDDCAUX separated.
2. The min. value for PERST_L Slew Rate is 50 mV/ns, which translates to the requirement that the time for PERST_L from 0V to 3.3V should be less than 66 ns.

## 12.3 AC SPECIFICATIONS

**Table 12-3 PCI Express Interface - Differential Transmitter (TX) Output (5.0 Gbps) Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Unit Interval | UI | 199.94 | 200.0 | 200.06 | ps |
| Differential p-p TX voltage swing | $V_{TX-DIFF-P-P}$ | 800 | - | - | mV ppd |


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| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Low power differential p-p TX voltage swing | $V_{TX-DIFF-P-P-LOW}$ | 400 | - | - | mV ppd |
| TX de-emphasis level ratio | $V_{TX-DE-RATIO-3.5dB}$ | -3.0 | - | -4.0 | dB |
| TX de-emphasis level ratio | $V_{TX-DE-RATIO-6dB}$ | -5.5 | | -6.5 | dB |
| Transmitter Eye including all jitter sources | $T_{TX-EYE}$ | 0.75 | - | - | UI |
| TX deterministic jitter > 1.5 MHz | $T_{TX-HF-DJ-DD}$ | - | - | 0.15 | UI |
| TX RMS jitter < 1.5 MHz | $T_{TX-LF-RMS}$ | - | - | 3.0 | Ps RMS |
| Transmitter rise and fall time | $T_{TX-RISE-FALL}$ | 0.15 | - | - | UI |
| TX rise/fall mismatch | $T_{RF-MISMATCH}$ | - | - | 0.1 | UI |
| Maximum TX PLL Bandwidth | $BW_{TX-PLL}$ | - | - | 16 | MHz |
| Minimum TX PLL BW for 3dB peaking | $BW_{TX-PLL-LO-3DB}$ | 8 | - | - | MHz |
| TX PLL peaking with 8 MHz min BW | $PKG_{TX-PLL1}$ | - | - | 3.0 | dB |
| DC Differential TX Impedance | $Z_{TX-DIFF-DC}$ | 80 | - | 120 | Ω |
| Transmitter Short-Circuit Current Limit | $I_{TX-SHORT}$ | - | - | 90 | mA |
| TX DC Common Mode Voltage | $V_{TX-DC-CM}$ | 0 | - | 3.6 | V |
| Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle | $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$ | 0 | - | 100 | mV |
| Absolute Delta of DC Common Mode Voltage between D+ and D– | $V_{TX-CM-DC-LINE-DELTA}$ | 0 | - | 25 | mV |
| Electrical Idle Differential Peak Output Voltage | $V_{TX-IDLE-DIFF-AC-p}$ | 0 | - | 20 | mV |
| DC Electrical Idle Differential Output Voltage | $V_{TX-IDLE-DIFF-DC}$ | 0 | - | 5 | mV |
| The Amount of Voltage Change Allowed During Receiver Detection | $V_{TX-RCV-DETECT}$ | - | - | 600 | mV |
| Lane-to-Lane Output Skew | $L_{TX-SKEW}$ | - | - | 500 ps + 4 UI | ps |

**Table 12-4 PCI Express Interface - Differential Transmitter (TX) Output (2.5 Gbps) Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Unit Interval | UI | 399.88 | 400.0 | 400.12 | ps |
| Differential p-p TX voltage swing | $V_{TX-DIFF-P-P}$ | 800 | - | - | mV ppd |
| Low power differential p-p TX voltage swing | $V_{TX-DIFF-P-P-LOW}$ | 400 | - | - | mV ppd |
| TX de-emphasis level ratio | $V_{TX-DE-RATIO}$ | -3.0 | - | -4.0 | dB |
| Minimum TX eye width | $T_{TX-EYE}$ | 0.75 | - | - | UI |
| Maximum time between the jitter median and max deviation from the median | $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | - | - | 0.125 | UI |
| Transmitter rise and fall time | $T_{TX-RISE-FALL}$ | 0.125 | - | - | UI |
| Maximum TX PLL Bandwidth | $BW_{TX-PLL}$ | - | - | 22 | MHz |
| Maximum TX PLL BW for 3dB peaking | $BW_{TX-PLL-LO-3DB}$ | 1.5 | - | - | MHz |
| Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle | $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$ | 0 | - | 100 | mV |
| Absolute Delta of DC Common Mode Voltage between D+ and D– | $V_{TX-CM-DC-LINE-DELTA}$ | 0 | - | 25 | mV |
| Electrical Idle Differential Peak Output Voltage | $V_{TX-IDLE-DIFF-AC-p}$ | 0 | - | 20 | mV |
| The Amount of Voltage Change Allowed During Receiver Detection | $V_{TX-RCV-DETECT}$ | - | - | 600 | mV |
| Transmitter DC Common Mode Voltage | $V_{TX-DC-CM}$ | 0 | - | 3.6 | V |
| Transmitter Short-Circuit Current Limit | $I_{TX-SHORT}$ | - | - | 90 | mA |
| DC Differential TX Impedance | $Z_{TX-DIFF-DC}$ | 80 | 100 | 120 | Ω |
| Lane-to-Lane Output Skew | $L_{TX-SKEW}$ | - | - | 500 ps + 2 UI | ps |

**Table 12-5 PCI Express Interface - Differential Receiver (RX) Input (5.0 Gbps) Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Unit Interval | UI | 199.94 | 200.0 | 200.06 | ps |
| Differential RX Peak-to-Peak Voltage | $V_{RX-DIFF-PP-CC}$ | 120 | - | 1200 | mV |
| Total jitter tolerance | $TJ_{RX}$ | 0.68 | - | - | UI |


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| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Receiver DC common mode impedance | $Z_{RX-DC}$ | 40 | - | 60 | Ω |
| RX AC Common Mode Voltage | $V_{RX-CM-AC-P}$ | - | - | 150 | mV |
| Electrical Idle Detect Threshold | $V_{RX-IDLE-DET-DIFFp-p}$ | 65 | - | 175 | mV |

**Table 12-6 PCI Express Interface - Differential Receiver (RX) Input (2.5 Gbps) Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Unit Interval | UI | 399.88 | 400.0 | 400.12 | ps |
| Differential RX Peak-to-Peak Voltage | $V_{RX-DIFF-PP-CC}$ | 175 | - | 1200 | mV |
| Receiver eye time opening | $T_{RX-EYE}$ | 0.4 | - | - | UI |
| Maximum time delta between median and deviation from median | $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | - | - | 0.3 | UI |
| Receiver DC common mode impedance | $Z_{RX-DC}$ | 40 | - | 60 | Ω |
| DC differential impedance | $Z_{RX-DIFF-DC}$ | 80 | - | 120 | Ω |
| RX AC Common Mode Voltage | $V_{RX-CM-AC-P}$ | - | - | 150 | mV |
| DC input CM input impedance during reset or power down | $Z_{RX-HIGH-IMP-DC}$ | 200 | - | - | kΩ |
| Electrical Idle Detect Threshold | $V_{RX-IDLE-DET-DIFFp-p}$ | 65 | - | 175 | mV |
| Lane to Lane skew | $L_{RX-SKEW}$ | - | - | 20 | ns |

## 12.4 OPERATING AMBIENT TEMPERATURE

**Table 12-7 Operating Ambient Temperature**

(Above which the useful life may be impaired.)

| Item | Min. | Max. | Units |
|---|---|---|---|
| Ambient Temperature with power applied | -40 | 85 | °C |

**Note:**
Exposure to high temperature conditions for extended periods of time may affect reliability.

## 12.5 POWER CONSUMPTION

**Table 12-8 Power Consumption**

| Active Lane per Port | 1.0VDDC | | 1.0VAUX | | 1.0AVDD | | 3.3AVDDH | | 3.3VDDR | | 3.3VAUX | | Total | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Typ | Max | |
| 1/1/1 | 123.20 | 327.91 | 2.20 | 2.42 | 144.10 | 346.06 | 35.31 | 38.84 | 319.44 | 351.38 | 0.03 | 0.03 | 624.28 | 1,066.65 | mW |
| 1/1/1, ec[1] | 123.20 | 327.91 | 2.20 | 2.42 | 144.10 | 346.06 | 35.31 | 38.84 | 6.60 | 7.26 | 0.03 | 0.03 | 311.44 | 722.52 | mW |

**Note**:
[1]: Use external clock buffer, Disable internal clock buffer.
Test Conditions:
- Typical power measured under the conditions of 1.0V/ 3.3V power rail without device usage on all downstream ports.
- Maximum power measured under the conditions of 1.1V/ 3.63V with PCIe2 devices usage on all downstream ports.
- Ambient Temperature at 25°C
- Power consumption in the table is a reference, be affected by various environments, bus traffic and power supply etc.


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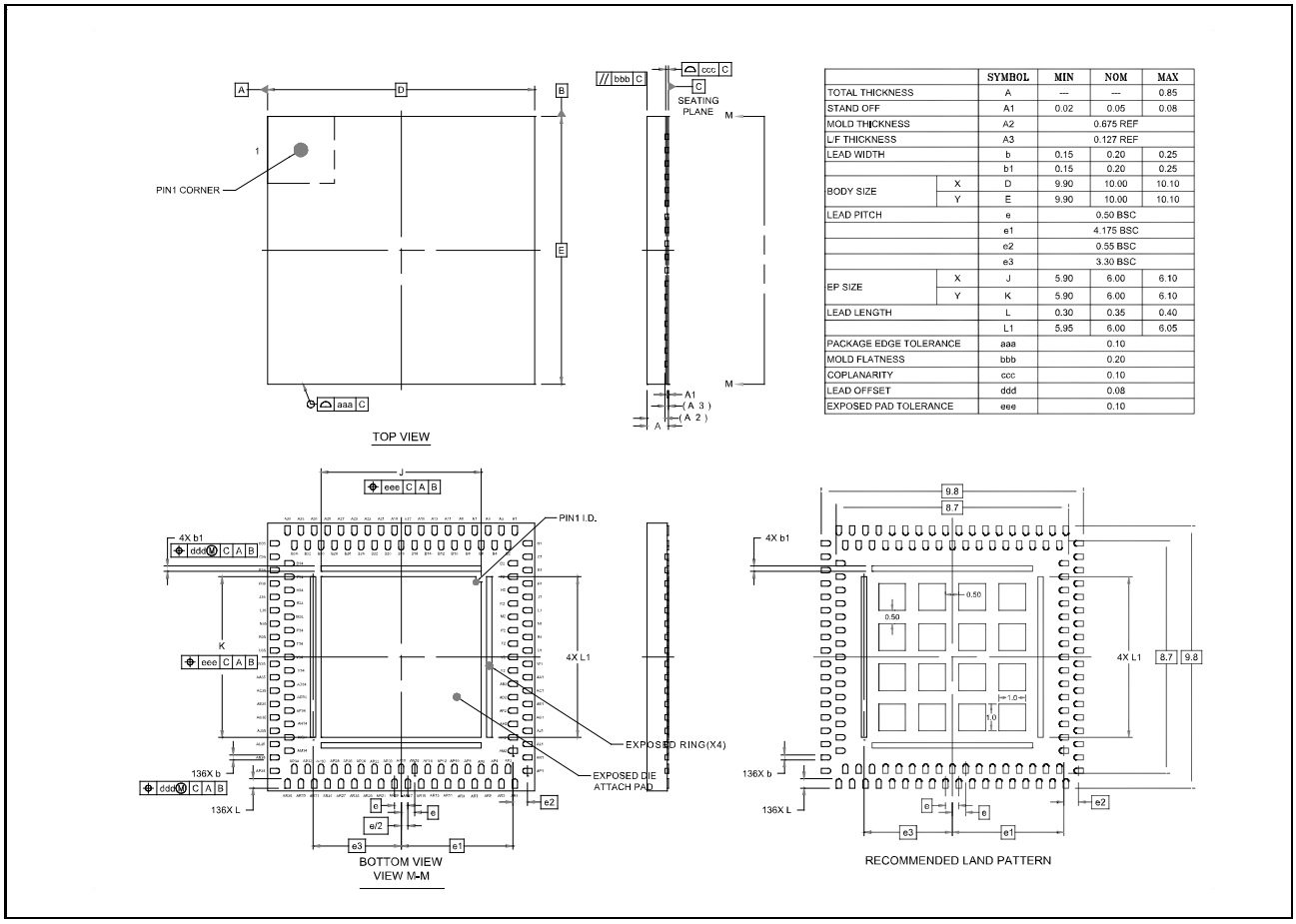
# 13 PACKAGE INFORMATION

The package of PI7C9X2G304EL is a 10mm x 10mm aQFN (136 Pin) package. The following are the package information and mechanical dimension:




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | --- | --- | 0.85 |
| STAND OFF | | A1 | 0.02 | 0.05 | 0.08 |
| MOLD THICKNESS | | A2 | | 0.675 REF | |
| L/F THICKNESS | | A3 | | 0.127 REF | |
| LEAD WIDTH | | b | 0.15 | 0.20 | 0.25 |
| | | b1 | 0.15 | 0.20 | 0.25 |
| BODY SIZE | X | D | 9.90 | 10.00 | 10.10 |
| | Y | E | 9.90 | 10.00 | 10.10 |
| LEAD PITCH | | e | | 0.50 BSC | |
| | | e1 | | 4.175 BSC | |
| | | e2 | | 0.55 BSC | |
| | | e3 | | 3.30 BSC | |
| EP SIZE | X | J | 5.90 | 6.00 | 6.10 |
| | Y | K | 5.90 | 6.00 | 6.10 |
| LEAD LENGTH | | L | 0.30 | 0.35 | 0.40 |
| | | L1 | 5.95 | 6.00 | 6.05 |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.10 | |
| MOLD FLATNESS | | bbb | | 0.20 | |
| COPLANARITY | | ccc | | 0.10 | |
| LEAD OFFSET | | ddd | | 0.08 | |
| EXPOSED PAD TOLERANCE | | eee | | 0.10 | |

**Figure 13-1 Package outline drawing**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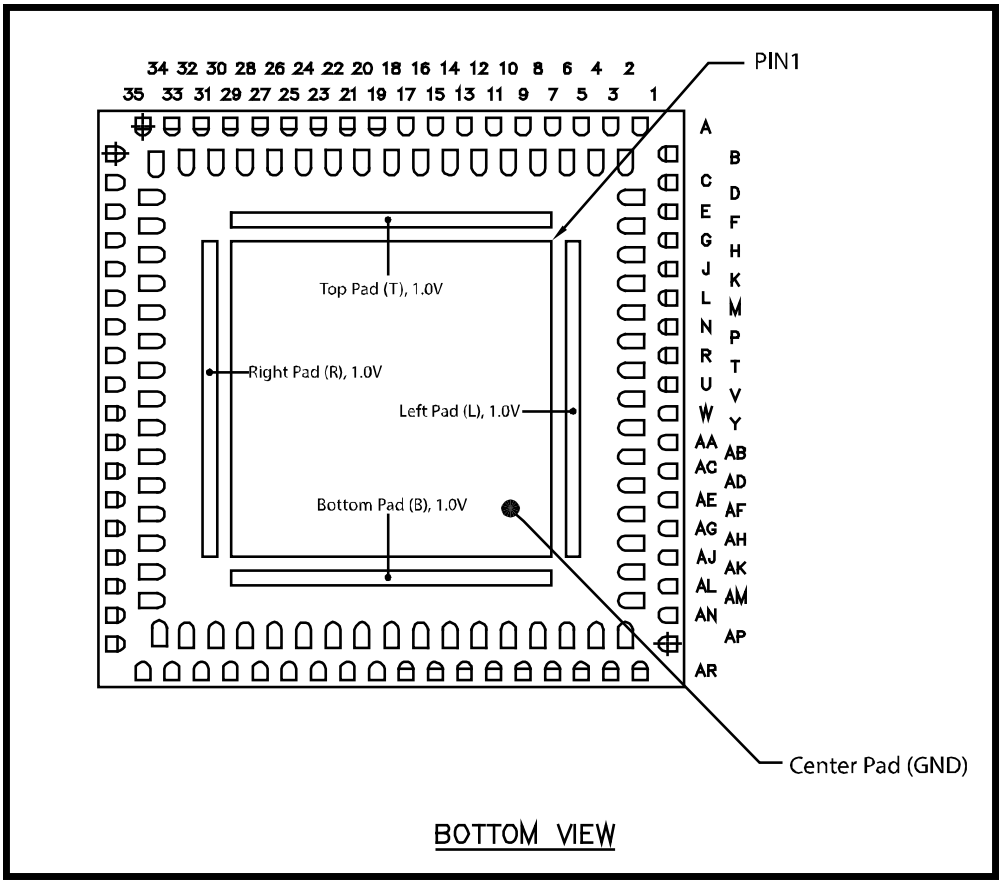


**Figure 13-2 Package bottom view**


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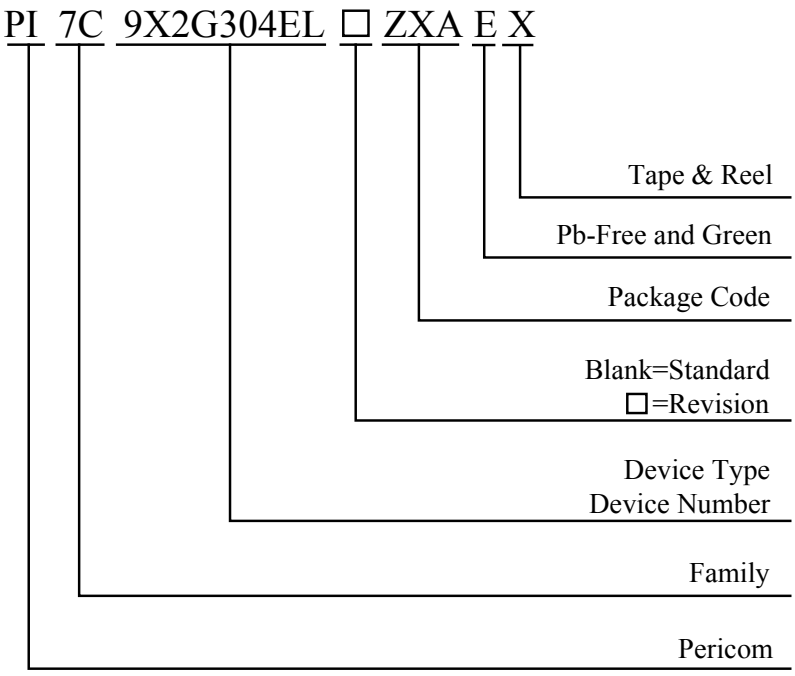
# 14 ORDERING INFORMATION

| Part Number | Temperature Range | Package | Pb-Free & Green |
|---|---|---|---|
| PI7C9X2G304EL□ZXAEX | -40° to 85°C<br>(Industrial Temperature) | 136-pin aQFN<br>10mm x 10mm | Yes |





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