Evaluation Board User Guide
UG-075

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AD9516-x, AD9517-x, and AD9518-x Evaluation Board

FEATURES

- Simple power connection using 6 V wall adapter and on-board LDO voltage regulators
- LDOs are easily bypassed for power measurements
- 8 ac-coupled differential LVPECL SMA connectors
- 2 ac-coupled LVPECL differential headers
- 2 dc-coupled differential LVDS SMA connectors that are reconfigurable to four CMOS SMA connectors
- 2 dc-coupled LVDS differential headers that are reconfigurable to four CMOS connectors
- SMA connectors for
  - 2 reference inputs
  - Charge pump output
  - Clock distribution input
- USB connection to PC
- Microsoft Windows-based evaluation software with simple graphical user interface
- On-board PLL loop filter
- Easy access to digital I/O and diagnostic signals via I/O header
- Status LEDs for diagnostic signals

APPLICATIONS

- Clocking of analog-to-digital and digital-to-analog converters up to 2.9 GHz
- Networking and communications line cards
- Test and measurement equipment
- Wireless base stations, controllers
- Clock cleanup/jitter attenuation
- Clock distribution

GENERAL DESCRIPTION

The AD9516-x, AD9517-x, and AD9518-x are very low noise PLL clock synthesizers featuring an integrated VCO, clock dividers, and up to 14 outputs. The AD9516 features automatic holdover and a flexible reference input circuit allowing for very smooth reference clock switching. The AD9516 family also features the necessary provisions for an external VCXO.

The AD9516 evaluation board is a compact, easy-to-use platform for evaluating all features of the AD9516. This user guide covers all six versions of the AD9516 family, as well as the AD9517 and AD9518 families (hereafter referred to as AD951x). The AD9516, AD9517, and AD9518 differ only in package size, and the number of outputs. The evaluation software main window for the AD9517 and AD9518 reflects fewer outputs, but the operation is identical for all devices.

Although the Quick Start Guide to the AD9516 PLL section applies specifically to the AD9516-3, increasing the N (feedback) divider and channel divider increases the VCO frequency to the allowable frequency range of other AD9516 versions.

For the AD9516-5, which lacks an internal VCO, certain portions of this document that apply to the internal VCO (such as VCO calibration) can be ignored.

For convenience, detailed information from the AD9516 data sheet has been included here. Use this user guide in conjunction with the AD9516, AD9517, and AD9518 data sheets, as well as additional documentation available at www.analog.com.

AD9516 EVALUATION BOARD

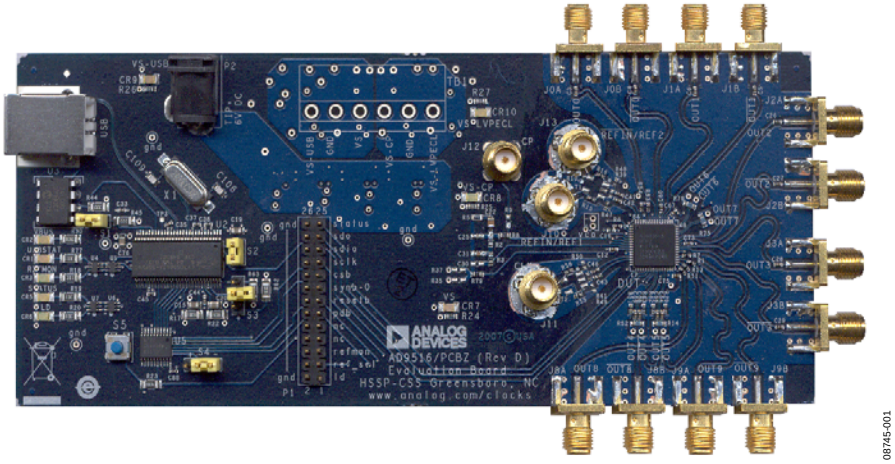

Figure 1.

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REVISION HISTORY

1/10—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The following instructions are for setting up the physical connections to the AD951x evaluation board.

When connecting the evaluation board to a PC for the first time, the user must install the evaluation software prior to connecting the evaluation board.

POWER AND PC CONNECTIONS

Use the following steps to connect the AD951x evaluation board to its power supply and lab equipment.

1. Install the AD951x evaluation software. Administrative privileges are required for installation. The 64-bit versions of Windows® are not supported.
2. Connect the wall power supply to the main power connector labeled P2. The following five LEDs should be on: CR1 (USBSTAT), CR7 (VS), CR8 (VS-CP), CR9 (VS_USB), and CR10 (VS_LVPECL).
3. Connect the USB cables to the evaluation board and the computer. The red LED labeled CR2 (VBUS) on the AD951x evaluation board should illuminate and the CR1 (USBSTAT) LED should start blinking.
4. If the **Found New Hardware Wizard** window automatically appears when the evaluation board is connected, select **Install the software automatically** and click **Next**.
   The **Found New Hardware Wizard** window may appear twice, and a system restart may be required.
   Refer to the Evaluation Board Software section for details on running the AD951x evaluation board software.

If the USBSTAT LED is not blinking, ensure that:

- Jumpers are installed on Position S1 and Position S2.
- The jumper on S4 is across the center pin and the minus symbol.
- The USB port on the PC is operational and that the USB cable is not damaged.

SIGNAL CONNECTIONS

To connect signals, use the following steps:

1. Connect a signal generator to the J10 SMA connector. By default, the reference inputs on this evaluation board are ac-coupled and terminated 50 Ω to ground. An amplitude setting of 0 dBm to 6 dBm is fine.
2. If the user wants to connect a signal to REF2, connect that signal to the J13 SMA connector. DC-coupling is recommended in applications requiring automatic hitless reference switching. There is a possibility that the device receive buffer can chatter when an ac-coupled clock stops toggling.
3. Connect an oscilloscope, spectrum analyzer, or other lab equipment to any of the J0 to J9 SMA connectors on the right side of the board.

OUT0 through OUT5 are ac-coupled LVPECLs. OUT8 and OUT9 are dc-coupled and have no output termination. These allow the user to evaluate the AD951x output driver in either LVDS or CMOS mode.

BYPASSING THE WALL POWER SUPPLY

To bypass the wall power supply, remove the following ferrite beads (on the backside of the board): F7, F4, F2, and F6. Connect a bench power supply to TB1 on the evaluation board. This is useful for making AD951x power consumption measurements.

BYPASSING THE PLL (CLOCK DISTRIBUTION ONLY)

To bypass the PLL, connect a signal generator to the SMA connector labeled CLK. By default, this connection is ac-coupled to the CLK pin and terminated with a 50 Ω resistor to ground. Refer to the Evaluation Software Components section for details on running the AD951x evaluation board software.

USING AN EXTERNAL VCXO

To use an external VCXO, use the following steps.

1. Install a 0 Ω resistor at R9 and remove R8.
2. Connect a loop filter and external VCO/VCXO input to J12.
3. Connect the external VCO/VCXO output to the J11 SMA connector (CLK input).

EVALUATION BOARD SOFTWARE

Use the following instructions to set up the AD951x evaluation board software.

SOFTWARE INSTALLATION

Do not connect the evaluation board until the software installation is complete.

1. The evaluation software and documentation can be downloaded from www.analog.com.
2. If the software was downloaded, skip to Step 3.If installing from the CD, insert the AD951x evaluation software CD. Double-click **My Computer** and then double-click the **AD9516_17_18EV** CD icon. A window opens showing the contents of the CD divided into four sections: **Datasheet**, **Layout**, **Schematic**, and **Software**. The file named **readme.txt** contains a description of the CD contents as well as any additional instructions or information. Double-click the **Software** folder.
3. Double-click **AD9516_17_18Eval_Setup1.1.0.exe**. (Note that the website may have a version newer than Version 1.1.0.) Follow the installation instructions. The default location for installation of the evaluation software is: **C:\Program Files\Analog Devices\AD9516 Eval Software**.

RUNNING THE SOFTWARE

Power up and connect the evaluation board to the PC. See Evaluation Board Hardware section for details on the various connectors on the evaluation board.

1. Double-click **AD9516_17_18 Eval Software** to run the AD951x evaluation software. Depending on whether the evaluation board was found by the software, either light blue text appears in a pop-up window, indicating that the evaluation board was found, or red text appears, indicating that the evaluation board was not found.
2. If the evaluation board is found, click anywhere in the pop-up window with the **Evaluation Software Ready** message, and the main window for the software appears. Proceed to the Evaluation Software Components section for details about running the software.
   If the evaluation board is not found, a dialog box appears allowing you to select which AD951x evaluation board is connected while the software runs in standalone mode.

See the Evaluation Board Hardware section for information on connecting the evaluation board.

If the evaluation board is connected while the evaluation software is running, the window in Figure 2 appears to prompt you to load the evaluation board with the evaluation software settings or read the evaluation board settings into the software.

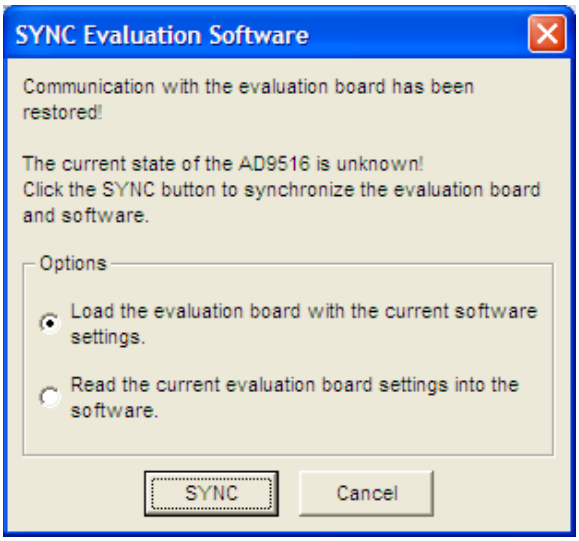

Figure 2. SYNC Evaluation Software Window

If the evaluation board was not automatically detected when it was connected, you can also select the **Select Evaluation Board** option from the **I/O** menu (see Figure 24), and select **Ezssp-0**, **Ezssp-1**, or **Ezssp-2**.

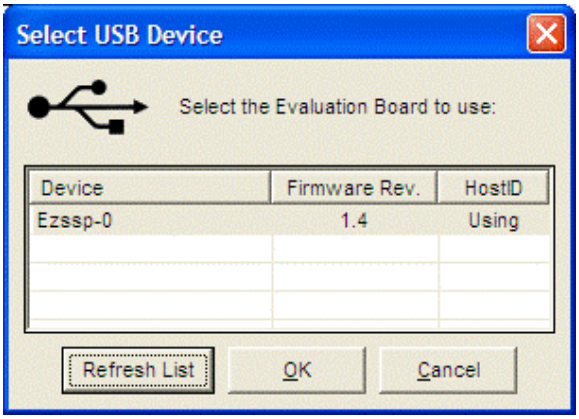

Figure 3. Select USB Device Window

See the Evaluation Software Components section for a description of the evaluation software features, or the Quick Start Guide to the AD9516 PLL section for details on the individual blocks of the AD951x.

QUICK START GUIDE TO THE AD9516 PLL

When the evaluation software is installed, the evaluation board is connected, and the software is loaded, use the following steps to configure and lock the PLL. These steps assume that the input signal is present, the evaluation board has not been modified, and that the PLL loop filter is suitable for the user's application.

This quick start guide covers only simple PLL operation to start the PLL. See the AD9516 data sheet and Evaluation Software Components section for a detailed explanation of the various AD9516 features.

The following case is an example for the AD9516-3 using the values in Table 1.

Table 1.

Parameter	Value
Input Frequency	20 MHz on REF1
Output Frequency	200 MHz on OUT1
Reference Divider	2
Phase Detector Frequency	10 MHz
Feedback Divider	200
VCO Frequency	2000 MHz
VCO Divider	2
Channel Divider	5

1. Turn the PLL on by selecting **Normal Op** from the **PLL MODE** box found at the top of the main window (see Figure 8).
2. Enter the intended reference input frequency (in megahertz) in the **REF 1 (MHz)** box at the upper left corner of the main window.
3. Click the triangular buffer symbol immediately to the right of the input reference frequency (see Figure 4) boxes to load the **Reference Input Control** window shown in Figure 5. Turn the REF1 reference input buffer on by selecting the **Enable REF1** check box, and then clicking **OK**.

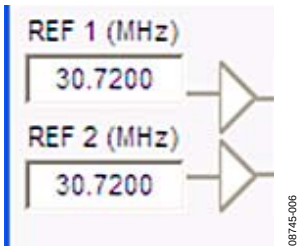

Figure 4. Buffer Symbol

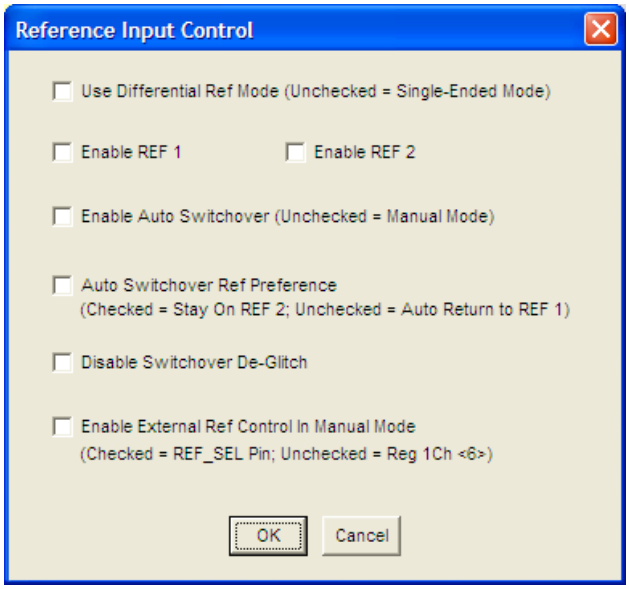

Figure 5. Reference Input Control Window

4. When the window closes, the **WRITE** button under the **REGISTER W/R** section in the main window blinks red. This indicates there are settings that have not been loaded to the AD9516 evaluation board. Click the blinking red **WRITE** button to load these settings to the evaluation board.
5. Select the VCO as the input to the clock distribution circuitry by clicking the mux symbol that is located immediately to the right of the **VCO (MHz)** box (see Figure 6).

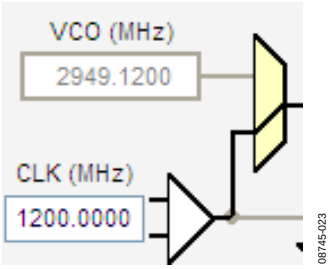

Figure 6. Buffer Symbol

When the VCO is selected, the border of the **VCO (MHz)** box changes from gray to black. The current VCO frequency is shown in the **VCO (MHz)** box.

6. Program the R (reference) divider by clicking the **R DIVIDER** box at the top of the main window. Set the desired value and click **OK** (see Figure 12).
7. Program the N (feedback) divider by clicking the **N DIVIDER** box at top of the main window. Set the desired value and click **OK**. For the example, N = 200 can use 8/9 dual modulus mode with A = 0 and B = 25.
8. Set the charge pump current by clicking the **CHARGE PUMP** box in the upper right corner of the main window, and then click **OK**.
9. Note that if the desired configuration has the phase detector frequency above 50 MHz, an antibacklash pulse width of 1.3 ns may work better. This setting is accessed by clicking the **PFD** button to the left of the **CHARGE PUMP** box. However, this setting normally does not need to be modified.
10. Set the VCO divider by clicking the green **VCO** box in the center of the main window, immediately to the left of the **Cal VCO** button.
11. Power down unused drivers, click the numbered triangular symbol on the right side of the main window (see Figure 7), select **2 - Safe Power Down**, and click **OK** (see Figure 20).

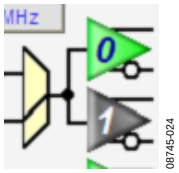

Figure 7. Driver Symbol

12. Set the channel dividers by clicking **DIVIDER 0** through **DIVIDER 4** and enter the divider ratio.
13. Click the flashing red **WRITE** button under the **REGISTER W/R** section. This loads the desired settings to the AD951x evaluation board,
14. Click the blinking yellow **Cal VCO** button to load the VCO calibration window. The default VCO divide ratio (16) works for all applications. Click the **Cal VCO** button in the **Calibrate VCO** window to begin calibration (see Figure 17). The PLL should now be locked and the **LD** (lock detect) LED on the left side of the board should be on.

EVALUATION SOFTWARE COMPONENTS

MAIN WINDOW

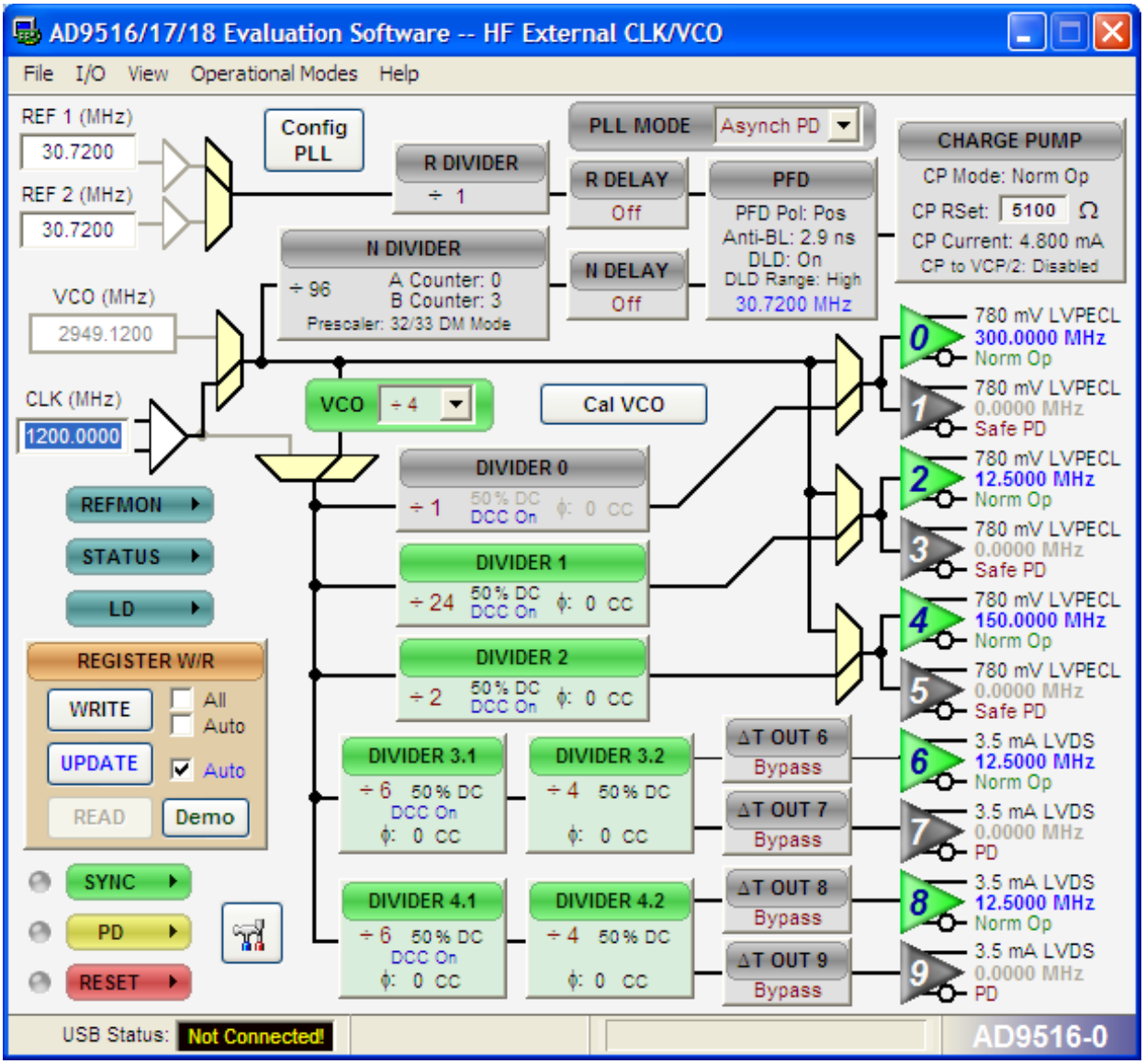

Figure 8. Evaluation Software Main Window

The AD951x evaluation software is composed of subsections that correspond to the major functional blocks of the AD951x. These subsections are listed in the following sections and each of these has its own window. From the main window, each functional block can be accessed by clicking that block in the main window.

When a subwindow closes after clicking **OK**, the **WRITE** box on the main window (under the **REGISTER W/R** section) may blink red. This indicates that there are settings that have not been loaded to the AD951x evaluation board. Clicking the blinking red **WRITE** button loads these settings to the evaluation board.

PLL REFERENCE INPUT WINDOW

The **Reference Input Control** window is shown in Figure 10 and is accessed by clicking either of the triangular buffer symbols immediately to the right of the **REF 1 (MHz)** and **REF 2 (MHz)** input reference frequency boxes (see Figure 9).

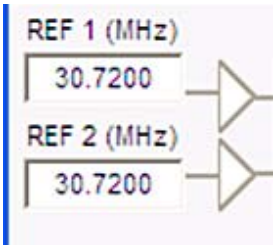

Figure 9. Buffer Symbol

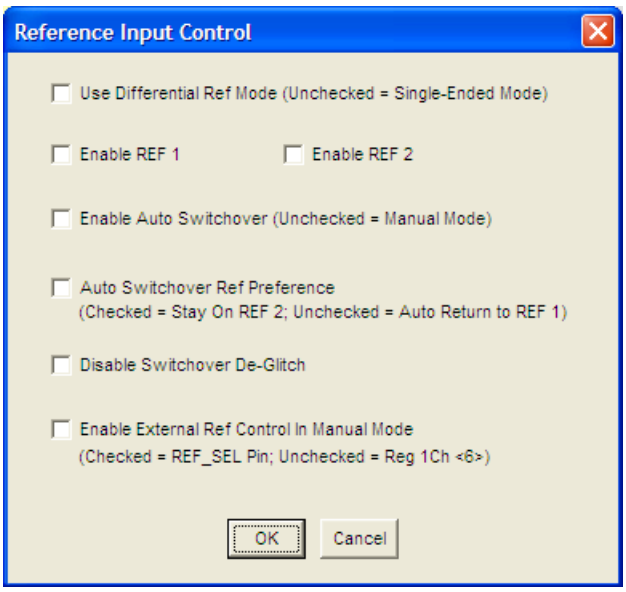

Figure 10. Reference Input Control Window

This window is used to enable the PLL reference inputs, which are powered down by default.

Select **Enable REF 1**, or **Enable REF 2**, or both to enable the appropriate reference input, and click **OK** when finished. If a differential input is used, select the **Use Differential Ref Mode (Unchecked = Single-Ended Mode)** check box. Note that this mode should not be used simultaneously with **Enable REF 1** or **Enable REF 2**.

The remaining four check boxes control the reference switchover modes. If **Disable Switchover De-Glitch** is activated, the AD951x maintains the phase relationship between the active input and PLL output during a reference switchover. Otherwise, the AD951x minimizes the phase disturbance at the output during a reference switchover.

PLL CONFIGURATION WINDOW

The **PLL Configuration** window shown in Figure 11 is opened by clicking the **Config PLL** button on the main screen. This window has three sections: **SyncB Counter Reset Mode**, **ReadBack Registers**, and **Settings**.

The **SyncB Counter Reset Mode** section indicates whether the R, A, and B counters are reset when the $\overline{\text{SYNC}}$ pin is activated, and controls R0x019[7:6]. See the AD951x data sheet for more details.

The **ReadBack Registers** section allows you to see the current value of the read-only PLL status register (Address 0x01F). This function is very useful for ensuring that the AD951x VCO has finished VCO calibration, and that the PLL is locked.

The **Settings** section controls the various PLL settings such as hold-over. The AD951x data sheet describes these functions in detail.

Note that the automatic holdover feature should not be enabled during VCO calibration.

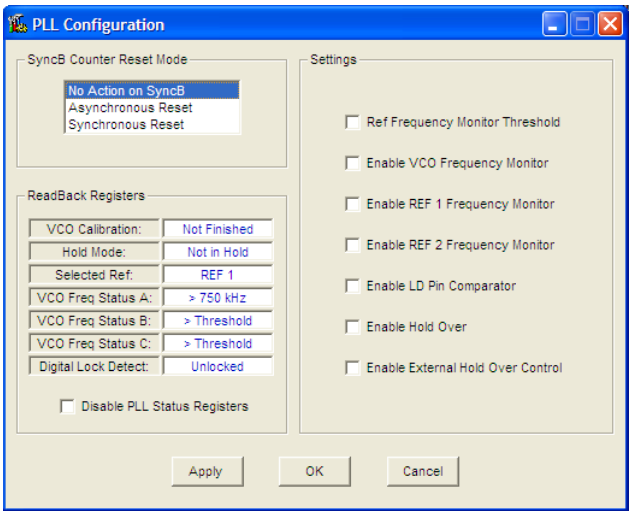

Figure 11. PLL Configuration Window

REFMON, STATUS, AND LD BUTTONS

These three blue buttons (**REFMON**, **STATUS**, and **LD**) allow you to select which signals appear at the REFMON, STATUS, and LD pins at Connector P1. Connector P1 is located in the center of the evaluation board. The pins in the left column of Connector P1 are ground pins, and the ones in the right column are signal pins.

There are many useful diagnostic signals available at these pins. The R divider output is particularly useful. In the example used in the Quick Start Guide to the AD9516 PLL section, the 80 kHz signal is visible on the STATUS pin to ensure that the reference inputs and R divider are working properly.

Dynamic signals (such as the R divider output) are primarily intended for diagnostics. These diagnostic signals may adversely affect PLL performance in critical applications if left on in normal operation.

REGISTER W/R BOX

The **REGISTER W/R** (write/read) box has four buttons and three check boxes.

The **WRITE** button transfers the values stored in the evaluation software to the evaluation board. It blinks red when register values have changed.

The **READ** button transfers the values stored in the evaluation board to the evaluation software.

The **UPDATE** button issues an I/O update command by writing 0x01 to Register 0x232.

Selecting the **All** check box transfers all of the registers when the **WRITE** button is clicked. When this check box is cleared, only the registers whose value has changed are written.

Selecting the **Auto** check box adjacent to the **WRITE** box forces the evaluation software to write the register changes to the evaluation board automatically when they occur.

Selecting the **Auto** check box adjacent to the **UPDATE** box forces the evaluation software to issue an I/O update command whenever registers are written to the AD951x. It is checked by default.

SYNC, PD (POWER DOWN), AND RESET BUTTONS

The **SYNC**, **PD**, and **RESET** buttons allow you to control the $\overline{\text{SYNC}}$, PD, and RESET pins on the AD951x.

Each button has three options: **Strobe**, **Latch**, and **Release**. **Strobe** activates the pin, and then releases it. **Latch** holds the pin active until the **Release** command is issued.

REFERENCE (R) DIVIDER WINDOW

The **R Divider** window shown in Figure 12 is accessed by clicking the **R DIVIDER** box on the main window. It allows you to set the reference divider. If this box is colored gray, the PLL is off. To turn the PLL on, click the **PLL MODE** box at the top of the main window, and select **Norm Op**.

The **R Divider** window has a check box for holding the R divider in reset. When the R divider is held in reset, the PLL loop is opened. Therefore, this feature is seldom used.

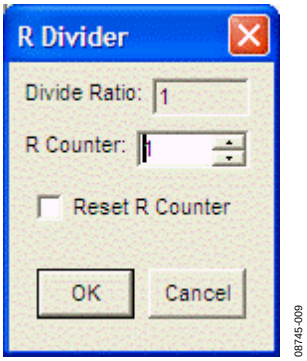

Figure 12. R Divider Window

R AND N DELAY WINDOW

The AD951x features two delay circuits (one on the reference divider path, and one on the feedback divider path) that allow the user to control the static phase offset between the reference input and the PLL output. The **R Path Delay** window shown in Figure 13 is accessed by clicking the **R DELAY** button on the main screen. The **R DELAY** box is identical to the **N DELAY** box. These delay settings allow you to vary the static phase offset of the PLL.

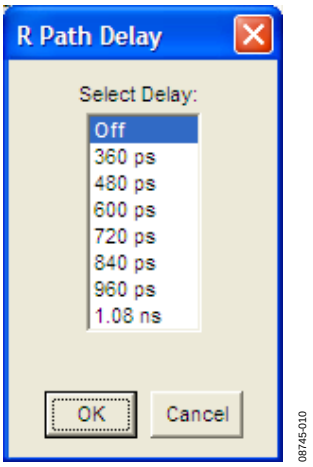

Figure 13. R Path Delay Window

FEEDBACK (N) DIVIDER WINDOW

The reference divider window shown in Figure 14 is accessed by clicking the **N DIVIDER** box on the main screen. If this box is colored gray, the PLL is off. To turn the PLL on, click the **PLL MODE** box at the top of the main screen, and select **Norm Op**.

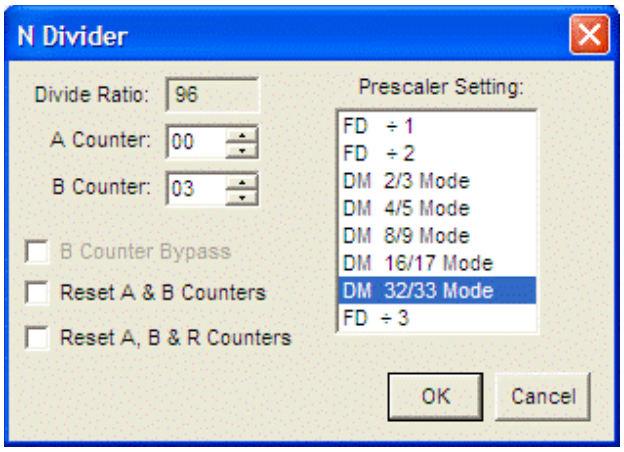

Figure 14. N Divider Window

The various modes of the N divider are described in detail in the AD951x data sheet. For most applications, the 8/9 or 16/17 dual modulus modes are used. For applications requiring a divider value larger than 131,119, the 32/33 mode is provided. Different applications require different settings, and you can experiment with the different settings.

The evaluation software has internal checking to ensure that invalid settings are not programmed. For example, the B counter must always be larger than the A counter. Another restriction is that 8/9 dual modulus mode cannot be used for VCO frequencies greater than 2400 MHz. In cases where a feedback divider restriction cannot be resolved, you may need to adjust the R (reference) divider to allow a different feedback divider value. For example, it is not possible to use the internal VCO, and a feedback divider of 30. However, the R divider can be doubled, which allows a feedback divider of 60.

The feedback divider window has a check box for holding the N divider in reset. When the N divider is held in reset, the PLL loop is open. Therefore, this feature is seldom used.

PHASE FREQUENCY DETECTOR (PFD) WINDOW

The **Phase Frequency Detector (PFD)** window shown in Figure 15 is accessed by clicking the **PFD** box on the main window.

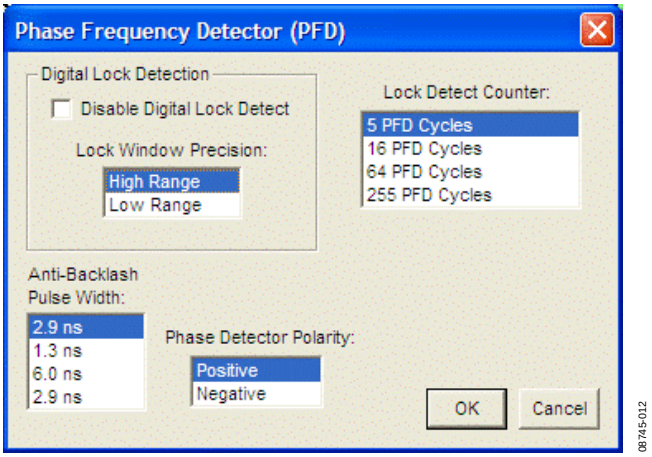

Figure 15. Phase Frequency Detector Window

The features accessible in this window are described in detail in the AD951x data sheet. The most commonly used settings are the **Anti-Backlash Pulse Width** and the **Lock Detect Counter**.

For phase detector frequencies greater than 50 MHz, the PLL may work better with the 1.3 ns antibacklash pulse width setting.

Setting the lock detect counter to values greater then 5 PFD cycles can be useful in applications where the loop bandwidth is low and the lock detect counter chatters during acquisition.

CHARGE PUMP WINDOW

The **Charge Pump Setup** window shown in Figure 16 is accessed by clicking the **CHARGE PUMP** box on the main screen.

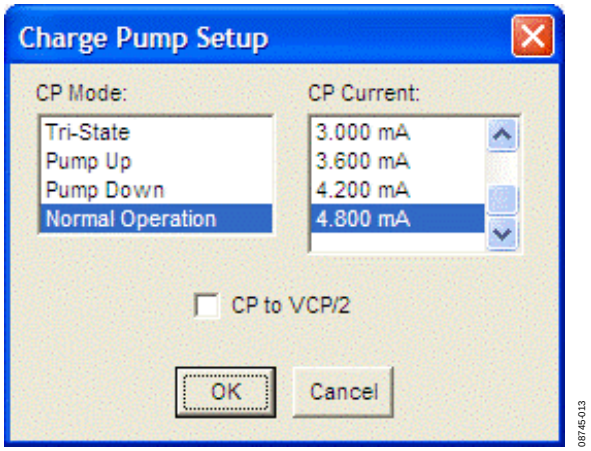

Figure 16. Charge Pump Setup Window

This window is most often used to vary the charge pump current.

The window also has a check box for setting the charge pump voltage to $V_{CP}/2$, which is very useful for debugging the PLL and isolating the output driver section of the AD951x from the PLL section.

VCO CALIBRATION WINDOW

The **Calibrate VCO** window shown in Figure 17 is accessed by clicking the **Cal VCO** button on the main window.

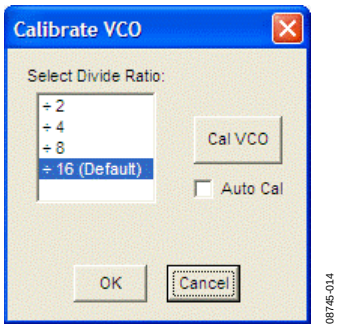

Figure 17. Calibrate VCO Window

A valid reference input signal must be present to complete VCO calibration, and the VCO must be recalibrated any time the VCO frequency changes by more than 40 MHz.

A VCO divider of 16 is suitable for all applications. However, for applications where the phase detector frequency is <12 MHz, using a smaller VCO calibration divider reduces calibration time. Refer to the AD951x data sheet for more details.

Note that the automatic holdover feature must not be enabled during VCO calibration. See the PLL Configuration Window section, and make sure that the **Enable Hold Over** check box is cleared during VCO calibration.

CHANNEL DIVIDER WINDOW

The channel divider window shown in Figure 18 is accessed by clicking the appropriate channel divider. It is usually sufficient to change only the divide ratio because the evaluation software and the AD951x duty cycle correction ensure that the output duty cycle remains very close to 50%.

You can also vary the phase offset by changing the **Phase Offset Bits** setting. However, to have the new phase take effect, the SYNC signal needs to be toggled by using the **SYNC** button in the lower left corner of the main window.

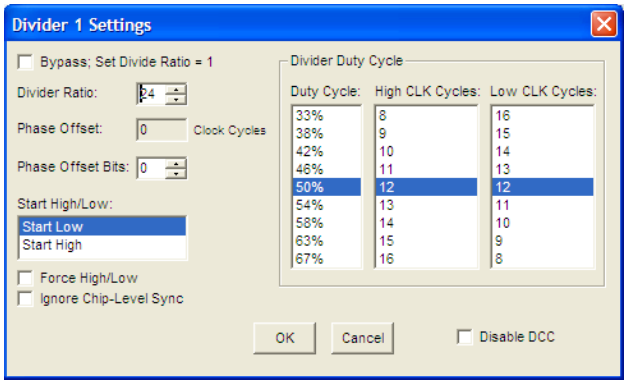

Figure 18. Divider 1 Settings Window

LVPECL OUTPUT DRIVER WINDOW

The **LVPECL Output 0 Settings** window shown in Figure 20 is accessed by clicking the OUT0 through OUT5 output driver symbols on the right side of the main window (see Figure 19).

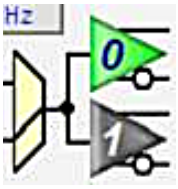

Figure 19. OUT0 Through OUT5 Output Driver Symbols

It is important to power down unused outputs on the evaluation board because they can be a source of unwanted spurs.

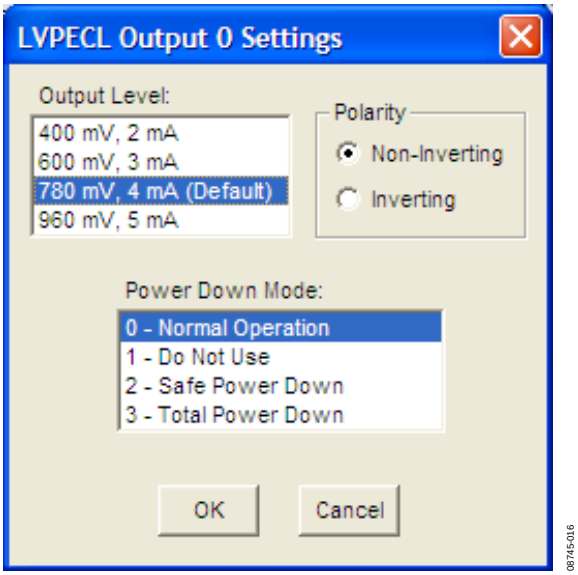

Figure 20. LVPECL Output 0 Driver Window

LVDS/CMOS OUTPUT DRIVER WINDOW

The **LVDS/CMOS Output 6 Settings** window shown in Figure 21 is accessed by clicking the OUT6 through OUT9 output driver symbols on the lower right side of the main window.

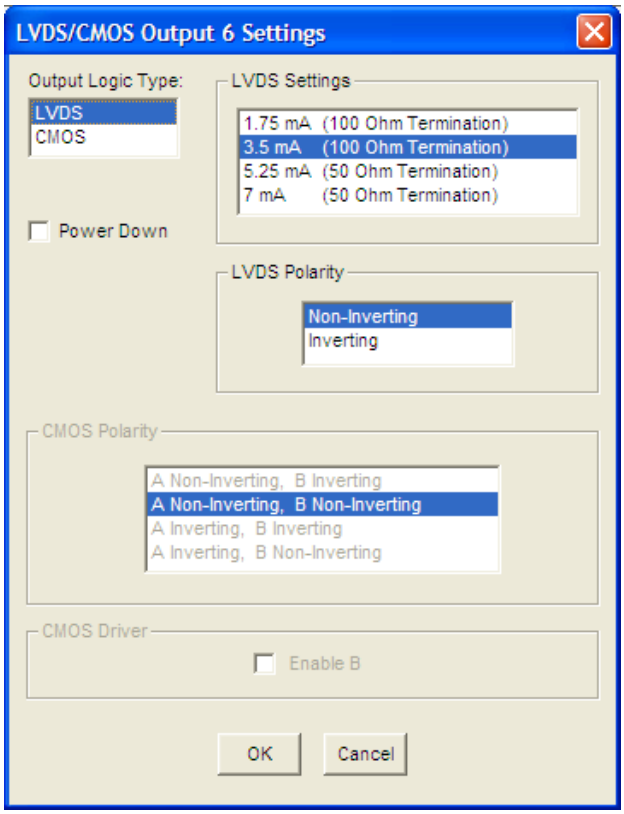

Figure 21. LVDS/CMOS Output 6 Settings Window

If LVDS mode is selected, the bottom (CMOS) portion of the window is grayed out. Likewise, if CMOS mode is selected, the top (LVDS) portion of the window is grayed out.

It is important to power down unused outputs on the evaluation board because they can be a major source of unwanted spurs. This is especially true of the CMOS drivers.

LVDS/CMOS OUTPUT DELAY WINDOW

The **Output 6 Delay** window shown in Figure 22 is accessed by clicking the **ΔT OUT 6** button on the right of the main screen. To access any other output delay window, click the appropriate **ΔT OUT x** button.

Selecting the various combinations of ramp current and ramp capacitors changes the amount of delay for that driver, and the estimated amount of delay is shown in the right half of the window. The feature is described in detail in the AD951x data sheet.

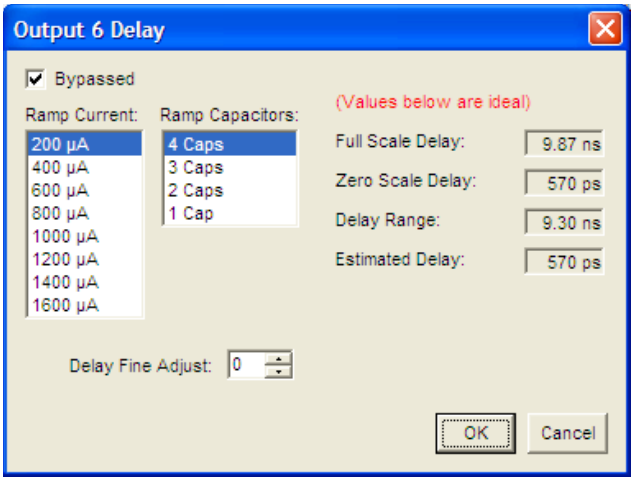

Figure 22. Output 6 Delay Window

DEBUG WINDOW

The **Debug** window shown in Figure 23 is accessed by clicking **Debug** from the **View** menu from on the main window menu bar (see Figure 24).

The **Serial I/O** section of this window is a convenient way to read and write registers directly.

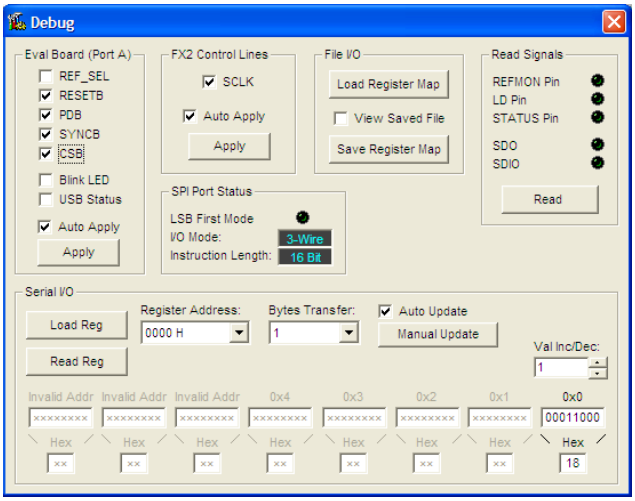

Figure 23. Debug Window

EVALUATION SOFTWARE MENU ITEMS

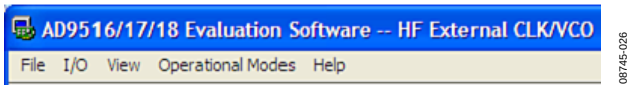

Figure 24. Menu Bar

MENU BAR

File Menu

The **File** menu has the following options:

Load Setup

Selecting **Load Setup** loads a previously saved AD951x setup file (.stp). A setup file is a text file that contains the AD951x register setup file, plus any evaluation board settings. Note that you must still perform a VCO calibration.

Save Setup

Selecting **Save Setup** saves an AD951x setup file (.stp). A setup file is a text file that contains the AD951x register setup file, plus any evaluation board settings.

Exit

Exits the evaluation software. No checking is performed to ensure that the existing setup is saved.

I/O Menu

The **I/O** menu has the following options:

Select Evaluation Board

The AD951x evaluation system allows one PC to control multiple evaluation boards. This window allows you to select which evaluation board the software is controlling. Click **Refresh List** to detect a recently connected evaluation board (see Figure 25).

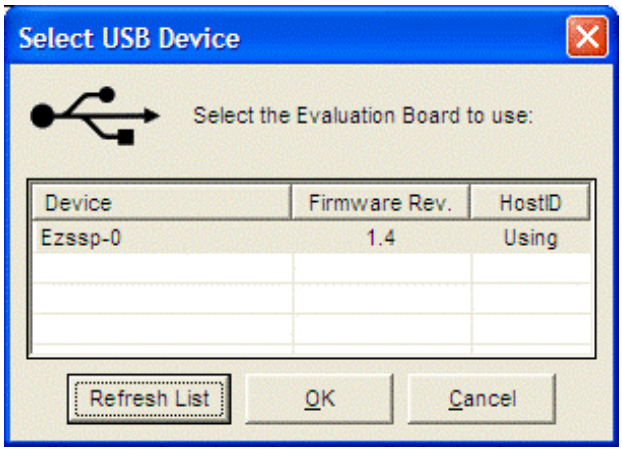

Figure 25. Select USB Device Window

Configure Serial Port

The **Serial Port Config** window allows you to control how the USB controller interacts with the AD951x serial port (see Figure 26).

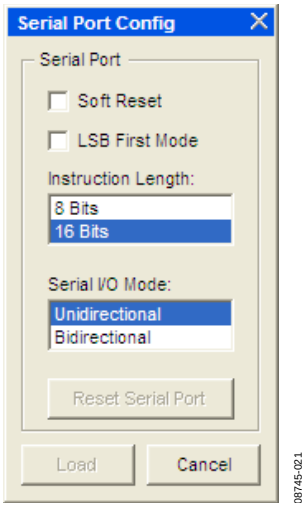

Figure 26. Serial Port Config Window

View Menu

The **View** menu includes the following options:

Debug

This window (see Figure 23) allows you to write and read registers directly, as well as force the various configuration pins high and low.

Options

This window allows you to select Windows® XP visual styles.

Operational Modes Menu

This menu allows you to select any of the three operational modes in the AD951x data sheet: high frequency clock distribution mode, external clock/VCO distribution, and internal VCO and clock distribution.

Help Menu

Selecting **Help** opens the **About AD951x** dialog box, which contains information such as revision number, region information, contact information.

AD9516 PLL LOOP FILTER

The AD9516 PLL requires an external loop filter whose components are tailored for different applications. The third-order passive configuration shown in Figure 27 usually offers the best performance and is the one found on the evaluation board.

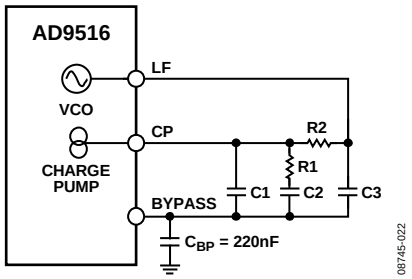

Figure 27. PLL Loop Filter

The default loop filter on the AD9516 evaluation board is optimized for clock generation where the input reference is relatively quiet. It has a transfer function with slight peaking (<3 dB) and loop bandwidths from 75 kHz to 200 kHz. In most of these applications, the phase detector is run at 10 MHz to 50 MHz. Table 2 shows the correspondence between the component numbers shown in Figure 27 and those on the evaluation board, as well as the default values for each version of the evaluation board. The Quick Start Guide to the AD9516 PLL section uses these default values. The phase detector frequency is 10 MHz, and the charge pump current for this example is 3.0 mA. The resulting loop bandwidth is 75 kHz with 50 degrees of phase margin.

When using this loop filter, the same PLL loop dynamics can be maintained with a higher input reference frequency by proportionately reducing the charge pump current, or by increasing the R divider such that the PFD frequency remains the same.

For SONET and Ethernet line cards, as well as applications where the reference clock is relatively high jitter, the low loop BW loop filter shown in Table 3 is a better choice. It has a flat transfer function with peaking <0.1 dB and loop bandwidths from 0.5 kHz to 10 kHz. In most of these applications, the phase detector should be run at 1 MHz or less. A loop filter design such as this optimal for hitless reference clock switching.

The user should not consider the previous recommendations as a substitute for using ADIsimCLK™ to determine the best loop filter for a given application. ADIsimCLK is a free program that can help with the design and exploration of the capabilities and features of the AD9516, including the design of the PLL loop filter. The website has three sample ADIsimCLK files that include the AD9516/AD9517/AD9518 default loop filter titled:
AD9516EvalBoardExample_200MHz.clk
AD9517EvalBoardExample_200MHz.clk
AD9518EvalBoardExample_200MHz.clk

ADIsimCLK includes support for the AD9516. The AD9516, AD9517, and AD9518 share the same loop dynamics. ADIsimCLK is available at www.analog.com/clocks.

Table 2. AD9516 Default Loop Filter Values and PLL Setup

ADISimCLK Naming	Evaluation Board Location	AD9516-0/AD9516-2/AD9516-4	AD9516-1	AD9516-3
C1	C25	470 pF	470 pF	560 pF
R1	R5	910 Ω	820 Ω	750 Ω
C2	C22	8.2 nF	8.2 nF	10 nF
R2	R2	2.4 kΩ	2.4 kΩ	2 kΩ
C3	C31	150 pF	150 pF	180 pF
Input Frequency	N/A	10 MHz	10 MHz	10 MHz
R Divider	N/A	1	1	1
PFD	N/A	10 MHz	10 MHz	10 MHz
N Divider	N/A	–0: 280 –2: 220 –4: 160	250	200
VCO Frequency	N/A	–0: 2800 MHz –2: 2200 MHz –4: 1600 MHz	2500 MHz	2000 MHz
ICP	N/A	3.0 mA	3.0 mA	3.0 mA

LOOP FILTER FOR CLOCK CLEANUP

The component values in Table 3 are suitable for applications where the input reference clock is noisy or for cases where the frequency planning requires a phase detector frequency of 1 MHz or lower.

Table 3. AD9516 Evaluation Board Low Loop Bandwidth (Clock Cleanup) Filter Component Values

ADIsimCLK Component Naming	Evaluation Board Location	Component Value
C1	C25	1500 pF
R1	R5	2.1 kΩ
C2	C22	4.7 µF
R2	R2	3 kΩ
C3	C31	2200 pF

NOTES

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG08745-0-1/10(0)

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