Power Supply IC Series for TFT-LCD Panels

High-precision Gamma Correction ICs with built-in DAC

Pb Free ROHM Electronic Components   RoHS Directive Compliance

BD8132FV, BD8139AEFV

No.09035EBT02

●Description

These gamma correction voltage generation ICs feature built-in DACs and provide a single-chip solution with setting control via serial communications, a high-precision 10-bit DAC, an output amp (18-channel or 10-channel), and Vcom.

●Features

1) Single-chip design means fewer components
2) Built-in 10 bit DAC (18ch: BD8132FV, 10ch: BD8139AEFV)
3) Built-in DAC output amp
4) Built-in Vcom amp
5) Built-in auto-read function
6) 3-line serial interface (BD8132FV) or 2-wire serial (BD8139AEFV)
7) Thermal shutdown circuit
8) SSOP-B40 package (BD8132FV) / HTSSOP-B40 package (BD8139AEFV)

●Applications

These ICs can be used with TFT LCD panels used by large-screen and high-definition LCD TVs.

●Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limit	Unit
Power supply voltage 1		DVcc	7	V
Power supply voltage 2		Vcc	20	V
REFIN voltage		REF	20	V
Amp output current capacity		Io	50*1	mA
Junction temperature		Tjmax	150	℃
Power dissipation	BD8132FV	Pd	1125*2	mW
	BD8139AEFV		1600*3	
Operating temperature range		Topr	-30 to +85	℃
Storage temperature range		Tstg	-55 to +150	℃

*1 Must not exceed Pd.
*2 Reduced by 9.0 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).
*3 Reduced by 12.8 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

●Recommended Operating Ranges

Parameter	Symbol	Limit		Unit
		Min.	Max.	
Power supply voltage 1	DVcc	2.3	4.0	V
Power supply voltage 2	Vcc	6	18	V
REFIN voltage	REF	6	18	V
Amp output current capacity	Io	—	40	mA
Serial clock frequency (BD8132FV)	fCLK	—	5	MHz
2 wire serial frequency (BD8139AEFV)	fCLK	—	400	kHz
OSC frequency (BD8132FV)	fosc	10	200	kHz
OSC frequency (BD8139AEFV)	fosc	—	400	kHz

●Electrical Characteristics

BD8132FV(Unless otherwise specified, Vcc = 15 V, DVcc = 3.3 V, Ta = 25℃)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
[REFIN]						
Sinking current	Iref	25	50	75	μA	REF = 10 V
[Gamma correction amp block]						
Output current capacity	Io	150	300	—	mA	DAC = 3V, OUTx = 0 V
Load stability	ΔV	—	5	20	mV	Io = +10 mA to -10 mA, OUTx = 6 V
Slew rate	SR	—	3.5	—	V/μS	Ro = 100 kΩ, Co = 100 pF *
OUT max. output voltage	VOH	Vcc-0.16	Vcc-0.1	—	V	Io = -5 mA
OUT min. output voltage	VOL	—	0.15	0.24	V	Io = 5 mA
[Common amp block]						
Input bias current	Ib	—	0	1	μA	VFB = 6 V
Output current capacity	Io	150	300	—	mA	DAC = 3V, OUTx = 0 V
Load stability	ΔV	—	5	20	mV	Io = +10 mA to -10 mA, OUTx = 3 V
Slew rate	SR	—	3.5	—	V/μS	Ro = 100 kΩ, Co = 100 pF *
Input voltage range	VFB	0	—	VDAC	V	Ro = 100 kΩ, Co = 100 pF *
OUT max. output voltage	VOH	Vcc-0.16	Vcc-0.1	—	V	Io = -5 mA
OUT min. output voltage	VOL	—	0.15	0.24	V	Io = 5 mA
[DAC]						
Resolution	Res	—	10	—	Bit	
Nonlinearity error	LE	-2	—	2	LSB	Ideal line error: 00A to 3F5
Differential linearity error	DLE	-2	—	2	LSB	1 LSB ideal increase error: 00A to 3F5
[OSC]						
Oscillating frequency	fosc	—	80	—	kHz	Internal frequency mode
[Control signals]						
Sinking current	Ictl	—	16	25	μA	
Threshold voltage	VTH	0.7	—	2.6	V	DVCC = 3.3 V
Reset time	trst	—	45	—	μs	CCT = 1000 pF
[Overall]						
Total supply current	Icc	—	20	—	mA	When all output voltages are set to 5 V.

●**Electrical Characteristics**

BD8139AEFV (Unless otherwise specified, Vcc = 15 V, DVcc = 3.3 V, Ta = 25℃)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
[REFIN]						
Sinking current	Iref	25	50	75	μA	REF = 10V
[Gamma correction amp block]						
Output current capacity	Io	150	300	—	mA	DAC = 3 V, OUTx = 0 V
Load stability	ΔV	—	5	20	mV	Io = +10 mA to -10 mA, OUTx = 6 V
Slew rate	SR	—	3.5	—	V/μs	Ro = 100 kΩ, Co = 100 pF *
OUT max. output voltage	VOH	Vcc-0.16	Vcc-0.1	—	V	Io = -5 mA
OUT min. output voltage	VOL	—	0.1	0.16	V	Io = 5 mA
[Common amp block]						
Input bias current	Ib	—	0	1	μA	VFB = 6 V
Output current capacity	Io	150	300	—	mA	DAC = 3 V, OUTx = 0 V
Load stability	ΔV	—	5	20	mV	Io = +10 mA to -10 mA, OUTx = 3 V
Slew rate	SR	—	3.5	—	V/μS	Ro = 100 kΩ, Co = 100 pF *
Input voltage range	VFB	0	—	VDAC	V	Ro = 100 kΩ, Co = 100 pF *
OUT max. output voltage	VOH	Vcc-0.16	Vcc-0.1	—	V	Io = -5 mA
OUT min. output voltage	VOL	—	0.1	0.16	V	Io = 5 mA
[DAC]						
Resolution	Res	—	10	—	Bit	
Nonlinearity error	LE	-2	—	2	LSB	Ideal line error: 00A to 3F5
Differential linearity error	DLE	-2	—	2	LSB	1 LSB ideal increase error: 00A to 3F5
[OSC]						
Oscillating frequency	fosc	—	210	—	kHz	Internal frequency mode
[Control signals]						
Sinking current	Ictl	—	16	25	μA	Except for osc_mode
Sinking current	Ioscm	26	33	40	μA	Only osc_mode
Min. output voltage	VSDA	—	—	0.4	V	ISDA = 3.0 mA *
Sinking current	ILi	-10	—	10	μA	0.4 V to 0.9 V DVCC
Threshold voltage	VTH	0.7	—	2.6	V	DVCC = 3.3 V
Reset time	trst	—	45	—	μs	CCT = 1000 pF
[Overall]						
Total supply current	Icc	—	18	—	mA	When all output voltages are set to 5 V.

●Reference Data

(Unless otherwise specified, Ta = 25℃, BD8132FV and BD8139AEFV)

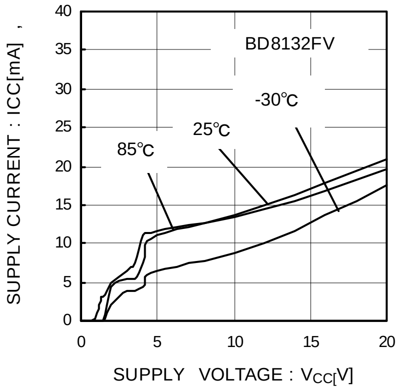


Fig. 1 VCC Total Supply Current

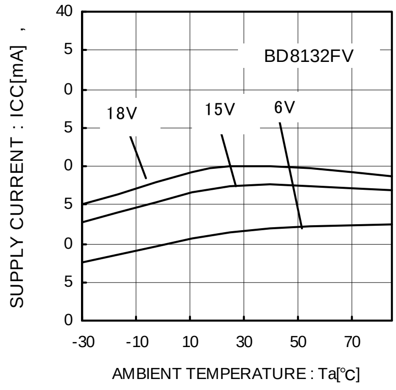


Fig. 2 Total Supply Current vs Temperature

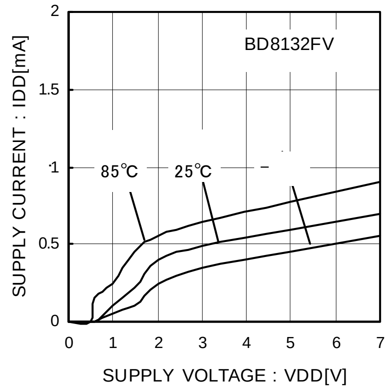


Fig. 3 VDD Total Supply Current

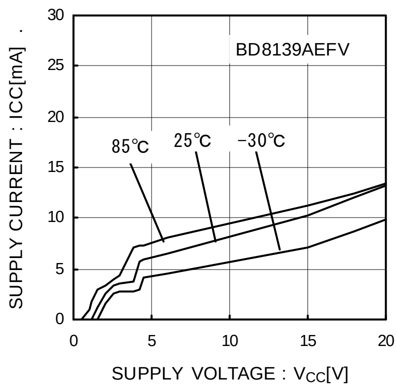


Fig. 4 VCC Total Supply Current

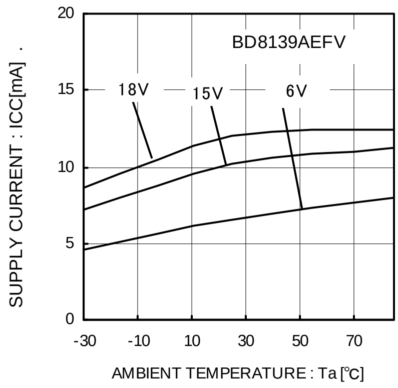


Fig. 5 Total Supply Current vs Temperature

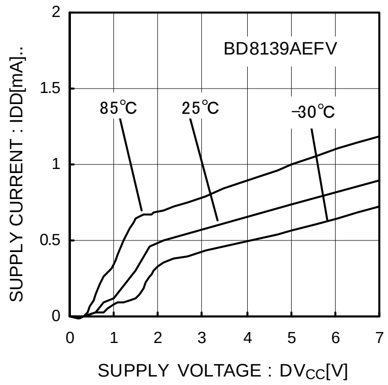


Fig. 6 VDD Total Supply Current

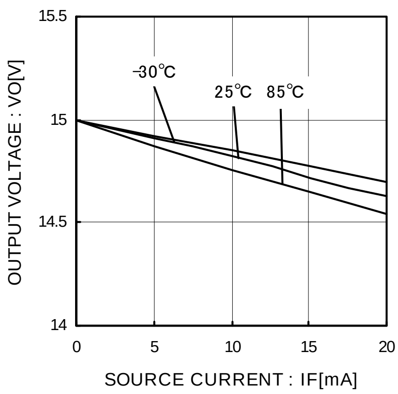


Fig. 7 High Output Voltage

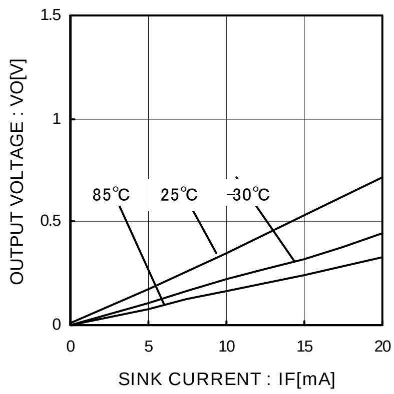


Fig. 8 Low Output Voltage

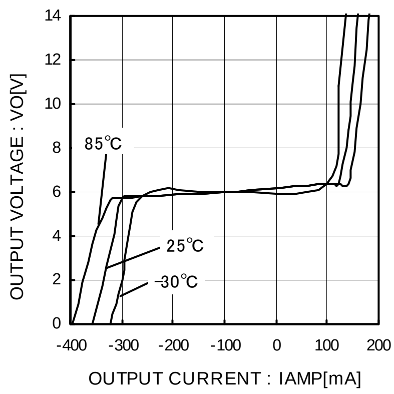


Fig. 9 Output Current Capacity

●Reference Data

(Unless otherwise specified, Ta = 25℃, BD8132FV and BD8139AEFV)

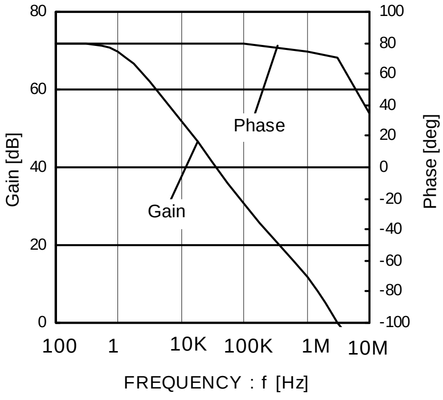


Fig. 10 Open Loop Waveform

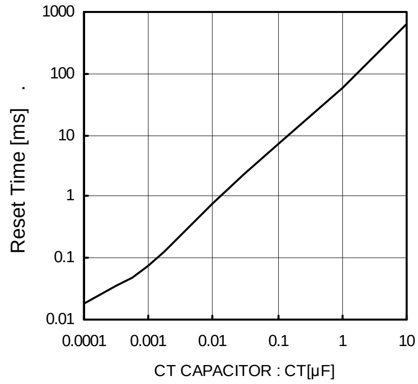


Fig. 11 Power-on Reset Time

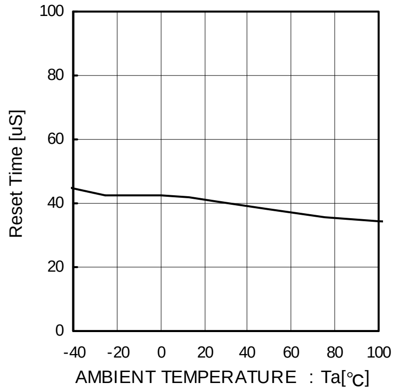


Fig. 12 Power-on Reset Time vs Temperature

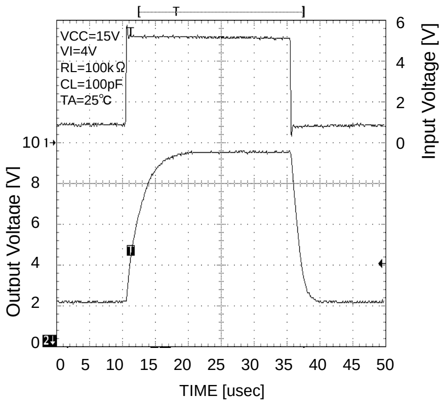


Fig. 13 Slew Rate Waveform (High-Amplitude)

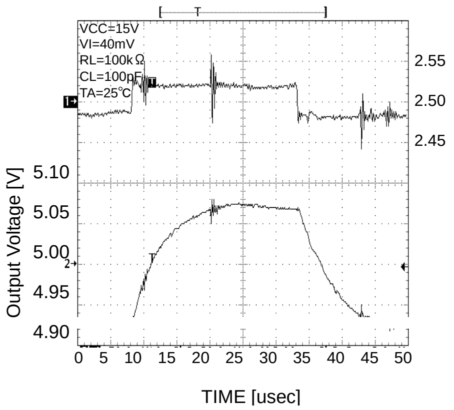


Fig. 14 Slew Rate Waveform (Small Signal)

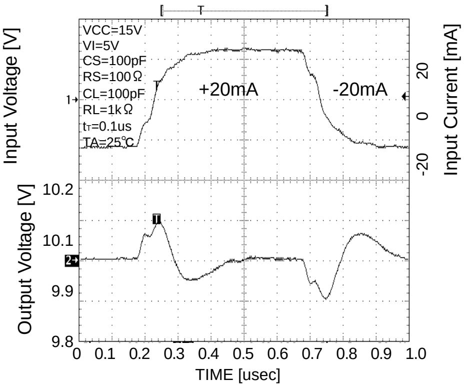


Fig. 15 Load Response Waveform (RL = 1 kΩ Pull-up)

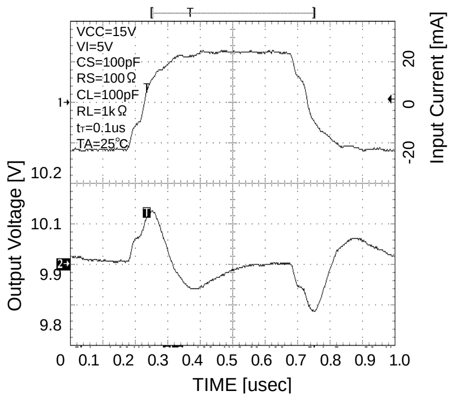


Fig. 16 Load Response Waveform (RL = 1 kΩ Pull-down)

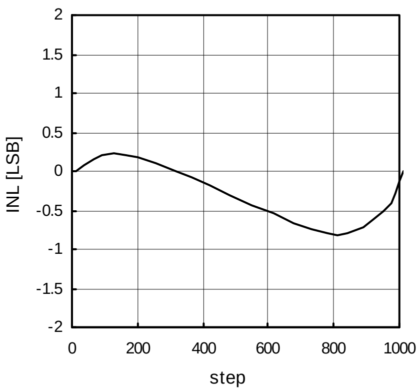


Fig. 17 Integral Linearity Error

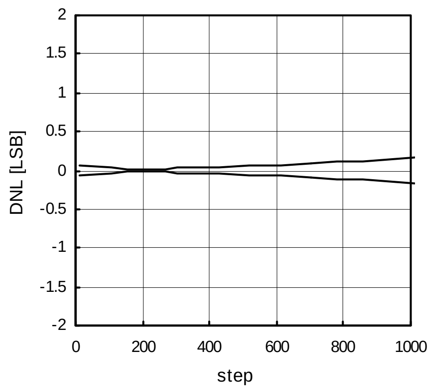
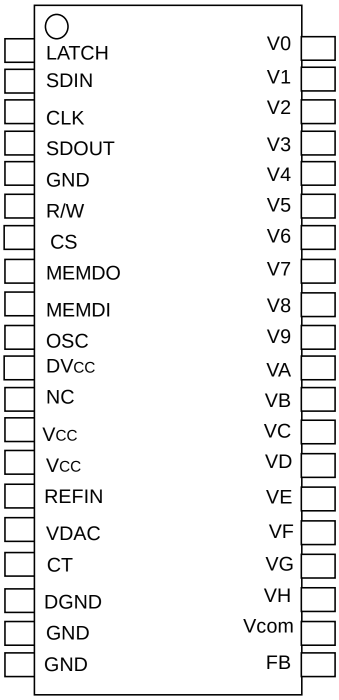


Fig. 18 Differential Linearity Error

●Pin Assignment Diagram

[BD8132FV]



●Block Diagram

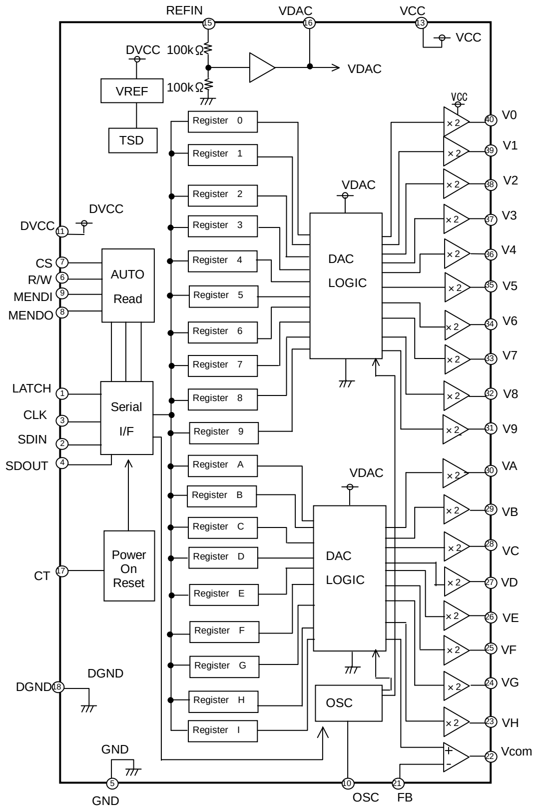


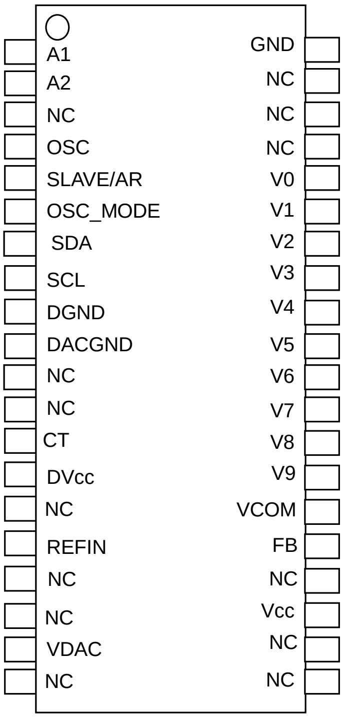
Fig. 19 Pin Assignment Diagram & Block Diagram

●Pin Name and Function

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	LATCH	Serial latch input	21	FB	Vcom amp negative feedback input
2	SDIN	Serial data input	22	Vcom	Vcom output pin
3	CLK	Serial clock input	23	VH	Gamma correction output pin
4	SDOUT	Serial data output	24	VG	Gamma correction output pin
5	GND	GND input	25	VF	Gamma correction output pin
6	R/W	Auto-read on/off input (On = Low, Off = High)	26	VE	Gamma correction output pin
7	CS	External memory selection output	27	VD	Gamma correction output pin
8	MEMDO	External memory output data signal	28	VC	Gamma correction output pin
9	MEMDI	External memory input data signal	29	VB	Gamma correction output pin
10	OSC	Tuning clock I/O	30	VA	Gamma correction output pin
11	DVcc	Logic power supply input	31	V9	Gamma correction output pin
12	NC	—	32	V8	Gamma correction output pin
13	Vcc	Buffer amp power supply input	33	V7	Gamma correction output pin
14	Vcc	Buffer amp power supply input	34	V6	Gamma correction output pin
15	REFIN	DAC reference input	35	V5	Gamma correction output pin
16	VDAC	DAC voltage output	36	V4	Gamma correction output pin
17	CT	Power-on reset capacitance connection pin	37	V3	Gamma correction output pin
18	DGND	DAC GND input	38	V2	Gamma correction output pin
19	GND	GND input	39	V1	Gamma correction output pin
20	GND	GND input	40	V0	Gamma correction output pin

●Pin Assignment Diagram

[BD8139AEFV]



●Block Diagram

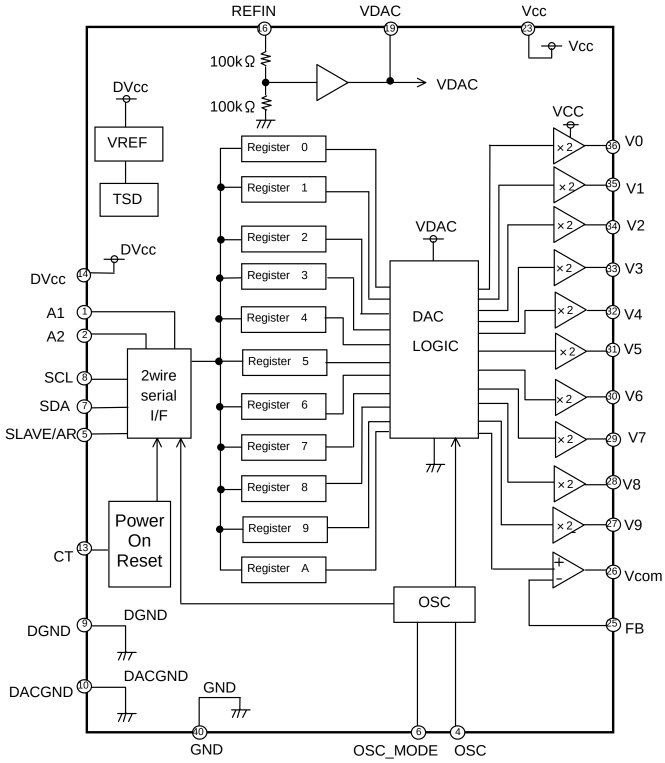


Fig. 20 Pin Assignment Diagram & Block Diagram

●Pin Name and Function

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	A1	Slave/address setting pin Auto-read/word address setting pin (1)	21	NC	—
2	A2	Slave/address setting pin Auto-read/word address setting pin (2)	22	NC	—
3	NC	—	23	Vcc	Buffer amp power supply input
4	OSC	Tuning clock I/O	24	NC	—
5	SLAVE/AR	Slave/auto-read selection pin	25	FB	Vcom amp negative feedback input
6	OSC_MODE	OSC switching pin	26	Vcom	Vcom output pin
7	SDA	Serial data input (2 wire serial)	27	V9	Gamma correction output pin 9
8	SCL	Serial clock input (2 wire serial)	28	V8	Gamma correction output pin 8
9	DGND	GND input	29	V7	Gamma correction output pin 7
10	DACGND	DAC GND input	30	V6	Gamma correction output pin 6
11	NC	—	31	V5	Gamma correction output pin 5
12	NC	—	32	V4	Gamma correction output pin 4
13	CT	Power-on reset capacitance connection pin	33	V3	Gamma correction output pin 3
14	DVcc	Logic power supply input	34	V2	Gamma correction output pin 2
15	NC	—	35	V1	Gamma correction output pin 1
16	REFIN	DAC reference input	36	V0	Gamma correction output pin 0
17	NC	—	37	NC	—
18	NC	—	38	NC	—
19	VDAC	DAC voltage output	39	NC	—
20	NC	—	40	GND	GND input

●Block Operation

- VDAC Amp
  The VDAC Amp amplifies the voltage applied to REFIN by 0.5x and outputs it to the VDAC pin. Connect a 1 μF phase compensation capacitor to the VDAC pin.
- DAC LOGIC
  The DAC LOGIC converts the 10-bit digital signal read to the register to a voltage.
- Amp
  The Amp amplifies the voltage output from the DAC LOGIC by 2x. Input includes a sample and hold function and is refreshed by the OSC.
- OSC
  The OSC generates the frequency that determines the Amp's refresh time.
  External input can be selected using serial input. (For the BD8139AEFV, external input is selected using the external pin.)
- Power On Reset
  When the digital power supply DVCC is activated, each IC generates a reset signal to initialize the serial interface, auto-read functionality, and registers.
  Adding a 1,000 pF capacitor to the CT pin ensures that reset operation can be performed reliably, without regard to the speed with which the power supply starts up.
- TSD (Thermal Shut Down)
  The TSD circuit turns output off when the chip temperature reaches or exceeds approximately 175°C in order to prevent thermal destruction or thermal runaway. When the chip returns to a specified temperature, the circuit resets.
  The TSD circuit is designed only to protect the IC itself. Application thermal design should ensure operation of the IC below the thermal shutdown detection temperature of approximately 175°C.
- Register
  A serial signal (consisting of 10-bit gamma correction voltage values) input using the serial interface or I^2C bus interface is held for each register address. Data is initialized by the reset signal generated during a power-on reset.
- Serial I/F(BD8132FV)
  The serial interface uses a 3-line serial data format (LATCH, CLK, SDIN). It is used to set gamma correction voltages, specify register addresses, and select OSC I/O.
- 2 wire serial I/F(BD8139AEFV)
  The serial interface uses a 2-line serial data format (SCL, SDA). It is used to set gamma correction voltages and specify register addresses.
- Autoread
  The BD8132FV uses the R/W, CLK, CS, and MEMDO pins to enable automatic reading of the IC's 1 kbit microwire type external memory.
  The BD8139AEFV uses the SCL and SDA pins to enable automatic reading of the 2 wire serial bus format external memory.

[BD8132FV]

●Serial communications

The serial data control block consists of a register that stores data from the LATCH, CLK, and SDIN pins, and a DAC circuit that receives the output from this register and provides adjusted voltages to other IC blocks.
When the IC's power supply is activated, the reset function operates to set the register to a preset value. The first bit is for testing use only and should always be set to 0. The next bit is used to select the OSC mode. Inputting a value of 0 selects internal frequency mode and uses a frequency of 80 kHz. Entering a value of 1 selects external frequency mode. Input an external clock signal from the OSC pin.

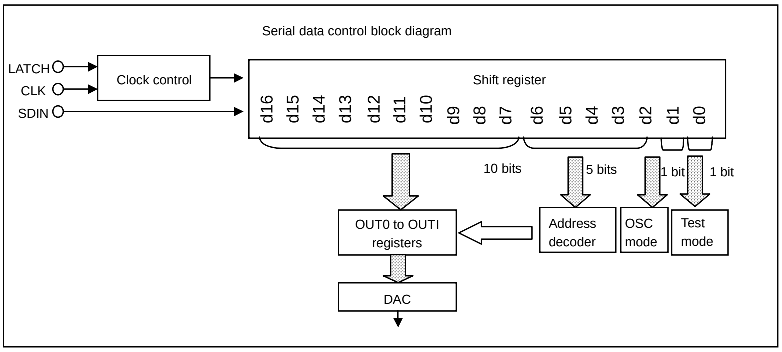


Fig. 21 Serial Block Diagram

(1) Serial communications timing

The 17-bit serial data input from the SDIN pin is read into the shift register using the rising edge of the signal input to the CLK pin. This data is then loaded to the DAC register using the rising edge of the signal input to the LATCH pin.
If the data loaded into the shift register while the LATCH pin is low consists of less than 17 bits, the loaded data is discarded. If the data exceeds 17 bits, the last 17 bits to be loaded are treated as valid.

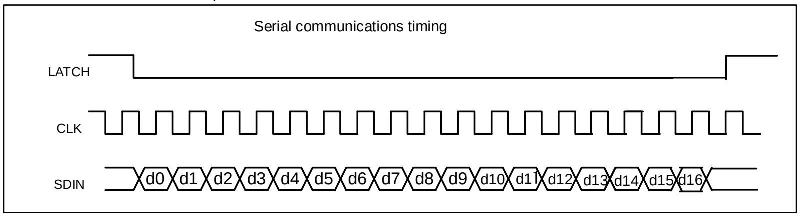


Fig. 22 Serial Communications Timing Chart

(2) Serial data

The following table illustrates the format of serial data input to the SDIN pin.

First → →Last

d0	d1	d2	d3	d4	d5	d6	d7	d8	d9	d10	d11	d12	d13	d14	d15	d16
0	X	Register address					Data									

Register	Address					Behavior when data increases	Preset value		
	d2	d3	d4	d5	d6		d7	to	d16
Register 0	0	0	0	0	0	V0 voltage value increases	00000		00000
Register 1	0	0	0	0	1	V1 voltage value increases	00000		00000
Register 2	0	0	0	1	0	V2 voltage value increases	00000		00000
Register 3	0	0	0	1	1	V3 voltage value increases	00000		00000
Register 4	0	0	1	0	0	V4 voltage value increases	00000		00000
Register 5	0	0	1	0	1	V5 voltage value increases	00000		00000
Register 6	0	0	1	1	0	V6 voltage value increases	00000		00000
Register 7	0	0	1	1	1	V7 voltage value increases	00000		00000
Register 8	0	1	0	0	0	V8 voltage value increases	00000		00000
Register 9	0	1	0	0	1	V9 voltage value increases	00000		00000
Register A	0	1	0	1	0	VA voltage value increases	00000		00000
Register B	0	1	0	1	1	VB voltage value increases	00000		00000
Register C	0	1	1	0	0	VC voltage value increases	00000		00000
Register D	0	1	1	0	1	VD voltage value increases	00000		00000
Register E	0	1	1	1	0	VE voltage value increases	00000		00000
Register F	0	1	1	1	1	VF voltage value increases	00000		00000
Register G	1	0	0	0	0	VG voltage value increases	00000		00000
Register H	1	0	0	0	1	VH voltage value increases	00000		00000
Register I	1	0	0	1	0	Vcom voltage value increases	00000		00000

●Auto-read function

The auto-read function enables the IC's 1 kbit microwire type external memory to be automatically read.
This block operates in synchronization with the external input CLK's falling edge to output the external memory chip select signal CS as well as the memory read data signal MEMDO.
The read data signal consists of a start bit for the external memory, a read code, and a read address. When this signal is sent to the external memory, the memory outputs the data corresponding to the indicated address. Data output from the memory is read from the MEMDI pin, and this block automatically generates the serial DATA and LATCH signals and writes the memory data to the register. Memory reads are synchronized to the CLK's falling edge.
Read addresses start from address 00H and repeat until address 12H, so data must be stored from address 00H to address 12H.
The auto-read function is controlled using the R/W signal. Read access to the external memory is performed continuously while the R/W signal is low. To access the external memory from another device, the R/W signal must be set to high. When the R/W signal is set to high, the CS and MEMDO pins enter a high-impedance state.

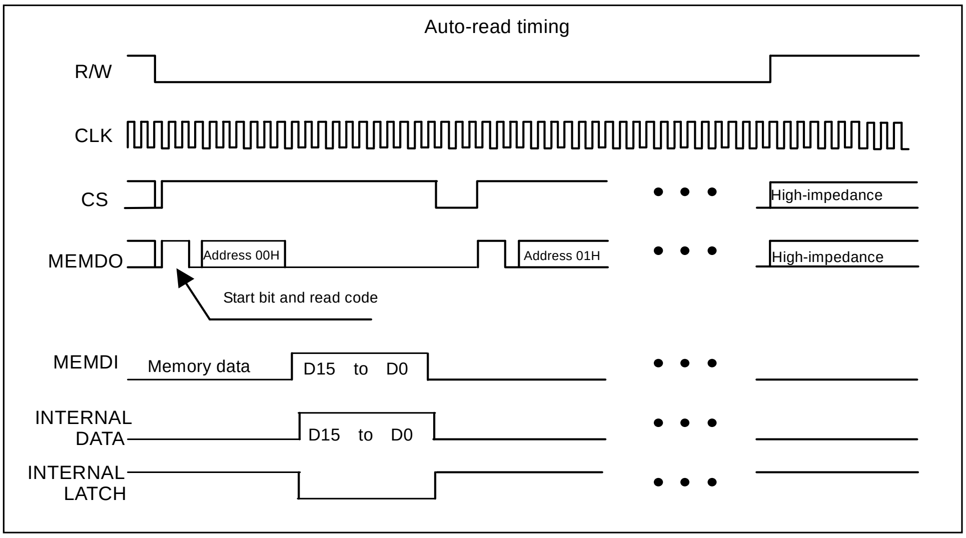


Fig. 23 Auto-read Timing Chart

External memory data format

MSB … LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
d1	d2	d3	d4	d5	d6	d7	d8	d9	d10	d11	d12	d13	d14	d15	d16
OSC mode	Register address					DAC data									

Fig. 24 External Memory Data Table

●Serial communications timing chart

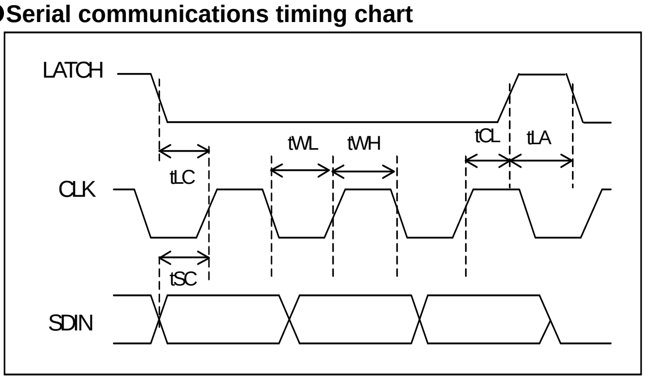


Fig.25

●Auto-read timing chart

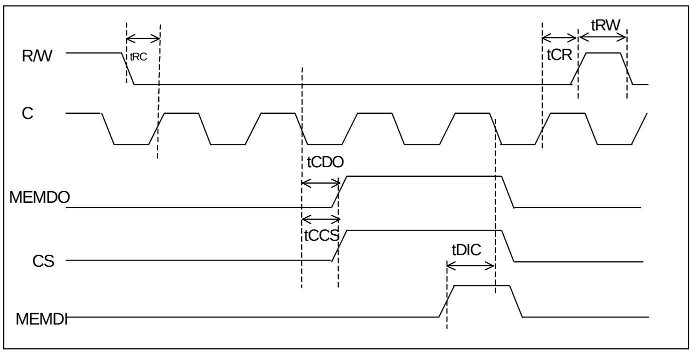


Fig.26

●Timing standard values

Parameter	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Latch setup time	tLC	0.1	—	—	µs
SDIN setup time	tSC	0.1	—	—	µs
RW setup time	tRC	0.1	—	—	µs
MEMDI setup time	tDIC	0.1	—	—	µs
Clock high time	tWH	0.1	—	—	µs
Clock low time	tWL	0.1	—	—	µs
Latch hold time	tCL	0.1	—	—	µs
RW hold time	tCR	0.1	—	—	µs
LATCH high time	tLA	0.6	—	—	µs
RW high time	tRW	0.6	—	—	µs
MEMDO delay time	tCDO	—	—	0.1	µs
CS delay time	tCCS	—	—	0.1	µs

●Gamma correction output setting (BD8132FV and BD8139AEFV)

Equation (1) describes the relationship between the gamma correction output voltage (V0 to VH) and the DAC setting.
Output voltage (V0 to VH) = [(DAC setting + 1) / 1,024] × (REFIN / 2) × 2 (1)

The Vcom voltage can be set by attaching resistor R1 between the Vcom and FB pins and resistor R2 between the FB and GND pins.Equation (2) describes the relationship between the Vcom voltage and the DAC setting when using these resistors.
Output voltage (Vcom) = [(DAC setting + 1) / 1,024] × (REFIN / 2) × (R1 + R2) / R2 (2)

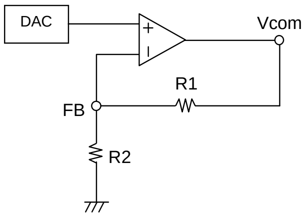


Fig. 27 Vcom Voltage Setting Circuit Diagram

●Power supply sequence

Activate the digital power supply DVcc before the Vcc power supply to prevent IC malfunctions due to undefined logic in the digital circuit. Input serial data after canceling the power-on reset. When turning off the IC's power supplies, turn off Vcc and then DVcc.

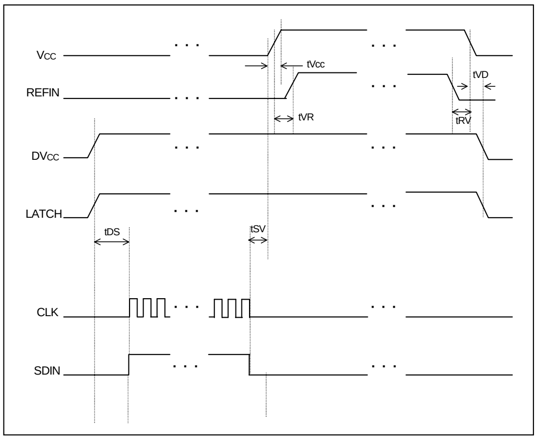


Fig. 28 Power Supply Sequence Diagram

●Power supply sequence standard values

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Serial input timing	tDS	100	—	—	µs	Cct = 1000 pF
VCC activation timing	tSV	0	10	—	µs	
REFIN activation timing	tVR	0	10	—	µs	
REFIN off timing	tRV	0	10	—	µs	
Power supply off timing	tVD	0	10	—	µs	
Vcc startup timing	tVCC	1	—	—	ms	

[BD8139AEFV]

●Serial communications

The 2 wire serial control block consists of a register that stores data from the SCL and SDA pins and a DAC circuit that receives the output from this register and provides adjusted voltages to other IC blocks.
When the IC's power supply is activated, the reset function operates to set the register to a preset value.

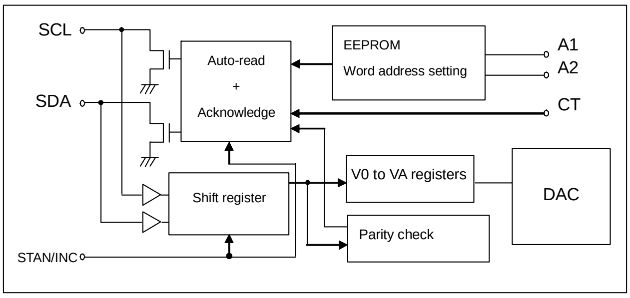


Fig. 29 2 wire serial Control Block Diagram

(1) 2 wire serial timing chart

Slave mode (SLAVE/AR = low; supports write mode only; A0 = low)

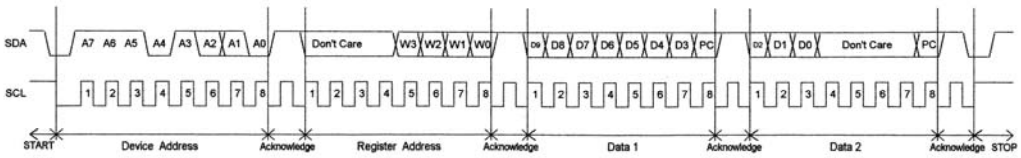


Fig. 30 2 wire serial Timing Chart (Slave)

Of device addresses A7 to A0, A7 to A3 and A0 are specific to the gamma correction voltage generation IC and should be set as follows: (A7 to A0) = 11101(A2)(A1)0.
A1 and A2 can be set externally. Because these signals are pulled down internally, they are set to 0 when in the open state. When setting them to 1, connect them to the DVcc power supply. For this reason, A1 and A2 can be used to create 4 setting combinations. When using only slave mode, a maximum of 4 BD8139AEFV ICs can be connected to the 2 wire serial line.
The lower 4 bits of the second byte are used to store the register address. The following table describes the correspondence between register addresses and amp output. The third and fourth bytes are used to store the gamma correction voltage setting. The LSB acts as a parity check bit. The method for setting the LSB is described below.

Register name	Address				Behavior when data increases	Preset value
	W3	W2	W1	W0		Data (9:0)
Register 0	0	0	0	0	V0 voltage value increases	00_0000_0000
Register 1	0	0	0	1	V1 voltage value increases	00_0000_0000
Register 2	0	0	1	0	V2 voltage value increases	00_0000_0000
Register 3	0	0	1	1	V3 voltage value increases	00_0000_0000
Register 4	0	1	0	0	V4 voltage value increases	00_0000_0000
Register 5	0	1	0	1	V5 voltage value increases	00_0000_0000
Register 6	0	1	1	0	V6 voltage value increases	00_0000_0000
Register 7	0	1	1	1	V7 voltage value increases	00_0000_0000
Register 8	1	0	0	0	V8 voltage value increases	00_0000_0000
Register 9	1	0	0	1	V9 voltage value increases	00_0000_0000
Register A	1	0	1	0	Vcom voltage value increases	00_0000_0000
Register 0-A	1	1	1	1	V0-Vcom voltage value increases	00_0000_0000

●SDA serial data map

SLAVE mode(SLAVE/AR=L)

First (MSB) Last (LSB)

Byte	bit							
	7	6	5	4	3	2	1	0
1	Device address (11101<A2><A1>)							0
2	Don't Care				Register address			
3	data(9:3)							PC
4	data(2:0)			Don't Care				PC

It needs 4 byte for slave mode.
When register address "1111", it is updated same data on all addresses.

Auto-read mode (SLAVE/AR = high)
The auto-read function enables automatic reading of the I^2C bus interface's 1 kbit built-in memory.
When the reset signal is cleared, automatic reads from EEPROM begin.
In auto-read mode, A1 and A2 serve as the EEPROM word address setting pins.
When A1 and A2 are both set to low, read access is available for word addresses 0 through 21.

A2	A1	Read start word address	Read end word address
L	L	0 (00h)	21 (h)
H	L	32 (20h)	53 (35h)
L	H	64 (40h)	85 (55h)
H	H	96 (60h)	117 (75h)

The following table describes the 22-word data format read from the EEPROM.

Word	7	6	5	4	3	2	1	0	Output
1	Data (9:3)							PC	V0
2	Data (2:0)			Don't Care				PC	
3	Data (9:3)							PC	V1
4	Data (2:0)			Don't Care				PC	
⋮	⋮								
21	Data (9:3)							PC	Vcom
22	Data (2:0)			Don't Care				PC	

The first and second words are used for the V0 setting, while the third and fourth words are used for the V1 setting. Including the Vcom setting, a total of 22 words of data are read. The LSB for all words contains an even parity check (PC). The LSBs for all EPROM data settings should be set. (Where the number 1 represents an even number.)

＜Example of setting for EEPROM＞

A1=L,A2=L

REFIN	15	V

	EEPROM WORD ADDRESS	BD8139AEFV	data d7	d6	d5	d4	d3	d2	d1	d0	bin	dec	Setting voltage	
1	00h	V0①	1	1	1	0	0	1	0	0	1110010011	915	13.418	V0
2	01h	V0②	0	1	1	0	0	0	0	0				
3	02h	V1①	1	0	1	1	1	1	1	0	1011111010	762	11.177	V1
4	03h	V1②	0	1	0	0	0	0	0	1				
5	04h	V2①	1	0	1	0	1	0	1	0	1010101100	684	10.034	V2
6	05h	V2②	1	0	0	0	0	0	0	1				
7	06h	V3①	0	1	1	1	1	0	0	0	0111100001	481	7.061	V3
8	07h	V3②	0	0	1	0	0	0	0	1				
9	08h	V4①	1	0	0	0	1	1	1	0	1000111110	574	8.423	V4
10	09h	V4②	1	1	0	0	0	0	0	0				
11	0Ah	V5①	1	0	0	0	0	0	0	1	1000000000	512	7.515	V5
12	0Bh	V5②	0	0	0	0	0	0	0	0				
13	0Ch	V6①	0	1	0	1	0	1	0	1	0101010111	343	5.039	V6
14	0Dh	V6②	1	1	1	0	0	0	0	1				
15	0Eh	V7①	0	1	0	1	1	1	1	1	0101111111	383	5.625	V7
16	0Fh	V7②	1	1	1	0	0	0	0	1				
17	10h	V8①	0	1	0	0	1	0	1	1	0100101010	298	4.380	V8
18	11h	V8②	0	1	0	0	0	0	0	1				
19	12h	V9①	0	0	0	1	1	1	1	0	0001111010	122	1.802	V9
20	13h	V9②	0	1	0	0	0	0	0	1				
21	14h	VCOM①	1	1	1	1	1	1	1	1	1111111111	1023	7.500	VCOM
22	15h	VCOM②	1	1	1	0	0	0	0	1				R1=R2

※Must set "1" at d7 of 16ch.

●Timing Chart

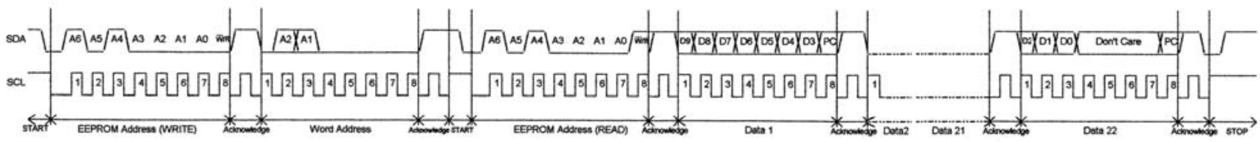


Fig. 31 2-wire serial Timing Chart (Auto-Read)

Only the EEPROM device address A3 = A2 = A1 = low is supported.
The auto-read function specifies the read start word address in EEPROM write mode. Then after resending the start signal, the data is read in read mode. When the parity check detects an error, a stop signal is sent and the auto-read function is repeated until no error is detected.If the auto-read function never completes, the EEPROM data settings should be reviewed.

・When operating in auto-read mode, a maximum of 2 BD8139AEFV ICs (A and B) can be connected to the I^2C bus line. When using 2 ICs, change the CT pin capacitance value to avoid auto-read timing collisions. The following figure illustrates auto-read timing when using 2 ICs.

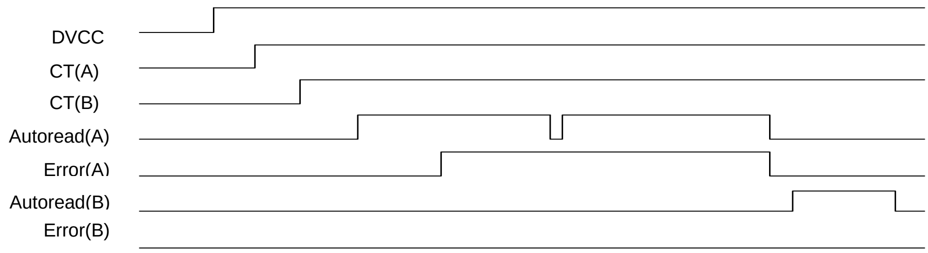
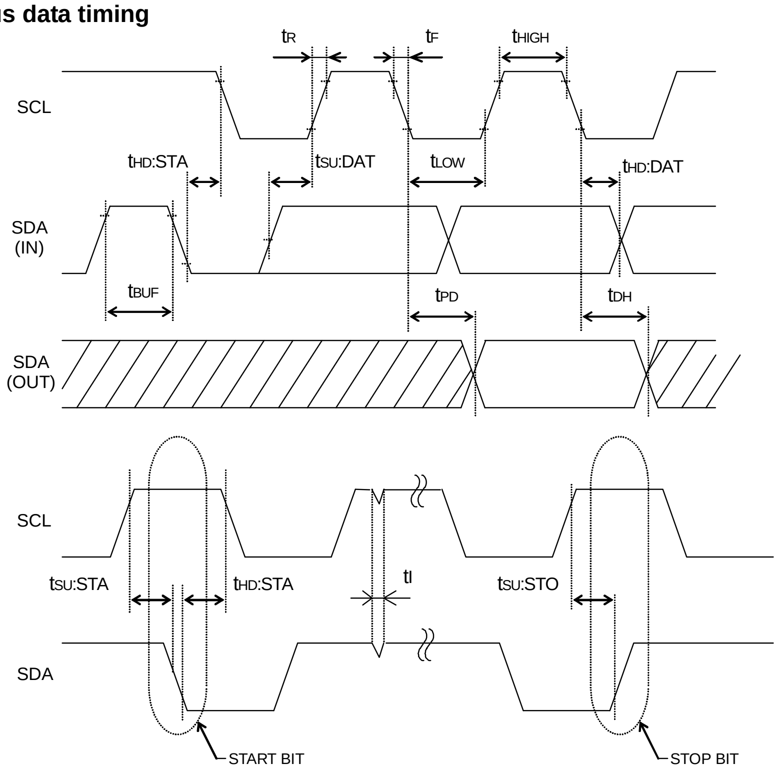


Fig 32 Auto-Read Timing Chart

Set the CT pin capacitance as follows:
Using an inappropriate capacitance setting may result in auto-read timing collisions, making it impossible to read data properly.

BD8139AEFV A	CT = 1000 pF	Scatter: Within 5%
BD8139AEFV B	CT = 3300 pF	Scatter: Within 5%

●2 wire serial bus data timing



* SDA latches at the SCL rising edge.

Fig 33

●Timing standard values

Parameter	Symbol	FAST-MODE 2.3 V ≤ DVcc ≤ 4.0 V			Unit
		Min.	Typ.	Max.	
SCL frequency	fSCL	—	—	400	kHz
SCL high time	tHIGH	0.6	—	—	µs
SCL low time	tLOW	1.2	—	—	µs
Rise Time	tR	—	—	0.3	µs
Fall Time	tF	—	—	0.3	µs
Start condition hold time	tHD:STA	0.6	—	—	µs
Start condition setup time	tSU:STA	0.6	—	—	µs
SDA hold time	tHD:DAT	100	—	—	ns
SDA setup time	tSU:DAT	100	—	—	ns
Acknowledge delay time	tPD	0.1	—	0.9	µs
Acknowledge hold time	tDH	0.1	—	—	µs
Stop condition setup time	tSU:STO	0.6	—	—	µs
Bus release time	tBUF	1.2	—	—	µs

●Power supply sequence

Activate the digital power supply DVcc before the Vcc power supply to prevent IC malfunctions due to undefined logic in the digital circuit. Input serial data after canceling the power-on reset. When turning off the IC's power supplies, turn off Vcc and then DVcc.

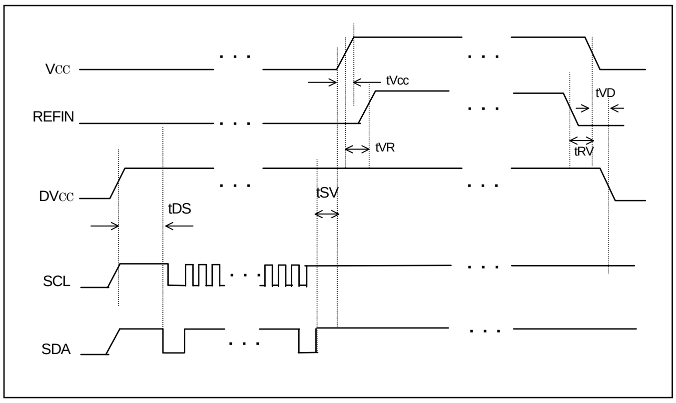


Fig. 34 Power Supply Sequence Diagram

●Power supply sequence standard values

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Serial input timing	tDS	100	—	—	µs	Cct = 1000 pF
Vcc activation timing	tSV	0	10	—	µs	
REFIN activation timing	tVR	0	10	—	µs	
REFIN off timing	tRV	0	10	—	µs	
Power supply off timing	tVD	0	10	—	µs	
Vcc startup timing	tVcc	1	—	—	ms	

●**Closing time for auto-read**

(Input Vcc ～ Beginning auto-read ～ Taking time for auto-read, when 2use.)

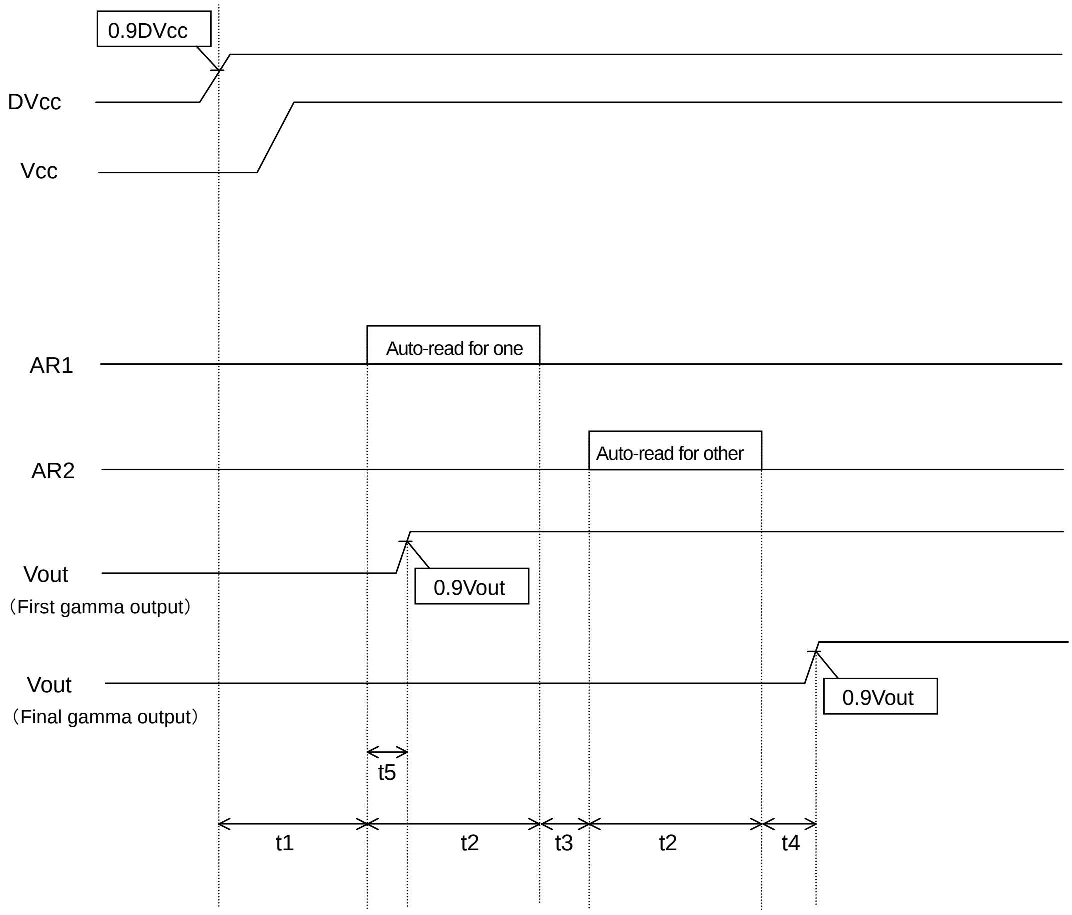


Fig. 35

Time from input Vcc until final gamma output

t total1 = t1 + t2 x 2 + t3 + t4

	min.	typ.	max
t1	108	169	240
t2	730	1160	1660
t3	156	248	356
t4	-	-	145
t total	1724	2737	4061

Unit : µsec

Time from input voltage until first gamma output (condition of input Vcc already)

t total2 = t1 + t5

	min.	typ.	max
t1	108	169	240
t5	194	308	442
t total	302	477	682

Unit : µsec

※CT1=1000pF, CT2=3300pF, scatter within 5%

●**When it inputs V_{CC}, it outputted the gamma output voltage.**

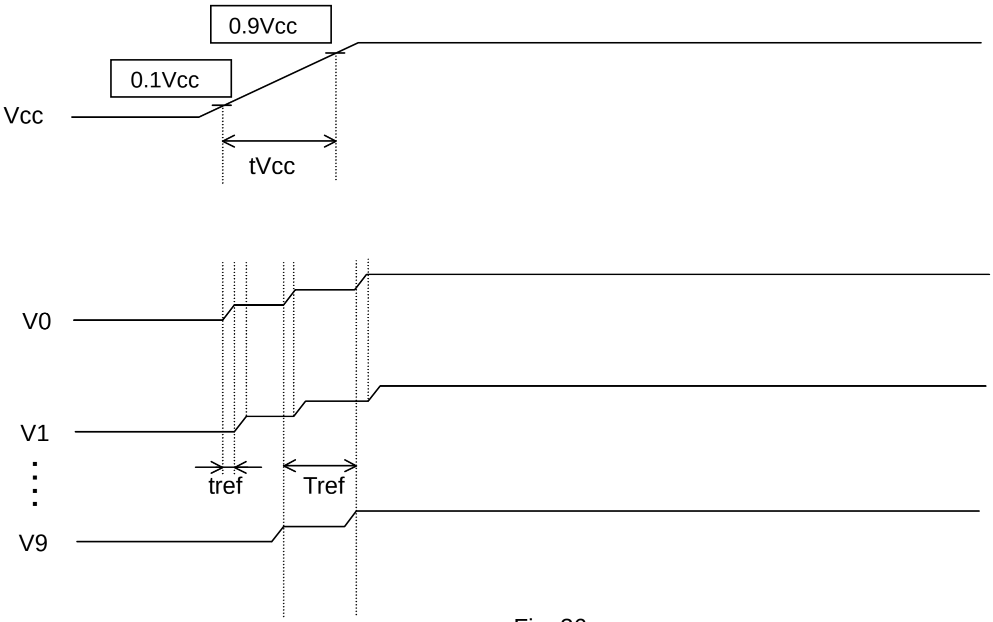


Fig. 36

DAC 1ch supports all gamma output amps by sample/hold function.
So, each amp operates reflesh by Tref.

	Min.	Typ.	Max.
Tref	63	101	145

Unit : µsec

Reflesh time of each amp is following.
tref = Tref / 11ch

Under condition of the small difference between setting voltage of amp and slew rate of V_{CC} is fast, when it inputs V_{CC}, it is possible that output voltage come from behind next output voltage.

$$\begin{cases} V0 = VDAC \times 2 \times \dfrac{n0 + 1}{1024} & \text{(n0 : Setting voltage of 10bit)} \\ V1 = VDAC' \times 2 \times \dfrac{n1 + 1}{1024} & \\ VDAC' = VDAC + \dfrac{SR}{2} \times tref & \text{(SR : Slew rate of } V_{CC}\text{)} \end{cases}$$

Condition of non-reverse-voltage is following
V0-V1>0

$$\frac{n0 + 1}{n1 + 1} > 1 + \frac{SR \times tref}{2VDAC}$$

Under condition of the big difference between output voltage or slew rate of V_{CC} is slow, reverse-voltage don't occur much.
Worst condition is following.
n0 / n1 > 1.0469
Notice that the setting voltage between V0 and V1 is within 720mV.
It is possible for reverse of voltage in transition.

●**Input equivalent circuit diagrams**

[BD8132FV]

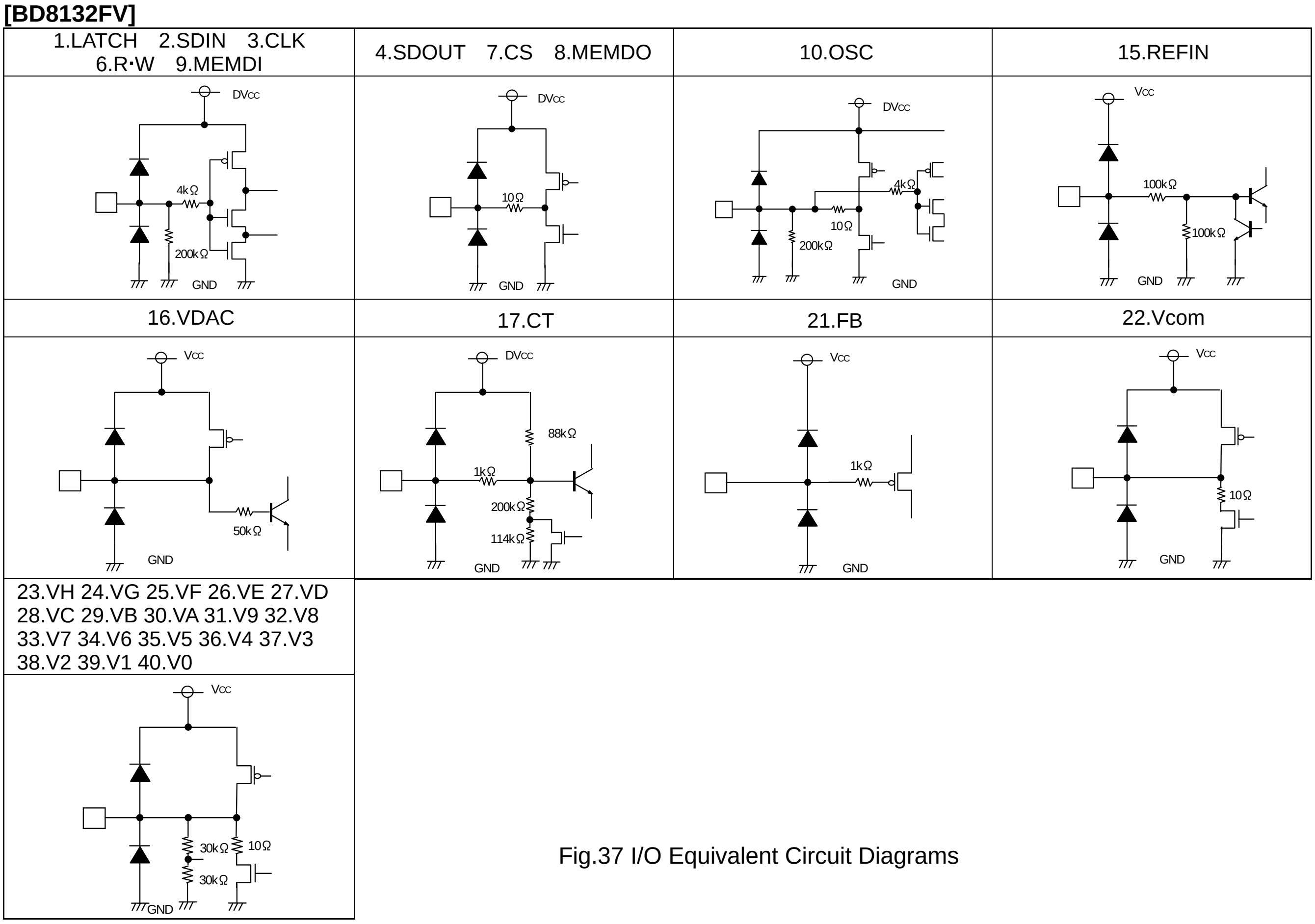


Fig.37 I/O Equivalent Circuit Diagrams

[BD8139AEFV]

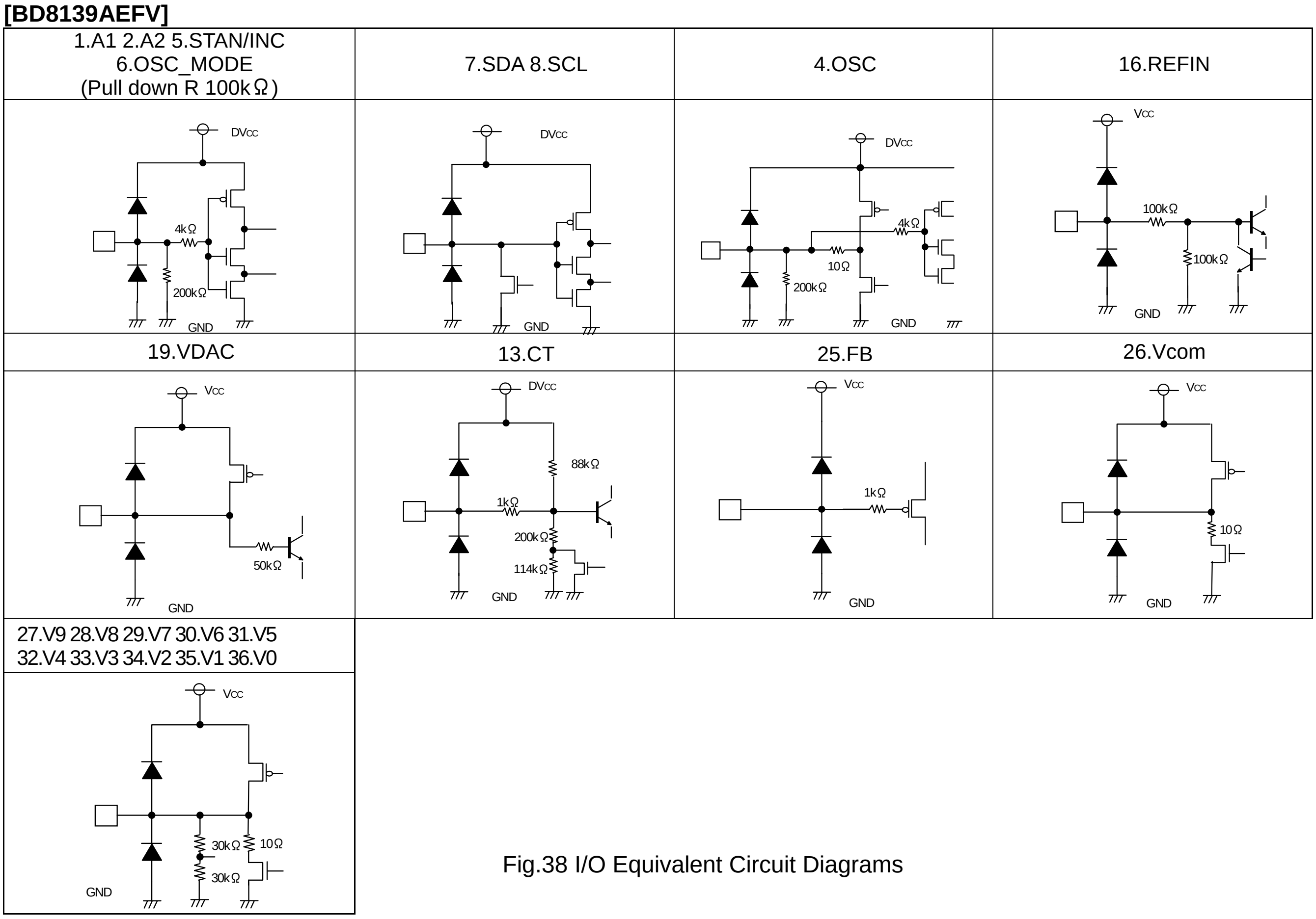


Fig.38 I/O Equivalent Circuit Diagrams

●Notes for use

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.For example, when the resistors and transistors are connected to the pins as shown in Fig.39, a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as the application of voltages lower than the GND (P substrate) voltage to input and output pins.

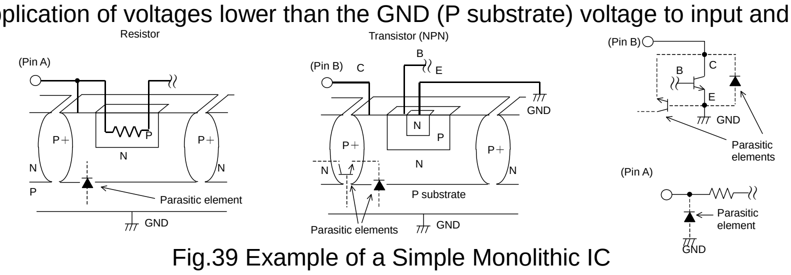


Fig.39 Example of a Simple Monolithic IC

9) Overcurrent protection circuits

An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

10) TSD (Thermal shutdown) circuit

This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature Tj will trigger the TSD circuit to turn off all output power elements. The circuit automatically resets once the junction temperature Tj drops.

Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11) Testing on application boards

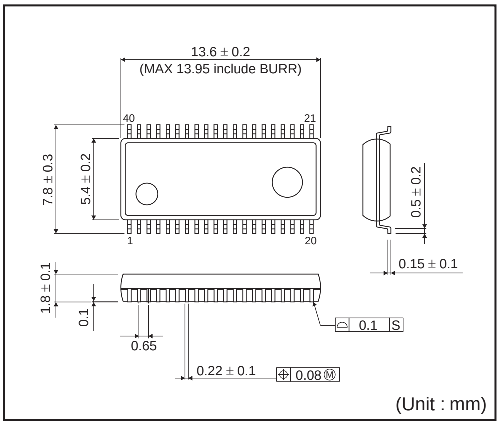
At the time of inspection of the installation boards, when the capacitor is connected to the pin with low impedance, be sure to discharge electricity per process because it may load stresses to the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

●Ordering part number

B	D	8	1	3	2	F	V	-	E	2

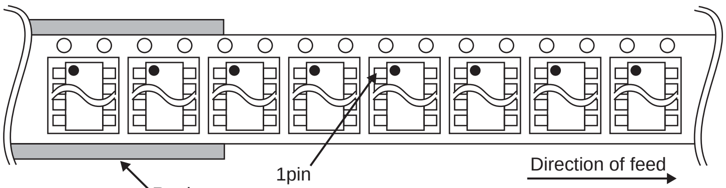
Part No. (BD)	Part No. (8132)	Package (FV)	Packaging and forming specification (E2)
Part No.	Part No. 8132 : 3-line serial 8139A: 2 wire serial	Package FV: SSOP-B40 EFV: HTSSOP-B40	Packaging and forming specification E2: Embossed tape and reel

SSOP-B40



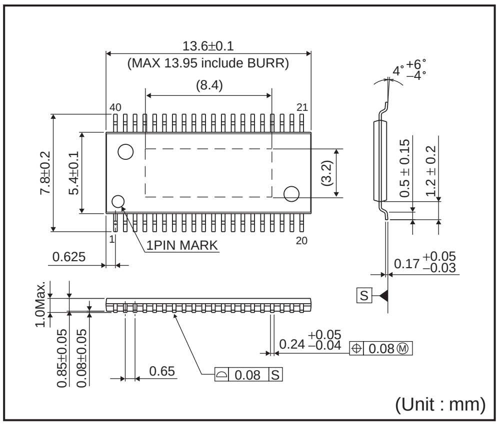
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



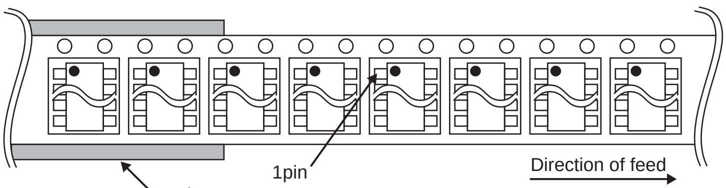
∗Order quantity needs to be multiple of the minimum quantity.

HTSSOP-B40



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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General Precaution

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ООО «ЛайфЭлектроникс» "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

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- *Регистрацию проекта у производителя компонентов.*
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Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru