

Sound Processor with Built-in 3-band Equalizer **BD37542FS**

General Description

BD37542FS is a sound processor with built-in 3-band equalizer for car audio. The functions are stereo input selector (which can switch single and ground isolation input), input-gain control, main volume, loudness, 5ch fader volume, LPF for subwoofer and mixing input. Moreover, "Advanced switch circuit", which is an original ROHM technology, can reduce various switching noise (ex. No-signal, low frequency like 20Hz & large signal inputs). Also, "Advanced switch" makes control of microcomputer easier, and can construct a high quality car audio system.

Features

- Reduced switching noise of input gain control, mute, main volume, fader volume, bass, middle, treble, loudness, mixing by using advanced switch circuit.
- Built-in differential input selector that can make various combination of single-ended / differential input.
- Built-in ground isolation amplifier inputs, which is ideal for external stereo input.
- Built-in input gain controller reduces switching noise for volume of a portable audio input.
- Decreased the number of external components due to built-in 3-band equalizer filter, LPF for subwoofer. It is possible to control Q, Gv, fo of 3-band equalizer, fc of LPF, and Gv of loudness by I²C BUS control.
- It is possible to adjust the gain of the bass, middle, treble up to ±20dB with 1 dB step gain adjustment.
- It is equipped with output terminals for Subwoofer. Moreover, the stereo signal output of the front and rear can also be chosen by the I²C BUS control.
- Built-in mixing input and mixing attenuator.
- Energy-saving design resulting in low-current consumption is achieved by utilizing the Bi-CMOS process. It has the advantage in guality over scaling down the power heat control of the internal regulators.
- Input terminals and output terminals are organized and separately laid out to keep the signal flow in one direction which results in simpler and smaller PCB layout.
- It is possible to control the I²C BUS by 3.3V / 5V.

Applications

It is optimal for car audio systems. It can also be used for audio equipment of mini Compo, micro Compo, TV, etc.

Κ

ey Specifications	
Power Supply Voltage Range:	7.0V to 9.5V
 Circuit Current (No Signal): 	38mA(Typ)
Total Harmonic Distortion 1:	
(FRONT,REAR)	0.001%(Typ)
Total Harmonic Distortion 2:	
(SUBWOOFER)	0.002%(Typ)
Maximum Input Voltage:	2.3Vrms (Typ)
Cross-talk Between Selectors:	-100dB (Typ)
Volume Control Range:	+15 dB to -79dB
Output Noise Voltage 1:	
(FRONT,REAR)	3.8µVrms(Typ)
Output Noise Voltage 2:	
(SUBWOOFER)	4.8µVrms(Typ)
	(1, 0,)/max = (T,)

- Residual Output Noise Voltage: 1.8µVrms(Typ) -40°C to +85°C Operating Temperature Range:

Package

W(Typ) x D(Typ) x H(Max)



OProduct structure : Silicon monolithic integrated circuit OThis product has no designed protection against radioactive rays

Typical Application Circuit



Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	A1	A input terminal of 1ch	17	LDB2	Loudness setting terminal of 2ch
2	A2	A input terminal of 2ch	18	LDA2	Loudness setting terminal of 2ch
3	B1	B input terminal of 1ch	19	MUTE	External compulsory mute terminal
4	B2	B input terminal of 2ch	20	N.C.	No Connection
5	C1	C input terminal of 1ch	21	TEST	Test Pin
6	C2	C input terminal of 2ch	22	OUTS2	Subwoofer output terminal of 2ch
7	DP1	D positive input terminal of 1ch	23	OUTS1	Subwoofer output terminal of 1ch
8	DN	D negative input terminal	24	OUTR2	Rear output terminal of 2ch
9	DP2	D positive input terminal of 2ch	25	OUTR1	Rear output terminal of 1ch
10	EP1	E positive input terminal of 1ch	26	OUTF2	Front output terminal of 2ch
11	EN1	E negative input terminal of 1ch	27	OUTF1	Front output terminal of 1ch
12	EN2	E negative input terminal of 2ch	28	VCC	Power supply terminal
13	EP2	E positive input terminal of 2ch	29	SCL	I ² C Communication clock terminal
14	MIN	Mixing input terminal	30	SDA	I ² C Communication data terminal
15	LDA1	Loudness setting terminal of 1ch	31	GND	GND terminal
16	LDB1	Loudness setting terminal of 1ch	32	FIL	VCC/2 terminal

Block Diagram



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	10.0	V
Input Voltage	Vin	V _{CC} +0.3 to GND-0.3	V
Power Dissipation	Pd	0.95 (Note 1)	W
Storage Temperature	Tstg	-55 to +150	°C

(Note 1) When mounted on the standard board (70 x 70 x 1.6 mm³), derate by 7.6mW/°C for Ta above 25°C.

Thermal resistance $\theta_{ja} = 131.6(^{\circ}C/W)$

Material : A FR4 grass epoxy board(3% or less of copper foil area)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Min	Тур	Max	Unit
Power Supply Voltage	Vcc	7.0	-	9.5	V
Temperature	Topr	-40	-	+85	°C

Electrical Characteristics

(Unless specified otherwise, Ta=25°C, V_{CC}=8.5V, f=1kHz, V_{IN}=1Vrms, Rg=600Ω, R_L=10kΩ, A1 input, Input gain 0dB, Mute OFF, Volume 0dB, Tone control 0dB, Loudness 0dB, LPF OFF, Mixing OFF, Fader 0dB)

Š	Deveryoter	C: maked		Limit		l lucit	Conditions
BLC	Parameter	Symbol	Min	Тур	Max	Unit	Conditions
	Circuit Current (No Signal)	lq	-	38	48	mA	No signal
	Voltage Gain	Gv	-1.5	0	+1.5	dB	Gv=20log(V _{OUT} /V _{IN})
	Channel Balance	СВ	-1.5	0	+1.5	dB	$CB = G_{V1}-G_{V2}$
	Total Harmonic Distortion 1 (FRONT,REAR)	THD+N1	-	0.001	0.05	%	V _{OUT} =1Vrms BW=400Hz-30KHz
	Total Harmonic Distortion 2 (SUBWOOFER)	THD+N2	-	0.002	0.05	%	V _{OUT} =1Vrms BW=400Hz-30KHz
ERAL	Output Noise Voltage 1 (FRONT,REAR) *	V _{NO1}	-	3.8	15	µVrms	Rg = 0Ω BW = IHF-A
GENE	Output Noise Voltage 2 (SUBWOOFER) *	V _{NO2}	-	4.8	15	µVrms	Rg = 0Ω BW = IHF-A
	Residual Output Noise Voltage *	Vnor	-	1.8	10	μVrms	Fader = -∞dB Rg = 0Ω BW = IHF-A
	Crosstalk Between Channels *	СТС	-	-100	-90	dB	Rg = 0Ω CTC=20log(V _{OUT} /V _{IN}) BW = IHF-A
	Ripple Rejection	RR	-	-70	-40	dB	f=1kHz V _{RR} =100mVrms RR=20log(V _{CC} IN/V _{OUT})
	Input Impedance(A, B,C)	RIN_S	70	100	130	kΩ	
~	Input Impedance(D, E)	R _{IN_D}	175	250	325	kΩ	
ECTOF	Maximum Input Voltage	VIM	2.1	2.3	-	Vrms	V _{IM} at THD+N(V _{OUT})=1% BW=400Hz-30KHz
JT SELE	Crosstalk Between Selectors *	CTS	-	-100	-90	dB	Rg = 0Ω CTS=20log(V _{OUT} /V _{IN}) BW = IHF-A
INPI	Common Mode Rejection Ratio *	CMRR	50	65	-	dB	XP1 and XN input XP2 and XN input CMRR=20log(V _{IN} /V _{OUT}) BW = IHF-A,[*XD,E]

Electrical Characteristics - continued

Ğ		Limit			Conditions			
BLO	Parameter	Symbol	Min	Тур	Max	Unit	Conditions	
BAIN	Minimum Input Gain	Gin_min	-2	0	+2	dB	Input gain 0dB V _{IN} =100mVrms G _{IN} =20log(V _{OUT} /V _{IN})	
NPUT 0	Maximum Input Gain	Gin_max	18	20	22	dB	Input gain 20dB V _{IN} =100mVrms G _{IN} =20log(V _{OUT} /V _{IN})	
	Gain Set Error	G_{IN_ERR}	-2	0	+2	dB	GAIN=+1dB to +20dB	
MUTE	Mute Attenuation *	G _{MUTE}	-	-105	-85	dB	Mute ON G _{MUTE} =20log(V _{OUT} /V _{IN}) BW = IHF-A	
	Maximum Gain	Gv max	13	15	17	dB	Volume = $15dB$ V _{IN} =100mVrms Gv=20log(V _{OUT} /V _{IN})	
UME	Maximum Attenuation *	G∨_min	-	-100	-85	dB	$G_{V}=20\log(V_{OUT}/V_{IN})$ BW = IHF-A	
NOI	Attenuation Set Error 1	Gv_err1	-2	0	+2	dB	GAIN & ATT=+15dB to -15dB	
	Attenuation Set Error 2	Gv_err2	-3	0	+3	dB	ATT=-16dB to -47dB	
	Attenuation Set Error 3	Gv_err3	-4	0	+4	dB	ATT=-48DB to -79DB	
	Maximum Boost Gain	Gb_bst	18	20	22	dB	Gain=+20dB f=100Hz V _{IN} =100mVrms G _B =20log (V _{OUT} /V _{IN})	
BASS	Maximum Cut Gain	G _{B_CUT}	-22	-20	-18	dB	Gain=-20dB f=100Hz V _{IN} =2Vrms G _B =20log (V _{OUT} /V _{IN})	
	Gain Set Error	Gb_err	-2	0	+2	dB	Gain=-20dB to +20dB f=100Hz	
ш	Maximum Boost Gain	G м_вst	18	20	22	dB	Gain=+20dB f=1kHz V _{IN} =100mVrms G _M =20log (V _{OUT} /V _{IN})	
MIDDL	Maximum Cut Gain	G м_сит	-22	-20	-18	dB	Gain=-20dB f=1kHz V _{IN} =2Vrms G _M =20log (V _{OUT} /V _{IN})	
	Gain Set Error	Gm_err	-2	0	+2	dB	Gain=-20dB to +20dB f=1kHz	
Щ	Maximum Boost Gain	G _{T_BST}	18	20	22	dB	Gain=+20dB f=10kHz V _{IN} =100mVrms GT=20log (V _{OUT} /V _{IN})	
TREBI	Maximum Cut Gain	Gt_cut	-22	-20	-18	dB	Gain=-20dB f=10kHz V _{IN} =2Vrms G _T =20log (V _{OUT} /V _{IN})	
	Gain Set Error	Gt_err	-2	0	+2	dB	Gain=-20dB to +20dB f=10kHz	
	Input Impedance	RIN_M	19	27	35	kΩ		
ŋ	Maximum Input Voltage	VIM_M	2.0	2.2	-	Vrms	V _{IM} at THD+N(V _{OUT})=1% BW=400Hz-30KHz	
MIXIN	Maximum Attenuation	GMX_MIN	-	-100	-85	dB	MIX=OFF G _{MX} =20log(V _{OUT} /V _{IN}) BW=INF-A	
	Maximum Gain	Gмх_мах	5	7	9	dB	ATT=+6dB G _{MX} =20log(V _{OUT} /V _{IN})	

Electrical Characteristics - continued

оск	Doromotor	Sumbol	Limit			L Incit	Conditions	
BLC	Parameter	Symbol	Min	Тур	Max	Unit	Conditions	
	Maximum Boost Gain	_					Fader=15dB	
		G _{F_BST}	13	15	17	dB	V _{IN} =100mVrms	
							GF=2010g(Vout/VIN)	
Ř	Asymum Attenuation *			-100	-90	dB	Fader = -∞dB	
OOFE	Maximum Attenuation *	GF_MIN	-				GF=20log(Vout/VIN)	
							BW = IHF-A	
BŇ	Gain Set Error	GF_err	-2	0	+2	dB	Gain=+1dB to +15dB	
NS/	Attenuation Set Error 1	G_{F_ERR1}	-2	0	+2	dB	ATT=-1dB to -15dB	
ER	Attenuation Set Error 2	G_{F_ERR2}	-3	0	+3	dB	ATT=-16dB to -47dB	
FAD	Attenuation Set Error 3	Gf_err3	-4	0	+4	dB	ATT=-48dB to -79dB	
	Output Impedance	Rout	-	-	50	Ω	V _{IN} =100mVrms	
	Maximum Qutrut Valtage		0	2.2			THD+N=1%	
	Maximum Output Voltage	VOM	2	2.2	-	vrms	BW=400Hz-30KHz	
							Gain 20dB	
S S	Maximum Gain	GL MAX	17	20	23	dB	V _{IN} =100mVrms	
NG		_				-	GL=20log(Vout/VIN)	
LOUI	Gain Set Error	Gl_err	-2	0	+2	dB	Gain=+1dB to +20dB	

VP-9690A(Average value detection, effective value display) filter by Matsushita Communication is used for * measurement. Phase between input / output is same.



Figure 1. Circuit Current (No Signal) vs Power Supply Voltage







25 BASS GAIN : -20dB to +20dB /1dB step fo : 60Hz Q : 0.5 20 15 10 Bass Gain [dB] 5 0 -5 -10 -15 -20 -25 10 100 100k 1k 10k Frequency [Hz]

Figure 3. Gain vs Frequency

Figure 4. Bass Gain vs Frequency



Figure 5. Bass fo vs Frequency





Figure 7. Middle Gain vs Frequency



Figure 8. Middle fo vs Frequency





Figure 11. Treble fo vs Frequency

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Figure 14. Output Noise vs Bass Gain



Figure 15. Output Noise vs Middle Gain





Figure 17. CMRR vs Frequency

Figure 18. Output Voltage vs RLOAD



Figure 19. Advanced Switch 1



Figure 20. Advanced Switch 2

Timing Chart

CONTROL SIGNAL SPECIFICATION

(1) Electrical Specifications and Timing for Bus Lines and I/O Stages



Figure 21. I²C-bus Signal Timing Diagram

Table 1 Characteristics of the SDA and SCL bus lines for I²C-bus devices (Ta=25°C, V_{CC}=8.5V)

	Parameter	Symbol	Fast-mode	l Init		
	T alameter	Symbol	Min	Max	Onit	
1	SCL clock frequency	fscl	0	400	kHz	
2	Bus free time between a STOP and START condition	t _{BUF}	1.3	-	μS	
3	Hold time (repeated) START condition. After this period, the first clock	tup.ota	0.6		211	
5	pulse is generated	LHD;STA	0.0		μΟ	
4	LOW period of the SCL clock	tLOW	1.3	-	μS	
5	HIGH period of the SCL clock	tнigн	0.6	-	μS	
6	Set-up time for a repeated START condition	t _{SU;STA}	0.6	-	μS	
7	Data hold time:	thd;dat	0.06 (Note)	-	μS	
8	Data set-up time	tsu;dat	120	-	ns	
9	Set-up time for STOP condition	t _{su;sto}	0.6	-	μS	

All values refer to VIH Min and VIL Max Levels (see Table 2).

(Note) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH Min of the SCL signal) in order to bridge the undefined region of the falling edge of SCL. For 7(tHD:DAT), 8(ts:DAT), make the setup in which the margin is full.

Table 2 Characteristics of the SDA and SCL I/O stages for I²C-bus devices

	Parameter		Fast-mode	Linit	
			Min	Max	Unit
10	LOW level input voltage:	VIL	-0.3	+1	V
11	HIGH level input voltage:	Vін	2.3	5	V
12	Pulse width of spikes which must be suppressed by the input filter.	tsp	0	50	ns
13	LOW level output voltage: at 3mA sink current	V _{OL1}	0	0.4	V
14	Input current each I/O pin with an input voltage between 0.4V and 4.5V.	h	-10	+10	μA



SCL clock frequency : 250kHz



(2) <u>I²C BUS FORMAT</u>

	MSB LSB		MSB	LSB		MSB	LSB			
S	Slave Address	Α	Select Add	ress	Α	C	Data	Α	Ρ	
1bit	8bit	1bit	8bi	t	1bit		8bit	1bit	1bit	
S = Start condition (Recognition of start bit)										
	Slave Address	ess = Recognition of slave address. The first 7 bits correspond to the slave addre						e address.		
		The least significant bit is "L" which corresponds to write mode.								
	A	= AC	KNOWLEDGE	bit (Rec	ognit	ion of ackn	owledgement))		
	Select Address	s = Select address corresponding to volume, bass or treble.								
	Data	= Data on every volume and tone.								
	Р	= Stop condition (Recognition of stop bit)								

(3) <u>I²C BUS Interface Protocol</u>

(a) Basic Format

(~) -									
S	Slave Addr	ess	Α	Select Addres	S	Α	Data	Α	Р
	MSB	LSB		MSB	LSB	N	ISB I	LSB	

/1	- \	A set a set a final second set of		1.4	
ır	าเ	Automatic increment i	Select Address increases i	(+ 1) according to the number of data)
11	"				according to the number of data.

	S	Slave Add	dress	А	Select Ad	dress	А	Data	a1	А	Data2	А		DataN	А	Ρ
-		MSB	LSB		MSB	LSB		MSB	LSE	3	MSB	LSB	5	MSB	LS	SB

(Example) (1) Data1 shall be set as data of address specified by Select Address.

②Data2 shall be set as data of address specified by Select Address +1.

③DataN shall be set as data of address specified by Select Address +N-1.

(c) Configuration Unavailable for Transmission (In this case, only Select Address1 is set.)

S	Sla	ave Add	lress	A	Select A	ddress1	Α	Da	ata	A	Select	Address 2	Α	Da	ata	А	Ρ
	MSI	3	LSB	Ν	1SB	LSB	N	ISB	LSE	3	MSB	LS	ΒI	MSB	LS	В	
		(Note)If an	y da	ta is transn	nitted as S	sele	ct Ac	ddres	s 2 i	next to d	lata, it is rec	ogn	ized			

(Note)If any data is transmitted as Select Address 2 next to data, it is recogni as data, not as Select Address 2.

(4) Slave Address

MSB							LSB	
A6	A5	A4	A3	A2	A1	A0	R/W	
1	0	0	0	0	0	0	0	80H

(5) <u>Select Address & Data</u>

Itomo	Select	MSB			Da	ata			LSB
nems	(hex)	D7	D6	D5	D4	D3	D2	D1	D0
Initial setup 1	01	Advanced switch ON/OFF	0	Advanced of Input G Tone/Fade Miz	switch time ain/Volume r/Loudness king	0	1	Advanc time o	ed switch of Mute
Initial setup 2	02	LPF Phase	0	Subwoof Se	er Output lect	0	Su	bwoofer LP	F fc
Initial setup 3	03	0	0	0	0	0	0	1	0
Input Selector	05	Full-diff Type	0	0		Ir	put selector	r	
Input gain	06	Mute ON/OFF	0	0			Input Gain		
Volume gain	20			١	/olume Gain	/ Attenuation	ו		
Fader 1ch Front	28				Fader Gain /	Attenuation			
Fader 2ch Front	29			Fader Gain / Attenuation					
Fader 1ch Rear	2A			Fader Gain / Attenuation					
Fader 2ch Rear	2B				Fader Gain /	Attenuation			
Fader Subwoofer	2C				Fader Gain /	Attenuation			
Mixing	30			[Mixing Gain	/ Attenuation			
Bass setup	41	0	0	Bas	ss f _o	0	0	Ba	ss Q
Middle setup	44	0	0	Mide	dle fo	0	0	Mid	dle Q
Treble setup	47	0	0	Treb	ole f _o	0	0	0	Treble Q
Bass gain	51	Bass Boost/ Cut	0	0			Bass Gain		
Middle gain	54	Middle Boost/ Cut	0	0 Middle Gain					
Treble gain	57	Treble Boost/ Cut	0) 0 Treble Gain					
Loudness Gain	75	0	Loudne	ss Hicut		Lo	udness Gai	n	
System Reset	FE	1	0	0	0	0	0	0	1

Note

: Advanced switch

- 1. The Advance Switch works in the latch part while changing from one function to another.
- 2. Upon continuous data transfer, the Select Address rolls over because of the automatic increment function, as shown below.



- 3. Advanced switch is not used for the function of input selector, subwoofer output select, etc. Therefore, please apply mute on the side when changing these settings.
- 4. When using mute function of this IC at the time of changing input selector, please switch mute ON/OFF while waiting for advanced-mute time.

Select address 01 (hex)

Timo	MSB	MSB Advanced switch time of Mute									
Time	D7	D6	D5	D4	D3	D2	D1	D0			
0.6msec	Advanced		Advanced	switch time			0	0			
1.0msec	Switch	0	of Input ga	ain/Volume	0	1	0	1			
1.4msec		0	Tone/Fade	r/Loudness	0	I	1	0			
3.2msec			Mix	king			1	1			

Time	MSB	Ad	vance gain/V Lo	d swite olume/ udnes	ch tim /Tone, s/Mix	e of In /Fader ing	put ⁄	LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
4.7 msec	Advonced		0	0					
7.1 msec	Advanced	0	0	1		1	Advanced switch		
11.2 msec		0	1	0	0	I	Time of Mute		
14.4 msec	UN/OFF		1	1					

Mada	MSB		Advanced switch ON/OFF							
IVIOUE	D7	D6	D5	D4	D3	D2	D1	D0		
OFF	0	0	Advanced switch time of Input gain/Volume			1	Advance	ed switch		
ON	1	Ũ	Tone/Fade Mix	r/Loudness king	Ŭ		Time o	of Mute		

Select address 02(hex)

fo	MSB		Sı	lpwoot	fer LPF	= fc		LSB
IC	D7	D6	D5	D4	D3	D2	D1	D0
OFF						0	0	0
55Hz						0	0	1
85Hz	LPF	0	Subwoof	er Output	0	0	1	0
120Hz	Phase	0	Se	lect	0	0	1	1
160Hz						1	0	0
Prohibition							Other setting	3

Modo	MSB		Subw	oofer (Dutput	Selec	t	LSB
WOUE	D7	D6	D5	D4	D3	D2	D1	D0
LPF			0	0				
Front	LPF		0	1				- ,
Rear	Phase	0	1	0	0	Su	bwooter LPF	- IC
Prohibition			1	1				

Bhasa	MSB			LPF F	Phase			LSB
FlidSe	D7	D6	D5	D4	D3	D2	D1	D0
0°	0	0	Subwoof	er output	0	S.	hwaafar	
180°	1	0	se	lect	U	50	bwooler Li	

Select address 05(hex)

Mada		,	MSB			Input	Selector			LSB
wode	OUTF1	OUTF2	D7	D6	D5	D4	D3	D2	D1	D0
А	A1	A2				0	0	0	0	0
В	B1	B2				0	0	0	0	1
С	C1	C2				0	0	0	1	0
D single	DP1	DP2				0	0	0	1	1
E1 single	EP1	EN1	Full-			0	1	0	1	0
E2 single	EN2	EP2	diff bias	0	0	0	1	0	1	1
A diff	A1	B1	type	0	0	0	1	1	1	1
C diff	B2	C2	select			1	0	0	0	0
D diff	DP1	DP2				0	0	1	1	0
E full diff	EP1	EP2				0	1	0	0	0
Inp	ut SHOR	T				0	1	0	0	1
Р	rohibition	1					0	ther setting	1	

Input SHORT : The input impedance of each input terminal is lowered from $100k\Omega(Typ)$ to $6 k\Omega(Typ)$. (For quick charge of coupling capacitor)

Mada	MSB	MSB Full-diff Bias Type Select							
Mode	D7	D6	D5	D4	D3	D2	D1	D0	
Negative Input	0	0	0		Inn	ut Solootor			
Bias	1	U	U		inp				



Select address 06 (hex)

Mada	MSB Input Gain									
Mode	D7	D6	D5	D4	D3	D2	D1	D0		
0dB				0	0	0	0	0		
1dB				0	0	0	0	1		
2dB				0	0	0	1	0		
3dB				0	0	0	1	1		
4dB				0	0	1	0	0		
5dB				0	0	1	0	1		
6dB				0	0	1	1	0		
7dB				0	0	1	1	1		
8dB				0	1	0	0	0		
9dB				0	1	0	0	1		
10dB				0	1	0	1	0		
11dB	Mute	0		1	1					
12dB	ON/OFF	0	0	0	1	1	0	0		
13dB				0	1	1	0	1		
14dB				0	1	1	1	0		
15dB				0	1	1	1	1		
16dB				1	0	0	0	0		
17dB				1	0	0	0	1		
18dB				1	0	0	1	0		
19dB				1	0	0	1	1		
20dB				1	0	1	0	0		
Prohibition				1	1	0	1	1		
				:	:	:	:			
				1	1	1	1	1		

Mode	MSB		Mute ON/OFF						
WOUE	D7	D6	D5	D4	D3	D2	D1	D0	
OFF	0	0	0			Input Coin			
ON	1	U	0			input Gain			

Select address 20, 28, 29, 2A, 2B, 2C (hex)

	MSB	Vo	I, Fad	er Gai	in / Att	enuati	ion	LSB
Gailt & ATT	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0
Prohibition	0	0	0	0	0	0	0	1
	:	•	:	•	:	•	:	•
	0	1	1	1	0	0	0	0
15dB	0	1	1	1	0	0	0	1
14dB	0	1	1	1	0	0	1	0
13dB	0	1	1	1	0	0	1	1
:	:	•••	:	:	:	:	:	:
-77dB	1	1	0	0	1	1	0	1
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
	1	1	0	1	0	0	0	0
Prohibition	:	:	:	:	:		:	
	1	1	1	1	1	1	1	0
-∞dB	1	1	1	1	1	1	1	1

Select address 30(hex)

	MSB		Mixing	Gain	/ Atter	nuatio	n	LSB
Gain & ATT	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
Prohibition	:	:	:	:	:	:	:	:
	0	1	1	1	1	0	0	0
7dB	0	1	1	1	1	0	0	1
6dB	0	1	1	1	1	0	1	0
5dB	0	1	1	1	1	0	1	1
:	:	:	:	:	:	:	:	:
-77dB	1	1	0	0	1	1	0	1
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
	1	1	0	1	0	0	0	0
Prohibition	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
MIX OFF	1	1	1	1	1	1	1	1

Select address 41(hex)

Ofactor	MSB		В	ass Q factor L				
QTACION	D7	D6	D5	D4	D3	D2	D1	D0
0.5							0	0
1.0	0	0	Bog	o f-	0	0	0	1
1.5	0	0	Dat	5510	0	0	1	0
2.0							1	1

fo	MSB			Bass	s fo			LSB
10	D7	D6	D5	D4	D3	D2	D1	D0
60Hz			0	0				
80Hz	0	0	0	1	0	0	Ba	ass
100Hz	0	0	1	0	0	0	Q fa	actor
120Hz			1	1				

Select address 44(hex)

O factor	MSB		Middle Q factor					
	D7	D6	D5	D4	D3	D2	D1	D0
0.75							0	0
1.0	0	0	Mide	dio fe	0	0	0	1
1.25	0	0	Wildo		0	0	1	0
1.5							1	1

fo	MSB			Middl	e fo			LSB
10	D7	D6	D5	D4	D3	D2	D1	D0
500Hz			0	0				
1kHz		0	0	1	0	0	Mic	dle
1.5kHz	0	0	1	0	0	0	Q fa	actor
2.5kHz			1	1				

Select address 47 (hex)

O factor	MSB		Tre	eble	Q fact	tor		LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0.75	0	0	Treble fo		0	0	0	0
1.25	0	0	Tiec	I reble to		0	0	1
fo	MSB		Treble fo LSE					
10	D7	D6	D5	D4	D3	D2	D1	D0
7.5kHz			0	0				
10kHz	0	0	0	1	0	0	0	Treble
12.5kHz		0	1	0] 0	0	0	Q factor
15kHz			1	1]			

Select address 51, 54, 57 (hex)

Coin	MSB		B	ass/Middle	/Treble Gai	n		LSB
Gain	D7	D6	D5	D4	D3	D2	D1	D0
0dB		7 D6 ss/ dle/ ble 0 ost ut		0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB	Bass/	Bass/ Middle/		0	1	0	1	0
11dB	Middle/			0	1	0	1	1
12dB	Treble	0	0	0	1	1	0	0
13dB	Boost			0	1	1	0	1
14dB	/cut			0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
				1	0	1	0	1
Prohibition					:	:		:
					1	1	1	1
				1	1	1	1	1

Mada	MSB	Bas	ss/Mic	ldle/Tr	eble E	Boost/0	Cut	LSB		
wode	D7 D6 D5 D4 D3 D2 D1									
Boost	0	0	0		Beee/	Middle/Trobl	o Coin			
Cut	1	0	0	Bass/Middle/Treble Gain						

Select address 75 (hex))							
Mada	MSB		L	oudne	ss Hic	cut		LSB
wode	D7	D6	D5	D4	D3	D2	D1	D0
Hicut1		0	0		•	•	•	•
Hicut2	0	0	1		1.		in	
Hicut3	0	1	0		L	ouuness Ga		
Hicut4		1	1					
	n							
Gain	MSB			oudne	<u>ss Ga</u>	in	_	LSB
Call	D7	D6	D5	D4	D3	D2	D1	D0
0dB				0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB	0	Loudne	se Hicut	0	1	0	1	1
12dB	U	Loudine	33 1 11001	0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
				1	0	1	0	1
Prohibition				:	:	:	:	:
				1	1	1	1	1

: Initial condition

(6) About Power ON Reset

Built-in IC initialization is made during power ON of the supply voltage. Please send initial data to all addresses at supply voltage on. And please turn on mute until this initial data is sent.

Parameter	Symbol	Limit			Lloit	Conditions	
		Min	Тур	Max	Unit	Conditions	
Rise Time of VCC	trise	33	-	-	µsec	V_{CC} rise time from 0V to 5V	
VCC Voltage of Release Power ON Reset	Vpor	-	4.1	-	V		

(7) About External Compulsory Mute Terminal

It is possible to force mute externally by setting an input voltage to the MUTE terminal.

Mute Voltage Condition	Mode
GND to 1.0V	MUTE ON
2.3V to V _{CC}	MUTE OFF

Establish the voltage of MUTE in the condition you want to set.

Application Information

1. Function and Specifications

Function	Specifications									
	Stereo input	t								
	Single-End/Diff/Full-Diff									
	(Possible to set the number of single-end/diff/full-diff as follows)									
		Single-End	Differential	Full-Differential						
Input	Mode 1	0	3	1						
Selector	Mode 2	3	1	1						
	Mode 4	4	0	1						
	Mode 5	5	1	0						
	Mode 6	6 Table 4 Cambi	0	0						
			nation of input se	elector						
Input gain	• +200B 10 00									
	Possible to	use "Advanced s	witch" for preven	tion of switching noise.						
Mute	Possible to	use "Advanced s	witch" for preven	tion of switching noise.						
Volume	• +15dB to -7	9dB (1dB step),	-∞dB							
	 Possible to 	use "Advanced s	witch" for preven	tion of switching noise.						
	+20dB to -20dB (1dB step)									
Bass	• Q=0.5, 1, 1.5, 2									
Duoo	• fo=60, 80, 100, 120Hz									
	Possible to use "Advanced switch" for prevention of switching noise.									
	· +20dB to -20dB (1dB step)									
Middle	· Q=0.75, 1, 1.25, 1.5									
Widdle	• fo =500, 1k, 1.5k 2.5kHz									
	Possible to use "Advanced switch" for prevention of switching noise.									
	· +20dB to -20dB (1dB step)									
Treble	· Q=0.75, 1.25									
110010	• fo =7.5k, 10k, 12.5k, 15kHz									
	Possible to use "Advanced switch" for prevention of switching noise.									
Fader	 +15dB to -79dB(1dB step), -∞dB 									
	Possible to use "Advanced switch" for prevention of switching noise.									
Loudness	· 20dB to 0dB(1dB step)									
Loudiness	Possible to	use "Advanced s	witch" for preven	tion of switching noise.						
IPF	• fc=55/85/12	0Hz/160Hz, pas	3							
	 Phase shift 	(0°/180°)								
	・Monaural in	put								
Mixing	 +7dB to -79dB (1dB step), -∞dB 									
	Possible to use "Advanced switch" for prevention of switching noise.									

2. Volume / Fader Volume / Mixing Attenuation Data

(dB)	D7	D6	D5	D4	D3	D2	D1	D0		(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+15	0	1	1	1	0	0	0	1		-33	1	0	1	0	0	0	0	1
+14	0	1	1	1	0	0	1	0		-34	1	0	1	0	0	0	1	0
+13	0	1	1	1	0	0	1	1		-35	1	0	1	0	0	0	1	1
+12	0	1	1	1	0	1	0	0		-36	1	0	1	0	0	1	0	0
+11	0	1	1	1	0	1	0	1		-37	1	0	1	0	0	1	0	1
+10	0	1	1	1	0	1	1	0		-38	1	0	1	0	0	1	1	0
+9	0	1	1	1	0	1	1	1		-39	1	0	1	0	0	1	1	1
+8	0	1	1	1	1	0	0	0		-40	1	0	1	0	1	0	0	0
+7	0	1	1	1	1	0	0	1		-41	1	0	1	0	1	0	0	1
+6	0	1	1	1	1	0	1	0		-42	1	0	1	0	1	0	1	0
+5	0	1	1	1	1	0	1	1		-43	1	0	1	0	1	0	1	1
+4	0	1	1	1	1	1	0	0		-44	1	0	1	0	1	1	0	0
+3	0	1	1	1	1	1	0	1		-45	1	0	1	0	1	1	0	1
+2	0	1	1	1	1	1	1	0		-46	1	0	1	0	1	1	1	0
+1	0	1	1	1	1	1	1	1		-47	1	0	1	0	1	1	1	1
0	1	0	0	0	0	0	0	0		-48	1	0	1	1	0	0	0	0
-1	1	0	0	0	0	0	0	1		-49	1	0	1	1	0	0	0	1
-2	1	0	0	0	0	0	1	0		-50	1	0	1	1	0	0	1	0
-3	1	0	0	0	0	0	1	1		-51	1	0	1	1	0	0	1	1
-4	1	0	0	0	0	1	0	0		-52	1	0	1	1	0	1	0	0
-5	1	0	0	0	0	1	0	1		-53	1	0	1	1	0	1	0	1
-6	1	0	0	0	0	1	1	0		-54	1	0	1	1	0	1	1	0
-7	1	0	0	0	0	1	1	1		-55	1	0	1	1	0	1	1	1
-8	1	0	0	0	1	0	0	0		-56	1	0	1	1	1	0	0	0
-9	1	0	0	0	1	0	0	1		-57	1	0	1	1	1	0	0	1
-10	1	0	0	0	1	0	1	0		-58	1	0	1	1	1	0	1	0
-11	1	0	0	0	1	0	1	1		-59	1	0	1	1	1	0	1	1
-12	1	0	0	0	1	1	0	0		-60	1	0	1	1	1	1	0	0
-13	1	0	0	0	1	1	0	1		-61	1	0	1	1	1	1	0	1
-14	1	0	0	0	1	1	1	0		-62	1	0	1	1	1	1	1	0
-15	1	0	0	0	1	1	1	1		-63	1	0	1	1	1	1	1	1
-16	1	0	0	1	0	0	0	1		-64	1	1	0	0	0	0	0	1
-17	1	0	0	1	0	0	1			-00	1	1	0	0	0	0	1	0
-10	1	0	0	1	0	0	1	1		-00	1	1	0	0	0	0	1	1
-19	1	0	0	1	0	1	0	0		-07	1	1	0	0	0	1	0	0
-20	1	0	0	1	0	1	0	1		-60 -69	1	1	0	0	0	1	0	1
-27	1	0	0	1	0	1	1	0		<u>-03</u>	1	1	0	0	0	1	1	0
-23	1	0	0	1	0	1	1	1		-71	1	1	0	0	0	1	1	1
-24	1	0	0	1	1	0	0	0		-72	1	1	0	0	1	0	0	0
-25	1	0	0	1	1	0	0	1		-73	1	1	0	0	1	0	0	1
-26	1	õ	õ	1	1	0	1	0		-74	1	1	0	Ő	1	0	1	0
-27	1	Ő	Ő	1	1	0	1	1		-75	1	1	0	Ő	1	0	1	1
-28	1	Ő	Ő	1	1	1	0	0		-76	1	1	Ő	0	1	1	0	0
-29	1	Ő	Ő	1	1	1	0	1		-77	1	1	0	Ő	1	1	0	1
-30	1	Ő	Ő	1	1	1	1	0		-78	1	1	0	Ő	1	1	1	0
-31	1	0	0	1	1	1	1	1		-79	1	1	0	0	1	1	1	1
-32	1	0	1	0	0	0	0	0	1	-∞	1	1	1	1	1	1	1	1

Mixing Adjustable range is +7dB to -∞dB.





differential input to single input 4 to 6.

Unit
R : [Ω]
C : [F]

Figure 23. BD37543FS

①Please connect the decoupling capacitor of the power supply in the shortest possible distance to GND. 2 GND lines shall be one-point connected.

③Wiring pattern of Digital shall be away from that of analog unit and crosstalk shall not be acceptable.

④If possible, SDA and SCL lines of I²C BUS shall not be parallel.

The lines shall be shielded, if they are adjacent to each other.

(5) If possible, analog input lines should not be parallel. The lines should be shielded, if they are adjacent to each other. 6 About TEST pin (Pin 21), please leave it OPEN.

Power Dissipation

About the thermal design of the IC

Characteristics of an IC have a great deal to do with the temperature at which it is used, and exceeding absolute maximum ratings may degrade and destroy elements. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.



Figure 24. Temperature Derating Curve

(Note) Values are actual measurements and are not guaranteed.

Power dissipation values vary according to the board on which the IC is mounted.

I/O Equivalent Circuits

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
1 2 3 4 5 6	A1 A2 B1 B2 C1 C2	4.25		A terminal for signal input. The input impedance is 100kΩ(typ).
7 8 9 10 11 12 13	DP1 DN DP2 EP1 EN1 EN2 EP2	4.25		Input terminal available to Single/Differential mode. The input impedance is 250kΩ(Typ).
15 18	LDA1 LDA2	4.25	VCC GND GND GND GND GND GND GND GND GND GND	The loudness characteristic setting terminal.
16 17	LDB1 LDB2	4.25		The loudness characteristic setting terminal.
19	MUTE	-	VCC 0.58×V _{CC} 40 5250kΩ 1.65V GND	A terminal for external compulsory mute. If terminal voltage is High level, the mute is OFF. And if the terminal voltage is Low level, the mute is on.

Values in the pin explanation and input/output equivalent circuit are reference values only and are not guaranteed.

I/O Equivalent Circuits – continued

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
	Hamo	Voltago	VCC	A terminal for fader and Subwoofer output.
22 23 24 25 26 27	OUTS2 OUTS1 OUTR2 OUTR1 OUTF2 OUTF1	4.25		
28	VCC	8.5		Power supply terminal.
29	SCL	-	VCC	A terminal for clock input of I ² C BUS communication.
30	SDA	-	VCC GND GND GND GND GND GND GND GND GND GND	A terminal for data input of I ² C BUS communication.
31	GND	0		Ground terminal.
32	FIL	4.25		1/2 VCC terminal. Voltage for reference bias of analog signal system. The simple precharge circuit and simple discharge circuit for an external capacitor are built in.
14	MIN	4.25		A terminal for signal input. The input impedance is 27kΩ (Typ).
21	TEST	-		TEST terminal

Values in the pin explanation and input/output equivalent circuit are reference values only and are not guaranteed

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode. When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Figure 25. Example of monolithic IC structure

13. About Signal Input

(a) About Input Coupling Capacitor Constant Value

The constant value of input coupling capacitor C(F) is decided with respect to the input impedance $R_{IN}(\Omega)$ at the input signal terminal of the IC. The first HPF characteristic of RC is composed.



(b) About the Input Selector SHORT

SHORT mode is the command which makes switch $S_{SH} = ON$ of input selector part so that the input impedance R_{IN} of all terminals becomes small. Switch S_{SH} is OFF when SHORT command is not selected. The constant time brought about by the small resistance inside and the capacitor outside the LSI becomes small when this command is used. The charge time of the capacitor becomes short. Since SHORT mode turns ON the switch of S_{SH} and makes it low impedance, please use it at no signal condition.

Operational Notes – continued

14. About Mute Terminal (Pin 19) when Power Supply is OFF

There should be no applied voltage across the Mute terminal (Pin 19) when power-supply is OFF. If in case voltage is supplied to mute terminal, please insert a series resistor (about $2.2k\Omega$) to Mute terminal. (Please refer to Application Circuit Diagram.)

15. About TEST Pin

TEST Pin should be left as OPEN. Pin 21 is TEST Pin.

16. About MIX

(1) <u>About Specification of Fader -∞ at MIX ON.</u>

Mix_signal is added to Main_signal after Fader_Gain(+15dB to -79dB) like the figure. When Fader is set at -∞, the signal after a MIX signal is added is done with MUTE because the -∞ circuit of Fader is in the step after the addition circuit



Figure 26. About Front Fader and MIX

(2) About Advanced Switching of MIX Gain/ATT

When advanced switching of MIX_Gain/ATT works, MIX goes a switching movement that it passes through the state of MIX_OFF like in B figure below (from current settingof MIX_Gain/ATT to MIX_OFF to a target setting of MIX_Gain/ATT).





MIX_Gain/ATT 0dB to -6dB advanced switching

Figure 27. Advanced Switching Movement when MIX_Gain/ATT is Changed

Operational Notes – continued

17. About the External Parts Setting of Loudness Circuit

This IC is equipped with a Loudness circuit.

The Loudness gain is fixed inside the IC but its frequency characteristic can be changed freely by adjusting the external part filter. The circuit composition of the Loudness part is shown below. Incidentally, when not using the Loudness circuit, please short the pins between LDA1(Pin 15) and LDB1(Pin 16), and between LDA2(Pin 18) and LDB2(Pin 17), so as to avoid the inner amplifier inputs to become floating.



Figure 28. About the External Parts Setting of Loudness Circuit

The Loudness frequency characteristics are decided according to Figure 28. G_LOUD can be made 20dB when external parts used are the same with Figure 28 (the recommended value). G_LOUD is the amount of effect of Loudness when Loudness Gain is set at 20dB (P.20).

When Loudness frequency characteristics are changed, each parameter (Gain, Frequency) shown in Figure 28 can be decided using the following approximate equation below.

(Note) Design fc2 value more than one digit bigger than fc1 to get effect on Loudness.

Loudness cut-off frequency

$$fc1 = \frac{1}{2\pi C_2(R_1 + R_3)} \quad [Hz]$$
$$fc2 = \frac{1}{2\pi C_1(R_2 + R_3)} \quad [Hz]$$

Loudness Gain (The amount of effect of Loudness)

$$\begin{split} \mathbf{G}_{_\text{LOUD}} &= 20\log\left(\frac{R_3}{R_1 + R_3}\right) \quad \left[\mathsf{dB} \right] \\ \mathbf{G}_{_\text{HICUT}} &= 20\log\left(\frac{R_3}{R_1 / / R_2 + R_3}\right) \quad \left[\mathsf{dB} \right] \end{split}$$

Ordering Information



Marking Diagram





Revision History

Date	Revision	Changes
16.Dec.2015	001	New Release

Notice

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1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

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 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
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Precaution for Mounting / Circuit board design

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For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

- 1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
- 2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of lonizer, friction prevention and temperature / humidity control).

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- 1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
- 2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Тел: +7 (812) 336 43 04 (многоканальный) Email: org@lifeelectronics.ru

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