November 1998

# FDG6321C
# Dual N & P Channel Digital FET

## General Description

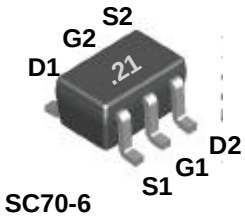
These dual N & P-Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETS. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.

## Features

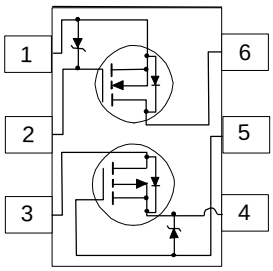
- N-Ch 0.50 A, 25 V, $R_{DS(ON)}$ = 0.45 Ω @ $V_{GS}$= 4.5V.
  $R_{DS(ON)}$ = 0.60 Ω @ $V_{GS}$= 2.7 V.
- P-Ch -0.41 A, -25 V,$R_{DS(ON)}$ = 1.1 Ω @ $V_{GS}$= -4.5V.
  $R_{DS(ON)}$ = 1.5 Ω @ $V_{GS}$= -2.7V.
- Very small package outline SC70-6.
- Very low level gate drive requirements allowing direct operation in 3 V circuits($V_{GS(th)}$ < 1.5 V).
- Gate-Source Zener for ESD ruggedness (>6kV Human Body Model).



SC70-6 | SOT-23 | SuperSOT™-6 | SOT-8 | SO-8 | SOIC-14




SC70-6




## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | N-Channel | P-Channel | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | 25 | -25 | V |
| $V_{GSS}$ | Gate-Source Voltage | 8 | -8 | V |
| $I_D$ | Drain Current - Continuous | 0.5 | -0.41 | A |
| | - Pulsed | 1.5 | -1.2 | |
| $P_D$ | Maximum Power Dissipation (Note 1) | 0.3 | | W |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Ranger | -55 to 150 | | °C |
| ESD | Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm) | 6 | | kV |
| **THERMAL CHARACTERISTICS** | | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1) | 415 | | °C/W |

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## Electrical Characteristics ($T_A$ = 25 °C unless otherwise noted )

| Symbol | Parameter | Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | N-Ch | 25 | | | V |
| | | $V_{GS}$ = 0 V, $I_D$ = -250 µA | P-Ch | -25 | | | |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | $I_D$ = 250 µA, Referenced to 25 °C | N-Ch | | 26 | | mV/°C |
| | | $I_D$ = -250 µA, Referenced to 25 °C | P-Ch | | -22 | | |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | N-Ch | | | 1 | µA |
| | | $T_J$ = 55°C | | | | 10 | |
| $I_{GSS}$ | Gate - Body Leakage Current | $V_{DS}$ = -20 V, $V_{GS}$ = 0 V | P-Ch | | | -1 | µA |
| | | $T_J$ = 55°C | | | | -10 | |
| $I_{GSS}$ | Gate - Body Leakage Current | $V_{GS}$ = 8 V, $V_{DS}$ = 0 V | N-Ch | | | 100 | nA |
| | | $V_{GS}$ = -8 V, $V_{DS}$ = 0 V | P-Ch | | | -100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | N-Ch | 0.65 | 0.8 | 1.5 | V |
| | | $V_{DS}$ = $V_{GS}$, $I_D$ = -250 µA | P-Ch | -0.65 | -0.82 | -1.5 | |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Temp. Coefficient | $I_D$ = 250 µA, Referenced to 25 °C | N-Ch | | -2.6 | | mV/ °C |
| | | $I_D$ = -250 µA, Referenced to 25 °C | P-Ch | | 2.1 | | |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 4.5 V, $I_D$ = 0.5 A | N-Ch | | 0.34 | 0.45 | Ω |
| | | $T_J$ =125°C | | | 0.55 | 0.72 | |
| | | $V_{GS}$ = 2.7 V, $I_D$ = 0.2 A | | | 0.44 | 0.6 | |
| | | $V_{GS}$ = -4.5 V, $I_D$ = -0.41 A | P-Ch | | 0.85 | 1.1 | |
| | | $T_J$ =125°C | | | 1.2 | 1.8 | |
| | | $V_{GS}$ = -2.7 V, $I_D$ = -0.25 A | | | 1.15 | 1.5 | |
| $I_{D(ON)}$ | On-State Drain Current | $V_{GS}$ = 4.5 V, $V_{DS}$ = 5 V | N-Ch | 0.5 | | | A |
| | | $V_{GS}$ = -4.5 V, $V_{DS}$ = -5 V | P-Ch | -0.41 | | | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 0.5 A | N-Ch | | 1.45 | | S |
| | | $V_{DS}$ = -5 V, $I_D$ = -0.41 A | P-Ch | | 0.9 | | |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $C_{iss}$ | Input Capacitance | N-Channel | N-Ch | | 50 | | pF |
| | | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, | P-Ch | | 62 | | |
| $C_{oss}$ | Output Capacitance | f = 1.0 MHz | N-Ch | | 28 | | |
| | | P-Channel | P-Ch | | 34 | | |
| $C_{rss}$ | Reverse Transfer Capacitance | $V_{DS}$ = -10 V, $V_{GS}$ = 0V, | N-Ch | | 9 | | |
| | | f = 1.0 MHz | P-Ch | | 10 | | |

## Electrical Characteristics (continued)

**SWITCHING CHARACTERISTICS** (Note 2)

| Symbol | Parameter | Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{D(on)}$ | Turn - On Delay Time | N-Channel | N-Ch | | 3 | 6 | nS |
| | | $V_{DD}$ = 5 V, $I_D$ = 0.5 A, | P-Ch | | 7 | 15 | |
| $t_r$ | Turn - On Rise Time | $V_{GS}$ = 4.5 V, $R_{GEN}$ = 50 Ω | N-Ch | | 8.5 | 18 | nS |
| | | | P-Ch | | 8 | 16 | |
| $t_{D(off)}$ | Turn - Off Delay Time | P-Channel | N-Ch | | 17 | 30 | nS |
| | | $V_{DD}$ = -5 V, $I_D$ = -0.5 A, | P-Ch | | 55 | 80 | |
| $t_f$ | Turn - Off Fall Time | $V_{GS}$ = -4.5 V, $R_{GEN}$ = 50 Ω | N-Ch | | 13 | 25 | nS |
| | | | P-Ch | | 35 | 60 | |
| $Q_g$ | Total Gate Charge | N-Channel | N-Ch | | 1.64 | 2.3 | nC |
| | | $V_{DS}$ = 5 V, $I_D$ = 0.5 A, | P-Ch | | 1.1 | 1.5 | |
| $Q_{gs}$ | Gate-Source Charge | $V_{GS}$ = 4.5 V | N-Ch | | 0.38 | | nC |
| | | P- Channel | P-Ch | | 0.31 | | |
| $Q_{gd}$ | Gate-Drain Charge | $V_{DS}$ = -5 V, $I_D$ = -0.41 A, | N-Ch | | 0.45 | | nC |
| | | $V_{GS}$ = -4.5 V | P-Ch | | 0.29 | | |
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | N-Ch | | | 0.25 | A |
| | | | P-Ch | | | -0.25 | |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 0.5 A (Note 2) | N-Ch | | 0.8 | 1.2 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = -0.5 A (Note 2) | P-Ch | | -0.85 | -1.2 | |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ = 415°C/W on minimum mounting pad on FR-4 board in still air.
2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics: N-Channel

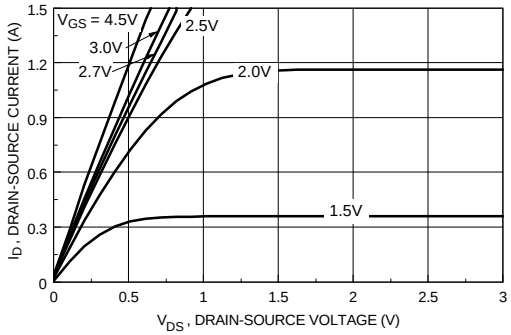



**Figure 1. On-Region Characteristics.**

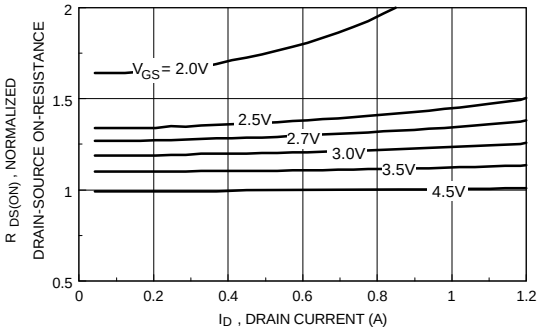



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

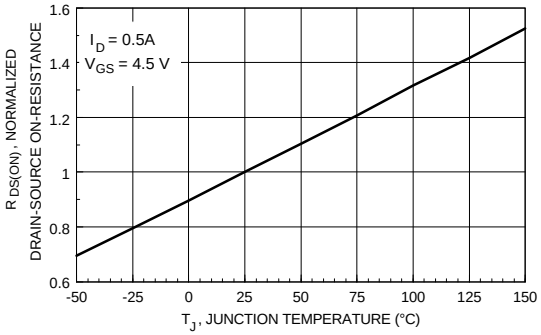



**Figure 3. On-Resistance Variation with Temperature.**

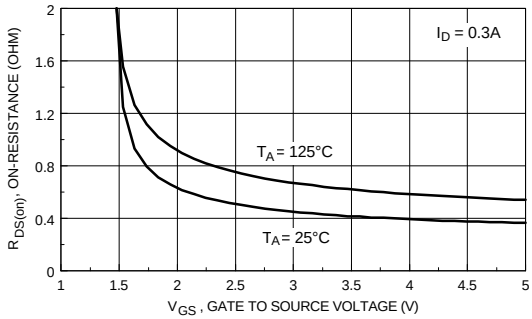



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

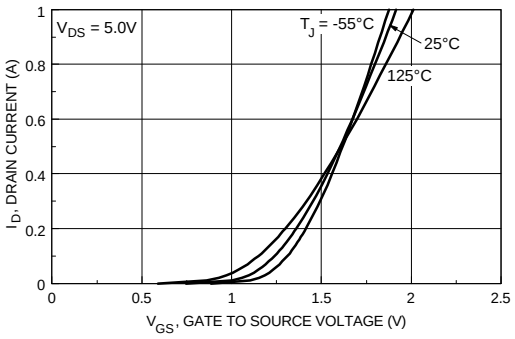



**Figure 5. Transfer Characteristics.**

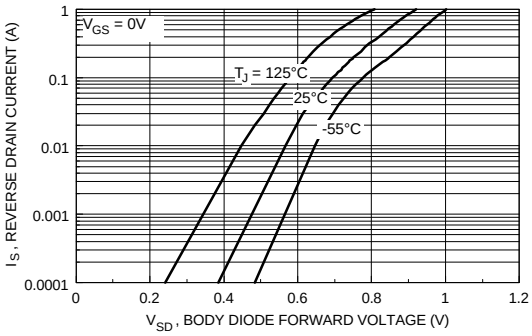



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Electrical Characteristics: N-Channel (continued)

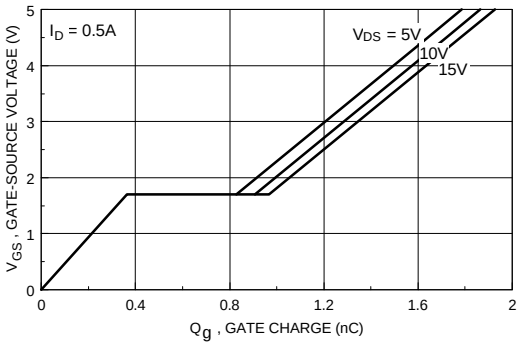



**Figure 7. Gate Charge Characteristics.**

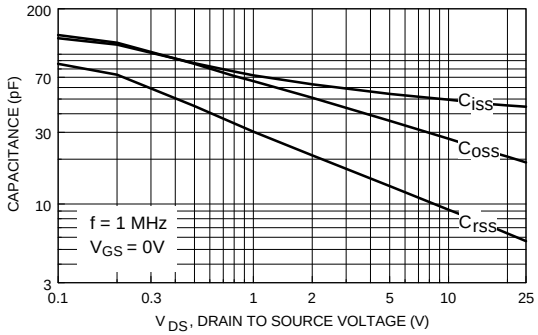



**Figure 8. Capacitance Characteristics.**

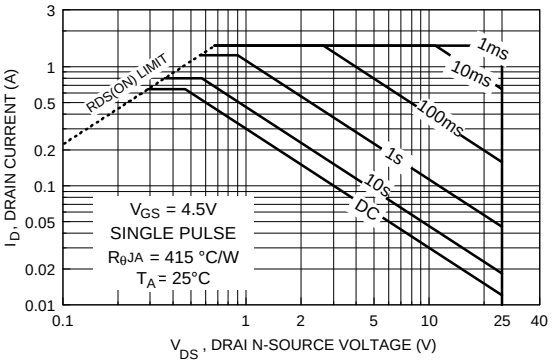



**Figure 9. Maximum Safe Operating Area.**

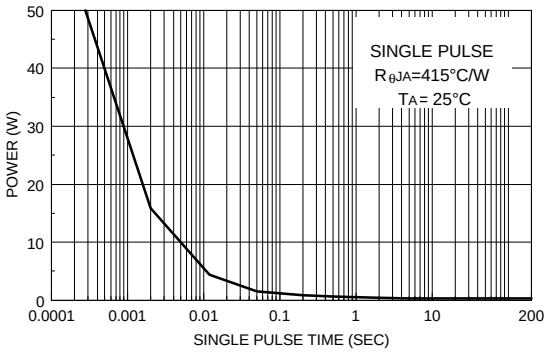



**Figure 10. Single Pulse Maximum Power Dissipation.**

## Typical Electrical Characteristics: P-Channel

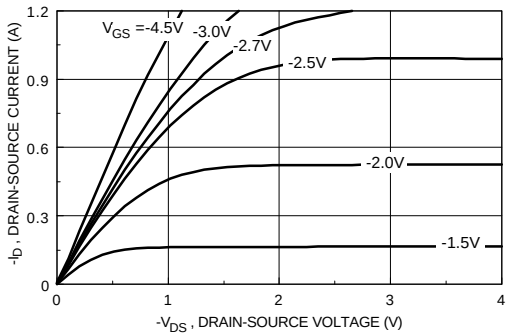



**Figure 11. On-Region Characteristics.**

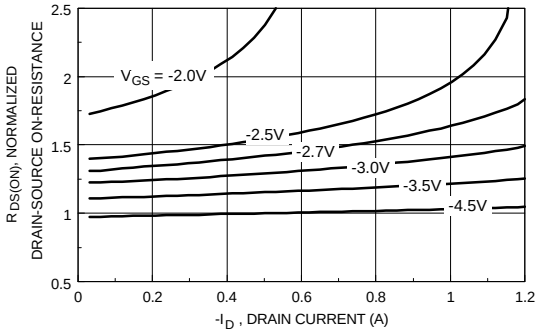



**Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.**

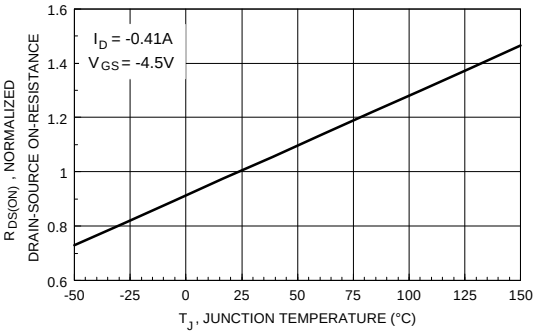



**Figure 13. On-Resistance Variation with Temperature.**

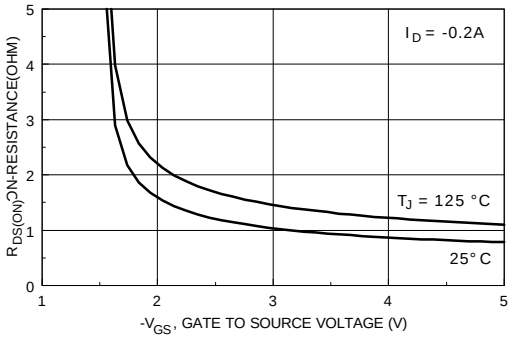



**Figure 14. On-Resistance Variation with Gate-to-Source Voltage.**

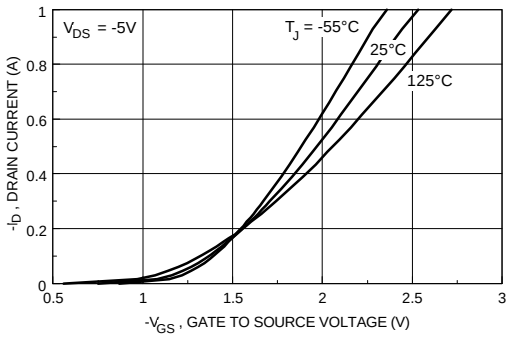



**Figure 15. Transfer Characteristics.**

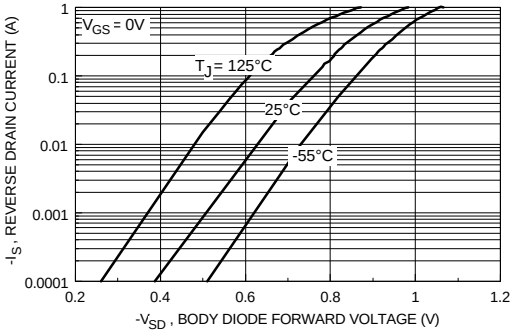



**Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Electrical Characteristics: P-Channel (continued)

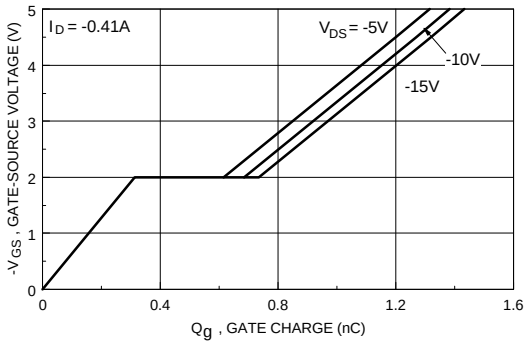



**Figure 17. Gate Charge Characteristics.**

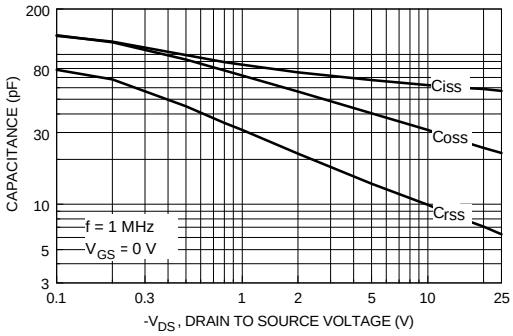



**Figure 18. Capacitance Characteristics.**

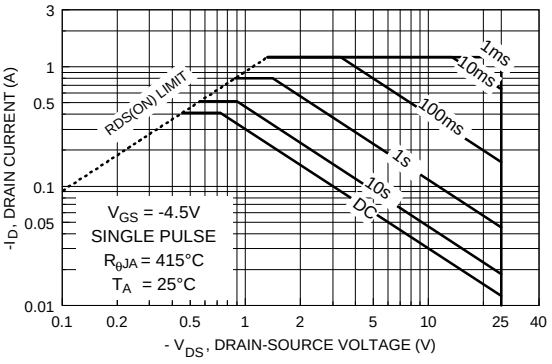



**Figure 19. Maximum Safe Operating Area.**

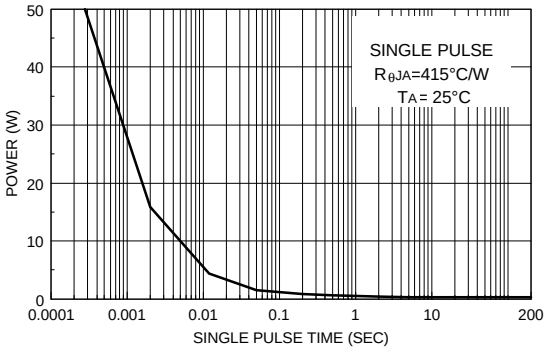



**Figure 20. Single Pulse Maximum Power Dissipation.**

## Typical Thermal Characteristics: N & P-Channel (continued)

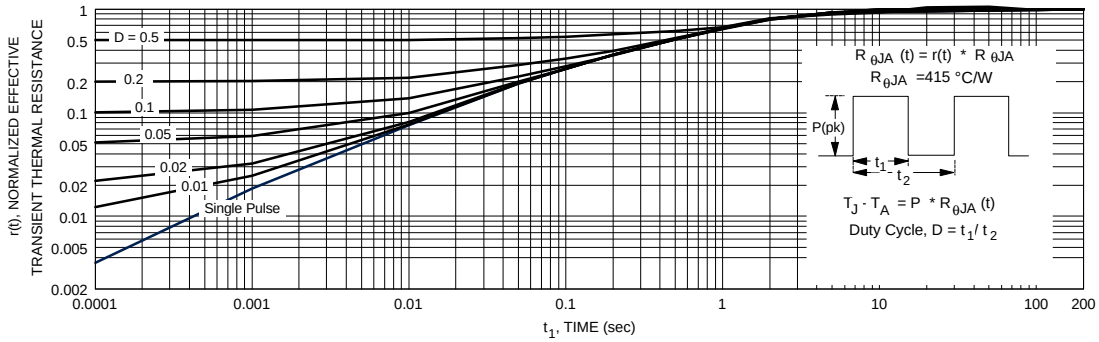



**Figure 21. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in note 1.
Transient thermalresponse will change depending on the circuit board design.

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