Description

The 9DMV0141B is a 1.8V member of IDT's full-featured PCIe family. The 9DMV0141B has integrated output terminations for direct connection to 100Ω transmission lines. The output has an OE# pin for optimal system control and power management. The parts provide asynchronous or glitch-free switching modes.

PCIe Clocking Architectures Supported

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Typical Applications

- Servers
- nVME drives
- Embedded systems/Industrial control
- High-performance computing
- Accelerators

Key Specifications

- Additive cycle-to-cycle jitter < 5ps
- Additive PCIe Gen4 phase jitter < 50fs rms
- 156.25MHz additive phase jitter 130fs rms typical (12kHz to 20MHz)

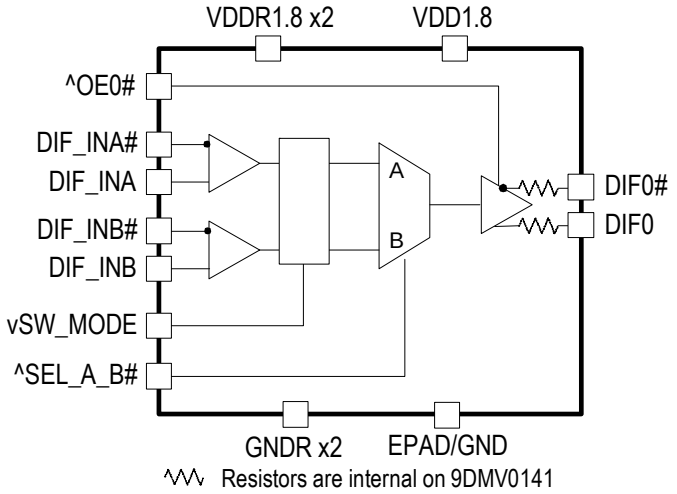
Features

- Direct connection to loads saves 4 resistors compared to standard PCIe devices
- 1.8V operation; 12mW typical power consumption
- Selectable asynchronous or glitch-free switching; allows the mux to be selected at power up even if both inputs are not running, then transition to glitch-free switching mode
- OE# pin for flexible power sequencing
- HCSL differential inputs
- Spread spectrum tolerant; allows reduction of EMI
- 1MHz to 200MHz operating frequency
- Configuration accomplished with strapping pins, no SMBus needed
- Space-saving 3 × 3 mm 16-VFQFPN; minimal board space

Output Features

- 1 Low-Power HCSL (LP-HCSL) DIF pair

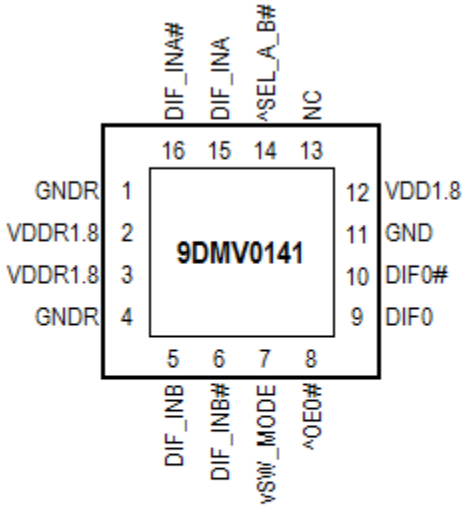
Block Diagram



Contents

Pin Assignments

Figure 1. Pin Assignments for 3 × 3 mm 16-VFQFPN Package – Top View



16-VFQFPN, 3 x 3 mm, 0.5mm pitch

^ prefix indicates internal 120kOhm pull-up resistor

v prefix indicates internal 120kOhm pull-down resistor

Note: Paddle may be connected to ground for thermal purposes. It is not required electrically.

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	GNDR	GND	Analog ground pin for the differential input (receiver).
2	VDDR1.8	Power	Power supply for differential input clock (receiver). This V_{DD} should be treated as an analog power rail and filtered appropriately. Nominally 1.8V.
3	VDDR1.8	Power	Power supply for differential input clock (receiver). This V_{DD} should be treated as an analog power rail and filtered appropriately. Nominally 1.8V.
4	GNDR	GND	Analog ground pin for the differential input (receiver).
5	DIF_INB	Input	True input of differential clock.
6	DIF_INB#	Input	Complement input of differential clock.
7	vSW_MODE	Input	Switch Mode. This pin selects either asynchronous or glitch-free switching of the mux. Use asynchronous mode if 0 or 1 of the input clocks is running. Use glitch-free mode if both input clocks are running. This pin has an internal pull down resistor of ~s. 0 = asynchronous mode, 1 = glitch-free mode.
8	^OE0#	Input	Active low input for enabling output 0. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output.
9	DIF0	Output	Differential true clock output.
10	DIF0#	Output	Differential complementary clock output.
11	GND	GND	Ground pin.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
12	VDD1.8	Power	Power supply, nominally 1.8V.
13	NC	—	No connection.
14	^SEL_A_B#	Input	Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor. 0 = Input B selected, 1 = Input A selected.
15	DIF_INA	Input	True input of differential clock.
16	DIF_INA#	Input	Complement input of differential clock.

Table 2. Power Management

OEx# Pin	DIF_IN	DIFx	
		True O/P	Complementary O/P
0	Running	Running	Running
1	Running	Low	Low

Table 3. Power Connections

Pin Number		Description
V_{DD}	GND	
2	1	Input A receiver analog.
3	4	Input B receiver analog.
12	11	DIF outputs,

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9DMV0141B at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units	Notes
V_{DDxx}	Supply Voltage	Applies to all V_{DD} pins.	-0.5		2.5	V	1,2
V_{IN}	Input Voltage		-0.5		V_{DD} + 0.5V	V	1,3
Ts	Storage Temperature		-65		150	°C	1
Tj	Junction Temperature				125	°C	1
ESD prot	Input ESD protection	Human Body Model.	2000			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 2.5V.

Thermal Characteristics

Table 5. Thermal Characteristics

Symbol	Parameter	Conditions	Package	Value	Units	Notes
θ_{JC}	Thermal Resistance	Junction to case.	NLG16	66	°C/W	1
θ_{JB}		Junction to board.		5	°C/W	1
θ_{JA0}		Junction to air, still air.		63	°C/W	1
θ_{JA1}		Junction to air, 1m/s air flow.		56	°C/W	1
θ_{JA2}		Junction to air, 3m/s air flow.		51	°C/W	1
θ_{JA3}		Junction to air, 5m/s air flow.		49	°C/W	1

[1] EPAD soldered to board.

Electrical Characteristics

$T_A = T_{AMB}$, supply voltages per normal operating conditions. See Test Loads for loading conditions.

Table 6. Electrical Characteristics–Input/Supply/Common Parameters – Normal Operating Condition

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units	Notes
V_{DDxx}	Supply Voltage	Applies to all V_{DD} pins.	1.7	1.8	1.9	V	
T_{AMB}	Ambient Operating Temperature	Industrial range.	-40	25	85	°C	1
V_{IH}	Input High Voltage	Single-ended inputs, except SMBus.	0.75 V_{DD}		V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	Single-ended inputs, except SMBus.	-0.3		0.25 V_{DD}	V	
I_{IN}	Input Current	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DD}.	-5		5	µA	
I_{INP}		Single-ended inputs. V_{IN} = 0 V; Inputs with internal pull-up resistors. V_{IN} = V_{DD}; Inputs with internal pull-down resistors.	-100		100	µA	
F_{ibyp}	Input Frequency		1		200	MHz	2
L_{pin}	Pin Inductance				7	nH	1
C_{IN}	Capacitance	Logic Inputs, except DIF_IN.	1.5		5	pF	1
C_{INDIF_IN}		DIF_IN differential clock inputs.	1.5		2.7	pF	1,4
C_{OUT}		Output pin capacitance.			6	pF	1
T_{STAB}	Clk Stabilization	From V_{DD} power-up and after input clock stabilization or de-assertion of PD# to 1st clock.			1	ms	1,2
$f_{MODINPCIe}$	Input SS Modulation Frequency PCIe	Allowable frequency for PCIe applications (triangular modulation).	30		33	kHz	
f_{MODIN}	Input SS Modulation Frequency non-PCIe	Allowable frequency for non-PCIe applications (triangular modulation).	0		66	kHz	
$t_{LATOE\#}$	OE# Latency	DIF start after OE# assertion. DIF stop after OE# deassertion.	1	2	3	clocks	1,3
t_F	Tfall	Fall time of single-ended control inputs.			5	ns	1,2
t_R	Trise	Rise time of single-ended control inputs.			5	ns	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

Table 7. Clock Input Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units	Notes
V_{CROSS}	Input Crossover Voltage – DIF_IN	Crossover voltage (common mode voltage).	200		725		
V_{SWING}	Input Swing–DIF_IN	Differential value.	300			mV	1
dv/dt	Input Slew Rate–DIF_IN	Measured differentially.	0.6			V/ns	1,2
I_{IN}	Input Leakage Current	V_{IN} = 0.8V , V_{IN} = GND.	-5		5	µA	
d_{tin}	Input Duty Cycle	Measurement from differential waveform.	45		55	%	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

Table 8. DIF Low-Power HCSL Outputs

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units	Notes
T_{RF}	Slew Rate	Scope averaging on, 9DMV0141B	2	2.9	4.0	V/ns	1,2,3
ΔT_{RF}	Slew Rate Matching	Slew rate matching, scope averaging on.		3	20	%	1,4
V_{HIGH}	Voltage High	Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on).	660	783	850	mV	
V_{LOW}	Voltage Low		-150	26	150		
V_{MAX}	Max Voltage	Measurement on single ended signal using absolute value (scope averaging off).		790	1150	mV	
V_{MIN}	Min Voltage		-300	9			
V_{CROSS_ABS}	Crossing Voltage (abs)	Scope averaging off.	250	393	550	mV	1,5
Δ-V_{CROSS}	Crossing Voltage (var)	Scope averaging off.		12	140	mV	1,6

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the V_{SWING} voltage range centered around differential 0V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] V_{CROSS} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all V_{CROSS} measurements in any particular system. Note that this is a subset of $V_{CROSS–MIN/MAX}$ (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting Δ-V_{CROSS} to be smaller than V_{CROSS} absolute.

Table 9. Current Consumption

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units	Notes
I_{DDOP}	Operating Supply Current	V_{DD} rails, all outputs active at 100MHz.		7.9	12	mA	
I_{DDDIS}	Disable Current	V_{DD} rails, all outputs disabled Low/Low.		1.5	2.5	mA	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Input clock stopped after outputs have parked Low/Low.

Table 10. Output Duty Cycle, Jitter, Skew and PLL Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units	Notes
t_{DCD}	Duty Cycle Distortion	Measured differentially, at 100MHz.	-0.5	-0.12	0.5	%	1,3
t_{pdBYP}	Skew, Input to Output	V_T = 50%.	1800	2409	3000	ps	1
$t_{jcyc-cyc}$	Jitter, Cycle to Cycle	*Additive* Jitter.			5	ps	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock.

Table 11. Filtered Additive Phase Jitter Parameters–PCIe Common Clocked (CC) Architectures

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions. See Test Loads for loading conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limits	Units	Notes
Additive Phase Jitter	$t_{jphPCIeG1-CC}$	PCIe Gen1.		0.69	5	N/A	ps (p-p)	1,2,3,4
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.01	0.01		ps (rms)	1,2,4,6
		PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.16	0.19		ps (rms)	1,2,4,6
	$t_{jphPCIeG3/4-CC}$	PCIe Gen3, Gen4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.07	0.08		ps (rms)	1,2,4,6

Table 12. Filtered Phase Jitter Parameters – PCIe Independent Reference (IR) Architectures

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions. See Test Loads for loading conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limits	Units	Notes
Additive Phase Jitter	$t_{jphPCIeG2-SRIS}$	PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz).		0.15	0.19	N/A	ps (rms)	1,2,4,6
	$t_{jphPCIeG3-SRIS}$	PCIe Gen3 (PLL BW of 2–4MHz, CDR = 10MHz).		0.04	0.05		ps (rms)	1,2,4,6

Notes for PCIe Filtered Phase Jitter tables:

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Calculated from Clock Jitter Tool, when driven by SMA100B.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] Additive jitter for RMS values is calculated by solving for b, where [$b = sqrt(c^2 - a^2)$], "a" is rms input jitter and "c" is rms total jitter.

[5] IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures. According to the PCIe Base Specification Rev4.0 version 1.0, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. The IR filters from the PCIe Base Specification, Rev 3.1a are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 or Gen4 data rates at the time of publication.

[6] Measured using SMA100B signal source, or equivalent, and a phase noise analyzer.

Table 13. Unfiltered Phase Jitter Parameters–12kHz to 20MHz

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions. See Test Loads for loading conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Additive Phase Jitter	$t_{jph12k-20Madd}$	156.25MHz.		130		N/A	fs (rms)	1,2,3

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Calculated after applying 12k-20M brickwall filter, when driven by SMA100B source.

[3] Additive jitter for RMS values is calculated by solving for b, where [$b = sqrt(c^2 - a^2)$], "a" is rms input jitter and "c" is rms total jitter.

Test Loads

Figure 2. Low-Power HCSL Output Test Load (standard PCIe source-terminated test load with high impedance receiver)

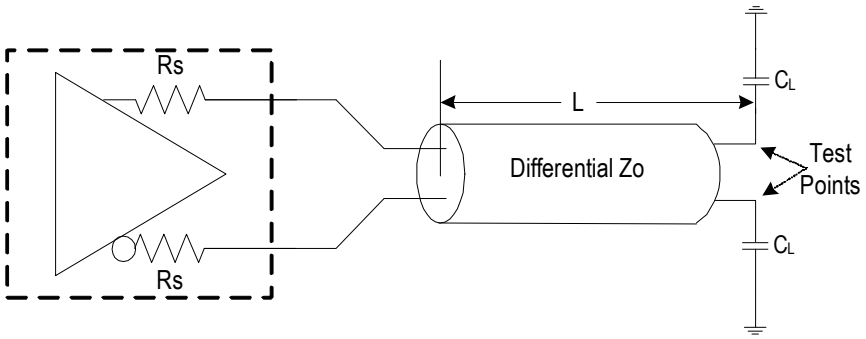


Table 14. Parameters for Low-Power HCSL Output Test Load

Device	Rs (Ω)	Zo (Ω)	L (inches)	C_L (pF)
9DMV0141	Internal	100	5	2

Alternate Terminations

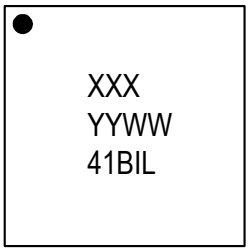
The LP-HCSL output can easily drive other logic families. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for termination schemes for LVPECL, LVDS, CML, and SSTL.

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/16-vfqfpn-package-outline-drawing-30-x-30-x-09-mm-05-mm-170-x-170-mm-epad-nlnlg16p2

Marking Diagram



- Line 1: "XXX" is the Asm lot number.
- Line 2 indicates the following:
  - "YY" is the last two digits of the year; "WW" is the work week number when the part was assembled.
- Line 3: truncated part number.

Ordering Information

Orderable Part Number	Description	Package	Carrier Type	Temperature
9DMV0141BKILF	Differential Z_{OUT} = 100Ω	3 × 3 × 0.9 mm, 16-VFQFPN	Tray	-40° to +85°C
9DMV0141BKILFT	Differential Z_{OUT} = 100Ω	3 × 3 × 0.9 mm, 16-VFQFPN	Tape and Reel	-40° to +85°C

Revision History

Revision Date	Description of Change
February 25, 2019	Initial release.

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