

### 3.3V Low Skew 1-to-4 LVTTL/LVCMOS to LVPECL Fanout Buffer

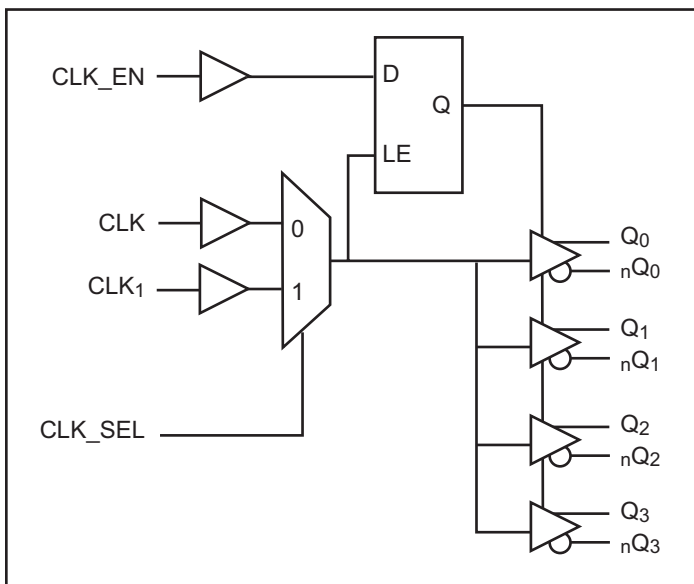
#### Features

- Maximum operation frequency: 500 MHz
- 4 pair of differential LVPECL outputs
- Selectable CLK<sub>0</sub> and CLK<sub>1</sub> inputs
- CLK<sub>0</sub>, CLK<sub>1</sub> accept LVCMOS, LVTTL input level
- Output Skew: 80ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 1.9ns (maximum)
- 3.3V power supply
- Additive jitter of 36.7fs (typical)
- Operating Temperature: -40°C to 85°C
- Packaging (Pb-free & Green available):  
— 20-pin TSSOP (L)

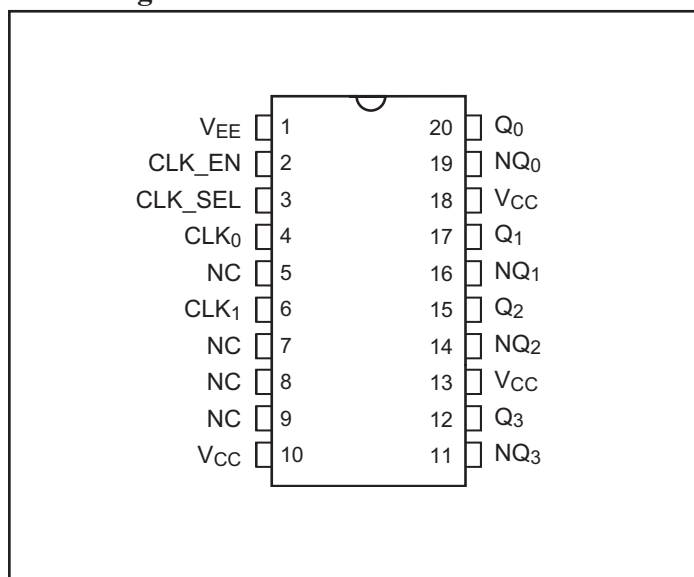
#### Description

The PI6C48535-01 is a high-performance low-skew LVPECL fanout buffer. PI6C48535-01 features two selectable single-ended clock inputs and translates to four LVPECL outputs. The CLK<sub>0</sub> and CLK<sub>1</sub> inputs accept LVCMOS or LVTTL signals. The outputs are synchronized with input clock during asynchronous assertion/deassertion of CLK\_EN pin. PI6C48535-01 is ideal for single-ended LVTTL/LVCMOS to LVPECL translations. Typical clock translation and distribution applications are data-communications and telecommunications.

#### Block Diagram



#### Pin Configuration



### Pin Description

| Name                | Pin #      | Type | Description  |
|---------------------|------------|------|--|
| V <sub>EE</sub>     | 1          | P    | Connect to Negative power supply   |
| CLK_EN              | 2          | I_PU | Synchronizing clock enable. When high, clock outputs follow clock input. When low, Qx outputs are forced low, nQx outputs are forced high. LVCMOS/LVTTL level with 50KΩ pull up. |
| CLK_SEL             | 3          | I_PD | Clock select input. When high, selects CLK <sub>1</sub> input. When low, selects CLK <sub>0</sub> input. LVCMOS/LVTTL level with 50KΩ pull down.                                 |
| CLK <sub>0</sub>    | 4          | I_PD | LVCMOS / LVTTL clock input   |
| CLK <sub>1</sub>    | 6          | I_PD | LVCMOS / LVTTL clock input   |
| NC                  | 5, 7, 8, 9 |      | No internal connection.  |
| V <sub>CC</sub>     | 10, 13, 18 | P    | Connect to 3.3V.   |
| Q <sub>3, nQ3</sub> | 11, 12     | O    | Differential output pair, LVPECL interface level.  |
| Q <sub>2, nQ2</sub> | 14, 15     | O    | Differential output pair, LVPECL interface level.  |
| Q <sub>1, nQ1</sub> | 16, 17     | O    | Differential output pair, LVPECL interface level.  |
| Q <sub>0, nQ0</sub> | 19, 20     | O    | Differential output pair, LVPECL interface level.  |

#### Notes:

1. I = Input, O = Output, P = Power supply connection, I\_PD = Input with pull down, I\_PU = Input with pull up.

### Pin Characteristics

| Symbol                | Parameter                 | Conditions | Min. | Typ. | Max. | Units |
|-----------------------|---------------------------|------------|------|------|------|-------|
| C <sub>IN</sub>       | Input Capacitance         |            |      |      | 4    | pF    |
| R <sub>pullup</sub>   | Input Pullup Resistance   |            |      | 50   |      | KΩ    |
| R <sub>pulldown</sub> | Input Pulldown Resistance |            |      | 50   |      |       |

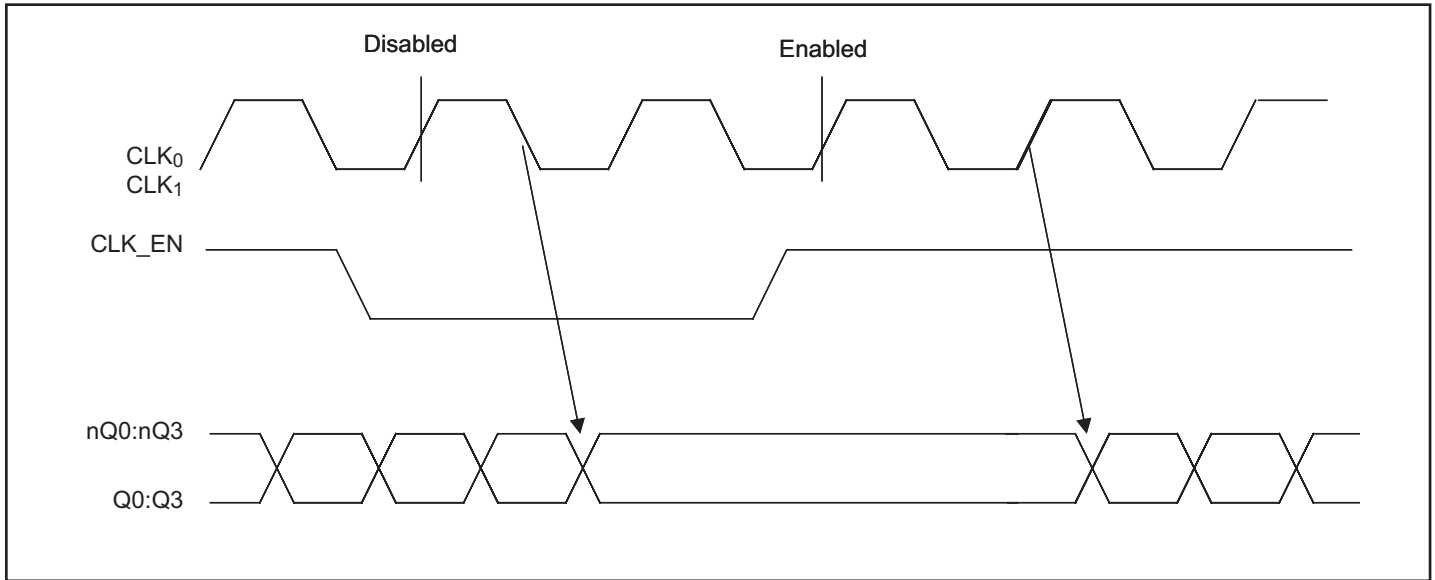
### Control Input Function Table

| Inputs |         |                  | Outputs                        |                                  |
|--------|---------|------------------|--------------------------------|----------------------------------|
| CLK_EN | CLK_SEL | Selected Source  | Q <sub>0</sub> :Q <sub>3</sub> | nQ <sub>0</sub> :nQ <sub>3</sub> |
| 0      | 0       | CLK <sub>0</sub> | Disabled: Low                  | Disabled: High                   |
| 0      | 1       | CLK <sub>1</sub> | Disabled: Low                  | Disabled: High                   |
| 1      | 0       | CLK <sub>0</sub> | Enabled                        | Enabled                          |
| 1      | 1       | CLK <sub>1</sub> | Enabled                        | Enabled                          |

#### Notes:

1. After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show below.

**Figure 1. CLK\_EN Timing Diagram**



**Clock Input Function Table**

| Inputs                               | Outputs                        |                                  |
|--------------------------------------|--------------------------------|----------------------------------|
| CLK <sub>0</sub> or CLK <sub>1</sub> | Q <sub>0</sub> :Q <sub>3</sub> | nQ <sub>0</sub> :nQ <sub>3</sub> |
| 0                                    | LOW                            | HIGH                             |
| 1                                    | HIGH                           | LOW                              |

**Absolute Maximum Ratings**

| Symbol           | Parameter           | Conditions        | Min. | Typ. | Max.                  | Units |
|------------------|---------------------|-------------------|------|------|-----------------------|-------|
| V <sub>CC</sub>  | Supply voltage      | Referenced to GND |      |      | 4.6                   | V     |
| V <sub>IN</sub>  | Input voltage       | Referenced to GND | -0.5 |      | V <sub>CC</sub> +0.5V |       |
| V <sub>OUT</sub> | Output voltage      | Referenced to GND | -0.5 |      | V <sub>CC</sub> +0.5V |       |
| T <sub>STG</sub> | Storage temperature |                   | -65  |      | 150                   | °C    |

**Notes:**

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**Operating Conditions**

| Symbol          | Parameter            | Conditions | Min. | Typ. | Max. | Units |
|-----------------|----------------------|------------|------|------|------|-------|
| V <sub>CC</sub> | Power Supply Voltage |            | 3.0  | 3.3  | 3.6  | V     |
| T <sub>A</sub>  | Ambient Temperature  |            | -40  |      | 85   | °C    |
| I <sub>EE</sub> | Power Supply Current | 500 MHz    |      |      | 60   | mA    |

**LVCMOS/LVTTL DC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 3.0\text{V}$  to  $3.6\text{V}$  unless otherwise stated below.)

| Symbol   | Parameter          |   | Conditions                                    | Min. | Typ. | Max.         | Units |
|----------|--------------------|---|---|------|------|--------------|-------|
| $V_{IH}$ | Input High Voltage | CLK <sub>0</sub> , CLK <sub>1</sub> , CLK_EN, CLK_SEL |   | 2    |      | $V_{CC}+0.3$ | V     |
| $V_{IL}$ | Input Low Voltage  | CLK <sub>0</sub> , CLK <sub>1</sub>                   |   | -0.3 |      | 1.3          | V     |
|          |                    | CLK_EN, CLK_SEL                                       |   | -0.3 |      | 0.8          | V     |
| $I_{IH}$ | Input High Current | CLK <sub>0</sub> , CLK <sub>1</sub> , CLK_SEL         | $V_{IN} = V_{CC} = 3.6\text{V}$               |      |      | 150          | uA    |
|          |                    | CLK_EN  | $V_{IN} = V_{CC} = 3.6\text{V}$               |      |      | 5            | uA    |
| $I_{IL}$ | Input Low Current  | CLK <sub>0</sub> , CLK <sub>1</sub> , CLK_SEL         | $V_{IN} = 0\text{V}$ , $V_{CC} = 3.6\text{V}$ | -5   |      |              | uA    |
|          |                    | CLK_EN  | $V_{IN} = 0\text{V}$ , $V_{CC} = 3.6\text{V}$ | -150 |      |              | uA    |

**LVPECL DC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 3.0\text{V}$  to  $3.6\text{V}$  unless otherwise stated below.)

| Symbol      | Parameter                          | Conditions | Min.         | Typ. | Max.         | Units |
|-------------|------------------------------------|------------|--------------|------|--------------|-------|
| $V_{OH}$    | Output High Voltage <sup>(1)</sup> |            | $V_{CC}-1.4$ |      | $V_{CC}-0.9$ | V     |
| $V_{OL}$    | Output Low Voltage <sup>(1)</sup>  |            | $V_{CC}-2.0$ |      | $V_{CC}-1.7$ |       |
| $V_{SWING}$ | Peak-to-peak Output Voltage Swing  |            | 0.6          |      | 1.0          |       |

**Notes:**

1. Outputs terminated with  $50\Omega$  to  $V_{CC}-2.0\text{V}$

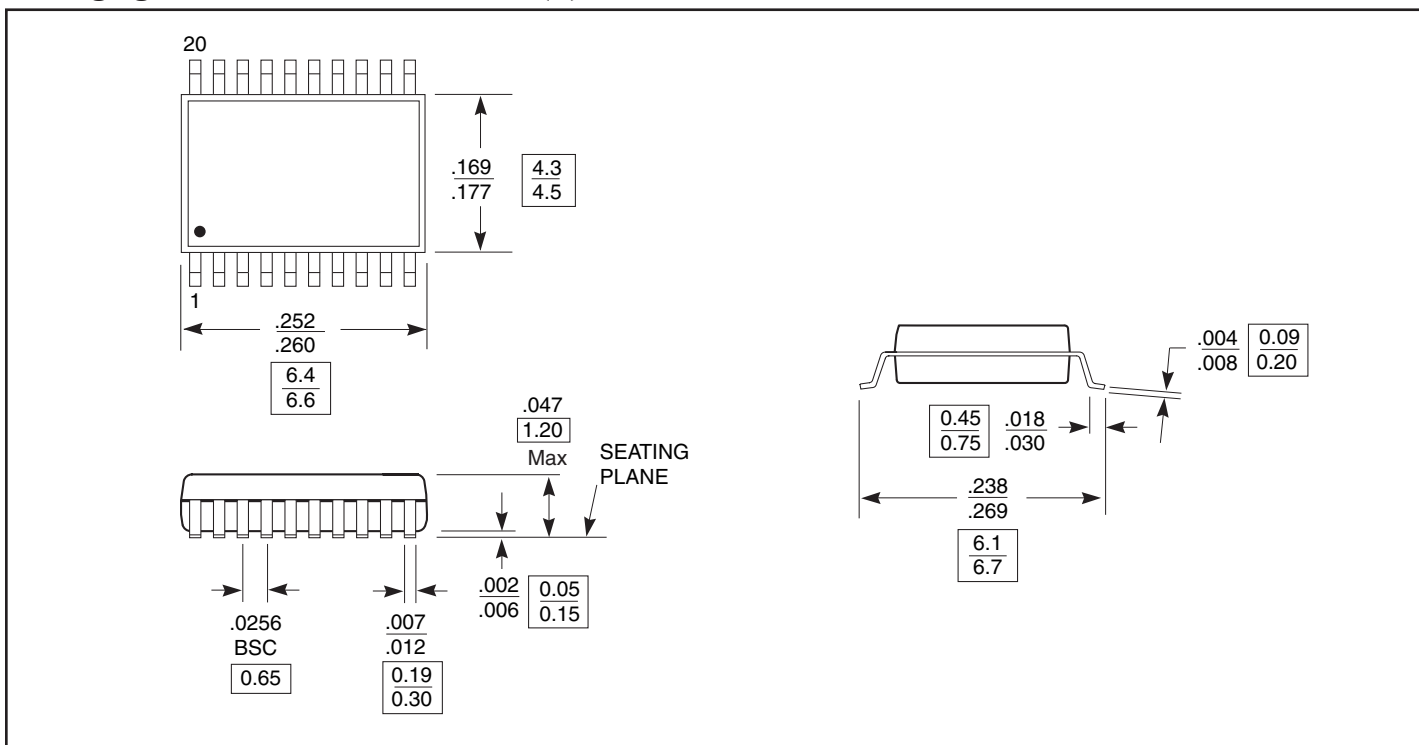
**AC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 3.0\text{V}$  to  $3.6\text{V}$ )

| Symbol       | Parameter                            | Conditions                       | Min. | Typ. | Max. | Units |
|--------------|--------------------------------------|----------------------------------|------|------|------|-------|
| $f_{max}$    | Output Frequency                     |                                  |      |      | 500  | MHz   |
| $t_{pd}$     | Propagation Delay <sup>(1)</sup>     |                                  | 1.0  |      | 1.9  | ns    |
| $T_{sk(o)}$  | Output-to-output Skew <sup>(2)</sup> |                                  |      |      | 80   | ps    |
| $T_{sk(pp)}$ | Part-to-part Skew <sup>(3)</sup>     |                                  |      |      | 150  |       |
| $t_r/t_f$    | Output Rise/Fall time                | 20% - 80%                        | 80   |      | 400  |       |
| odc          | Output Duty Cycle                    |                                  | 40   |      | 60   | %     |
| $J_{add}$    | Additive Jitter                      | At 155.25MHz over 12kHz to 20MHz |      | 36.7 |      | fs    |

**Notes:**

1. Measured from the  $V_{CC}/2$  of the input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
3. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
4. All parameters are measured at 500 MHz unless noted otherwise

### Packaging Mechanical: 20-Pin TSSOP (L)



### Ordering Information

| Ordering Code  | Package Code | Package Description                       |
|----------------|--------------|---|
| PI6C48535-01LE | L            | Pb-free & Green 20-pin 173-mil wide TSSOP |

#### Notes:

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- E = Pb-free & Green
- X suffix = Tape/Reel

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