

IRS2301S HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 5V to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Lower di/dt gate driver for better noise immunity
- Leadfree, RoHS compliant

Typical Applications

- Appliance motor drives
- Servo drives
- Micro inverter drives
- General purpose three phase inverters

Product Summary

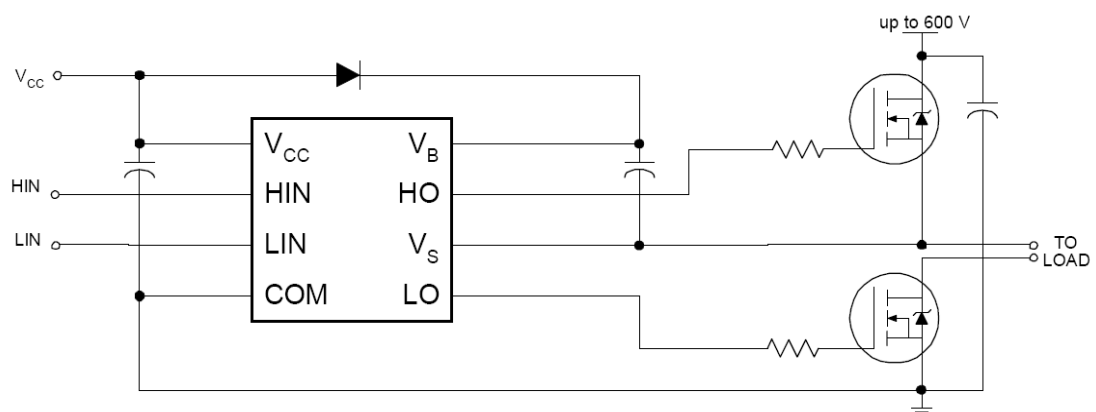
| | |
|--|---------------|
| V_{OFFSET} | 600V Max |
| V_{OUT} | 5V – 20V |
| I_{o+} & I_{o-} (min) | 120mA / 250mA |
| t_{ON} & t_{OFF} (typical) | 220ns / 200ns |
| Delay Matching | 50ns |

Package Options



8-Lead SOIC
IRS2301S

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

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Description

The IRS2301S is a high voltage, high speed power MOSFET and IGBT driver with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600V.

Qualification Information[†]

| | | |
|-----------------------------------|------------------|---|
| Qualification Level | | Industrial ^{††} |
| | | Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level. |
| Moisture Sensitivity Level | | MSL2 ^{†††} 260°C (per IPC/JEDEC J-STD-020) |
| ESD | Machine Model | Class B (per JEDEC standard JESD22-A115) |
| | Human Body Model | Class 2 (per EIA/JEDEC standard EIA/JESD22-A114) |
| IC Latch-Up Test | | Class I, Level A (per JESD78) |
| RoHS Compliant | | Yes |

- † Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>
- †† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.
- ††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Min. | Max. | Units |
|------------|---|-------------|----------------|---------------------------|
| V_B | High-side floating absolute voltage | -0.3 | 625 | V |
| V_S | High-side floating supply offset voltage | $V_B - 25$ | $V_B + 0.3$ | |
| V_{HO} | High-side floating output voltage | $V_S - 0.3$ | $V_B + 0.3$ | |
| V_{CC} | Low-side and logic fixed supply voltage | -0.3 | 25 | |
| V_{LO} | Low-side output voltage | -0.3 | $V_{CC} + 0.3$ | |
| V_{IN} | Logic input voltage (HIN & LIN) | COM -0.3 | $V_{CC} + 0.3$ | |
| dV_S/dt | Allowable offset supply voltage transient | — | 50 | V/ns |
| P_D | Package power dissipation @ $T_A \leq 25^\circ\text{C}$ | — | 0.625 | W |
| R_{thJA} | Thermal resistance, junction to ambient | — | 200 | $^\circ\text{C}/\text{W}$ |
| T_J | Junction temperature | — | 150 | $^\circ\text{C}$ |
| T_S | Storage temperature | -50 | 150 | |
| T_L | Lead temperature (soldering, 10 seconds) | — | 300 | |

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

| Symbol | Definition | Min. | Max. | Units |
|----------|--|-----------|------------|------------------|
| V_B | High-side floating supply absolute voltage | $V_S + 5$ | $V_S + 20$ | V |
| V_S | High-side floating supply offset voltage | † 1 | 600 | |
| V_{HO} | High-side floating output voltage | V_S | V_B | |
| V_{CC} | Low-side and logic fixed supply voltage | 5 | 20 | |
| V_{LO} | Low-side output voltage | 0 | V_{CC} | |
| V_{IN} | Logic input voltage (HIN & LIN) | COM | V_{CC} | |
| T_A | Ambient temperature | -40 | 125 | $^\circ\text{C}$ |

†: Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$.
 (Please refer to the Design Tip DT97 -3 for more details).

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IL} , V_{IH} and I_{IN} parameters are referenced to COM and are applicable to the respective input leads: HIN and LIN. The V_O , I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

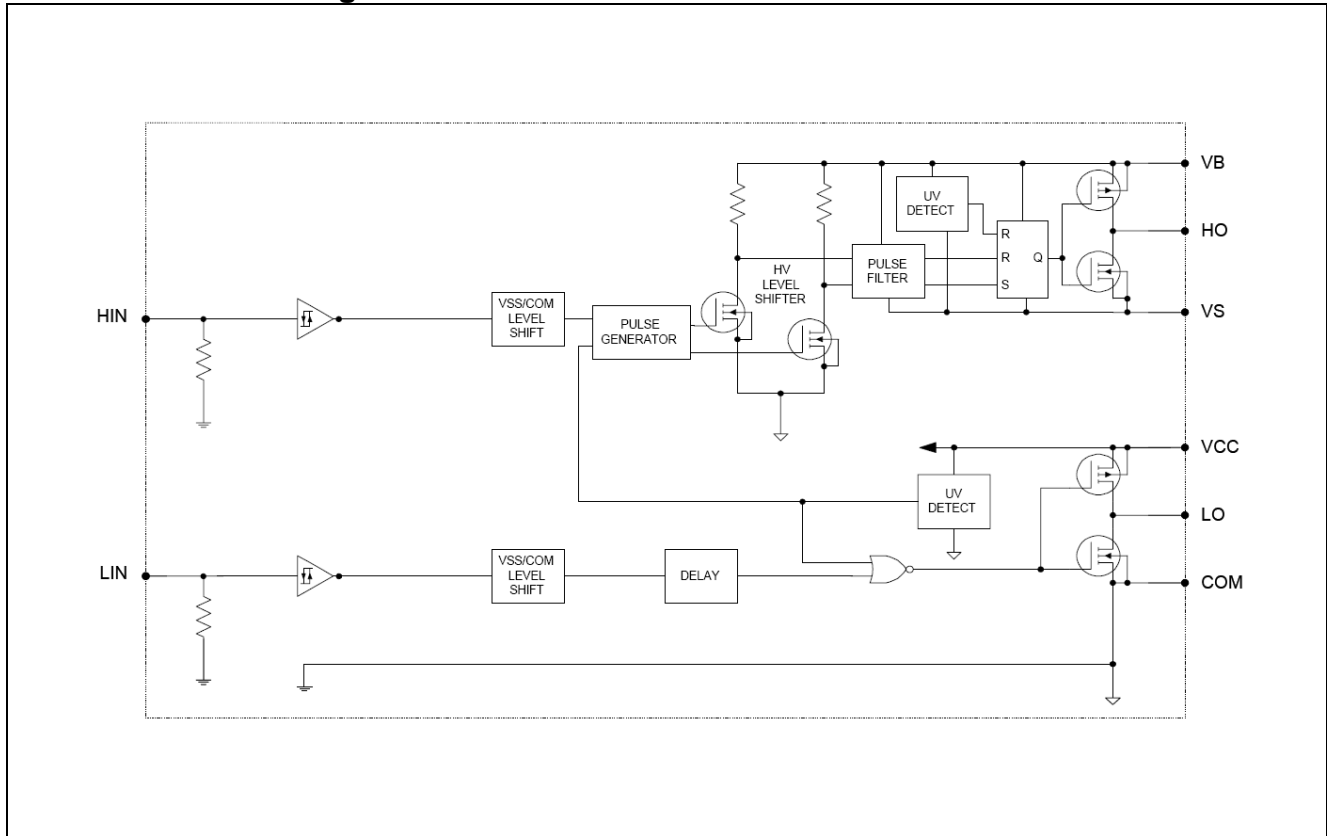
| Symbol | Definition | Min | Typ | Max | Units | Test conditions |
|----------------------------|--|-----|-----|-----|---------|------------------------------------|
| V_{IH} | Logic "1" input voltage | 2.5 | — | — | V | $V_{CC} = 10V$ to 20V |
| V_{IL} | Logic "0" input voltage | — | — | 0.8 | | |
| V_{OH} | High level output voltage, $V_{BIAS} - V_O$ | — | — | 0.2 | V | $I_O = 2mA$ |
| V_{OL} | Low level output voltage, V_O | — | — | 0.1 | | |
| I_{LK} | Offset supply leakage current | — | — | 50 | μA | $V_B = V_S = 600V$ |
| I_{QBS} | Quiescent V_{BS} supply current | 60 | 160 | 260 | | $V_{IN} = 0V$ or 5V |
| I_{QCC} | Quiescent V_{CC} supply current | 60 | 160 | 260 | | $V_{IN} = 5V$ |
| I_{IN+} | Logic "1" input bias current | — | 5 | 20 | | $V_{IN} = 0V$ |
| I_{IN-} | Logic "0" input bias current | — | — | 5 | | |
| V_{CCUV+} V_{BSUV+} | V_{CC} and V_{BS} supply undervoltage positive going threshold | 3.3 | 4.1 | 5 | V | |
| V_{CCUV-} V_{BSUV-} | V_{CC} and V_{BS} supply undervoltage negative going threshold | 3 | 3.8 | 4.7 | | |
| V_{CCUVH} V_{BSUVH} | Hysteresis | 0.1 | 0.3 | — | | |
| I_{O+} | Output high short circuit pulsed current | — | 200 | — | mA | $V_O = 0V$, $PW \leq 10\mu s$ |
| I_{O-} | Output low short circuit pulsed current | — | 350 | — | | $V_O = 15V$, $PW \leq 10\mu s$ |

Dynamic Electrical Characteristics

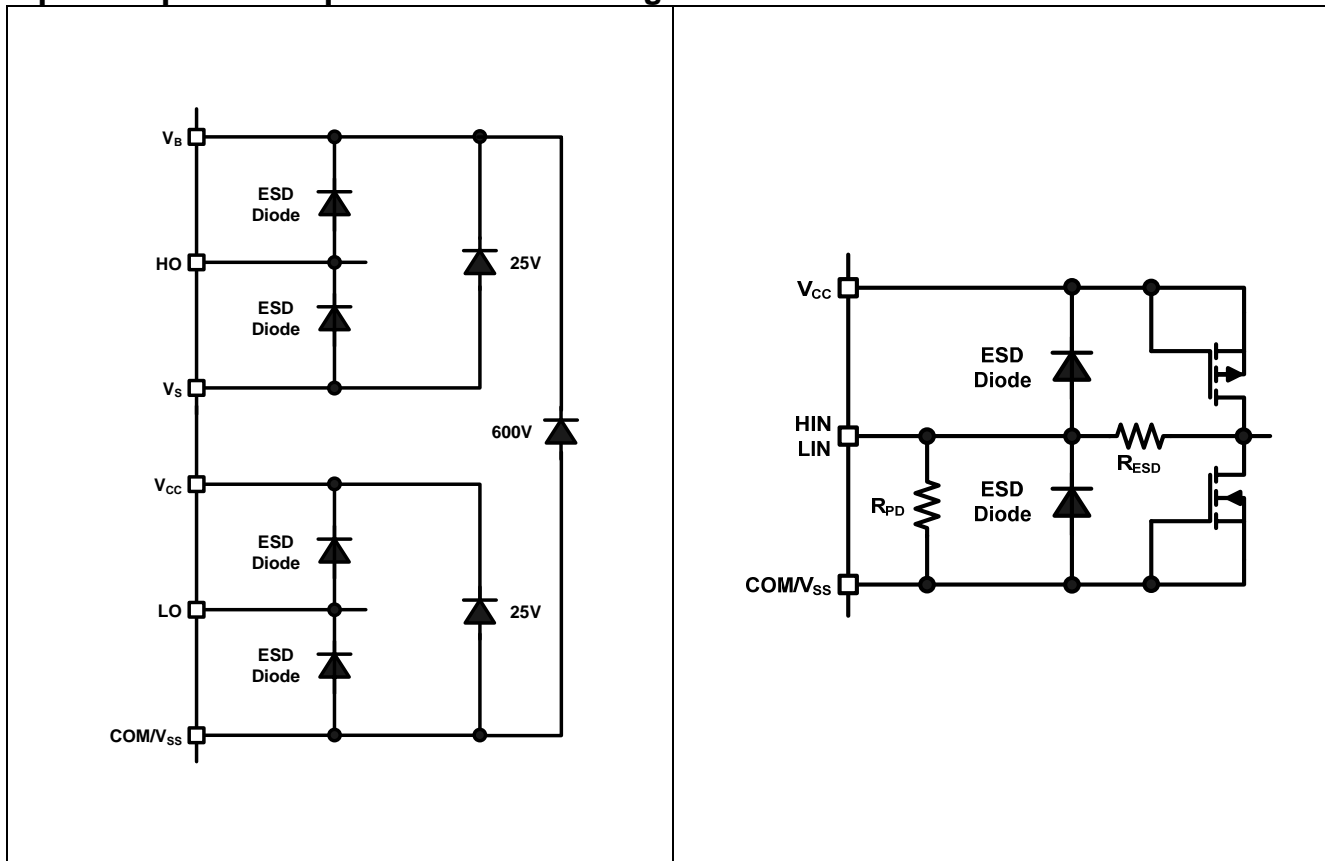
V_{BIAS} (V_{CC} , V_{BS}) = 15V, $C_L = 1000pF$, $T_A = 25^\circ C$ unless otherwise specified.

| Symbol | Definition | Min | Typ | Max | Units | Test conditions |
|-----------|-------------------------------------|-----|-----|-----|-------|--------------------|
| t_{on} | Turn-on propagation delay | — | 220 | 300 | ns | $V_S = 0V$ |
| t_{off} | Turn-off propagation delay | — | 200 | 280 | | $V_S = 0V$ or 600V |
| MT | Delay matching, HS & LS turn-on/off | — | 0 | 50 | | |
| t_r | Turn-on rise time | — | 130 | 220 | | $V_S = 0V$ |
| t_f | Turn-off fall time | — | 50 | 80 | | |

Functional Block Diagram:



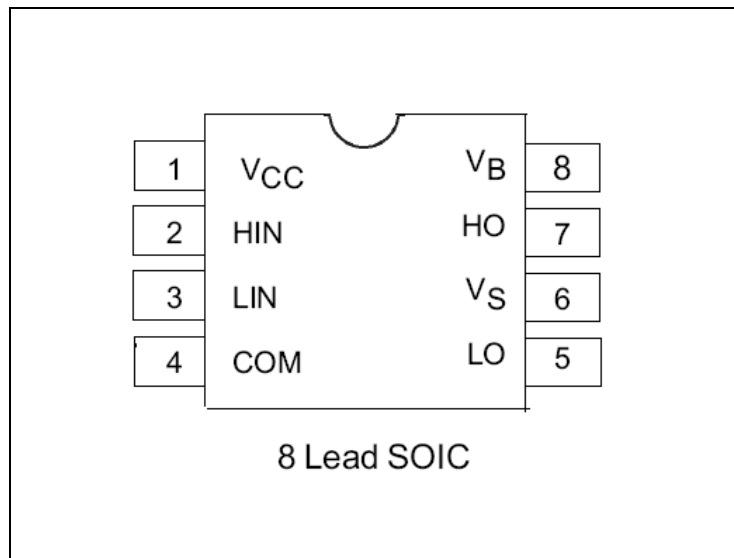
Input/Output Pin Equivalent Circuit Diagrams:



Lead Definitions:

| PIN# | Symbol | Description |
|------|-----------------|--|
| 1 | V _{CC} | Low-side and logic fixed supply |
| 2 | HIN | Logic input for high-side gate driver outputs (HO), in phase with HO |
| 3 | LIN | Logic input for low-side gate driver outputs (LO), in phase with LO |
| 4 | COM | Low-side return |
| 5 | LO | Low-side gate drive output |
| 6 | V _S | High-side floating supply return |
| 7 | HO | High-side gate drive output |
| 8 | V _B | High-side floating supply |

Lead Assignments



Application Information and Additional Details

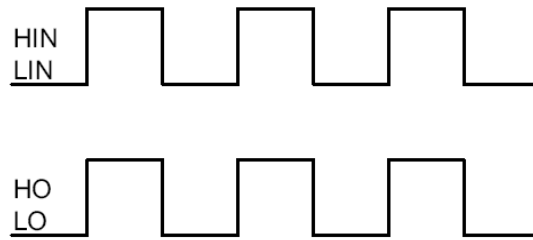


Figure 1: Input/Output Timing Diagram

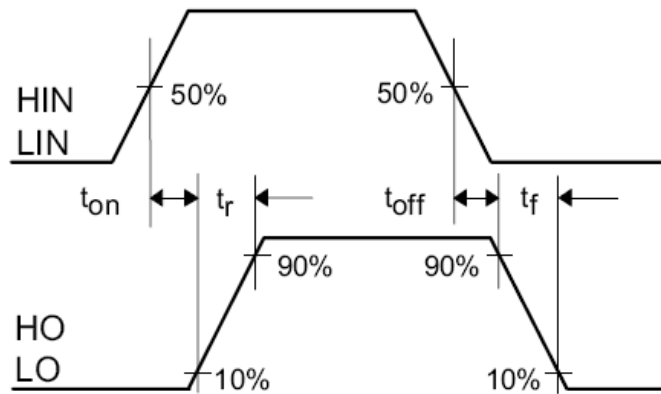


Figure 2: Switching Time Waveform Definitions

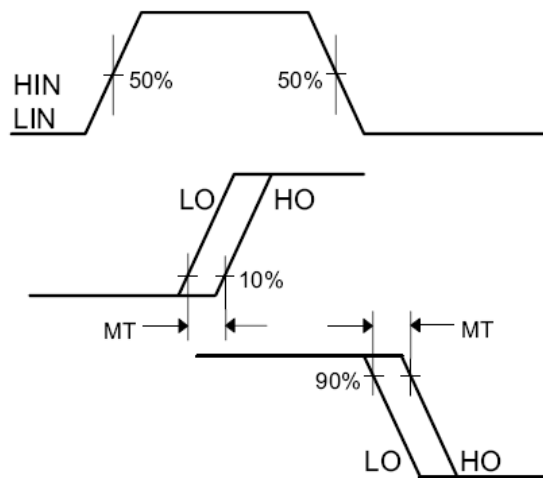


Figure 3: Delay Matching Waveform Definitions

Tolerability to Negative V_s Transients

The IRS2301S has been seen to withstand negative V_s transient conditions on the order of -25V for a period of 100 ns (V_{BIAS} (V_{CC} , V_{BS}) = 15V and T_A = 25°C).

An illustration of the IRS2301S performance can be seen in Figure 4.

Even though the IRS2301S has been shown able to handle these negative V_s transient conditions, it is highly recommended that the circuit designer always limit the negative V_s transients as much as possible by careful PCB layout and component use.

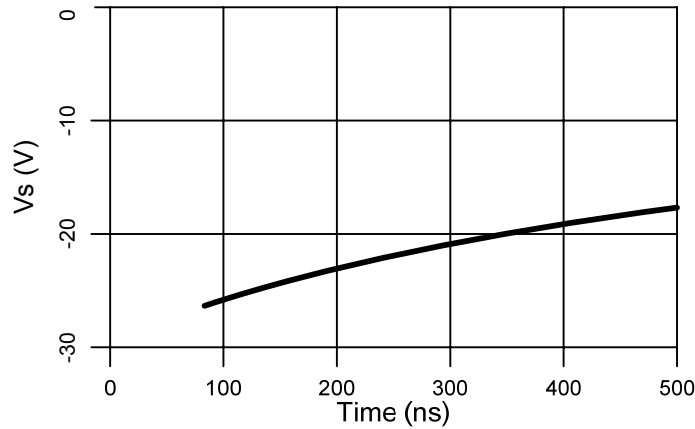
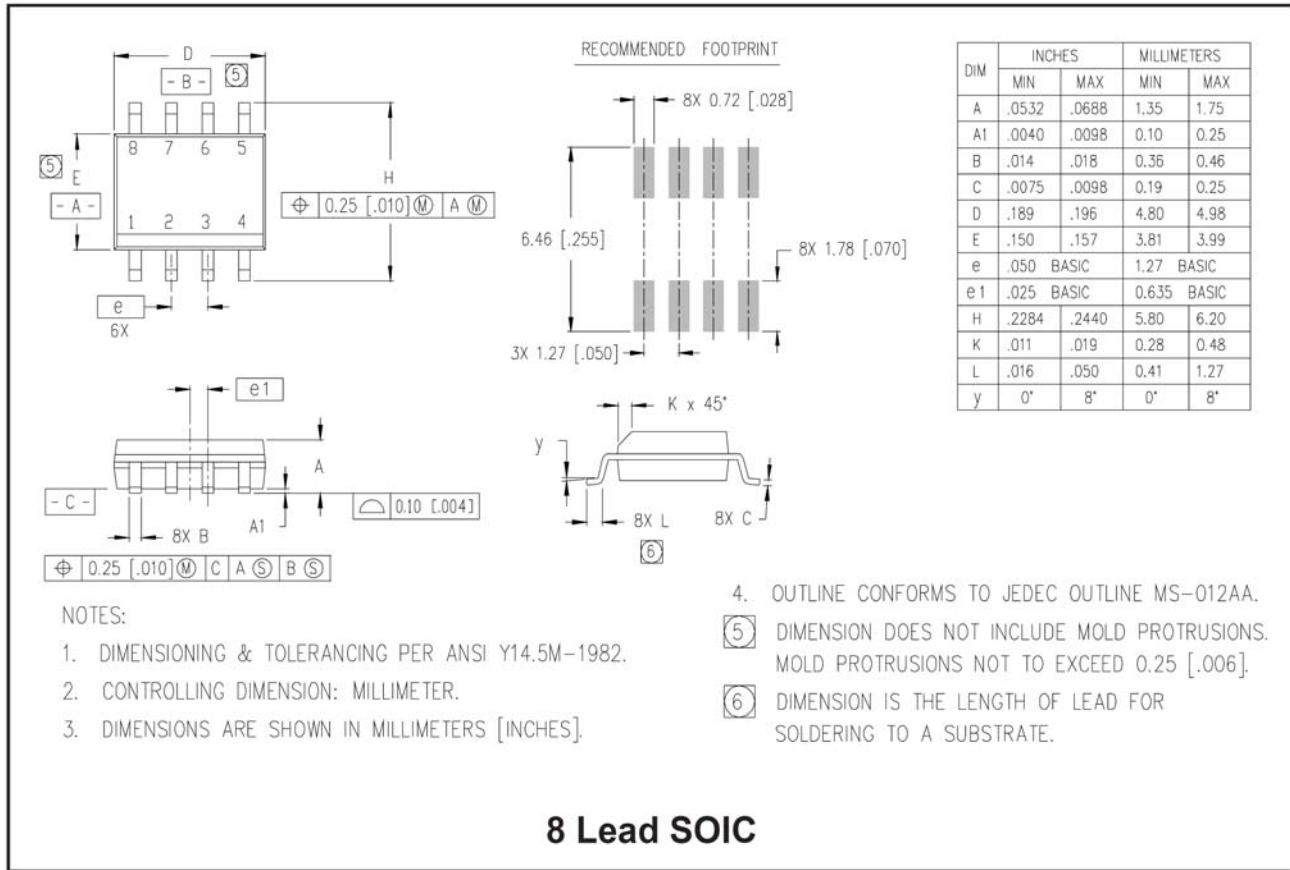
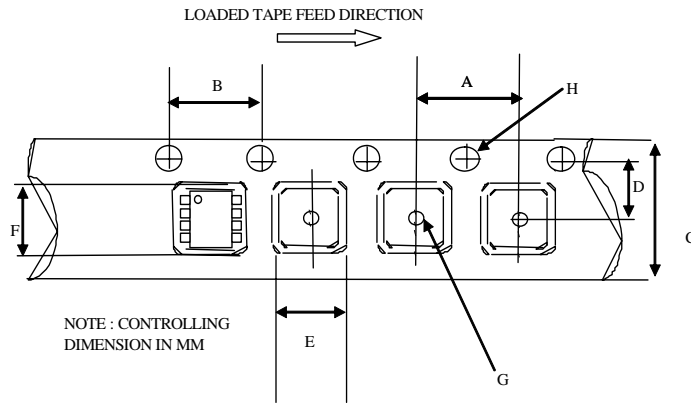


Figure 4: - V_s Transient results

Package Details

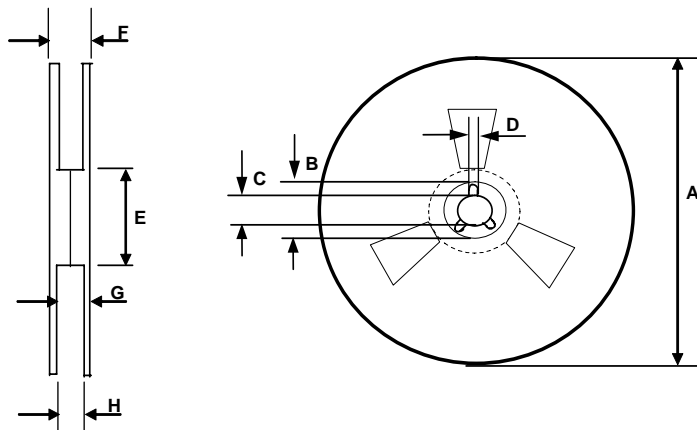


Tape and Reel Details



CARRIER TAPE DIMENSION FOR 8SOICN

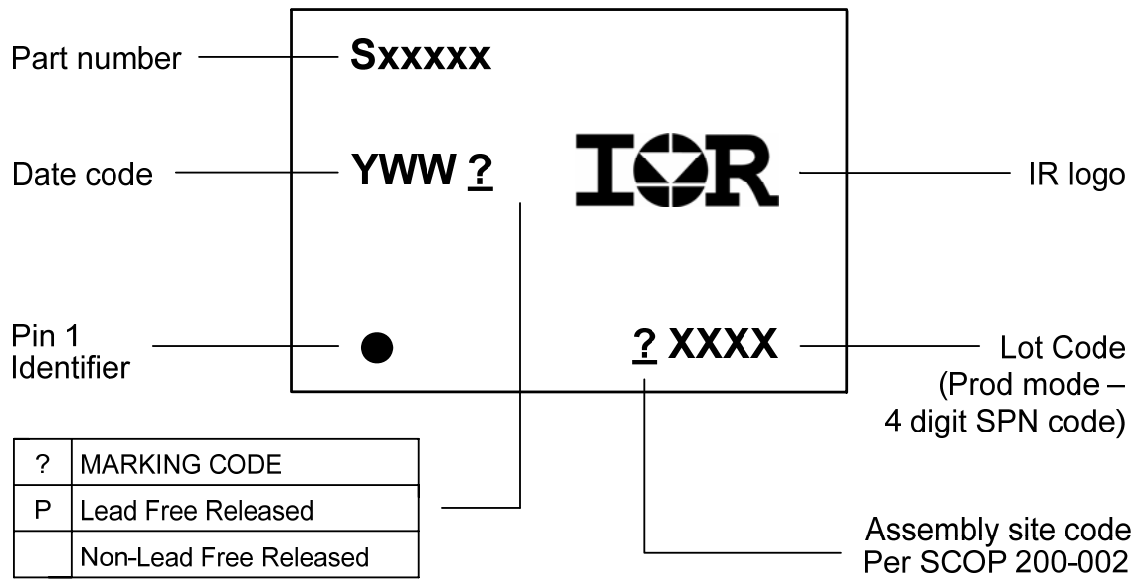
| Code | Metric | | Imperial | |
|------|--------|-------|----------|-------|
| | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 11.70 | 12.30 | 0.46 | 0.484 |
| D | 5.45 | 5.55 | 0.214 | 0.218 |
| E | 6.30 | 6.50 | 0.248 | 0.255 |
| F | 5.10 | 5.30 | 0.200 | 0.208 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |



REEL DIMENSIONS FOR 8SOICN

| Code | Metric | | Imperial | |
|------|--------|--------|----------|--------|
| | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 18.40 | n/a | 0.724 |
| G | 14.50 | 17.10 | 0.570 | 0.673 |
| H | 12.40 | 14.40 | 0.488 | 0.566 |

Part Marking Information



Ordering Information

| Base Part Number | Package Type | Standard Pack | | Complete Part Number |
|------------------|--------------|---------------|----------|----------------------|
| | | Form | Quantity | |
| IRS2301 | SOIC8N | Tube/Bulk | 95 | IRS2301SPBF |
| | | Tape and Reel | 2500 | IRS2301STRPBF |

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