Dual 2 MHz, 800 mA, Synchronous, Low Quiescent Current Buck Regulator

Data Sheet

ADP2230

FEATURES

- Input voltage range: 2.3 V to 6.5 V
- Fixed and adjustable output voltage options
  - Fixed output voltage pair options: 1.2 V/1.8 V, 1.2 V/3.3 V, 1.8 V/3.3 V
  - Adjustable output voltage range: 0.8 V to 6 V
- Minimum guaranteed continuous output current: 800 mA
- Up to 94% efficiency
- Low quiescent current of 15 µA for both channels in power saving mode (PSM)
- Low shutdown current: 0.1 µA (typical)
- 100% duty cycle for low dropout operation
- SYNC pin switching frequency options
  - 2 MHz fixed pulse-width modulation (PWM) mode
  - 2 MHz PSM/PWM automatic transitioning mode
  - External clock synchronization from 1.5 MHz to 2.5 MHz
- Enable input with precision thresholds for each output
- 180° phase shifted PWM outputs for minimum V_{IN} ripple
- Current-limit and thermal shutdown (TSD) protection
- Quick output discharge (QOD)
- 10-lead, 3 mm × 3 mm × 0.75 mm LFCSP package

APPLICATIONS

- Portable and battery-powered equipment
- Automatic meter readers (WSN)
- Point of sales and transaction processing instruments
- Mobile phones
- Digital cameras and audio devices
- Medical instruments
- Medium format display tablets and pads

GENERAL DESCRIPTION

The ADP2230 includes two high efficiency, low quiescent current, 800 mA, step-down, dc-to-dc converters in a small, 10-lead, 3 mm × 3 mm, LFCSP package. The total solution requires only five tiny external components. When the ADP2230 is used with three 0603 capacitors and two 2 mm × 2 mm inductors, the total solution size is about 48 mm^2, resulting in the smallest footprint solution to meet a variety of portable applications.

The ADP2230 buck regulator uses a proprietary, high speed, current mode, constant frequency, PWM control scheme for excellent stability and transient response. The buck outputs operate out of phase to reduce the input current ripple. To ensure the longest battery life in portable applications, the ADP2230 has a power saving variable frequency mode that reduces the switching frequency under light load conditions.

TYPICAL APPLICATION CIRCUIT

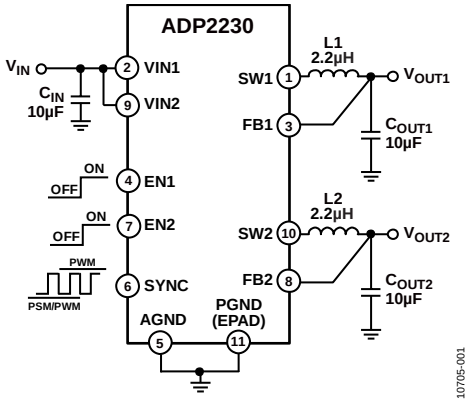

Figure 1. Fixed Output Voltage Typical Application Circuit

During logic controlled shutdown, the input is disconnected from the output, and it draws less than 0.1 µA from the input source. The ADP2230 operates from input voltages from 2.3 V to 6.5 V, allowing the use of multiple alkaline, NiMH, or lithium cells and other standard power sources.

The ADP2230 offers multiple options for setting the operating frequency. To maximize light load efficiency, the ADP2230 can operate at a reduced switching frequency in PSM and switch automatically to PWM as the load increases. The ADP2230 can be forced to operate at 2 MHz in PWM only mode when noise considerations are more important than efficiency. The ADP2230 can also be synchronized with a 1.5 MHz to 2.5 MHz external clock via the SYNC pin. When using the external clock synchronization control, both buck outputs operate in phase with the applied clock signal.

The ADP2230 includes an internal power switch, synchronous rectifier, and compensation to minimize external part count and maximize efficiency. Other key protection features include undervoltage lockout to prevent deep battery discharge, internal soft start to prevent input current overshoot at startup, and an integrated, switched resistor, QOD function that automatically discharges the output when the device is disabled. Short-circuit protection and thermal overload protection circuits prevent damage in adverse conditions.

Rev. A
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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Typical Application Circuit ... 1
Revision History ... 2
Specifications ... 3
Recommended Component Specifications ... 4
Absolute Maximum Ratings ... 5
Thermal Data ... 5
Thermal Resistance ... 5
ESD Caution ... 5
Pin Configuration and Function Descriptions ... 6
Typical Performance Characteristics ... 7
Theory of Operation ... 12
Overview ... 12
Operating Conditions ... 12
SYNC Pin Control Schemes ... 13
Features Descriptions ... 13
Applications Information ... 15
Setting the Output Voltage ... 15
Selecting the Inductor ... 15
Selecting the Input and Output Capacitors ... 16
PCB Layout Considerations ... 17
Outline Dimensions ... 18
Ordering Guide ... 18

REVISION HISTORY

11/14—Rev. 0 to Rev. A

Changes to Ordering Guide ... 18

10/14—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = V_{ENx} = 5.0 V, V_{OUT} = 3.3 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Input Voltage Range	V_{IN}		2.3		6.5	V
Quiescent Current	I_Q	V_{SYNC} = GND, no load, device not switching				
		One channel enabled		8	23	µA
		Both channels enabled		15	34	µA
Standby Current		V_{ENx} = 1 V		55		µA
Shutdown Current	I_{SD}	V_{ENx} = GND, T_J = −40°C to +85°C		0.1	2.5	µA
Undervoltage Lockout						
V_{IN} Rising Threshold				2.23	2.28	V
V_{IN} Falling Threshold			1.96	2.05		V
Soft Start Time	t_{SS}		185	270	395	µs
FIXED AND ADJUSTABLE OUTPUT						
Load Regulation PWM	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 0 mA to 800 mA		0.1		%/A
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 2.3 V to 6.5 V, V_{OUT} = 1.2 V, I_{OUT} = 500 mA		0.1		%/V
PSM Rising Threshold		V_{IN} = 5 V, V_{OUT} = 3.3 V		230		mA
PSM Hysteresis				25		mA
FIXED OUTPUT VOLTAGE						
Fixed V_{OUT} Accuracy		V_{IN} = 5 V, no load				
V_{OUT} = 1.2 V	$V_{OUT_1.2V}$		1.168	1.2	1.220	V
V_{OUT} = 1.8 V	$V_{OUT_1.8V}$		1.748	1.8	1.851	V
V_{OUT} = 3.3 V	$V_{OUT_3.3V}$		3.202	3.3	3.363	V
Fixed V_{OUT} FB Pin Current[1]	I_{FB_FIXED}	V_{FB} = 1.2 V	1.1	2.0	2.8	µA
ADJUSTABLE OUTPUT VOLTAGE						
Feedback Voltage	V_{FB}		0.774	0.8	0.818	V
Adjustable V_{OUT} Range	V_{OUT_ADJ}		0.8		6	V
Adjustable V_{OUT} FB Pin Current	I_{FB_ADJ}	V_{FB} = 0.8 V		10	150	nA
SWITCHING CHARACERISTICS						
On Resistance		V_{IN} = 5 V, I_{SW} = 400 mA				
P-Channel	R_{DSON_P}			230	325	mΩ
N-Channel	R_{DSON_N}			180	275	mΩ
Current Limit						
P-Channel			930	1300	1475	mA
N-Channel			300	500	625	mA
P-Channel Leakage Current		V_{IN} = 5 V, V_{SW} = GND, T_J = −40°C to +85°C			2	µA
Minimum On Time	t_{ON-MIN}		3	35	65	ns
SWx Node Discharge Resistor				250	340	Ω
Phase Shift Between SW1 and SW2		V_{SYNC} = GND or V_{SYNC} = V_{IN} (no external clock)		180		Degrees
OSCILLATOR						
Fixed PWM Oscillator Frequency	f_{SW_FIXED}	V_{SYNC} = GND or V_{SYNC} = V_{IN}	1600	2000	2300	kHz
External Clock Synchronization Range	f_{SW_RANGE}		1.5		2.5	MHz
External Clock Duty Cycle Range			20		85	%
SYNC Pin						
High Threshold			1.3			V
Low Threshold					0.4	V
Leakage Current		V_{SYNC} = GND or V_{SYNC} = V_{IN}		0.01	1	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
ENABLE STANDBY LOGIC LEVELS		2.3 V ≤ V_{IN} ≤ 6.5 V				
High			1.15			V
Low					0.4	V
Hysteresis				200		mV
ENABLE PRECISION LOGIC LEVELS		2.3 V ≤ V_{IN} ≤ 6.5 V				
Operating Maximum						
EN1	V_{EN1}				5.5	V
EN2	V_{EN2}				6.5	V
High		ENx pin rising		1.2	1.255	V
Low		ENx pin falling	1	1.1		V
ENx Pin Leakage Current		V_{ENx} = V_{IN} or GND		0.01	1	µA
THERMAL SHUTDOWN						
Threshold		T_J rising		150		°C
Hysteresis				15		°C

[1] The fixed V_{OUT} feedback pin current is the internal feedback voltage, 0.8 V (typical), divided by the bottom feedback resistor, typically 400 kΩ.

RECOMMENDED COMPONENT SPECIFICATIONS

T_A = −40°C to +125°C

Table 2.

Parameter	Symbol	Min[1]	Typ	Max	Unit
INPUT AND OUTPUT CAPACITANCE[2]	C_{IN}, C_{OUT}	7	10		µF
Capacitor Equivalent Series Resistance (ESR)	ESR_{CIN}, ESR_{COUT}	0.001		0.01	Ω
INDUCTANCE	L	1.5	2.2		µH

[1] Minimum values represent the minimum effective values of the components under the application operating conditions. To achieve the minimum effective values, components specified as 2.2 µH inductors and 10 µF capacitors are recommended.

[2] Ensure that the minimum input and output capacitance is greater than 7 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VINx, FBx, EN2, SYNC to AGND, PGND	−0.3 V to +7 V
EN1	−0.3 V to +6 V
SWx to AGND, PGND	−0.3 V to VINx
Operating Ambient Temperature Range	−40°C to +85°C
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination.

THERMAL DATA

Exceeding the junction temperature (T_J) limit can cause damage to the ADP2230. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. The maximum ambient temperature may require derating in applications with high power dissipation and poor thermal resistance.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature of the device is dependent on the ambient temperature, the power dissipation of the device, and the junction-to-ambient thermal resistance (θ_{JA}) of the package.

Maximum T_J is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

θ_{JA} of the package is based on modeling and calculation using a 4-layer board. θ_{JA} is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} can vary, depending on PCB material, layout, and environmental conditions.

The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. See JEDEC JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, for detailed information on board construction. For more information, see AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. The Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in junction-to-board thermal resistance (θ_{JB}). Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum T_J is calculated from the board temperature (T_B) and P_D using the formula

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (2)$$

For more information regarding Ψ_{JB}, see JESD51-12 and JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JC} is a parameter for surface-mount packages with top mounted heat sinks.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
10-Lead, 3 mm × 3mm LFCSP	44.6	5.45	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

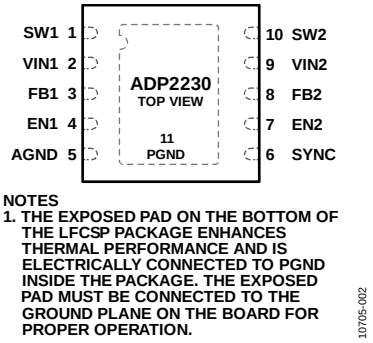

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SW1	Connection from MOSFET Power Switches to the Inductor for Buck 1.
2	VIN1	Analog and Power Voltage Input for Buck 1. Connect VIN1 to VIN2.
3	FB1	Output Voltage Feedback for Buck 1.
4	EN1	Precision Enable for Buck 1. Do not leave the EN1 pin floating.
5	AGND	Analog Ground.
6	SYNC	Frequency Synchronization. Drive SYNC high to force the device to operate in 2 MHz fixed PWM mode. Drive SYNC low to force the device to operate in 2 MHz PSM/PWM automatic transitioning mode. Apply an external clock between 1.5 MHz and 2.5 MHz to the SYNC pin to synchronize the ADP2230 switching to the applied external clock. Do not leave the SYNC pin floating.
7	EN2	Precision Enable for Buck 2. Do not leave the EN2 pin floating.
8	FB2	Output Voltage Feedback for Buck 2.
9	VIN2	Analog and Power Voltage Input for Buck 2. Connect VIN2 to VIN1.
10	SW2	Connection from MOSFET Power Switches to the Inductor for Buck 2.
11	EPAD	Exposed Pad, Power Ground (PGND). The exposed pad on the bottom of the LFCSP package enhances thermal performance and is electrically connected to PGND inside the package. The exposed pad must be connected to the ground plane on the board for proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{ENx} = 5.0 V, C_{IN1} = C_{IN2} = C_{OUT1} = C_{OUT2} = 10 µF (GRM21BR61C106KE15), L1 = L2 = 2.2 µH (XFL3012-222MEB), typical values are at T_A = 25°C, and minimum/maximum limits are guaranteed for T_J = −40°C to +125°C, unless otherwise noted. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

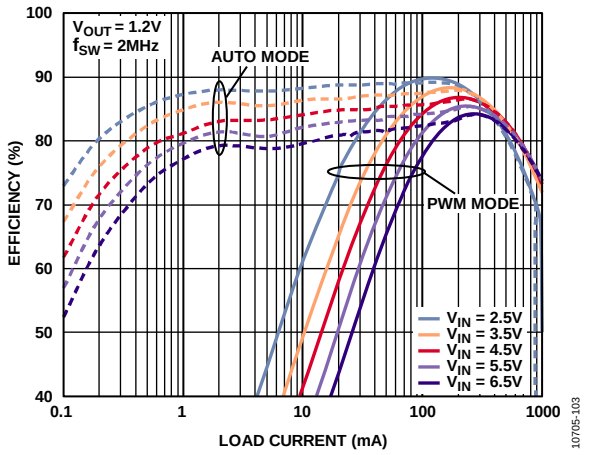

Figure 3. Efficiency vs. Load Current, V_{OUT} = 1.2 V, Different Input Voltages

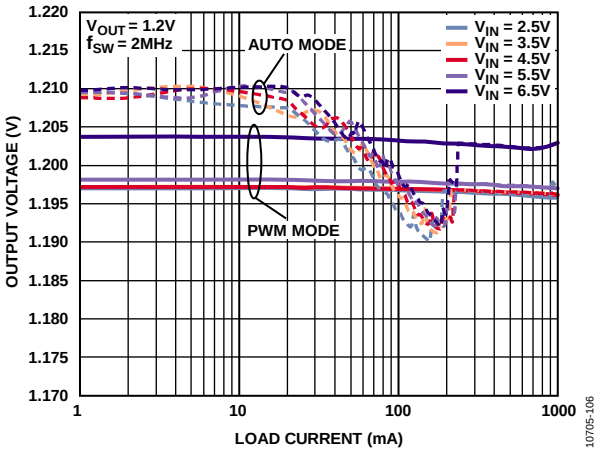

Figure 6. Load Regulation, V_{OUT} = 1.2 V

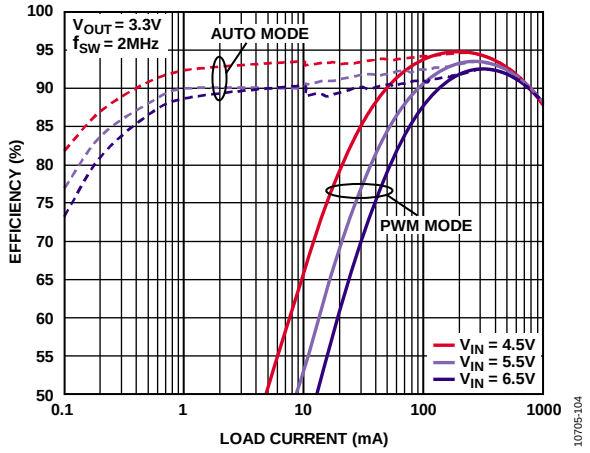

Figure 4. Efficiency vs. Load Current, V_{OUT} = 3.3 V, Different Input Voltages

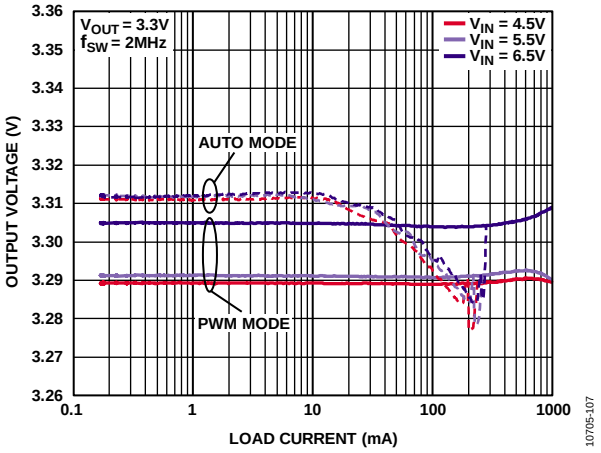

Figure 7. Load Regulation, V_{OUT} = 3.3 V

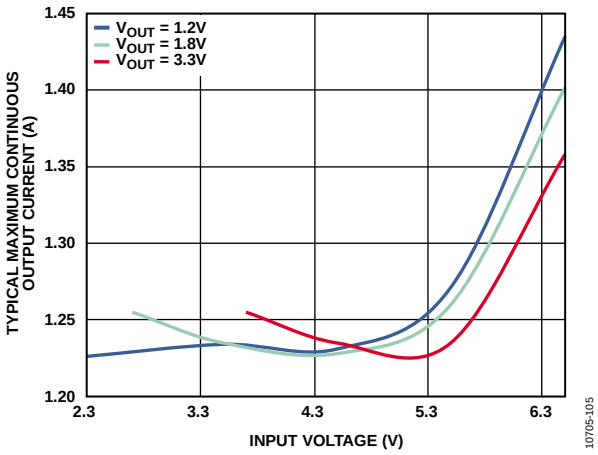

Figure 5. Typical Maximum Continuous Output Current vs. Input Voltage

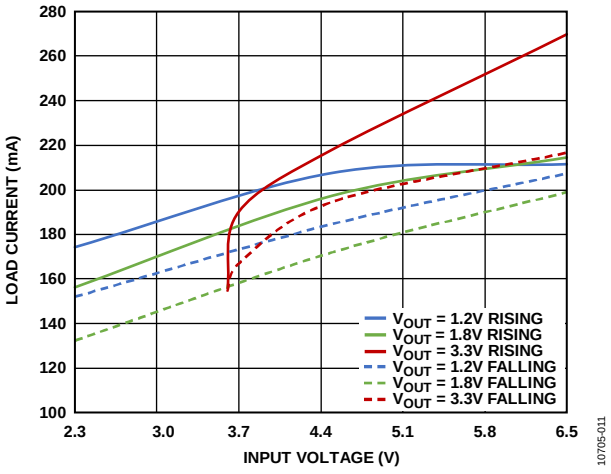

Figure 8. PSM to PWM Mode Transition Threshold vs. Input Voltage

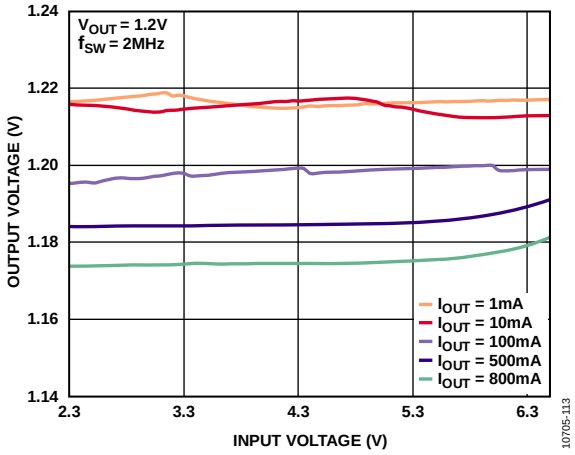

Figure 9. Line Regulation, V_{OUT} = 1.2 V, Different Loads

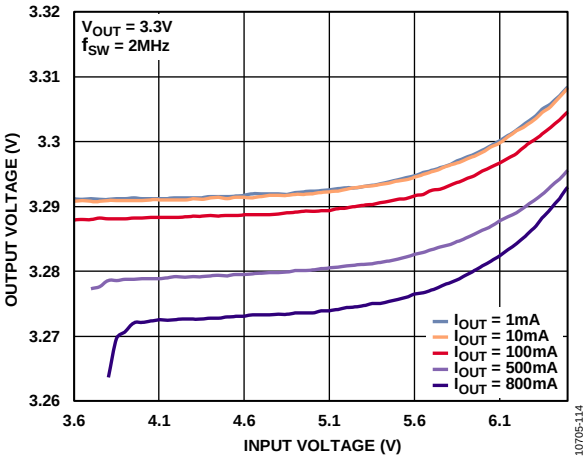

Figure 10. Line Regulation, V_{OUT} = 3.3 V, Different Loads

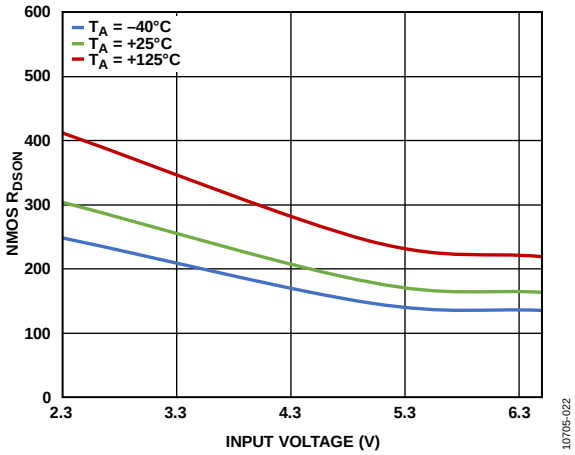

Figure 11. NMOS Drain-to-Source On Resistance (R_{DSON})

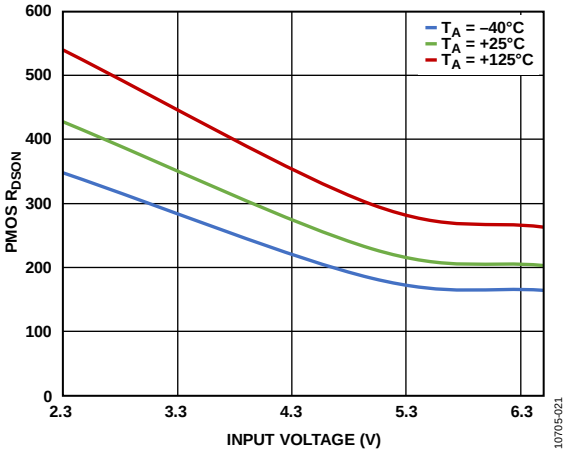

Figure 12. PMOS Drain-to-Source On Resistance (R_{DSON})

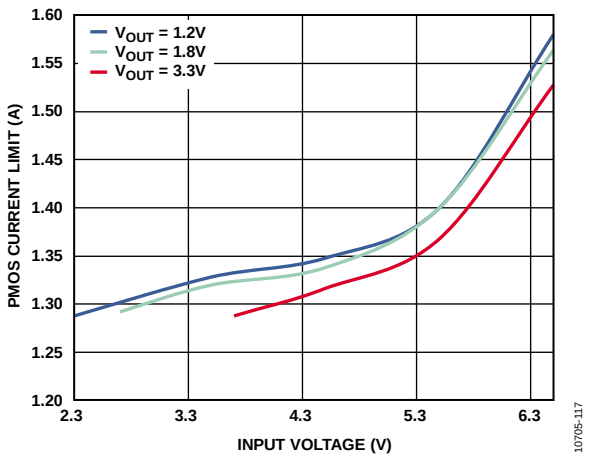

Figure 13. PMOS Current Limit vs. Input Voltage, Different Output Voltages

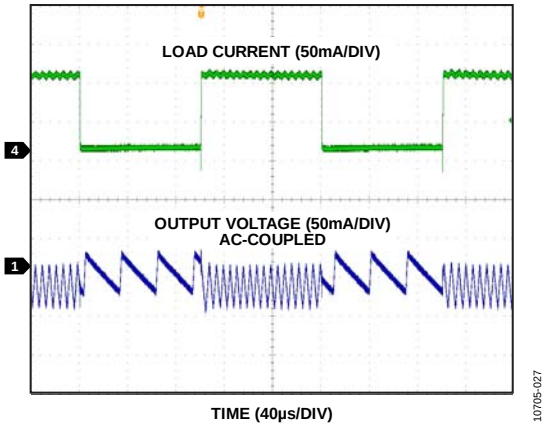

Figure 14. Load Transient Response, V_{OUT} = 1.2 V, Auto Mode, 10 mA to 110 mA

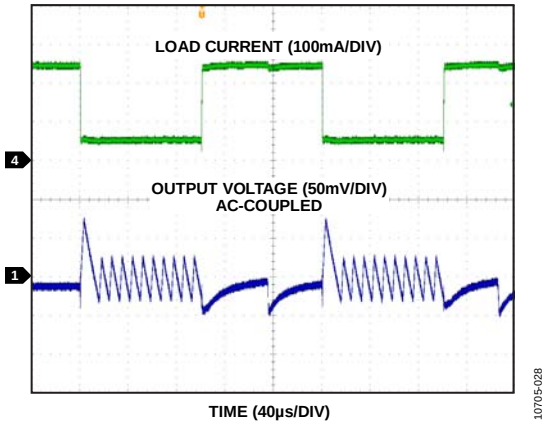

Figure 15. Load Transient Response, V_{OUT} = 1.2 V, Auto Mode, 50 mA to 250 mA

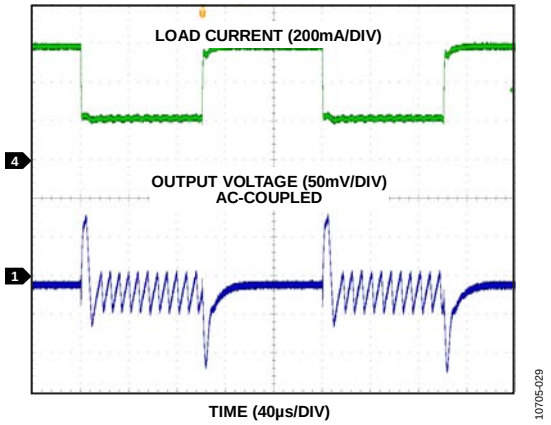

Figure 16. Load Transient Response, V_{OUT} = 1.2 V, Auto Mode, 200 mA to 600 mA

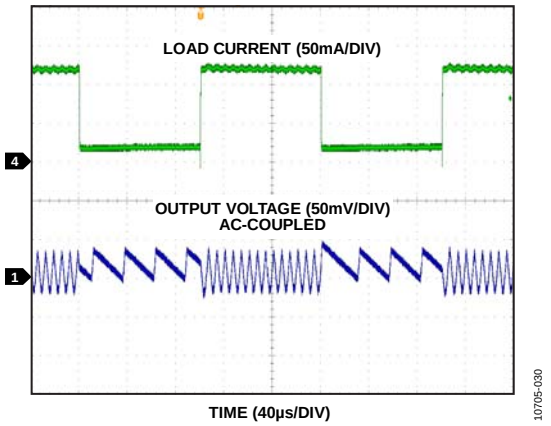

Figure 17. Load Transient Response, V_{OUT} = 1.8 V, Auto Mode, 10 mA to 110 mA

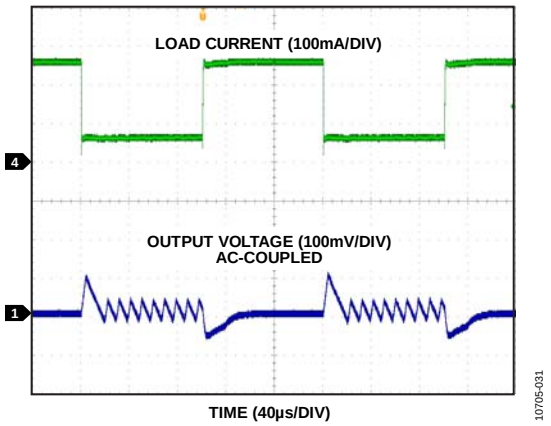

Figure 18. Load Transient Response, V_{OUT} = 1.8 V, Auto Mode, 50 mA to 250 mA

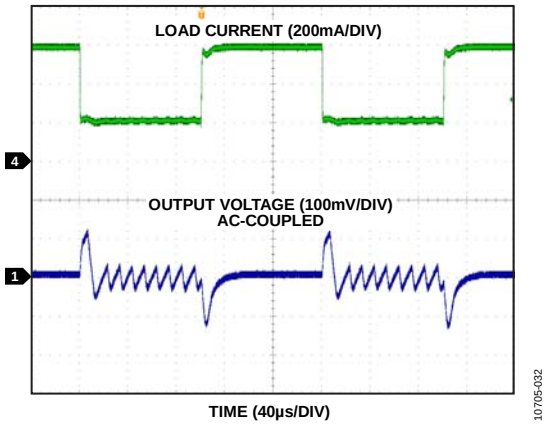

Figure 19. Load Transient Response, V_{OUT} = 1.8 V, Auto Mode, 200 mA to 600 mA

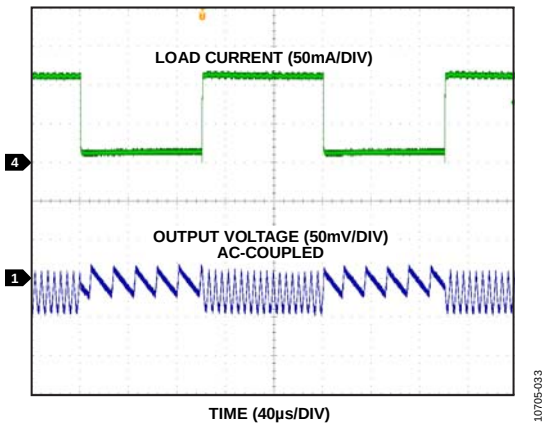

Figure 20. Load Transient Response, V_{OUT} = 3.3 V, Auto Mode, 10 mA to 110 mA

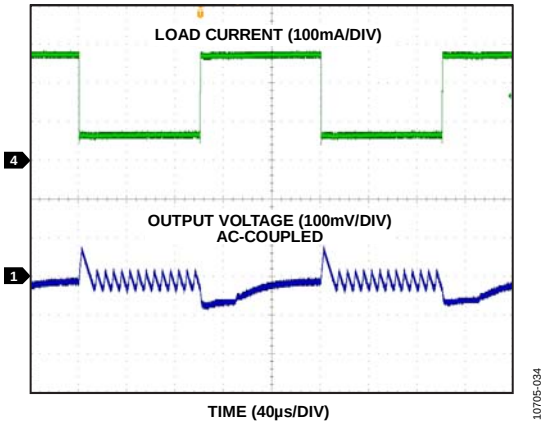

Figure 21. Load Transient Response, V_{OUT} = 3.3 V, Auto Mode, 50 mA to 250 mA

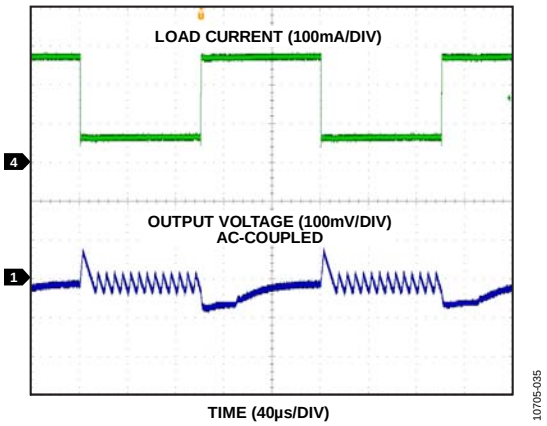

Figure 22. Load Transient Response, V_{OUT} = 3.3 V, Auto Mode, 200 mA to 600 mA

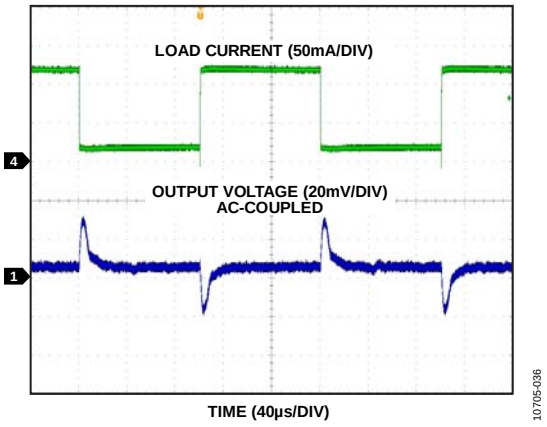

Figure 23. Load Transient Response, V_{OUT} = 1.8 V, PWM Mode, 10 mA to 110 mA

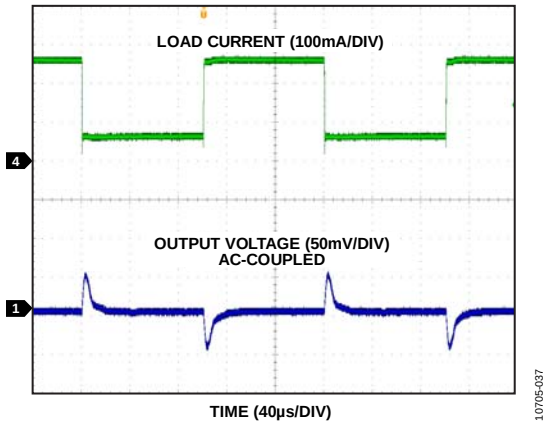

Figure 24. Load Transient Response, V_{OUT} = 1.8 V, PWM Mode, 50 mA to 250 mA

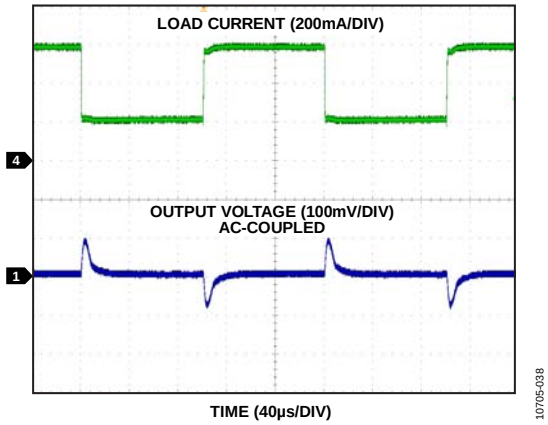

Figure 25. Load Transient Response, V_{OUT} = 1.8 V, PWM Mode, 200 mA to 600 mA

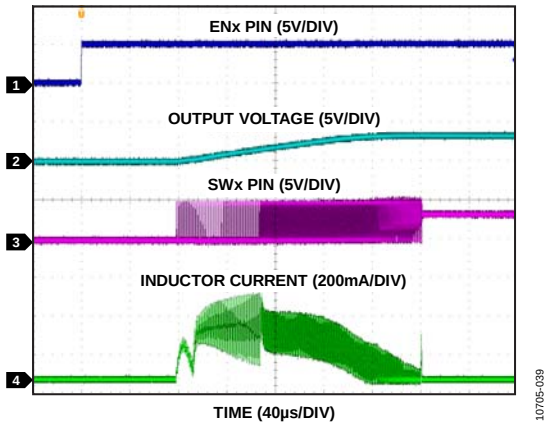

Figure 26. Startup, V_{OUT} = 3.3 V, No Load

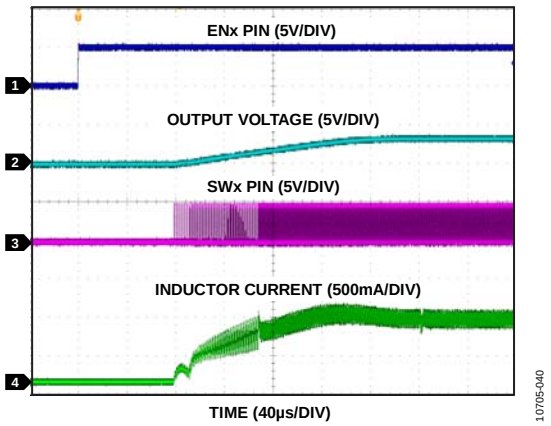

Figure 27. Startup, V_{OUT} = 3.3 V, 800 mA

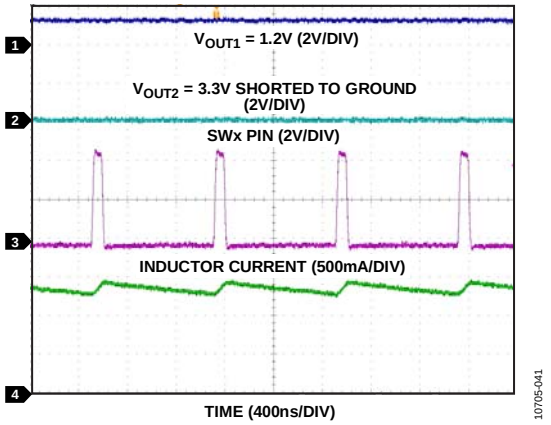

Figure 28. Short-Circuit Response

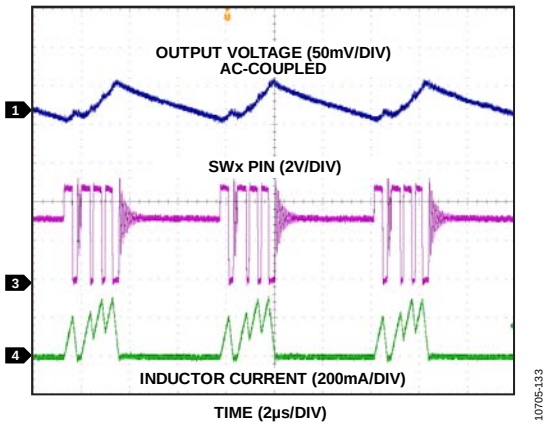

Figure 29. Typical PSM Operation, V_{OUT} = 3.3 V, I_{LOAD} = 50 mA, 150 mA

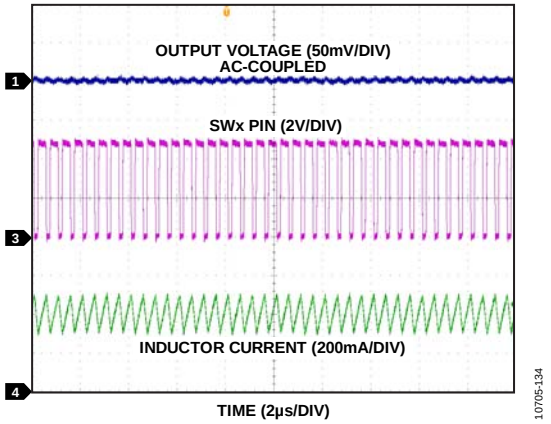

Figure 30. Typical PWM Operation, V_{OUT} = 3.3 V, I_{LOAD} = 400 mA

THEORY OF OPERATION

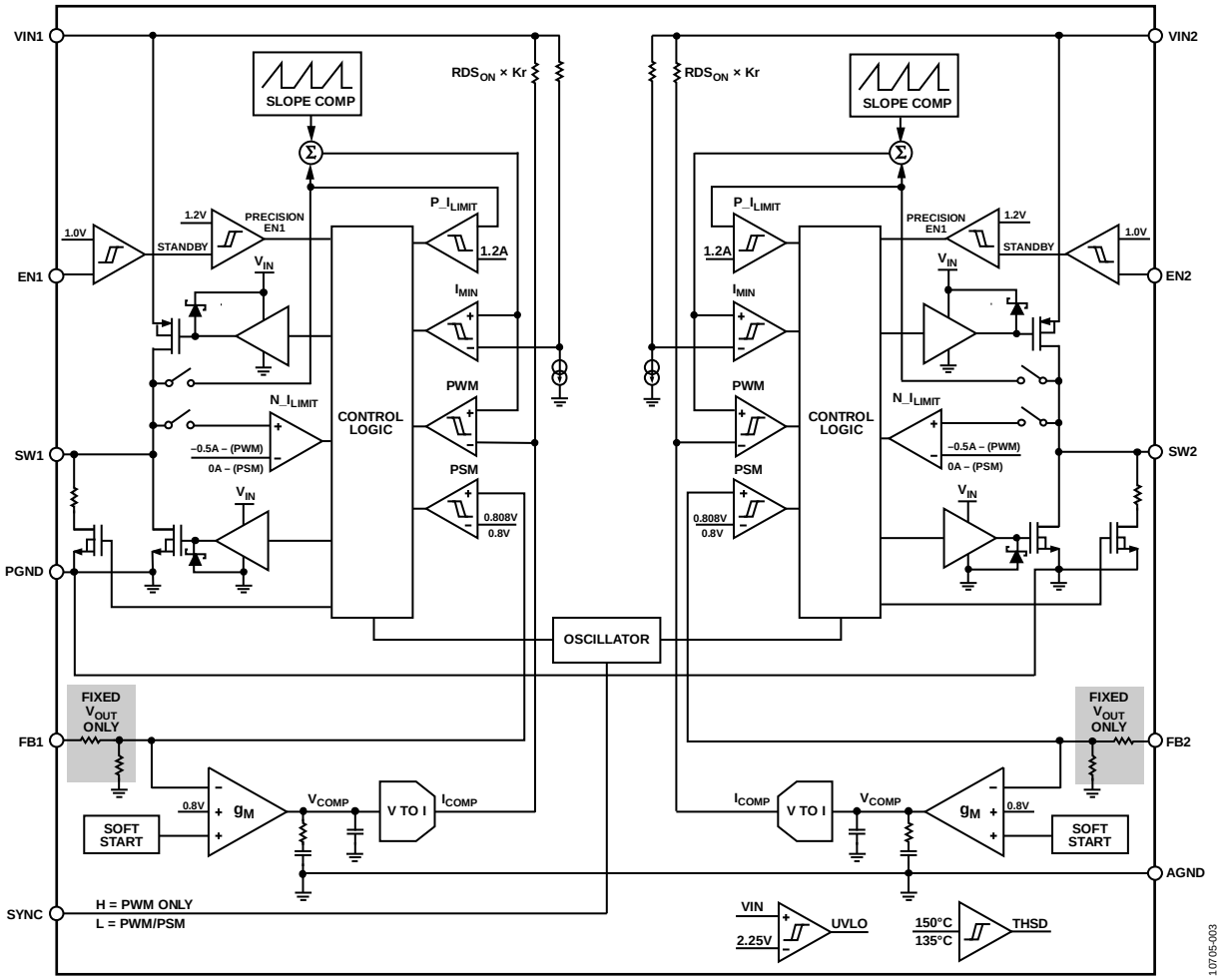

Figure 31. Internal Block Diagram

OVERVIEW

The ADP2230 contains two, high efficiency, step-down, dc-to-dc converters that use a proprietary, high speed, current mode, constant frequency, PWM control scheme for excellent stability and transient response. To ensure long battery life, the ADP2230 also has a PSM mode that reduces the switching frequency under light load conditions. The architecture ensures smooth transitions between PWM mode and PSM, and maintains high efficiencies at light loads.

The ADP2230 operates with an input voltage between 2.3 V and 6.5 V and buck to output voltages between 0.8 V and 6 V.

The ADP2230 buck outputs operate out of phase to reduce the input current ripple. All versions include an internal power switch, synchronous rectifier, and internal compensation for minimal external part count. The ADP2230 also includes internal protection features such as precision enable, soft start, UVLO, TSD, and short-circuit protection.

The ADP2230 also includes an integrated, 200 Ω, switched resistor, quick output discharge (QOD) function that automatically discharges the output when the device is disabled.

The following sections describe the operating conditions, the modes of operation, and the features of the ADP2230.

OPERATING CONDITIONS

Input Voltage

The ADP2230 operates with an input voltage between 2.3 V and 6.5 V. The VIN1 and VIN2 pins cannot be controlled separately. VIN1 and VIN2 must be tied together and powered from a single source.

Output Voltage

The ADP2230 step-down, dc-to-dc converter is available with adjustable output voltages that can be set between 0.8 V and 6 V. The ADP2230 is also available in three fixed output voltage pair options: 1.2 V/1.8 V, 1.2 V/3.3 V, or 1.8 V/3.3 V. For additional output voltage options, contact a local sales or distribution representative.

SYNC PIN CONTROL SCHEMES

There are three possible switching control schemes for the ADP2230 that can be selected using the SYNC pin: PWM mode, PSM/PWM automatic transitioning mode, and external clock synchronization. In PWM mode and PSM/PWM automatic transitioning mode, the two bucks operate 180° out of phase. When using the external clock synchronization control scheme, the two bucks operate in phase.

PWM Mode

When the SYNC pin is fixed high ($V_{SYNC} \geq 1.3$ V), the ADP2230 operates in the fixed 2 MHz PWM mode. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted to regulate the output voltage. The switching frequency is 2 MHz, typical, over all input, output, and load conditions.

At the start of each oscillator cycle in PWM, the P-channel MOSFET switch is turned on, putting a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current level that turns off the P-channel MOSFET switch and turns on the N-channel MOSFET synchronous rectifier. This puts a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on until the next clock cycle.

PSM/PWM Automatic Transitioning Mode

When the SYNC pin is fixed low ($V_{SYNC} \leq 0.4$ V), the ADP2230 is able to automatically transition between PWM mode and PSM to maintain the highest efficiency. The ADP2230 operates in fixed frequency PWM mode for medium to high load currents. If the load current falls below the PSM/PWM threshold level, the converter smoothly transitions to the reduced frequency PSM. The PSM/PWM threshold varies with the operating conditions. The PSM/PWM transition level for various operating conditions is shown in Figure 8. The two buck converters operate independently and can have different PSM/PWM current thresholds for the same output voltage.

When the device enters PSM, the ADP2230 switches only when necessary to maintain the output voltage within regulation. When the output voltage falls below the lower regulation threshold, the ADP2230 enters PWM mode for a few oscillator cycles until the output voltage reaches the upper regulation threshold. When it reaches the upper threshold, the ADP2230 enters sleep mode and waits for the output voltage to fall below the lower regulation threshold. During the wait time between the bursts, both power switches are off to minimize quiescent current, and the output capacitor supplies the entire load current. Due to the PSM architecture, the output voltage ripple in this mode is larger than the ripple in the PWM mode of operation. Figure 29 shows the typical operation in PSM mode.

External Clock Synchronization

When a 1.5 MHz to 2.5 MHz external clock is applied to the SYNC pin, the ADP2230 automatically detects the rising edge of the first clock and synchronizes to the external clock. If the device is synchronized to an external clock, the two bucks operate in phase, PSM is disabled, and the device is forced to operate in PWM mode only.

FEATURES DESCRIPTIONS

Precision Enable

The ADP2230 has two enable inputs, EN1 and EN2, that allow each of the buck outputs to be enabled and shut down independently. The enable circuits of the ADP2230 minimize the input current during shutdown and simultaneously provide precision enable thresholds. When the enable input voltages are below 0.4 V, the regulators are in shutdown mode. When both buck converters are in shutdown mode, the supply current is 0.1 µA (typical). As the enable input voltages rise above the standby enable threshold of 1.15 V (minimum), the internal bias currents and voltages are activated, turning on the precision enable circuitry. This allows the precision enable circuitry to accurately detect when the ENx pin voltage exceeds the precision enable rising threshold of 1.2 V (maximum).

Due to device constraints, EN1 and EN2 have different operating maximums. EN2 has a 6.5 V operating maximum and can be directly connected to VINx for any application. EN1 has a 5.5 V operating maximum and cannot be directly connected to VINx for applications where V_{IN} is greater than 5.5 V. Connect a resistor divider from VINx to EN1 to reduce the voltage applied to the EN1 pin to 5.5 V or less.

Quick Output Discharge

The ADP2230 includes an internal, 200 Ω discharge resistor on the SWx pin that forces the output voltage to zero when the buck is disabled. This ensures that the output of the buck is always in a well defined state.

Output Short-Circuit Protection

The ADP2230 includes frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin (FBx) falls below 0.3 V, indicating the possibility of a hard short at the output, the switching frequency is reduced to half of the internal oscillator frequency. The reduction in the switching frequency provides more time for the inductor to discharge, preventing a runaway of output current.

Undervoltage Lockout

To protect against battery discharge, an undervoltage lockout (UVLO) circuit is incorporated into the ADP2230. When the input voltage drops below the UVLO threshold, the ADP2230 shuts down, and both power switches and both synchronous rectifiers turn off. If EN1 and EN2 are logic high, when the input voltage rises above the UVLO threshold, the soft start periods are initiated and the two buck converters are enabled.

Thermal Shutdown

In the event that the junction temperature of the ADP2230 rises above 150°C, the thermal shutdown protection circuit turns off the regulator. Extreme junction temperature can be the result of high current operation, poor circuit board design, and/or high ambient temperature. A 15°C hysteresis is included in the protection circuit so that when a thermal shutdown occurs, the device does not return to normal operation until the on-chip temperature drops below 135°C. Upon exiting thermal shutdown, the soft start sequences are initiated.

Soft Start

The ADP2230 has an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter. Typical soft start time is 350 µs. The ADP2230 is also capable of starting up into a precharged output capacitor. If soft start is invoked when the output capacitor charge is greater than zero, the device delays the start of switching until the internal soft start ramp reaches the corresponding FB voltage. This feature prevents discharging the output capacitor at the beginning of soft start.

Current Limit

The ADP2230 has protection circuitry that limits the direction and amount of current that flows through the power switch and synchronous rectifier, cycle by cycle. The positive current limit of 1300 mA (typical) on the power switch limits the amount of current that can flow from the input to the output. In PWM, the ADP2230 also has a negative current limit of 500 mA (typical), on the synchronous rectifier that prevents the inductor current from reversing direction and flowing out of the load.

100% Duty Cycle

The ADP2230 enters and exits 100% duty cycle smoothly. The control loop seeks the next clock cycle while the high-side switch is engaged. When this occurs, the clock signal is masked, and the PMOS remains on. When the input voltage increases, the internal V_{COMP} node decreases its signal to the control loop; thus, the device stops skipping clock cycles and exits 100% duty cycle.

APPLICATIONS INFORMATION

The ADP2230 is designed with a high 1.5 MHz to 2.5 MHz operating frequency that enables the use of small chip inductors and capacitors that are ideal for use in applications with solution size constraints. The external component selection for the ADP2230 application circuit is also driven by the input and output operating requirements. Compatible components for the application circuits in Figure 32 and Figure 33 are identified using the recommended inductors in Table 6 and selection guides in the following sections.

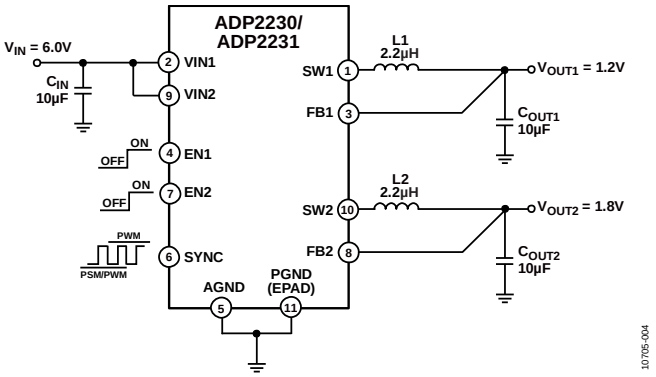

Figure 32. Typical Application Circuit Fixed Output Voltage

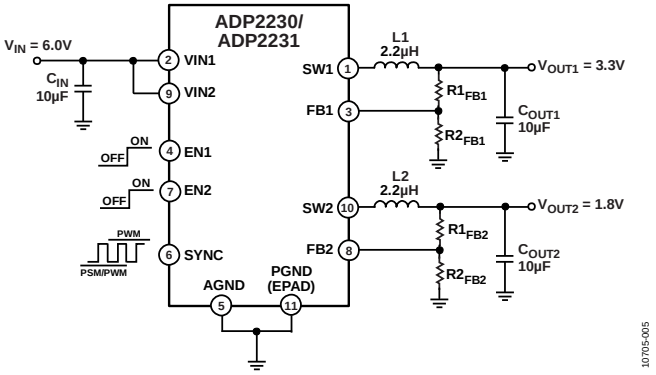

Figure 33. Typical Application Circuit Adjustable Output Voltage

SETTING THE OUTPUT VOLTAGE

The ADP2230 is available with 1.2 V/1.8 V, 1.2 V/3.3 V, or 1.8 V/3.3 V fixed output voltage pairs. For these options, the output voltage is set by an internal resistive feedback divider, and no external resistors are necessary to set the output, as shown in Figure 32.

The ADP2230 is available with adjustable output voltage pairs and can be configured for output voltages between 0.8 V and 6 V. The output voltage is set by a resistor voltage divider, $R1_{FBx}$, from the output voltage (V_{OUT}) to the 0.8 V feedback input at FBx and $R2_{FBx}$ from FBx to ground (see Figure 33).

Use the following equation to determine R1 and R2 for the desired V_{OUT}:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times V_{FB} \quad (3)$$

where V_{FB} = 0.8 V, typical.

SELECTING THE INDUCTOR

The ADP2230 is designed for optimal performance with 2.2 µH inductors that have favorable saturation currents and lower dc resistances (DCR) for their given physical size. Other inductor values are not recommended.

To ensure stable and efficient performance with the ADP2230, select a compatible inductor with a sufficient current rating, saturation current, and low DCR. The specifications and value of the selected inductor affect efficiency, output ripple, transient response, and the transition level between PSM/PWM. Suggested inductors are shown in Table 6.

The saturation current of the selected inductor must be greater than the maximum peak inductor current, I_{PK}, of the application. The maximum peak inductor current is the maximum load current plus half the inductor ripple current determined by the following equation:

$$I_{PK} = I_{LOAD(MAX)} + \left(\frac{\Delta I_L}{2}\right) \quad (4)$$

where ΔI_L is the ripple current of the inductor.

The ripple current can be calculated as follows:

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

where:
f_{SW} is the switching frequency in MHz (2 MHz, typical).
L is the inductor value.

The largest ripple current, ΔI_L, occurs at the maximum input voltage.

Table 6. Suggested Inductors

Manufacturer	Part Number	Inductance (µH)	DCR (mΩ) Typ	Current Rating (A)	Saturation Current (A)	Size (L × W × H) (mm)	Package
TDK	MLP2016S2R2M	2.2 ± 20%	110	1.20	N/A	2.00 × 1.60 × 1.00	0806
	MLP2520S2R2S	2.2 ± 20%	110	1.20	1.20	2.50 × 2.00 × 1.00	1008
	VLF252012MT-2R2M	2.2 ± 20%	57	1.67	1.04	2.50 × 2.00 × 1.00	1008
	VLF302510MT-2R2M	2.2 ± 20%	70	1.23	1.37	3.00 × 2.50 × 1.00	N/A
	VLF302515MT-2R2M	2.2 ± 20%	42	2.71	1.57	3.00 × 2.50 × 1.40	N/A
Murata	LQM2HPN2R2MG0	2.2 ± 20%	80	1.30	N/A	2.50 × 2.00 × 0.90	1008
	LQH32PN2R2NNC	2.2 ± 30%	64	1.85	N/A	3.20 × 2.50 × 1.55	1210
Wurth	74479787222	2.2 ± 20%	80	1.50	0.70	2.50 × 2.00 × 1.00	1008
	7440430022	2.2 ± 30%	23	2.50	2.35	4.80 × 48.0 × 2.80	N/A
Taiyo Yuden	BRC2012T2R2MD	2.2 ± 20%	110	1.00	1.10	2.00 × 1.25 × 1.40	0805
Toko	MDT2520-CR2R2M	2.2 ± 20%	90	1.35	N/A	2.50 × 2.00 × 1.00	1008
	DEM2810C (1224AS-H-2R2M)	2.2 ± 20%	85	1.10	1.40	3.20 × 3.00 × 1.00	N/A
	DEM2815C (1226AS-H-2R2M)	2.2 ± 20%	43	1.40	2.20	3.20 × 3.00 × 1.50	N/A
Coilcraft	XPL2010-222	2.2 ± 20%	156	0.96	0.94	1.90 × 2.00 × 1.00	N/A
	XFL3010-222	2.2 ± 20%	111	1.0	0.94	3.00 × 3.00 × 1.00	N/A
	XFL3012-222	2.2 ± 20%	81	1.40	1.00	3.00 × 3.00 × 1.30	1212

[1] N/A means not applicable.

SELECTING THE INPUT AND OUTPUT CAPACITORS

The ADP2230 is designed for optimal performance with 10 µF capacitors. Use any size, good quality, low ESR, X5R or X7R ceramic capacitors with the ADP2230, as long as they meet the capacitance and voltage requirements of the application. Capacitors less than 10 µF are not recommended.

Input Capacitor

The ADP2230 is designed to operate with a single 10 µF input capacitor (C_{IN}). The input capacitor must be able to support the maximum input operating voltage and the maximum rms input current.

Place the input capacitor as close as possible to the VINx pins to reduce input voltage ripple. Select an input capacitor capable of withstanding the rms input current for the maximum continuous load current in the application using the following equation:

$$I_{RMS} \approx I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad (6)$$

The input capacitor reduces the input voltage ripple caused by the switch currents on the VINx pin and reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance are encountered.

Output Capacitor

The ADP2230 requires two 10 µF capacitors, C_{OUT1} and C_{OUT2}, with one capacitor on each buck output. The output capacitor selection affects both the output voltage ripple (ΔV_{OUT}) and the stability of the control loop.

The ADP2230 is designed for operation with small, space saving ceramic capacitors, but function with most commonly used capacitors as long as care is taken to calculate the effective ESR value. Capacitors with low ESR values produce the lowest output voltage ripple. A capacitor with an ESR between 0.001 Ω and 0.01 Ω is recommended to ensure stability of the ADP2230. To determine the maximum ESR for a given ΔV_{OUT}, use the following equation:

$$ESR_{C_{OUT}(MAX)} < \frac{\Delta V_{OUT}}{\Delta I_L} \quad (7)$$

where ΔV_{OUT} is the peak-to-peak output voltage ripple as calculated in Equation 8.

The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor. The output voltage ripple is determined by the following equation:

$$\Delta V_{OUT} \approx \Delta I_L \times (ESR_{C_{OUT}} + 1/(8 \times C_{OUT} \times f_{SW})) \quad (8)$$

where:

$ESR_{C_{OUT}}$ is the ESR of the chosen capacitor.

ΔI_L is the ripple current of the inductor calculated in Equation 7.

The largest voltage ripple occurs at the highest input voltage. At light load currents, if SYNC is set low, the converter operates in PSM, and the output voltage ripple increases.

To improve the transient response of the ADP2230, increase the value of C_{OUT}. Capacitors less than 10 µF are not recommended.

PCB LAYOUT CONSIDERATIONS

For high efficiency, good regulation, and stability with the ADP2230, a well designed PCB is required. Poor layout can affect the ADP2230 buck performance, causing electromagnetic interference (EMI), poor electromagnetic compatibility (EMC), ground bounce, and voltage losses.

Improve heat dissipation from the package by increasing the amount of copper attached to the pins of the ADP2230.

Use the following guidelines when designing PCBs:

- Keep the low ESR input and output capacitors, CIN and COUT, and the inductors, L1 and L2, as close as possible to the ADP2230. Avoid long trace lengths from the device to the capacitors that add series inductance and may cause instability or increased ripple.
- Route the output voltage path away from the inductor and SWx node to minimize noise and magnetic interference.
- Keep high current traces as short and as wide as possible.
- Avoid routing high impedance traces near any node connected to SWx or near the inductor to prevent radiated noise injection.
- Use a ground plane with several vias connected to the component side ground to reduce noise interference on sensitive circuit nodes.
- The use of 0402 or 0603 capacitors achieves the smallest possible footprint solution where board area is limited.

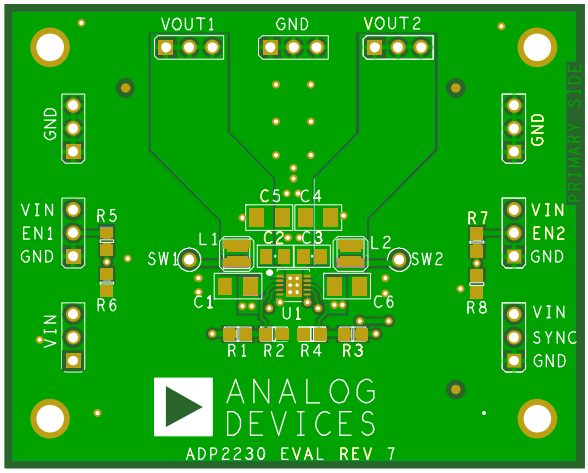

Figure 34. PCB Layout, Top

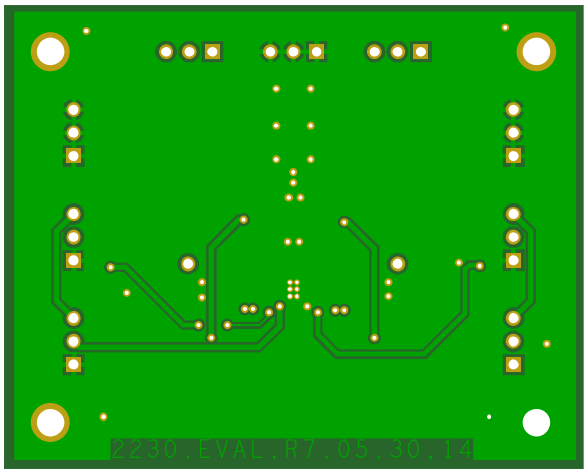

Figure 35. PCB Layout, Bottom

OUTLINE DIMENSIONS

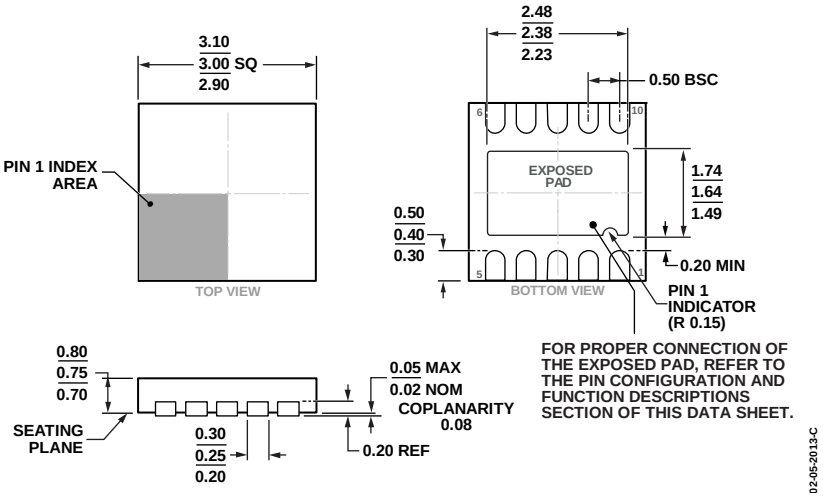

Figure 36. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Buck 1 Output Voltage (V)[2]	Buck 2 Output Voltage (V)[2]	Temperature Range	Package Description	Package Option	Branding
ADP2230ACPZ-1218R7	1.2	1.8	–40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	LJ3
ADP2230ACPZ-1233R7	1.2	3.3	–40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	LM3
ADP2230ACPZ-1833R7	1.8	3.3	–40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	LMK
ADP2230ACPZ-R7	Adjustable	Adjustable	–40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	LMQ
ADP2230CP-EVALZ				Evaluation Board with Adjustable Output Voltage Option		

[1] Z = RoHS Compliant Part.
[2] For additional output voltage options, contact a local sales or distribution representative.

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D10705-0-11/14(A)

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- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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