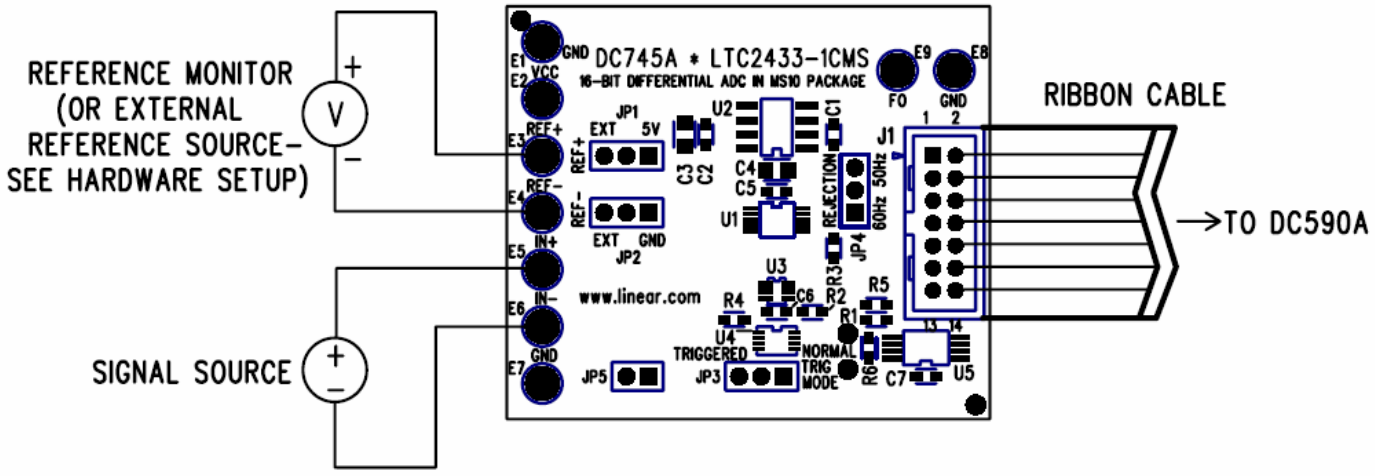
DESCRIPTION

Demonstration circuit 745 features the LTC2433-1, a 16-bit high performance ΔΣ analog-to-digital converter (ADC). The LTC2433-1 features 0.12 LSB linearity, 0.16 LSB full-scale accuracy, 5μV offset, and 1.45μV RMS noise. The inputs and reference are fully differential, with input common mode rejection of 140 dB. The LTC2433-1 is available in a 10 pin MSOP package and has an easy to use SPI interface.

DC745 is a member of Linear Technology's QuickEval™ family of demonstration boards. It is designed to allow easy evaluation of the LTC2433-1 and may be connected directly to the target application's analog signals while using the DC590 USB Serial Controller board and supplied software to measure performance. The exposed ground planes allow proper grounding to prototype circuitry. After evaluating with Linear Technology's software, the digital signals can be connected to the end application's processor / controller for development of the serial interface.

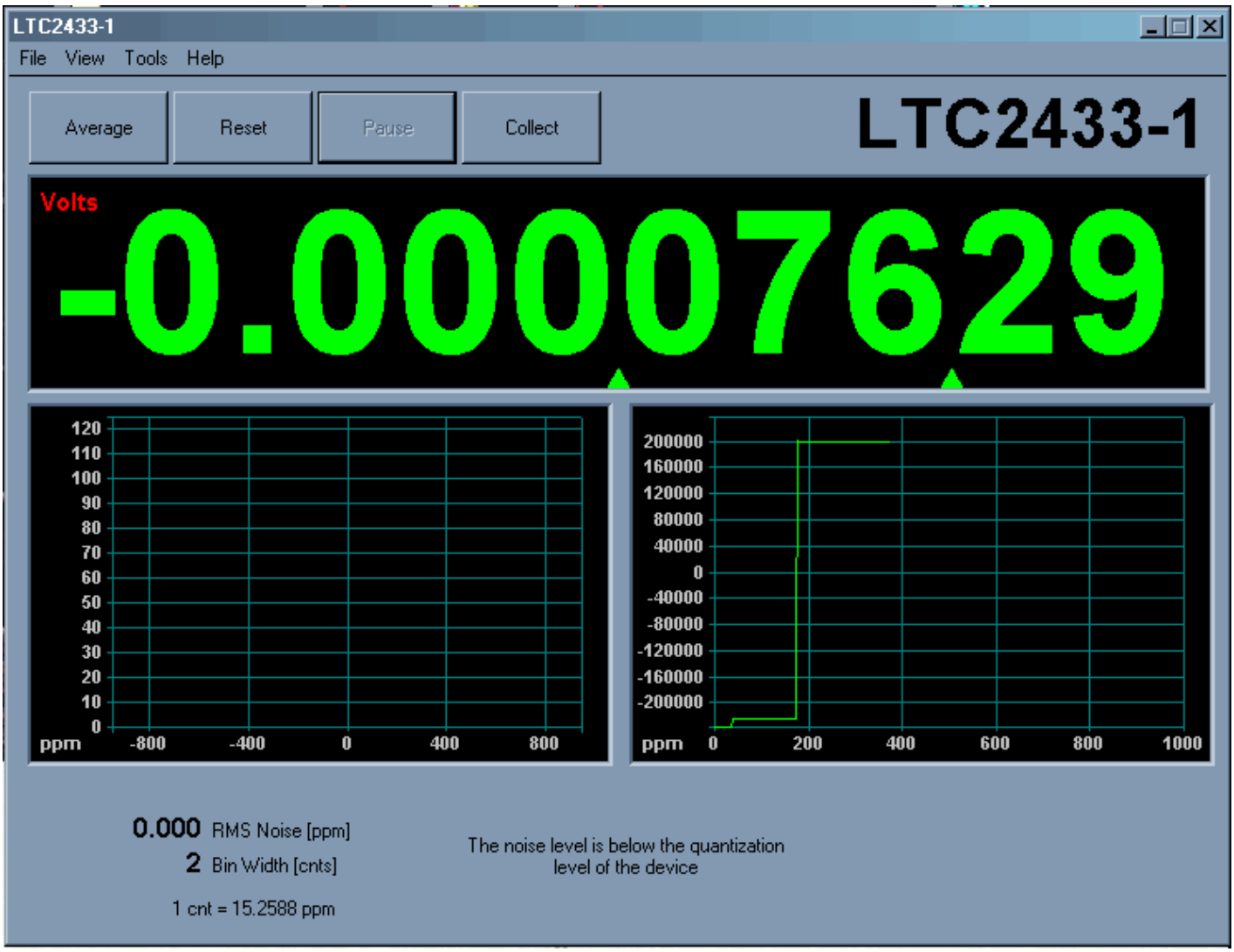
Design files for this circuit board are available. Call the LTC factory.



QUICK START PROCEDURE

Connect DC745 to a DC590 USB Serial Controller using the supplied 14 conductor ribbon cable. Connect DC590 to a host PC with a standard USB A/B cable. Run the evaluation software supplied with DC590 or downloaded from http://www.linear.com/software. The correct program will be loaded automatically. Click the COLLECT button to start reading the input voltage. Details on software features are documented in the control panel's help menu.

Tools are available for logging data, changing reference voltage, changing the number of points in the strip chart and histogram, and changing the number of points averaged for the DVM display.



HARDWARE SET-UP

JUMPERS

JP1 – Select the source for REF+, either external or 5.00 volts from the onboard LT1236 reference (default.)

JP2 – Select the source for REF-, either external or Ground (0 volts, default.)

JP3 – Trigger mode, either normal (default) or externally triggered.

JP4 – Notch frequency. Connect to 60Hz for normal operation (Fo = GND.) The LTC2433-1 is trimmed to reject both 50Hz and 60Hz by at least 87dB when Fo is grounded. Remove this jumper when supplying an external clock to the Fo turret.

JP5 – Trigger input signal. Pin 1 is a 5 volt logic signal, pin 2 is ground. When triggered mode is selected on JP3, a rising edge starts a new conversion. Note that a conversion in progress cannot be stopped, so this signal can only be used to slow down the rate at which samples are read from the LTC2433-1. When Fo is grounded, the maximum trigger frequency is 5Hz.

CONNECTION TO DC590 SERIAL CONTROLLER

J2 is the power and digital interface connector. Connect to DC590 serial controller with supplied 14 conductor ribbon cable.

An external conversion clock may be applied to the Fo turret to modify the frequency rejection characteristics or data output rate of the LTC2433-1. Be sure to remove JP4 before applying an external clock. This should be a square wave with a low level equal to ground and a high level equal to Vcc. While up to a 2MHz clock can be used, performance may be compromised. Refer to the LTC2433-1 data sheet.

ANALOG CONNECTIONS

Analog signal connections are made via the row of turret posts along the edge of the board. Also, when connecting the board to an existing circuit, the exposed ground planes along the edges of the board may be used to form a solid connection between grounds.

GND – Ground turrets are connected directly to the internal ground planes.

VCC – This is the supply for the ADC. Do not draw any power from this point.

REF+, REF- – These are connected to the LTC2433-1 REF+ and REF- pins. If the onboard reference is being used, the reference voltage may be monitored from this point. An external reference may be connected to these terminals if JP1 and JP2 are configured for external reference.

IN+, IN- – These are the differential inputs to the LTC2433-1.

EXPERIMENTS

INPUT NOISE

One of the characteristics of the LTC2433-1 is that the 1.45μV input noise floor is far below the quantization level of 76uV when a 5-volt reference is used. This means that the output will be stable if the input noise level is also below 76uV. In this sense, the LTC2433-1 is a true 16 effective bit part, whereas many 16-bit SAR converters have several LSBs of noise.

Solder a short wire from the IN- turret post to the IN+ turret post. Noise should be below the quantization level of the LTC2433-1. This will result in a noise reading of zero on the control software.

Applying an external reference of 100mV results in a 1.52μV LSB, and the noise reading will be approximately 250ppm of 100mV, or 2.5μV. This is slightly higher than the 1.45μV input thermal because quantization noise is also a factor.

COMMON MODE REJECTION

Tie the two inputs (still connected together) to ground through a short wire and note the indicated voltage. Tie the inputs to REF+; the difference should be less than 1LSB due to the 130 dB CMRR of the LTC2433-1.

BIPOLAR SYMMETRY

To demonstrate the symmetry of the ADCs transfer function, connect a stable, low noise, floating voltage source (with a voltage less than Vref/2) from IN+ to IN- and note the indicated voltage. Reverse the polarity; the indicated voltage will typically be within one LSB of the first reading multiplied by –1.

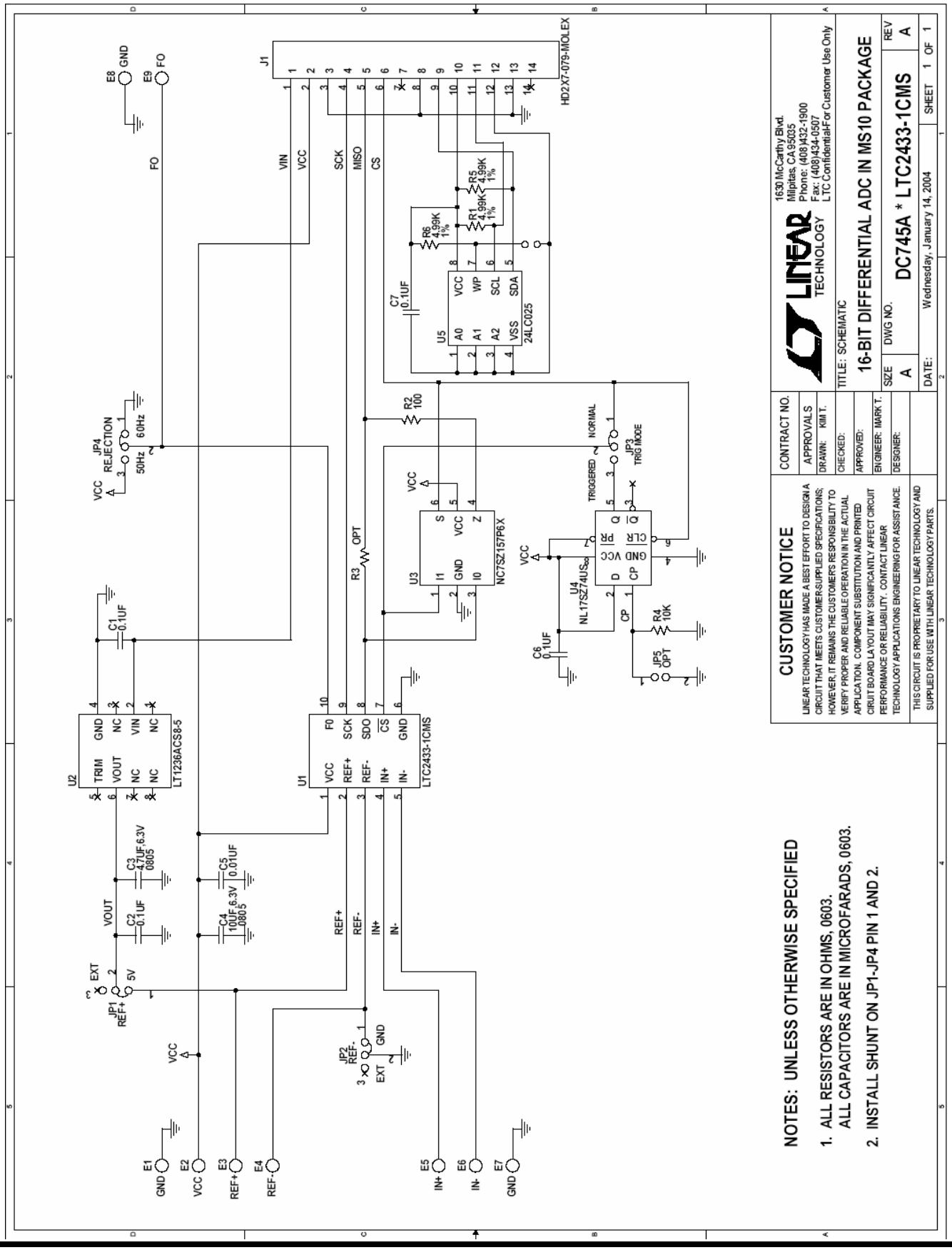
One convenient voltage source for this experiment is a single alkaline battery. While a battery has fairly low noise, it is sensitive to temperature drift. It is best to use a large (D-size) battery that is insulated from air currents. A better source is a battery powered series reference such as the LT1790. This part is available with output voltages of 1.25V, 2.048V, 2.5V, 3V, 3.3V, 4.096V and 5V.

INPUT NORMAL MODE REJECTION

The LTC2433-1's SINC4 digital filter is trimmed to strongly reject 50 or 60Hz line noise when operated with the internal conversion clock. To measure input normal mode rejection, connect IN- to a 2.5 volt source such as an LT1790-2.5 reference or a power supply. Apply a 10Hz, 2V peak-to-peak sine wave to IN+ through a 1uF capacitor. No DC bias is required because the 2-3MΩ input impedance of the LTC2433-1 tends to self-bias the input to mid-reference (see datasheet applications information for details.)

Start taking data. The input noise will be quite large, and the graph of output vs. time should show large variations.

Next, slowly increase the frequency to 60Hz. The noise should be almost undetectable in the graph. Note that the indicated noise in ppm may still be above that of the datasheet specification because the inputs are not connected to a DC source.


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 0603.
ALL CAPACITORS ARE IN MICROFARADS, 0603.
2. INSTALL SHUNT ON JP1-JP4 PIN 1 AND 2.
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LTC Confidential-For Customer Use Only
TITLE: SCHEMATIC
16-BIT DIFFERENTIAL ADC IN MS10 PACKAGE
SIZE A
DWG NO. DC745A * LTC2433-1CMS
REV A
DATE: Wednesday, January 14, 2004
SHEET 1 OF 1
U1 LTC2433-1CMS
U2 LT1236ACS8-5
U3 NC7SZ157P6X
U4 NL17SZ74US
U5 24LC025
J1 HD2X7-079-MOLEX
JP1 REF+
JP2 REF-
JP3 TRIG MODE
JP4 REJECTION
JP5 OPT
R1 4.99K 1%
R2 100
R3 OPT
R4 10K
R5 4.99K 1%
R6 4.99K 1%
C1 0.1UF
C2 0.1UF
C3 4.7UF 6.3V 0805
C4 10UF 6.3V 0805
C5 0.01UF
C6 0.1UF
C7 0.1UF
E1 GND
E2 VCC
E3 REF+
E4 REF-
E5 IN+
E6 IN-
E7 GND
E8 GND
E9 FO

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